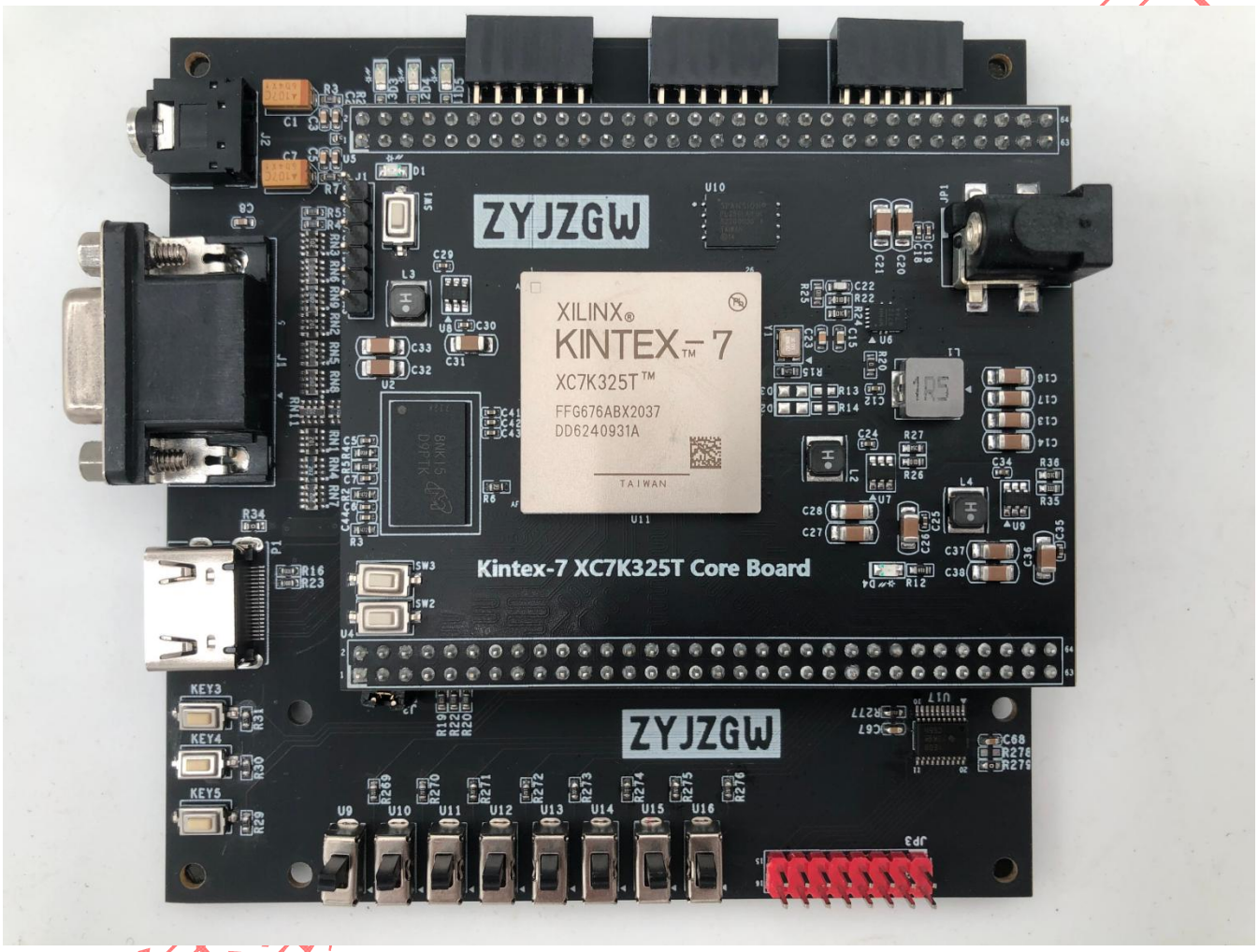
ZYJZGW XC7K325T STARTER KIT

USER MANUAL



Preface

The ZYJZGW® XC7K325T Starter Kit uses Xilinx Kintex®-7 devices to demonstrate best price performance watt at 28nm while giving you high DSP ratios, cost-effective packaging, and support for mainstream standards like PCIe® Gen3 and 10 Gigabit Ethernet. The Kintex-7 family is ideal for applications including 3G and 4G wireless, flat panel displays, and video over IP solutions.

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1. Introduction

1.1 Document Scope

This demo user manual introduces the ZYJZGW XC7K325T Starter Kit and describes how to setup the Starter Kit running with application software Xilinx Vivado 2018.3. Users may employee the on board rich logic resource FPGA XC7K325T-1FFG676C and large DDR3 memory MT41K128M16 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the core board:

- On-Board FPGA: XC7K325T-1FFG676C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7K325T-1FFG676C has rich block RAM resource up to 16,020Kb;
- XC7K325T-1FFG676C has 326,080 logic cells;
- On-Board S25FL256L SPI Flash, 32M bytes for user configuration code;
- On-Board 256MB Micron DDR3, MT41K128M16JT-125:K;
- On-Board core power supply for FPGA by using MP8712 wide input range DC/DC, it can provide 12A continuous/15A peak output current;
- XC7K325T core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- XC7K325T core board has 3 user switches;
- XC7K325T core board has 2 user LEDs;
- XC7K325T core board has JTAG interface, by using 6p, 2.54mm pitch header;
- XC7K325T core board PCB size is: 6.7cm x 8.4cm;
- Default power source for board is: 2A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

Figure 1-1. ZYJZGW XC7K325T Core Board Bottom View

Below section lists the parameters of the daughter board:

- Daughter board provides HDMI display port, by using ADV7513;
- Daughter board provides 1.8V power supply for FPGA bank12/13/32/33, by using TPS563201 DC/DC;
- Daughter board provides MicroSD card slot;
- Daughter board provides VGA display port, by using resistor dividers;
- Daughter board provides PWM driven audio output port;
- Daughter board provides 8 user switches;
- Daughter board provides 3 user LEDs;
- Daughter board provides 3 user keys;
- Daughter board provides 8-channel voltage level shifter, by using TXB0108;
- Daughter board provides 3 PMOD standard interfaces.

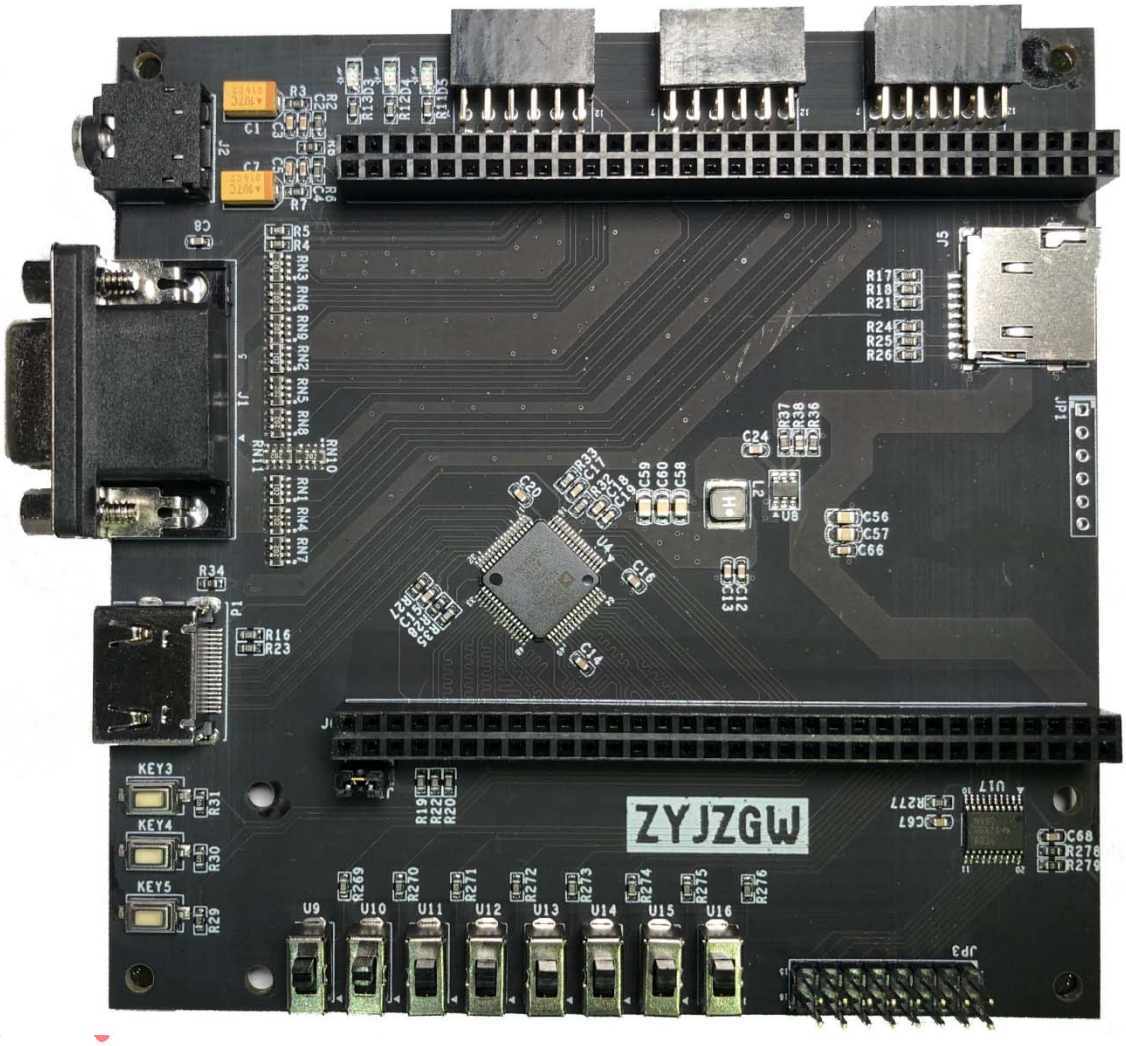

Figure 1-2. ZYJZGW XC7K325T Daughter Board Top View

1.3 Board Dimension

Below image shows the dimension of the ZYJZGW XC7K325T core board: 67.1mm x 84.1mm. The unit in below image is millimeter(mm).

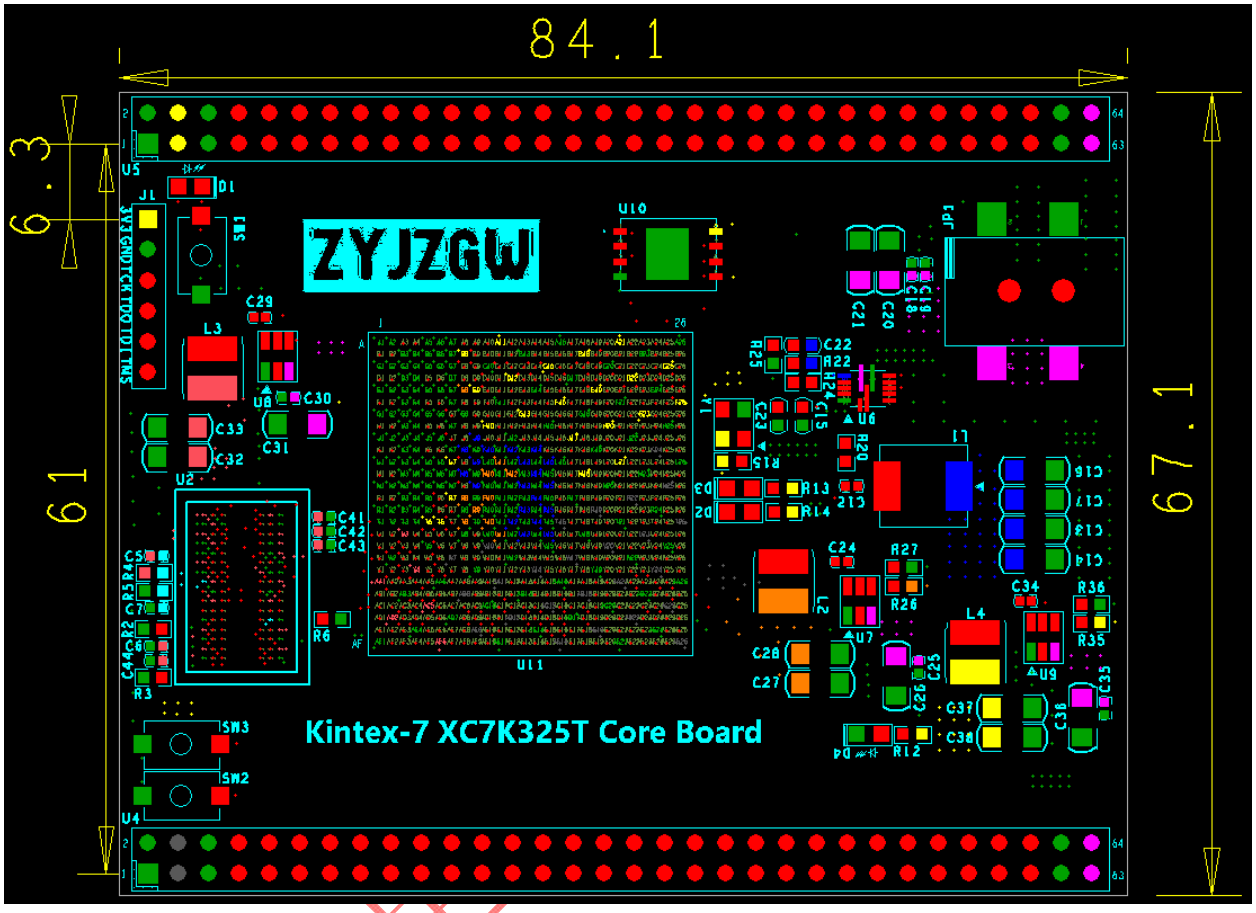

Figure 1-3. ZYJZGW XC7K325T Core Board Dimension

Below image shows the dimension of the ZYJZGW XC7K325T daughter board: 109.22mm x 109.22mm. The unit in below image is millimeter(mm).

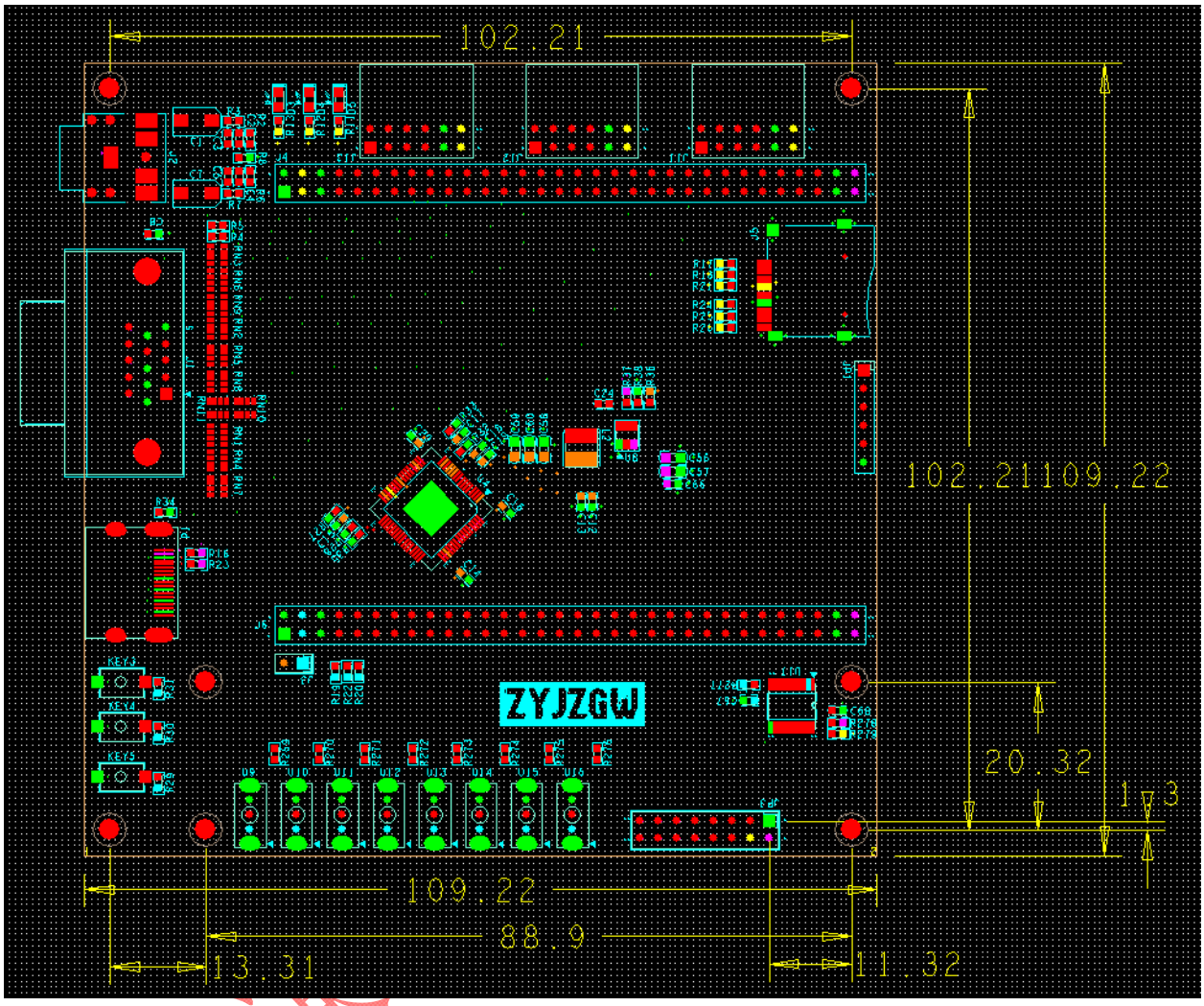

Figure 1-4. ZYJZGW XC7K325T Daughter Board Dimension

1.4 Development Tools

Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

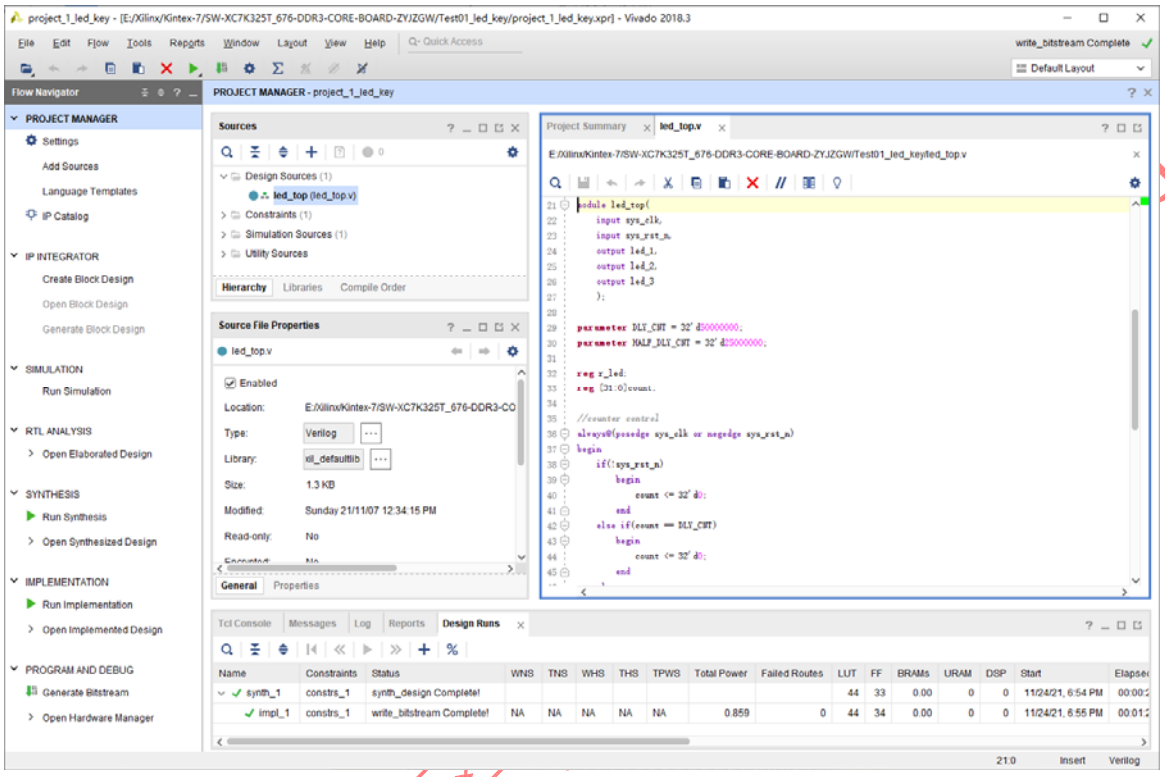

Figure 1-5. Vivado 2018.3

Users need to prepare the Xilinx USB platform cable for the development. Below image shows the JTAG connection between Xilinx USB platform cable and XC7K325T Starter Kit:

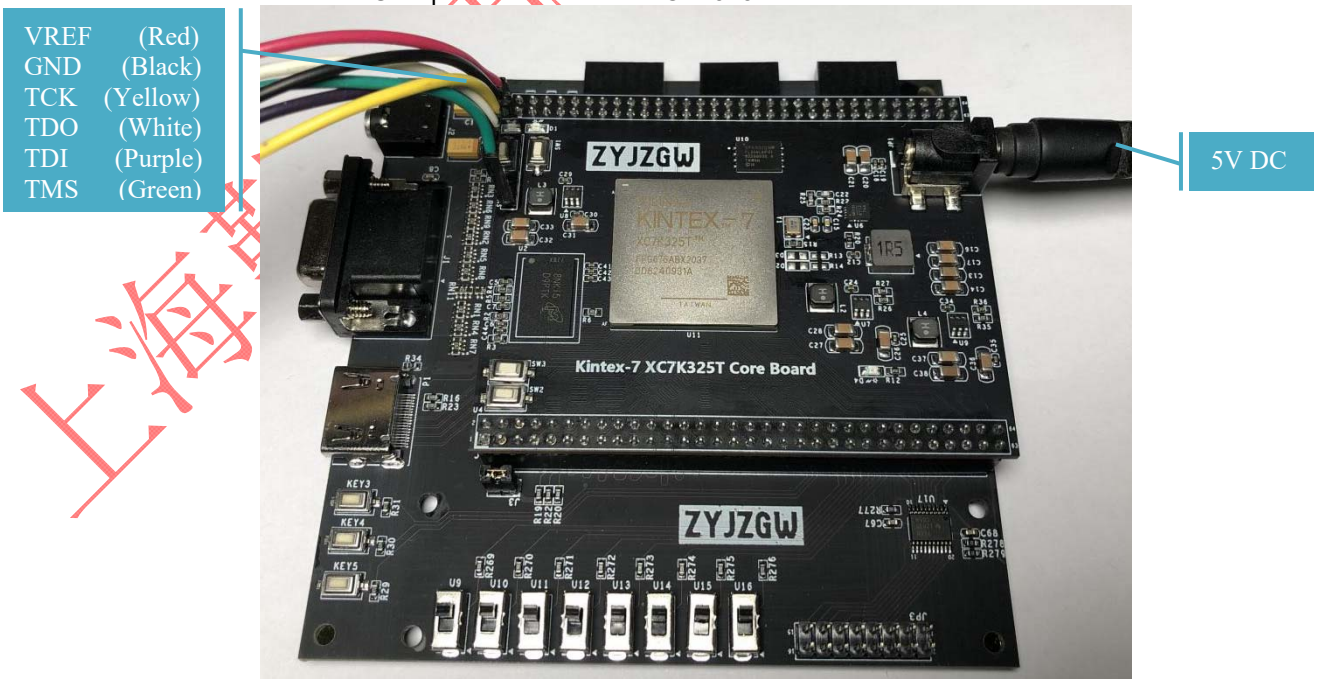

Figure 1-6. JTAG Connection and Power Supply

2. Core Board Hardware Design

2.1 Core Board Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P female header U4/U5. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active.

The IO voltage level for BANK14, BANK15 and BANK16 is 3.3V. In default, the BANK12, BANK13, BANK32 and BANK33 voltage level is 1.8V. The 1.8V power source is provided by daughter board and injected from 64P female header U4's PIN3 and PIN4(net name VCC_12_13_32_33).

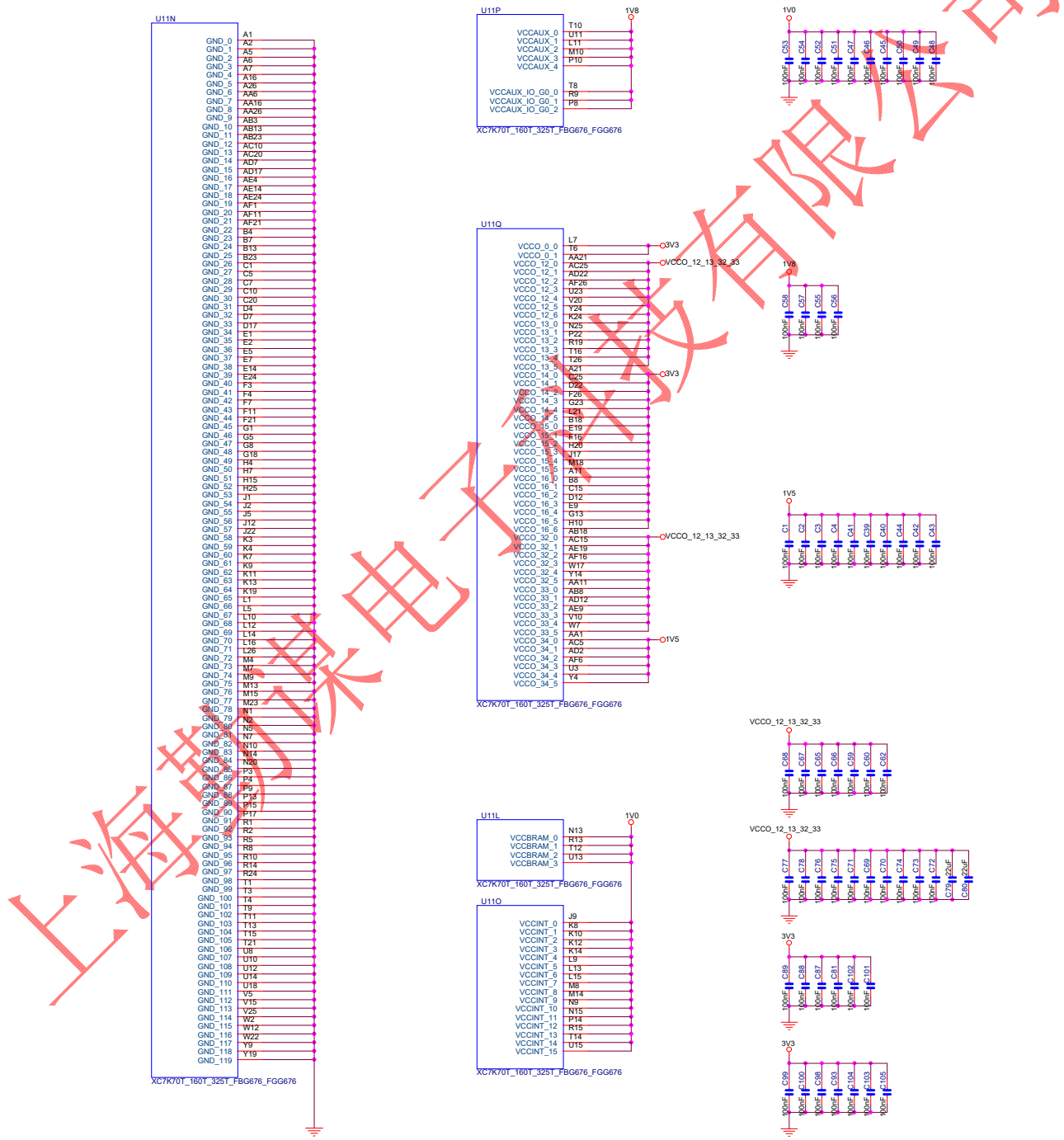

Figure 2-1. Power Supply for the FPGA

2.2 FPGA Core Power Supply

The FPGA's power on sequence is designed as this: 1.0V -> 1.8V -> 1.5V & 3.3V. The FPGA core voltage 1.0V power supply is using high efficiency DC/DC chip MP8712 provided by MPS Inc. The MP8712 supports wide voltage input range from 3V to 18V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP8712 hardware design:

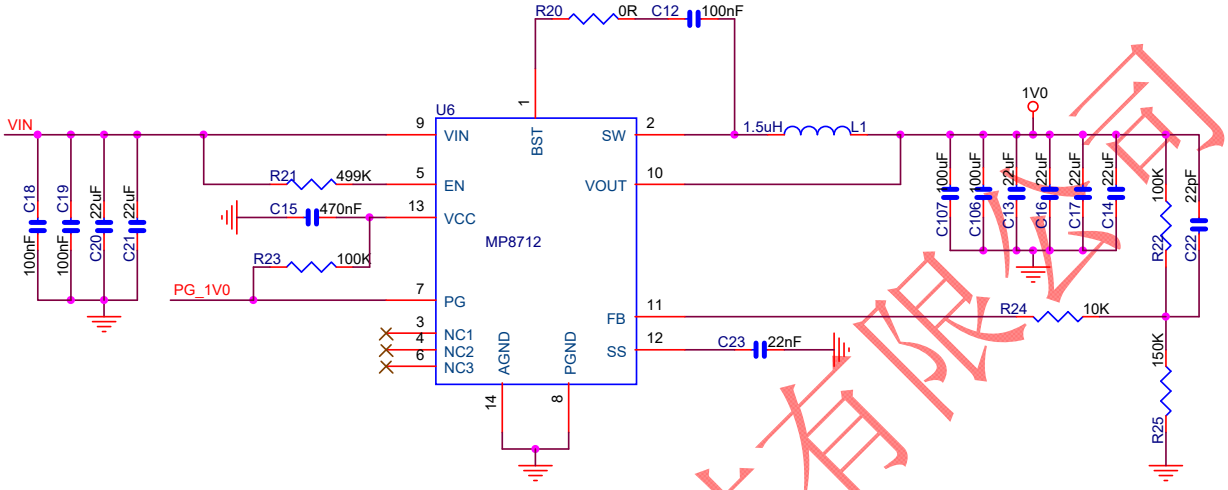

Figure 2-2. MP8712 Hardware Design

2.3 System Clock

FPGA chip XC7K325T-1FFG676C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

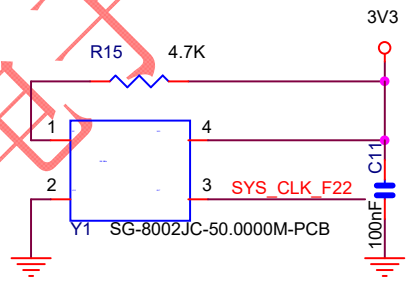

Figure 2-3. 50MHz System Clock

2.4 SPI Flash Boot

In default, the FPGA XC7K325T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using S25FL256L manufactured by Infineon(Spansion), with 256Mbit memory storage.

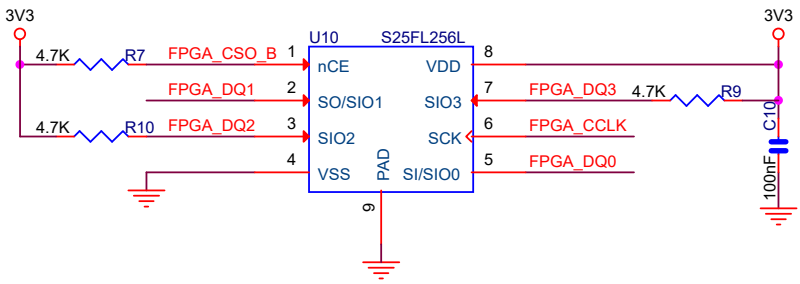

Figure 2-4. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

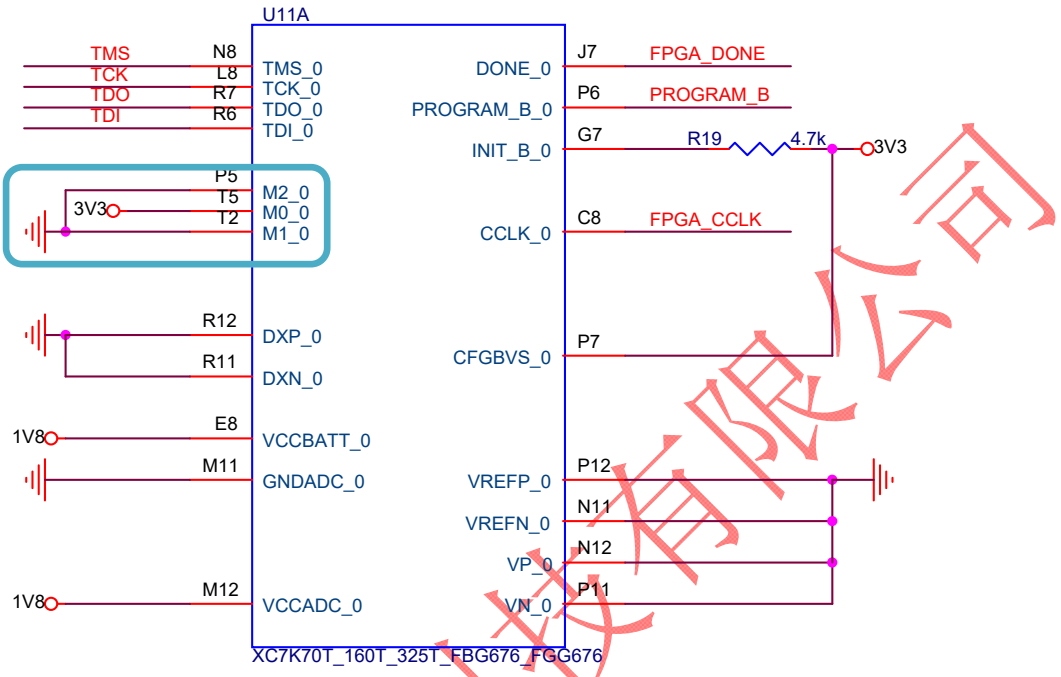

Figure 2-5. M0:M1:M2 Hardware Settings

The LED D1 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D1 could be used as FPGA loading status indicator.

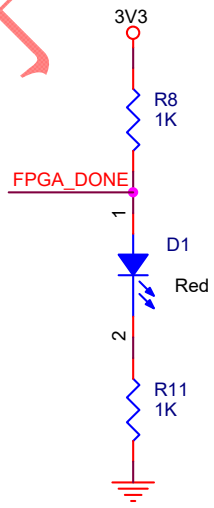

Figure 2-6. FPGA_DONE Status Indicator

2.5 User Extension IOs

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

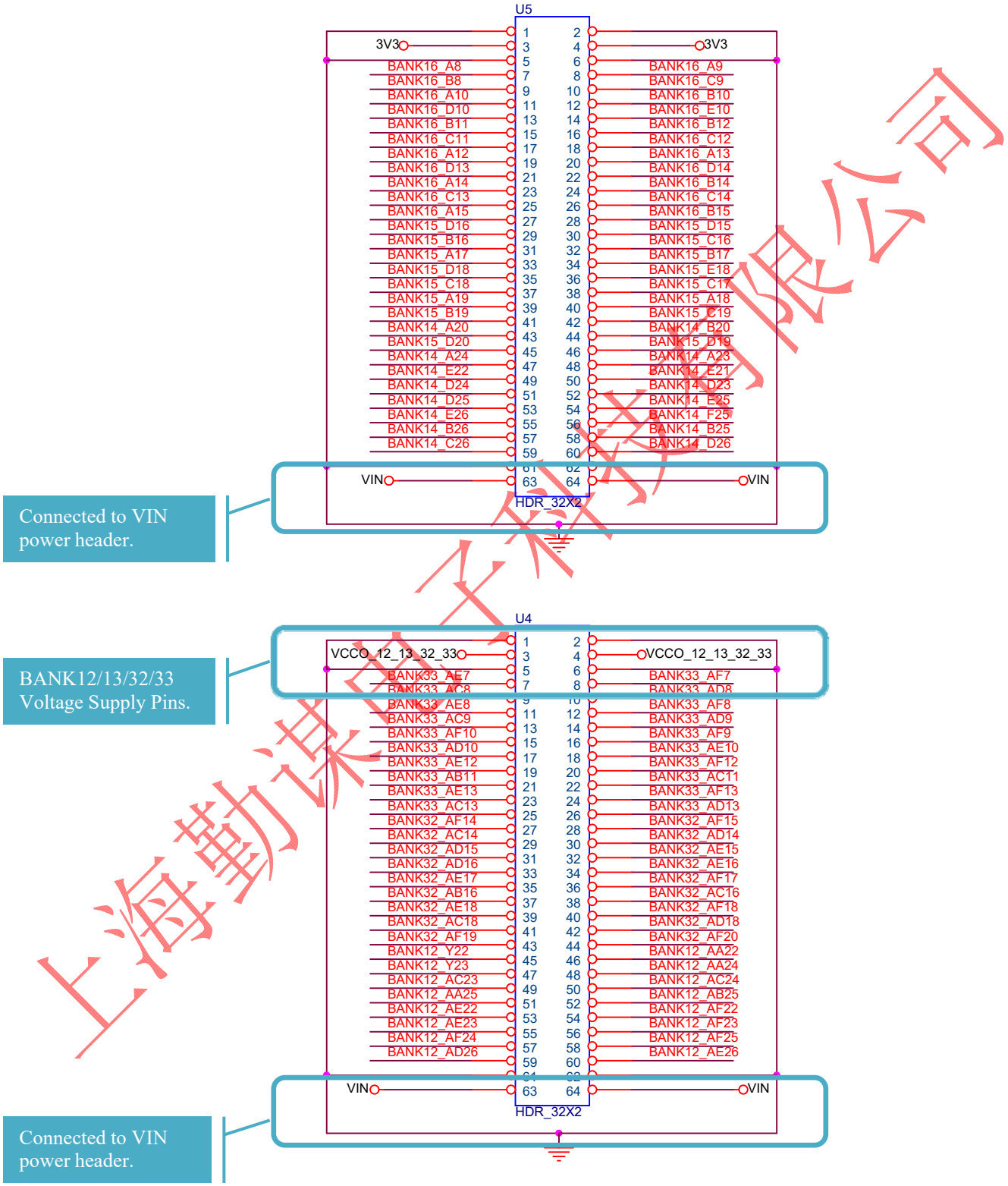

Figure 2-7. Extension IO

2.6 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

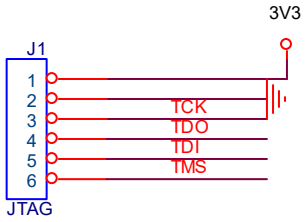

Figure 2-8. JTAG Port

2.7 User LEDs

Below image shows two user LEDs, one 3.3V power supply indicator and FPGA_DONE signal indicator(LED2 and LED3 are not mounted):

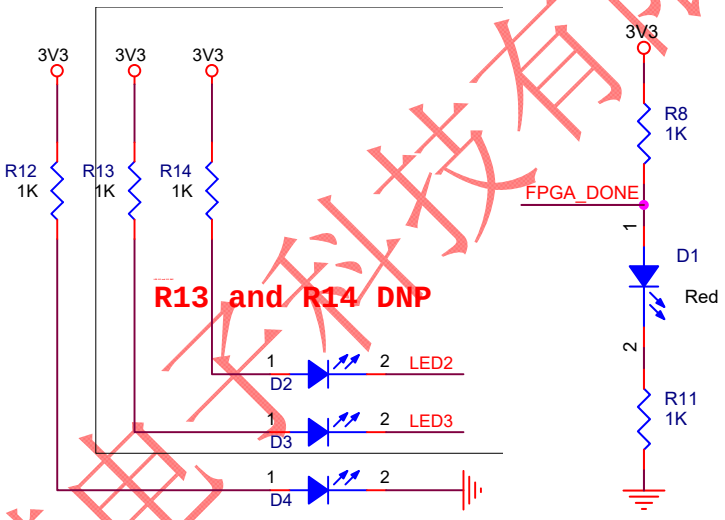

Figure 2-9. LEDs

2.8 User Keys

Below image shows the PROGRAM_B key and two user keys:

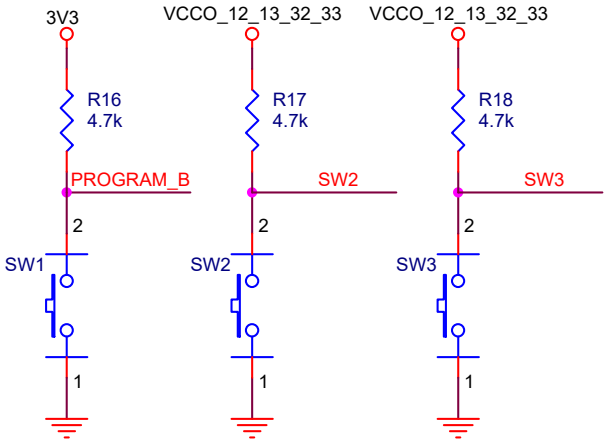

Figure 2-10. Keys

2.9 DDR3 Memory

The core board has on board 16bit width data bus, 256MB memory size DDR3 MT41K128M16JT-125:K provided by Micron. Below image shows the detailed hardware design:

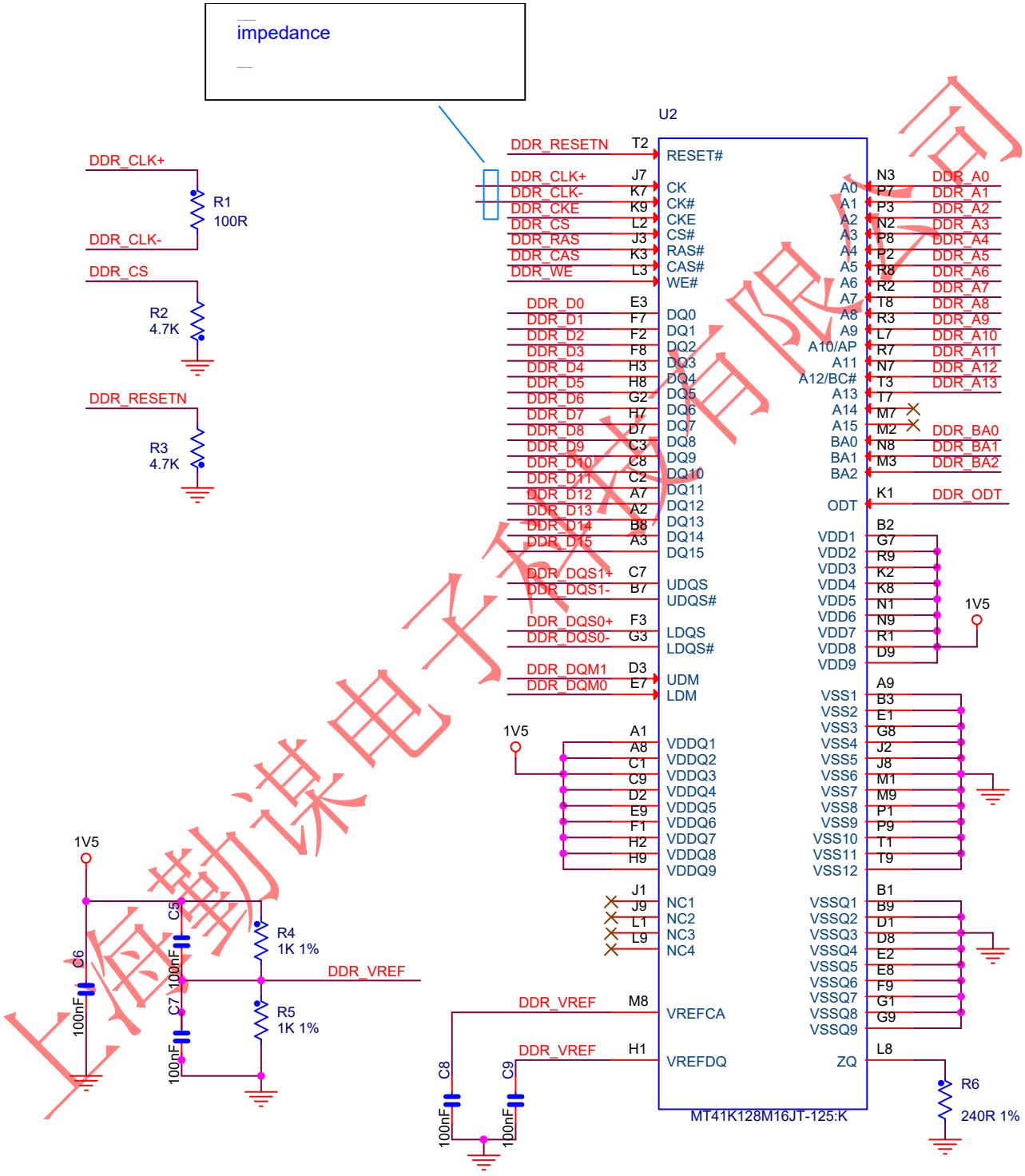

Figure 2-11. DDR3

3. Daughter Board Hardware Design

3.1 Daughter Board Power Supply

The daughter board uses TPS563201 DC/DC to generate 1.8V power source. The 1.8V is used to supply the FPGA Bank12/13/32/33 and the HDMI display chip ADV7513. Below image shows the hardware design of the TPS563201:

In default, please keep the jumper J3 **ON** to make the 1.8V power source supplied to Kintex-7 BANK12, BANK13, BANK32 and BANK33.

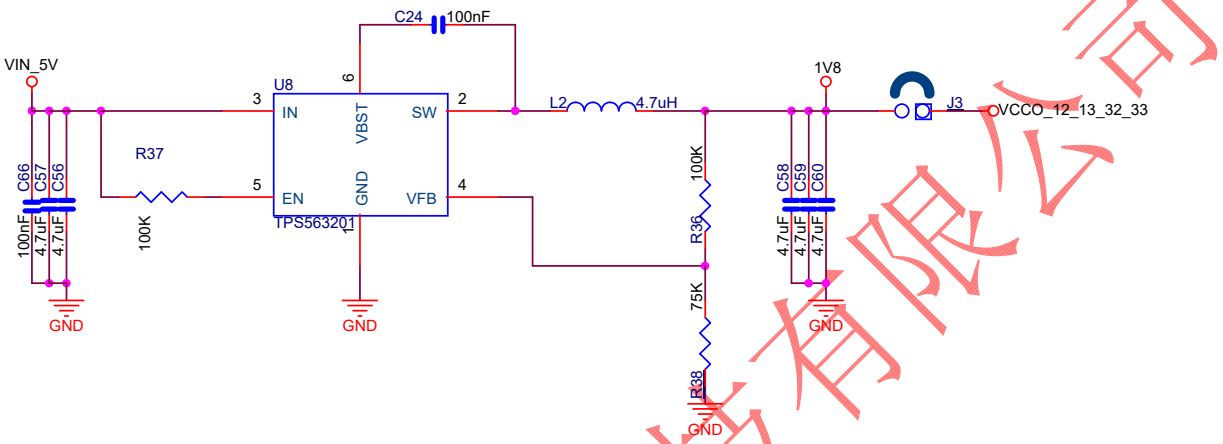

Figure 3-1. 1.8V Power Source

3.2 VGA Display Port

The RGB signal accepted by the color monitor is an analog signal, one for each color, in the range 0V to 0.7V according to the VGA spec. So the digital color signal generated by the video controller should be converted to an analog signal. The daughter board uses resistor to form a voltage divider circuit in combination with the 75 ohm load resistance of VGA monitor. Below image shows the hardware design.

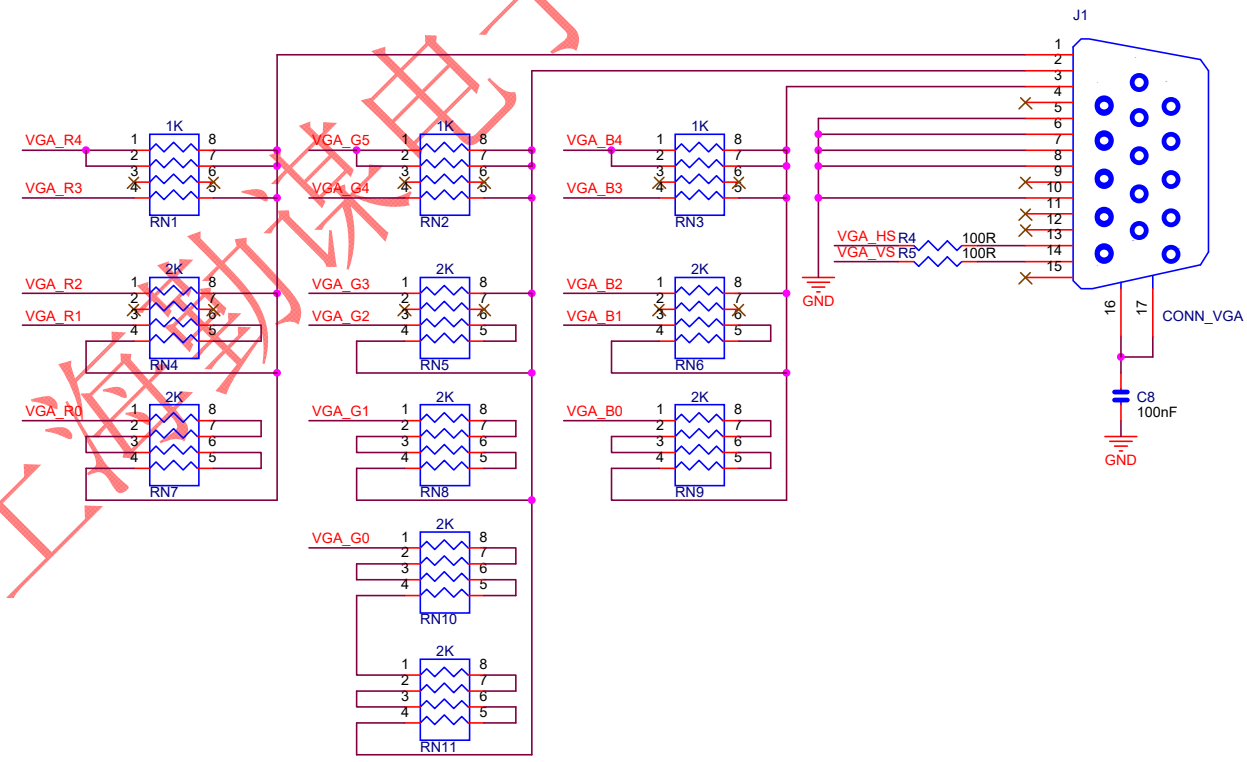

Figure 3-2. VGA Display Port

3.3 HDMI Display Port

The ADV7513 is a 165 MHz, High-Definition Multimedia Interface (HDMI®) transmitter. The digital video interface contains an HDMI v1.4 transmitter and supports 1 channel I2S audio. Below image shows the detailed hardware design:

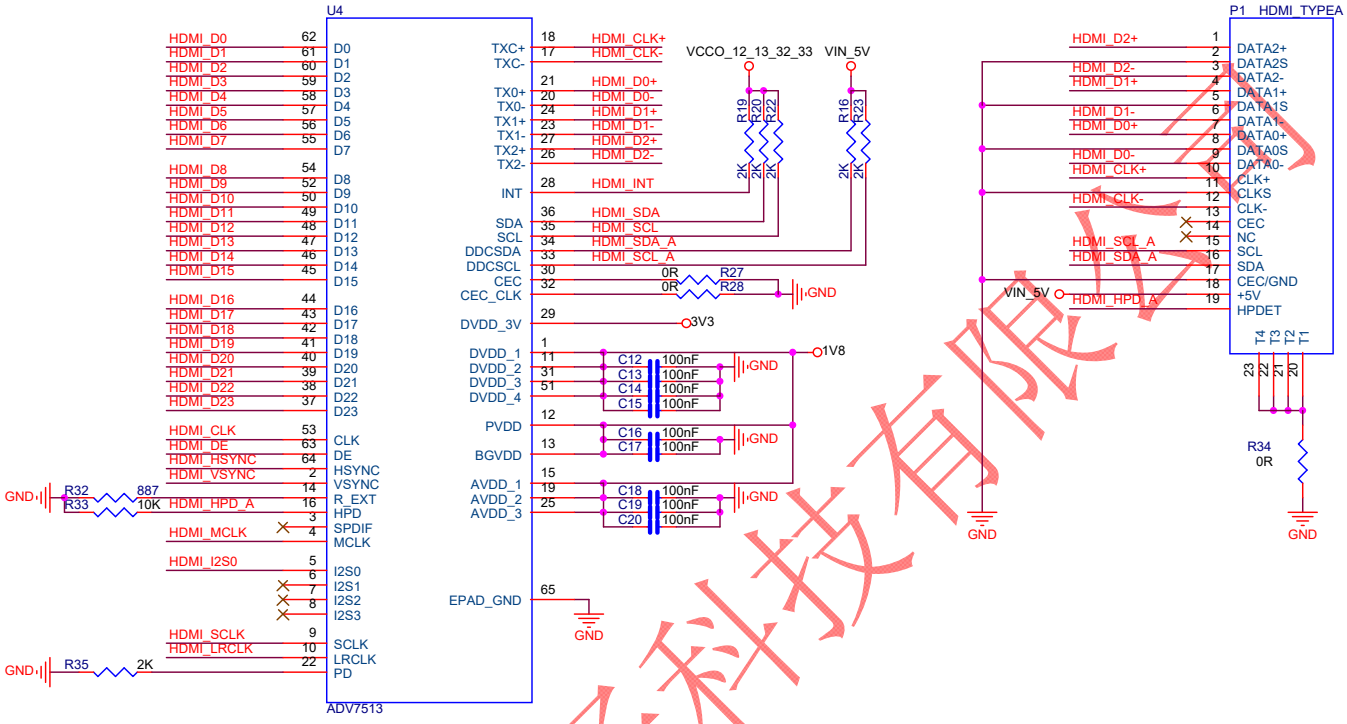

Figure 3-3. HDMI Display Port

3.4 MicroSD Slot

The daughter board provides a MicroSD card slot. Below images shows the hardware design:

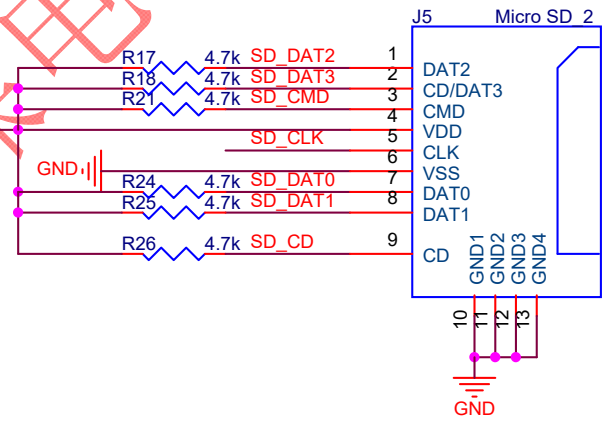

Figure 3-4. MicroSD Slot

3.5 8-Channel Level Shifter

The daughter boards provides 8-Channel level shifter. In default, the resistor R278 is not mounted. The B side of TXB0108 is working at 3.3V voltage level. The A side is working at 1.8V voltage level since the VCCO_12_13_32_33 is connected to 1.8V power source. Below image shows the hardware design:

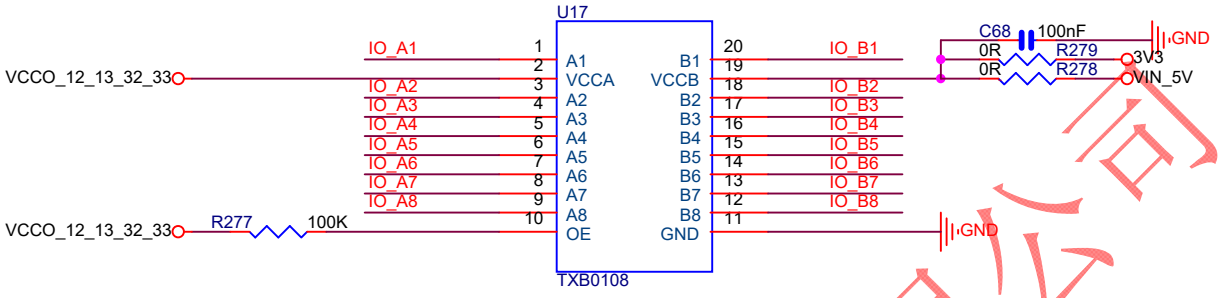

Figure 3-5. 8-Channel Level Shifter

3.6 PWM Audio Output

The daughter board provides PWM driven audio port. Each output channel contains one second-order low pass filter. Below image shows the detailed hardware design:

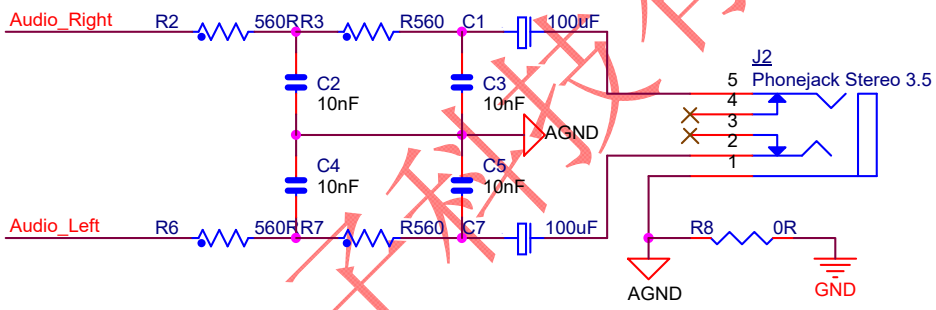

Figure 3-6. PWM Audio Output

4. Reference

[1] ug470_7Series_Config.pdf
[2] ds182_Kintex_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] S25FL256L_S25FL128L_256-MB_32-MB_128-MB_16-MB_3.0_V_FL-L_FLASH_MEMORY.pdf
[5] MT41K128M16.pdf
[6] TPS563201.pdf
[7] MP8712.PDF

5. Revision

Doc. Rev.	Date	Comments
0.1	01/01/2022	Initial Version.
1.0	07/01/2022	V1.0 Formal Release.