Hybrid Substrate by Fan-Out RDL-First Panel-Level Packaging

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***Abstract*— The panel-level redistribution-layer (RDL)-first fan-out packaging for hybrid substrate is studied. Emphasis is placed on the process, materials, design, and fabrication of: 1) heterogeneous integration of one large chip and one small chip with 50-μm pitch (minimum); 2) fine metal linewidth and spacing RDL-first substrate on a temporary panel carrier; 3) ordinary build-up package substrate on a panel; 4) hybrid substrate which is by soldering the RDL-first substrate on the build-up substrate; and 5) chips to hybrid substrate bonding and underfilling. Reliability assessment by thermomechanical simulation includes thermal cycling of the heterogeneous integration of the two-chip package on the hybrid substrate that is performed by a nonlinear temperature- and time-dependent finite-element analysis.**

***Index Terms*— Fan-out panel-level packaging, heterogeneous integration, hybrid substrate.**

I. Introduction

FIVE major applications have been identified by the semiconductor industry: 1) mobile such as smartphones, smartwatches, notebooks, wearables, tablets, and so on; 2) high-performance computing, also known as supercomputing, which is able to process data and perform complex calculations at high speeds on a supercomputer; 3) autonomous vehicle (or self-driving cars); 4) Internet of Things such as smart factory, smart health, and so on; and 5) big data (for cloud computing) and instant data (for edge computing). The system-technology drivers such as 5G (fifth generation technology standard for broadband cellular networks) and artificial intelligence (AI) are boosting the growths of these five semiconductor applications. Because of the drive of 5G and AI on these applications, the semiconductors' speed increases, density increases which require 2-μm redistribution layers (RDLs), bump pitch decreases to 50 μm, chip size increases, and power dissipation increases. All these provide challenges (opportunities) to advanced packaging technology such as the heterogeneous integration [1]–[3], which will be one of the focuses of this study.

2.5-D IC integration such as the through-silicon via (TSV) interposer is the best advanced packaging technology for extremely high density and performance applications. Unfortunately, because of making the TSVs, the cost of 2.5-D IC integration is very high. TSV-less interposer such as the 2.3-D IC integration is the alternative for very high performance and density applications.

TABLE I
METHOD FOR 2.3-D IC INTEGRATION

	2.3D IC Integration		
	SAP PCB	Fan-Out Chip-First	Fan-Out Chip-Last
Chip Size	Large	Medium	Large
Package Size	Large	Medium	Large
RDL Substrate (Metal L/S)	≧ 8μm	≧ 5μm	≧ 2μm
RDL Substrate (Layers)	≦10	≦ 4	≦ 6
Wafer Bumping	Yes	No	Yes
Chip-to-RDL Substrate bonding	Yes	No	Yes
Underfill or MUF	Yes	No	Yes
Build-up Package Substrate	Yes	Yes	Yes
Process Steps	More	Less	More
Performance	Medium	High	Very High
Cost	High	Medium	High
Applications	Medium performance	High performance	Very high performance

The 2.3-D IC integration is defined as fabricating an interposer (substrate) on a build-up package substrate. There are at least three methods to fabricate the coreless organic interposer, namely: 1) conventional semiadditive process (SAP)/printed circuit board (PCB) method [4]; 2) fan-out with chip-first method [5]–[7]; and 3) fan-out with RDL-first (chip-last) method [8]–[10]. Table I shows the comparison between these three methods. It can be seen that: 1) because of wafer bumping, chip-to-RDL substrate bonding, and underfilling, SAP/PCB [4] and fan-out with chip-last methods [5]–[7] are higher cost than the fan-out with chip-first method [8]–[10]; 2) on the other hand, SAP/PCB and fan-out with chip-last can house larger chips with larger package sizes; and 3) fan-out with chip-last method leads to the smallest metal linewidth and spacing of the RDL substrate. In this study, fan-out with chip-last process will be used.

The most unique feature of fan-out packaging technology is it needs a temporary carrier. The reason is because the saw street (spacing) between chips on a device wafer is very small (~50 μm) and there is not enough space to fan out the RDLs of the chip. Thus, for fan-out packaging, the device wafer is

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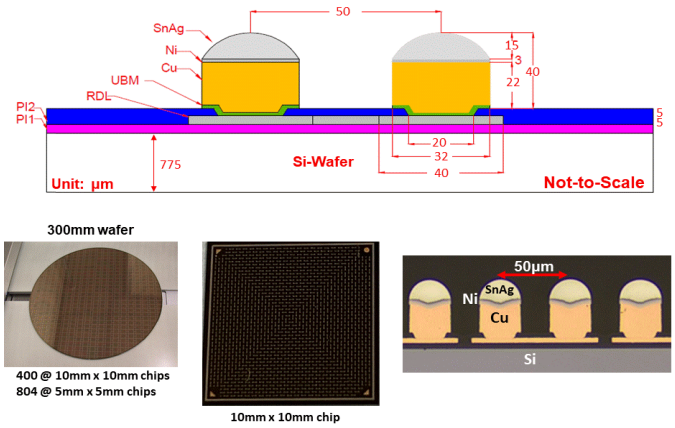

Fig. 1. Test chips with 50-μm pitch.

first tested and then diced into individual known good dies (KGDs). It is followed by picking and placing the KGDs on a temporary carrier (either round or rectangular) with certain distance apart. In the present study, in order to have a high throughput process, temporary rectangular panel [11]–[15] will be used for fabricating the RDLs.

The hybrid substrate consists of a fine metal L/S RDL substrate and an ordinary build-up package substrate. Because of the large RDL-substrate size (20 mm $\times$ 15 mm) with very fine metal L/S (2 μm/2 μm) of the three-layer RDLs, the substrate is fabricated by chip-last (or RDL-first) fan-out process. Also, in order to increase the throughput in making the RDLs, the temporary carrier is a glass rectangular panel (515 mm $\times$ 510 mm $\times$ 1.1 mm). After the RDLs are made, the carrier is diced into individual units. In parallel, the ordinary build-up substrate (23 mm $\times$ 23 mm) is fabricated on a 510 mm $\times$ 510 mm panel. Then, the fine L/S RDL-substrate individual unit is soldered on the ordinary build-up substrate and underfilled. It is followed by removing the temporary glass carrier. (The hybrid substrate is done.) Then, pick and place and bond the chips on top of the hybrid substrate. It is followed by underfilling and dicing of the panel into individual package. It should be noted that there is not any carrier transfer during the process.

II. Test Chips

The test chips are shown in Fig. 1. The dimensions of the large chip are 10 mm $\times$ 10 mm $\times$ 150 μm, and there are 3592 daisy-chained pads. The dimensions of the small chip are 5 mm $\times$ 5 mm $\times$ 150 μm with 1072 daisy-chained pads. For both chips, the pitch of the outer peripheral pads is 50 μm and of all the inner pads is 200 μm.

For both chips, the wafer bumping is with the standard physical vapor deposition (PVD) for seed layer and electrochemical deposition (ECD) for Cu-pillar and solder [16]. The wafers are then diced into individual bumped chips.

III. Heterogeneous Integration Test Package

Fig. 2(a) schematically shows the test package. It can be seen that there are two chips: Chip 1 (10 mm $\times$ 10 mm) and Chip 2 (5 mm $\times$ 5 mm). The gap (spacing) between Chip 1 and Chip 2 is 100 μm. The chips are bonded on the hybrid substrate which consists of the fine metal L/S RDL substrate (20 mm $\times$ 15 mm $\times$ 32 μm) and build-up substrate (23 mm $\times$ 23 mm $\times$ 1.3 mm), as shown in Figs. 2 and 3.

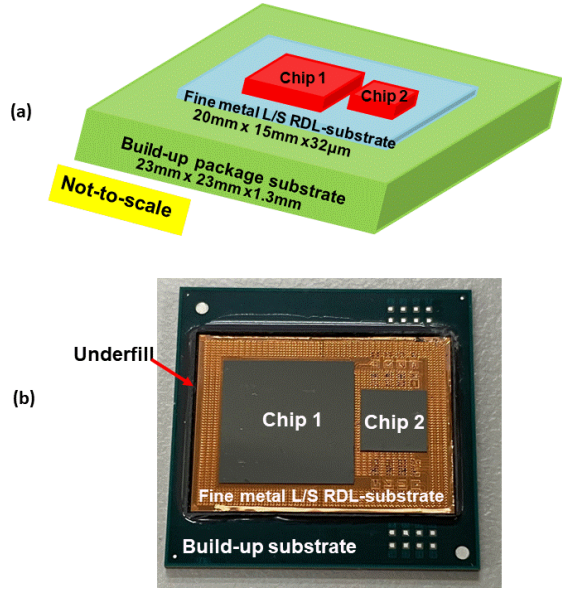

Fig. 2. (a) Schematic of the test package. (b) Assembled test package. Chips are bonded on the hybrid substrate which consists of the (20 mm $\times$ 15 mm) fine metal L/S RDL substrate and (23 mm $\times$ 23 mm) build-up substrate.

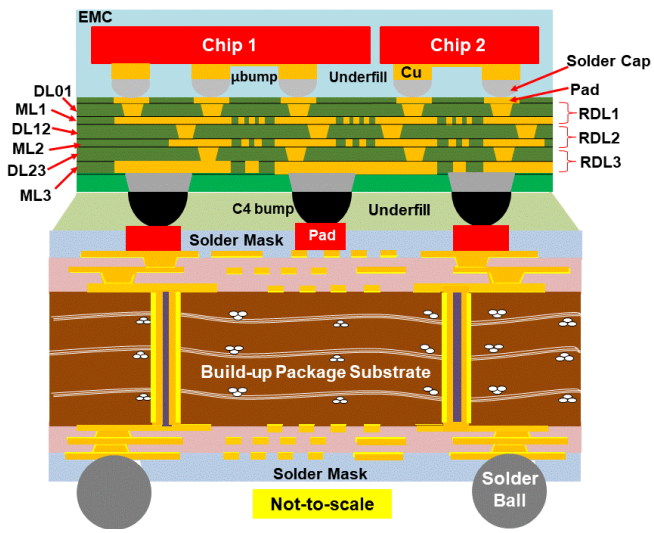

Fig. 3. Schematic of the cross section of the heterogeneous integration test package.

For both chips, the Cu pad dimensions are 40 μm $\times$ 40 μm, the Ti/Cu (0.1 μm/0.2 μm) under bump metallurgy (UBM) pad size is 32-μm diameter, and the PI2 (passivation) opening is 20-μm diameter. The diameter of the Cu-pillar is 32 μm and its height is 22 μm, and the height of the SnAg solder cap is 15 μm plus a 3-μm Ni-barrier.

There are three RDLs in the RDL substrate and each RDL consists of one metal layer (ML) and one dielectric layer (DL). Fig. 4(a) shows the definition and value of RDLx, MLx, DLxy,

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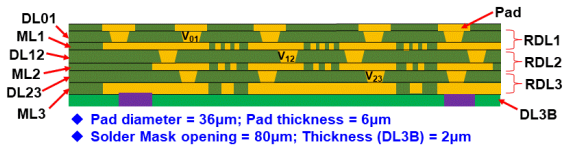

RDLs	Key Elements of RDL	Value	Line width (L) / Spacing (S)
RDL1	ML1 (Metal layer 1)	3μm	2/2μm
	DL01 (Dielectric layer between the contact pad and ML1)	3μm	NA
	V_{01} (Via opening between contact pad and ML1)	10μm	NA
RDL2	ML2 (Metal layer 2)	5μm	5/5μm
	DL12 (Dielectric layer between ML1 and ML2)	6μm	NA
	V_{12} (Via opening between ML1 and ML2)	20μm	NA
RDL3	ML3 (Metal layer 3)	5μm	10/10μm
	DL23 (Dielectric layer between ML2 and ML3)	4μm	NA
	V_{23} (Via opening between ML2 and ML3)	18μm	NA

(a)

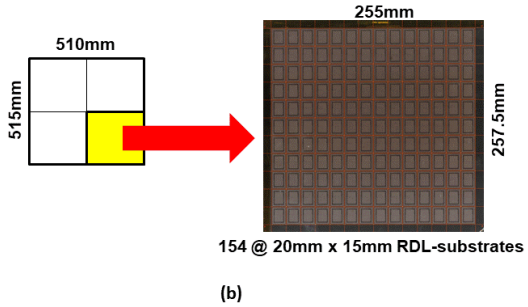

Fig. 4. (a) Fine metal *L*/*S* RDL substrate. (b) Panel for fabricating the RDL-substrate and the fabricated one.

V*xy*, and *L*/*S*. The solder resist opening and thickness are, respectively, 80 and 2 μm.

The temporary panel for fabricating the RDL substrate is shown in Fig. 4(b). It can be seen that the panel size is 515 mm $\times$ 510 mm $\times$ 1.1 mm and is made of glass with a coefficient of thermal expansion (CTE) equals to 8.5×10^{-6}/°C. The panel is divided into four strips and each strip (257.5 mm $\times$ 255 mm) has 154 (20 mm $\times$ 15 mm) RDL substrates. Thus, in one shot, it can make RDL substrates for 1232 chips in 616 heterogeneous integration packages.

Fig. 5 shows the top side and bottom side of the hybrid substrate.

1) On the top side, there are $3592 + 1072 = 4664$ pads, Fig. 5(a), which are for bonding the chips to the substrate.
2) On the bottom side, there are 4039 solder ball pads (105-μm diameter) on a 0.225-mm pitch, Fig. 5(c), which are solder mask defined (SMD) and its opening is 80 μm. These pads are for $Sn_3Ag_{0.5}Cu$ lead-free C4 solder bump mounting and the solder ball diameter is 80 μm.

IV. Hybrid Substrate Fabrication

The key process steps for making the hybrid substrate, RDL-first substrate, and build-up package substrate are shown in Fig. 6.

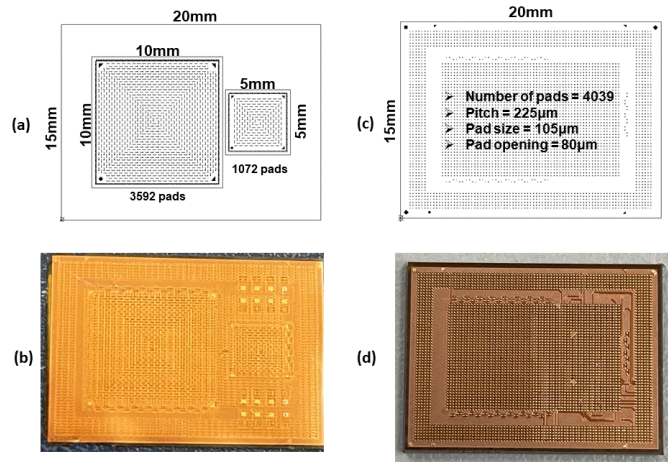

Fig. 5. (a) Schematic of the top view of RDL substrate. (b) Top view of the fabricated RDL substrate. (c) Schematic of the bottom view of RDL substrate. (d) Bottom view of the fabricated RDL substrate.

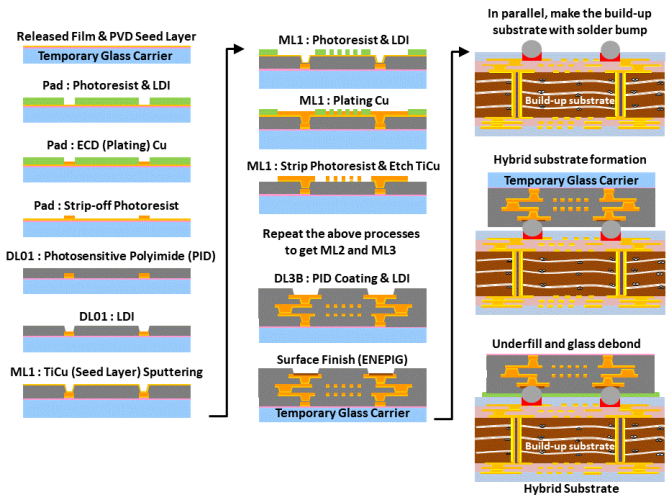

Fig. 6. Key steps to fabricate the hybrid substrate (fine metal *L*/*S* RDL substrate + build-up substrate).

A. RDL-First Substrate Fabrication

A released film (sacrificial layer) is slit coating on a glass panel and then a Ti/Cu seed layer is deposited on the top, as shown in Fig. 6. The thickness of the sacrificial layer is 1 μm and it is a light-to-heat conversion film. The contact pad can be obtained by photoresist, laser direct imaging (LDI), development, ECD Cu, and stripping off the photoresist. Then, a photoimageable dielectric (PID) is slit coating and the first DL DL01 of RDL1 is obtained by LDI. It is followed by PVD the Ti/Cu, photoresist, LDI and development, ECD the Cu, strip off the photoresist, and etch off the TiCu to obtain the first ML ML1 of RDL1. Fig. 5(b) shows the image of the RDL1 through the glass carrier. DL12 and ML2 of RDL2, and DL23 and ML3 of RDL3 can be obtained by repeating the same process steps.

The solder mask (passivation) can be obtained by slit coating a PID and LDI. Then, the surface is finishing with electroless nickel electroless palladium immersion gold (ENEPIG).

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TABLE II
RDLs: DESIGN VERSUS MEASUREMENT VALUES

RDLs	Items	Design (μm)	Measured (μm)
Metal of RDL1 (ML1)	Linewidth (L)	2	2.07, 2.08, …
	Spacing (S)	2	1.74, 1.81, …
	Thickness (H)	3	2.06, 2.17, …
Metal of RDL2 (ML2)	Linewidth (L)	5	5.6, 6.03, …
	Spacing (S)	5	3.91, 4.5, …
	Thickness (H)	5	4.35, 4.48, …
Metal of RDL3 (ML3)	Linewidth (L)	10	10.24, 10.69, …
	Spacing (S)	10	9.46, 10.18, …
	Thickness (H)	5	3.39, 5.11, …

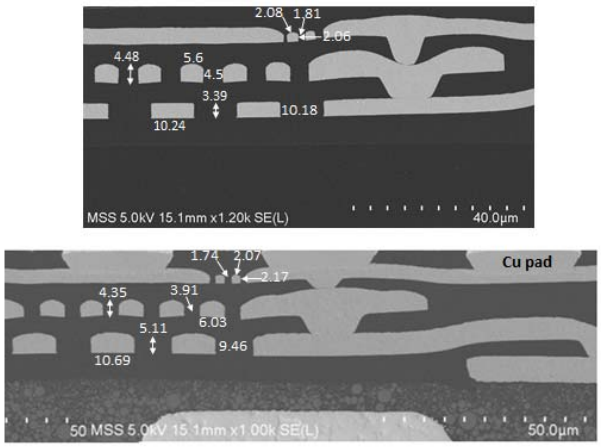

Fig. 7. Cross sections of SEM image of RDL substrate.

The fabrication of the fine metal L/S RDL substrate is completed. The bottom side of the RDL-substrate is shown in Fig. 5(d).

The SEM images of the RDL substrate are shown in Fig. 7. Table II shows the L, S, and thickness (H). For RDL1, $L = 2.07$ and 2.08 μm (not exactly 2 μm), $S = 1.74$ and 1.81 μm (not 2 μm), and $H = 2.06$ and 2.17 μm (not 3 μm). For RDL2, $L = 5.6$ and 6.03 μm (not 5 μm), $S = 3.91$ and 4.5 μm (not 5 μm), and $H = 4.35$ and 4.48 μm (not 5 μm). For RDL3, $L = 10.24$ and 10.69 μm (not 10 μm), $S = 9.46$ and 10.18 μm (not 10 μm), and $H = 3.39$ and 5.11 μm (not 5 μm). Thus, there are rooms for improvements such as use better PID, higher resolution LDI, or a stepper.

B. Fabrication of Build-Up Package Substrate

The package substrate (23 mm × 23 mm × 1.3 mm) is a 2–2–2 structure, as schematically shown in Fig. 8(a). There are 4039 pads on a 0.225-mm pitch on each substrate, which is made on a 510 mm × 510 mm panel, Fig. 8(b), by a conventional method. The image of the 2–2–2 build-up substrate is shown in Fig. 8(c). It can be seen that for the through via, the open size is 200 μm and the depth is 820 μm, and for the stacked via, the open size is 60 μm and the depth is 30 μm. The top side and bottom side of the fabricated build-up package substrate panel are shown in Fig. 8(d) and (e), respectively.

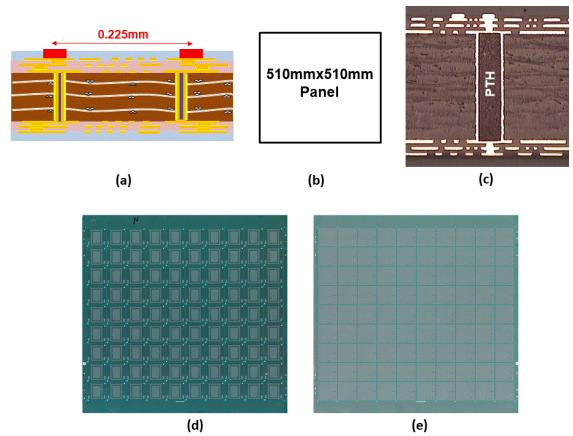

Fig. 8. 2–2–2 panel. (a) Schematic. (b) Panel size. (c) Cross section image. (d) Top view of the fabricated build-up substrate. (e) Bottom view of the fabricated build-up substrate.

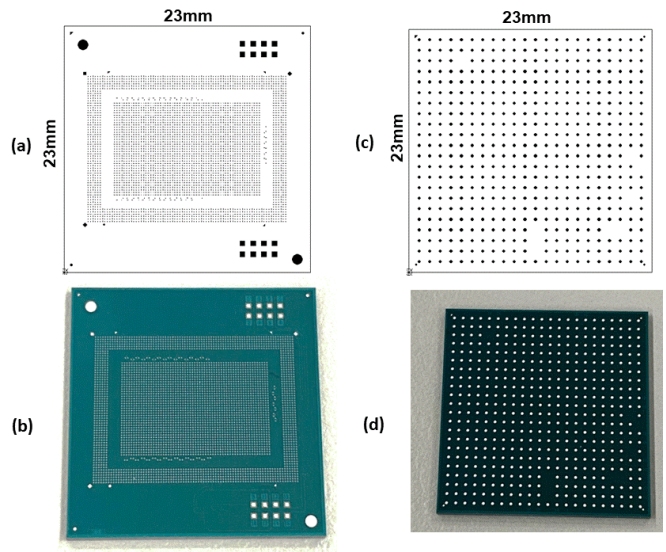

Fig. 9. Individual build-up package substrate. (a) Top side. (b) Fabricated top side. (c) Bottom side. (d) Fabricated bottom side.

Fig. 9 shows the individual build-up package substrate. Fig. 9(a) and (b) shows, respectively, the schematic and fabricated top side of the package, while Fig. 9(c) and (d) shows, respectively, the schematic and fabricated bottom side of the package. There are 475 pads with 1-mm pitch on the bottom side of the package. The pad size is 500 μm and is SMD with the solder mask opening = 300 μm.

C. C4 Bump Formation

The C4 bumps are fabricated by stencil printing a $Sn_3Ag_{0.5}Cu$ solder paste with a 29-μm-thick stainless steel stencil on the build-up package substrate. During solder-reflow process, due to the surface tension of the molten solder, which creates smooth truncated spherical 30-μm diameter solder bumps, as shown in Fig. 10.

D. Warpage Measurements

The warpage of the build-up package substrate (BU), fine metal L/S RDL substrate with glass carrier RDL (G), and fine

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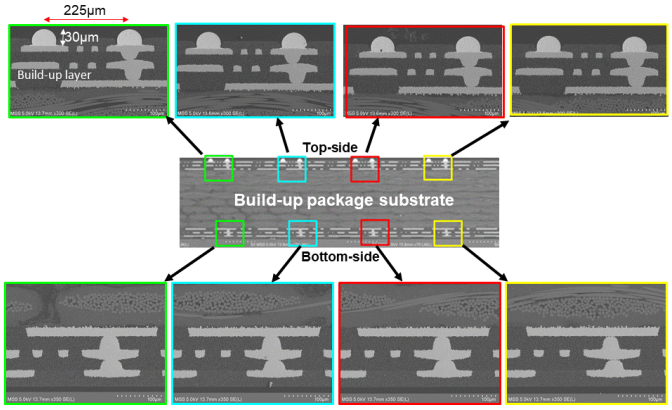
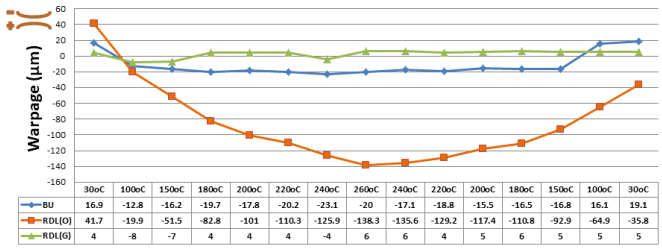


Fig. 10. SEM images of the fabricated package substrate with C4 bumps.



	30oC	100oC	150oC	180oC	200oC	220oC	240oC	260oC	240oC	220oC	200oC	180oC	150oC	100oC	30oC
BU	16.9	-12.8	-16.2	-19.7	-17.8	-20.2	-23.1	-20	-17.1	-18.8	-15.5	-16.5	-16.8	16.1	19.1
RDL(O)	41.7	-19.9	-51.5	-82.8	-101	-110.3	-125.9	-138.3	-135.6	-129.2	-117.4	-110.8	-92.9	-64.9	-35.8
RDL(G)	4	-8	-7	4	4	4	-4	6	6	4	5	6	5	5	5

Fig. 11. Shadow Moire warpage measurement of build-up substrate (BU), fine metal *L*/*S* RDL substrate on glass carrier RDL(G), and fine metal *L*/*S* RDL substrate on organic carrier RDL(O).

metal *L*/*S* RDL substrate with organic carrier RDL (O) at various temperatures has been measured by the shadow Moiré method via the TherMoire Platform. The results are shown in Fig. 11. It can be seen that the warpage of BU and RDL (G) is very small. However, the warpage of RDL (O) is very large compared with the others. (This is because the thermal expansion mismatch between the glass carrier and the RDL substrate is smaller than that between the organic carrier and the RDL substrate.) Thus, in this study, the hybrid substrate will be formed by the combination of the build-up package substrate and the fine metal *L*/*S* RDL substrate with the temporary glass carrier.

E. Hybrid Substrate Formation

Now that we have the fine metal *L*/*S* RDL substrate with glass carrier and the build-up package substrate with solder bumps ready, it is time to fabricate the hybrid substrate, as shown in Fig. 6. First, identify the location of the bumps on the package substrate and the pads on the RDL substrate with glass carrier by using a lookup and lookdown camera; second, apply flux on both the bumps and pads; and third, pick and place the RDL substrate with glass carrier on the package substrate and then reflow. The top view of an assembled hybrid substrate is shown in Fig. 12. A typical SEM image of the hybrid substrate is shown in Fig. 13 and close-up images are shown in Fig. 14. It can be seen that the fine metal *L*/*S* RDL substrate, solder joints, underfill, and the build-up package substrate are properly assembled.

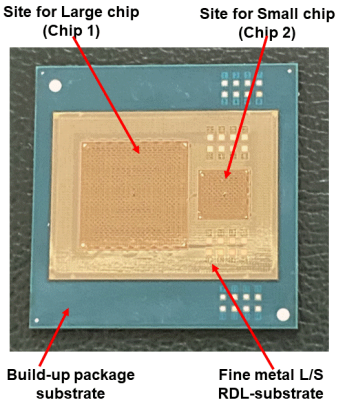


Fig. 12. Hybrid substrate = fine metal *L*/*S* RDL substrate with glass carrier soldered on the build-up package substrate.

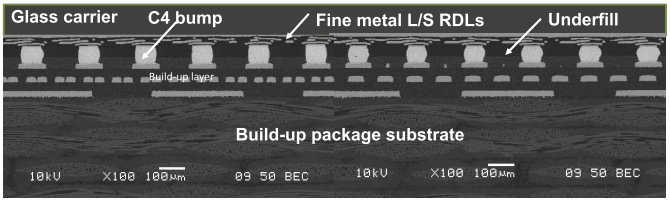


Fig. 13. Cross section image of the hybrid substrate.

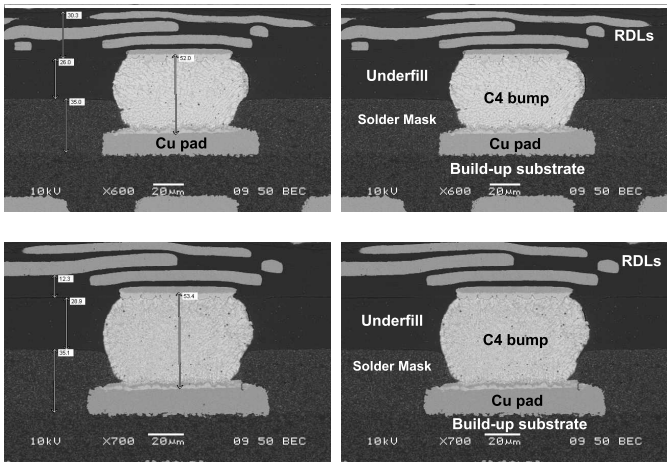


Fig. 14. Close-up look at the cross section SEM images of the hybrid substrate.

V. Final Package Assembly

A. Remove the Temporary Glass Panel

Before the final package assembly, we have to debond the glass panel to expose the bonding pads on the fine metal *L*/*S* RDL substrate, as shown in Fig. 6. By scanning a laser with 355 nm of wavelength on the glass, the sacrificial layer will become a powder and the glass carrier is removed. Then, chemicals clean the surface.

B. Chips-to-Hybrid Substrate Bonding

Now that we have the microbumped chips (Fig. 1) and the hybrid substrate (Figs. 12–14) ready, it is time to do the final

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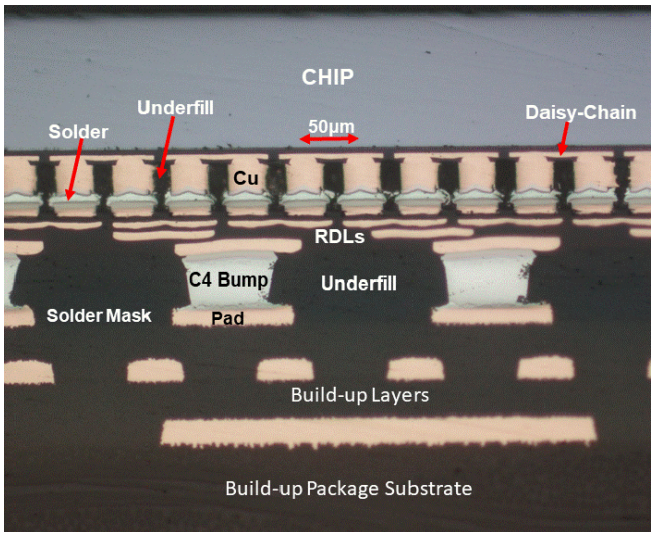

Fig. 15. Heterogeneous integration of two-chip package on the hybrid substrate which is the fine metal L/S RDL substrate and build-up substrate.

assembly. First, identify the location of the microbumps on the chips and the bonding pads on the hybrid substrate by using a lookup and lookdown camera; second, apply flux on both the bumps and pads; and third, pick and place the chips on the hybrid substrate and then reflow. The assembled two-chip package is shown in Fig. 2(b).

C. Underfill

The curing temperature, time, and CTE of the underfill are, respectively, 160 °C, 2 h, and 22×10^{-6}/°C ($<Tg = 115$ °C). Fig. 15 shows a typical cross section, which can be seen that the chip, microbumps, underfill, RDL substrate, C4-bumps, and build-up package substrate are properly done.

VI. Thermal Cycling Simulation

A. Finite Element Modeling

A 2-D generalized plane-strain finite element modeling, as shown in Figs. 16 and 17, is performed. Fine meshes are used for critical locations such as microbump solder joints I–IV connecting the chips and the RDL substrate (I and II are the corner solder joints of Chip 1, and III and IV are the corner solder joints of Chip 2) and the C4-bump solder joints V and VI connecting the RDL substrate and the build-up package substrate (V and VI are the corner solder joints of the RDL substrate). The three-layer RDL substrate consists of the Cu conductor layers and the PID DLs, which is represented as an equivalent block.

B. Material Properties for Simulation

Table III shows the material properties for modeling. All the materials are assumed to be constant except $Sn_3Ag_{0.5}Cu$ which is time and temperature dependent and its constitutive equation is also shown in Table III.

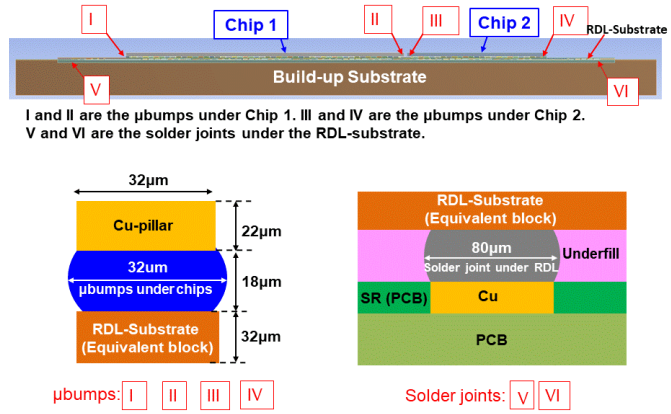

Fig. 16. Structure and μbump joints and solder joints.

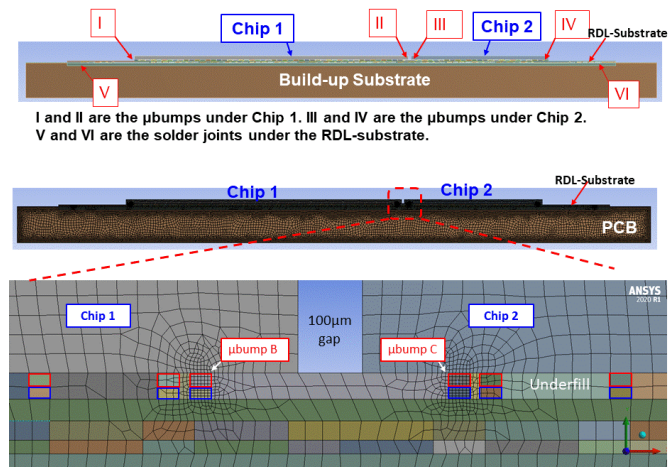

Fig. 17. FEM of the heterogeneous integration assembly of two chips on hybrid substrate.

TABLE III
Material Properties for Simulation

Materials	CTE (10^{-6}/°C)	Young's Modulus (GPa)	Poisson's Ratio
Copper	16.3	121	0.34
PCB	$\alpha_x = \alpha_y = 18$ $\alpha_z = 70$	$E_x = E_y = 22$ $E_z = 10$	0.28
Solder Mask (RDL)	7.0	7.0	0.3
Solder	21 + 0.017T(°C)	49 - 0.07T(°C)	0.3
EMC(ABF)	7.0	7.0	0.3
Silicon	2.8	131	0.278
Solder Mask (PCB)	39	4.1	0.3
RDL Equiv. block	14.08	70.53	0.32
Underfill	50	4.5	0.35

The constitutive equation of solder: $\frac{d\varepsilon}{dt} = 500000[sinh(0.01\sigma)]^5 exp\left(-\frac{5800}{T}\right)$
where T is in Kelvin and σ is in MPa.

C. Kinetic Boundary Condition

Fig. 18 shows the temperature boundary condition for simulation. The temperature is −40 °C ⇆ 85 °C. The cycle time is 60 min and the ramp-up, ramp-down, dwell-at-hot, and dwell-at-cold are each 15 min. The stress-free is at room temperature.

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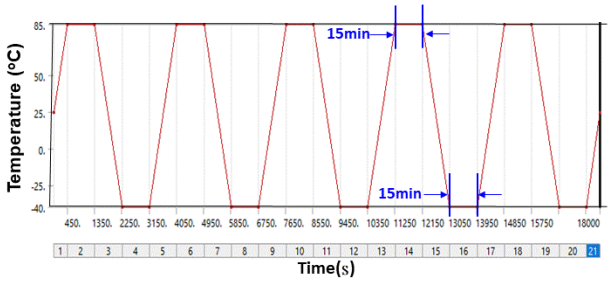

Fig. 18. Temperature boundary condition.

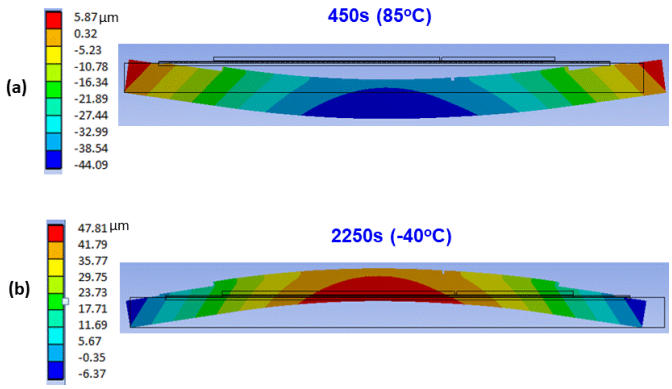

Fig. 19. Undeformed shape (dark lines) and deformed shape (color contours). (a) At 450 s (85 °C). (b) At 2250 s (−40 °C).

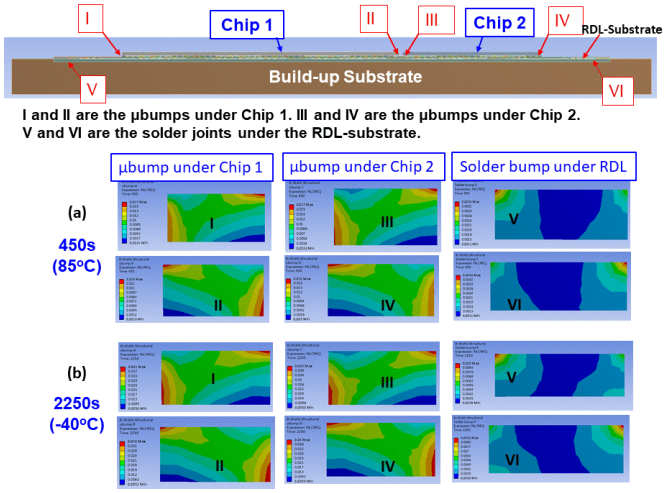

Fig. 20. Accumulated creep strain contour distributions in μbump joints I–IV and solder joints V and VI.

D. Simulation Results—Deformation

The deformed shape and undeformed shape of the assembly are shown in Fig. 19. At 450 s (85 °C), the hybrid substrate expands more than the chips and the structure is deformed in a concave shape (smiling face), Fig. 19(a). At 2250 s (−40 °C), the hybrid substrate shrinks more than the chips and the structure is deformed into a convex shape (crying face), Fig. 19(b).

E. Simulation Results–Accumulated Creep Strain

The accumulated creep strain contour distributions at the critical microbump solder joints I–IV and the critical C4-bump solder joints V and VI are shown in Fig. 20 and the maximum accumulated creep strain time history at these locations are shown in Fig. 21. It can be seen that the maximum accumulated creep strain occurs near the corner of the solder joints I–VI. Also, the maximum accumulated creep strain per cycle in the microbump solder joints I–IV is at least three times larger than that in the C4-bump solder joints V and VI. This is because the thermal expansion mismatch between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate. Also, the solder volume of the microbump solder joints is smaller than that of the C4-bump solder joints. Furthermore, the stiffness of the microbump could be larger than that of the C4-bump.

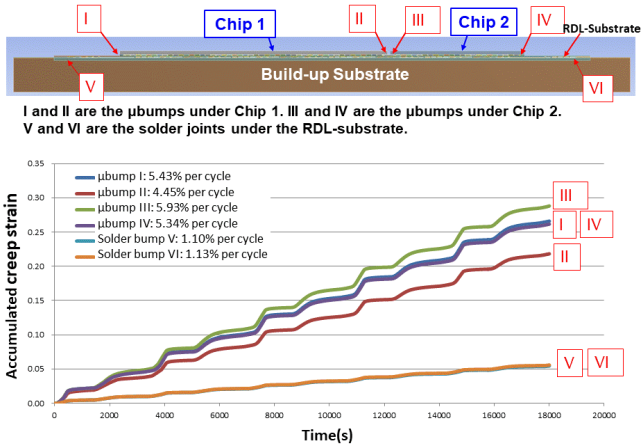

Fig. 21. Accumulated creep strain time history in μbump joints I–IV and solder joints V and VI.

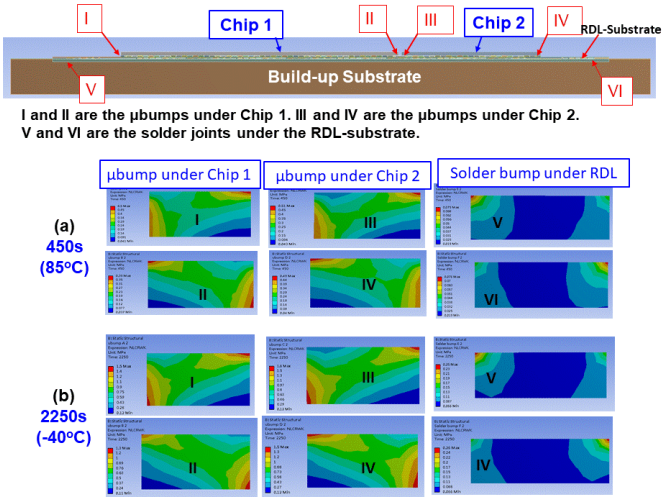

Fig. 22. Creep strain energy density contour distributions in μbump joints I–IV and solder joints V and VI.

The maximum accumulated creep strain per cycle in the microbump solder joints is 5.93% and it occurs at a very small area. Thus, this structure should be reliable for most operating conditions.

F. Simulation Results—Creep Strain Energy Density

The creep strain energy density contour distributions at the microbump solder joints I–IV and the C4-bump solder

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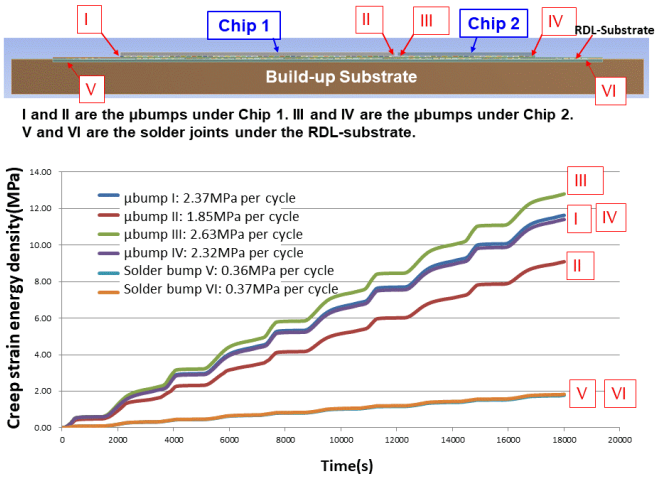

Fig. 23. Creep strain energy density time history in μbump joints I–IV and solder joints V and VI.

joints V and VI are shown in Fig. 22 and the maximum creep strain energy density time history at these solder joints are shown in Fig. 23. It can be seen that the maximum creep strain energy density occurs near the corner of the solder joints I–VI. Also, the maximum creep strain energy density per cycle in the microbump solder joints I–IV is at least five times larger than that in the C4-bump solder joints V and VI. Again, this is because the thermal expansion mismatch between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate.

The maximum creep strain energy density per cycle in the microbump solder joints is only 2.63 MPa and it occurs at a very small area. Again, this structure should be reliable for most operating conditions.

VII. Conclusion

Some important results are summarized as follows.

1) The feasibility of the design, materials, process, and fabrication of a heterogeneous integration of two chips with 50-μm pitch on a hybrid substrate by a fan-out RDL-first panel-level packaging has been demonstrated.
2) In order to increase throughput, the fine metal L/S (2 μm/2 μm) RDL substrate has been fabricated on a temporary glass panel.
3) The hybrid substrate has been fabricated by soldering the fine metal L/S RDL substrate on a build-up package substrate and underfilled.
4) The 50-μm pitch microbumped chips are bonded to the hybrid substrate and underfilled. There is not any carrier transferred.
5) Reliability of the assembly has been demonstrated by the thermal cycling simulation. It is found that: a) the creep response of the microbump solder joints between the chips and the RDL substrate is larger than that between the RDL substrate and the build-up package substrate and b) the maximum creep responses pre cycle are too small and localized to create reliability concerns in most operating conditions for mobile products.

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