Reliability Challenges of High-Density Fan-out Packaging for High-Performance Computing Applications

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2022 IEEE 72nd Electronic Components and Technology Conference (ECTC) | 978-1-6654-7943-1/22/$31.00 ©2022 IEEE | DOI: 10.1109/ECTC51906.2022.00232

***Abstract*—As the cost of advanced silicon nodes continue to rise, high-performance devices are shifting towards advanced packaging to reduce the overall cost, increase functionality, and improve performance. Fan-out packaging technology is an advanced packaging approach that has increasingly been adopted for networking, artificial intelligence, and high-performance computing (HPC) applications. Fan-out technology enables multi-chip integration using fine pitch and small line width copper redistribution layer (RDL) technology to interconnect different dies resulting in a flexible and cost-effective package solution. However, as the fan-out package size increases to accommodate higher I/O counts and higher bandwidth, package warpage and reliability become more challenging. The main challenges in building large size packages (⩾65x65mm2) with fan-out technology are warpage, RDL integrity, and package reliability. In this paper, we discuss the reliability assessment of a 1.6X reticle size integrated fan-out multi-chip assembly on large organic substrates for networking applications. The package integrates a 7 nm ASIC die and 8 I/O chiplets with 3 layers of fine-pitch RDL interconnection. The coefficient of thermal expansion (CTE) mismatch between different materials in the package structure can cause the device to warp and induce mechanical stresses that can cause RDL cracking and other failures in the package. We will discuss package design and processing methods for improving RDL integrity to enhance overall package reliability. By using finite element stress analysis to optimize the RDL design, robust large format multi-chip fan-out packages were developed and validated through reliability testing.**

Keywords-wafer level fan-out; redistribution layer (RDL); high performance computing (HPC); reliability

I. INTRODUCTION

The continuous drive for higher compute power and greater data bandwidth to meet the growing data demands from data centers, networking, and artificial intelligence has driven the development of advanced packaging solutions for higher performance devices. Since single advanced node system on chip (SOC) can no longer meet the increasing demands of HPC applications, there is a growing trend to use a chiplet architecture approach to split a large, monolithic die into multiple smaller functional blocks, called chiplets, and re-integrating the chiplet dies using advanced packaging. Chiplet architecture not only can bring the different functional blocks closer to each other to improve device performance but also can improve individual die yields and help reduce the overall device cost [1-6].

Among the advanced packaging technologies, wafer level fan-out has emerged as an attractive package solution for heterogenous integration. Wafer level fan-out, which uses fine-pitch RDL technology for die interconnection, can enable the development of high-performance products with large package footprint, and high interconnect density. Although silicon interposers had been widely used in the past for high end server products, silicon interposers which utilize through-silicon via (TSV) technology have high manufacturing cost. Wafer level fan-out with fine-pitch RDL is emerging as a lower cost alternative package solution.

However, package reliability is becoming a critical concern as the overall die size and package size increase to accommodate the integration of more chiplets for networking and high-performance applications. As the die size increases, the package stress also increases due to the CTE mismatch between the die and the substrate and increases the risk for package failures caused by bump cracks, mold compound delamination, and RDL failures in the fan-out package.

Our study assessed the reliability of large format fan-out packages assembled with an ASIC die and 8 I/O chiplets using the chip-first approach. The package robustness was investigated using stringent component-level reliability testing, which include temperature cycling (TC), an unbiased highly accelerated temperature stress test (uHAST), and a high-temperature storage (HTS) test.

II. PACKAGE DESCRIPTION

In our study, multi-chip fan-out packages with an integrated fan-out die size of 1.6X reticle size were evaluated. The fan-out package integrated the ASIC die and 8 I/O chiplets with 3 layers of RDL interconnections. The fan-out die module was 41 X 33 mm2 and was assembled on low loss organic substrates with sizes 74 X 74 mm2 and 91 X 91 mm2 as shown in Figure 1. Both packages used a copper stiffener ring for warpage control. The key attributes of the test vehicles are summarized in Table 1. The fan-out module was built using a process, where the different dies were attached to a temporary carrier and molded with epoxy mold compound to form a reconstituted wafer. After molding, the multi-layer RDL lines and C4 bumps were

2377-5726/22/$31.00 ©2022 IEEE
DOI 10.1109/ECTC51906.2022.00232

formed to create the fan-out die structure as shown in Figure 2. Since the different dies were directly connected to the RDL through the copper vias, the fan-out structure does not require the use of micro bumps or underfill between the die and the RDL layers.

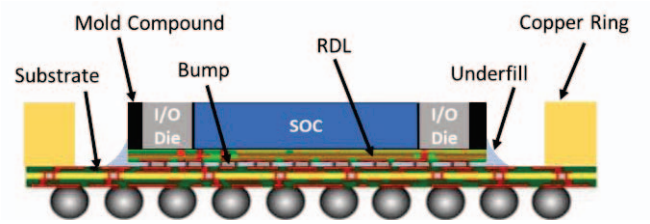


Figure 1. Cross section of fan-out package

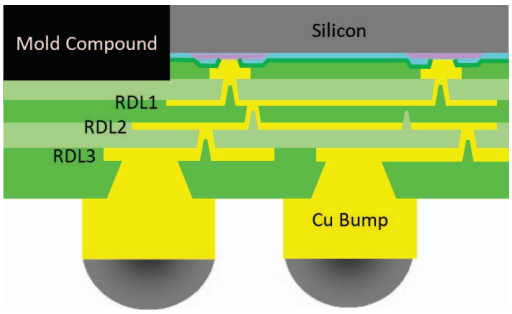


Figure 2. Cross section of RDL structure

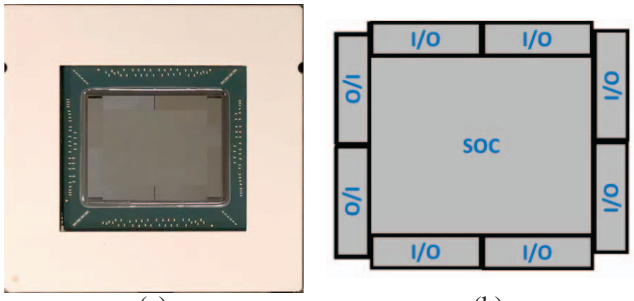
The fan-out package and floor plan are shown in Figure 3. In the package, the SOC was connected to 8 identical I/O dies with 3 RDL layers with line width and spacing of 2/2 um for the first two layers and 5/5 um for the third layer. After building the fan-out module, the integrated die was attached to an organic substrate using 130 um pitch copper pillar bumps. The key attributes for the fan-out module are shown in Table II.

TABLE I. PACKAGE ATTRIBUTES

Attribute	TV1	TV2
Fan-out Module Size (mm2)	41.3 x 33.6	41.3 x 33.6
Die Size (mm2)	SoC: 31.5 x 23.8 I/O die: 15.5 x 4	SoC: 31.5 x 23.8 I/O die: 15.5 x 4
Substrate Size (mm2)	74 x 74	91 x 91
Core Thickness (mm)	1.4	1.4
Ring Thickness (mm)	2.5	2.5
Ring Foot Width (mm)	13/10	17/19

TABLE II. FAN-OUT MODULE ATTRIBUTES

Attribute	Dimension
Fan-out Module Size (mm2)	41.3 x 33.6
Die Size (mm2)	SoC: 31.5 x 23.8 I/O die: 15.5 x 4
D2D Gap (um)	60
RDL Layer Count	3X
RDL W/S (um)	RDL1: 2/2 RDL2: 2/2 RDL3: 5/5
C4 bump Pitch (um)	130



. (a) (b)

Figure 3. (a) Fan-out package assembled on 91 X 91 mm2 substrate with stiffener ring; (b) Fan-out module floor plan

III. RESULTS AND DISCUSSION

A. *Package Warpage Assessment*

Since warpage will affect solder joint quality, shadow moiré was performed to characterize warpage variations over temperature of the fan-out module. The samples were measured from room temperature up to 250°C to simulate the solder joint reflow temperature and then down to room temperature. The simulated fan-out module warpage values closely matched the experimental data as shown in Figure 4. The fan-out module had a 69 um convex warpage shape at room temperature but changed to a -20 um concave shape at 250°C. X-ray analysis showed the C4 bumps have good solder joint formation as shown in Figure 5.

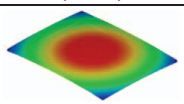
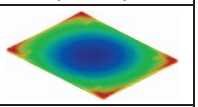
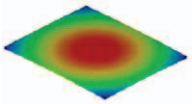
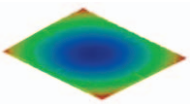
		Room Temp (25°C)	High Temp (250°C)
Warpage (+) Convex	Modeling		
		73 um	-22 um
(-) Concave	Exp.		
		69 um	-20 um

Figure 4. Fan-out module warpage contour plots

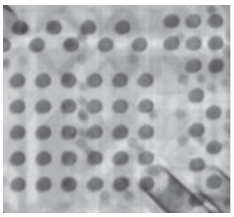


Figure 5. X-ray of C4 joints near die corner

The assembled package warpage is shown in Figure 6. Both TV1 and TV2 had a convex warpage shape at room temperature but turned to a concave shape at 250°C. The 91X91 mm2 package had 30% higher warpage at room temperature than the 74X74 mm2 package. At 250°C, the 91X91 mm2 package warpage was 60% higher compared to the 74X74 mm2 package.

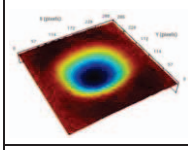
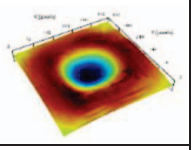
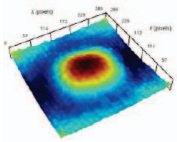
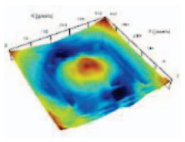
Test Vehicle		TV1	TV2
Package Size (mm2)		74 X 74	91 X 91
Warpage @ 25°C (+)	Exp.		
		1x	1.3X
Warpage @ 250°C (-)	Exp.		
		1x	1.6X

Figure 6. Package warpage contour plots

B. C4 Bump Reliability Assessment

Temperature cycling accelerates the thermo-mechanical failures caused by CTE mismatch. C4 bump joint crack risk increases as the fan-out module size increases. Finite element analysis (FEA) showed the bumps at the die corner experience the highest stress and are at the greatest risk for cracking as shown in Figure 7. Both fan-out package test vehicles passed temperature cycling testing without any C4 bump failures.

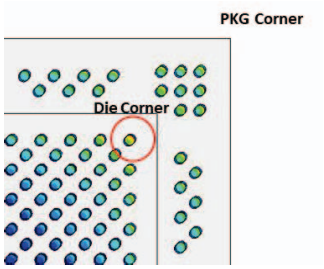


Figure 7. Copper pillar bump at die corner.

C. RDL Trace Reliability Assessment

The CTE differences between the dielectric materials and copper lines in the RDL structure cause copper/dielectric interface distortion during temperature cycling which can result in RDL trace cracking. Figure 8. shows the die to die (D2D) routing areas where the high density RDL lines interconnect the dies. Stress analysis showed the RDL traces between the gap of the dies experience high stress due to the low CTE and high modulus of the silicon die constraining the thermal expansion and shrinkage of the copper lines [7]. The smaller the gap, the more the RDL line is constrained by the silicon die and the higher the stress in the copper line, which increases the RDL trace crack risk.

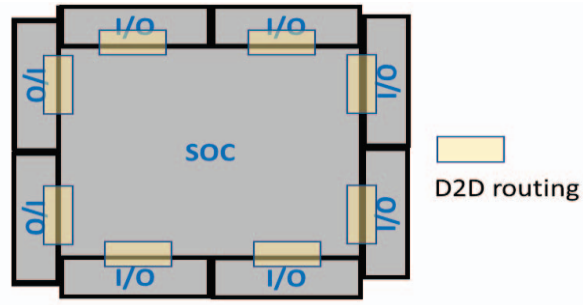


Figure 8. D2D RDL routing areas

After TV1 and TV2 underwent multi-reflow testing at 250°C, package failures were observed to have trace cracking in the RDL lines. The trace cracks were typically observed in the RDL2 lines underneath the main SOC near the die edge. The trace cracks were mainly found on the isolated lines near the tear drop turning point as shown in Figure 9. A cross section of the RDL trace crack is shown in Figure 10. No trace cracks were found in the dense RDL metal line areas.

In our study, FEA was used to investigate the risk for RDL cracking based on different trace dimensions and geometries such as trace width, trace thickness, trace length from via to turning point, and trace angle as shown in Figure 11. The simulation results of different trace widths and thicknesses are shown in Table III. An increase in RDL trace width or thickness reduces the risk for trace cracking. Increasing the trace width by 10% and thickness by 15% resulted in a 15% reduction in the trace stress. Optimizing the trace design can also reduce the RDL crack risk. FEA showed the bends in the traces are areas with high stress concentration. The simulation results showing the effect of different RDL lengths from the via to turning point and different teardrop angles are shown in Table IV. The results showed increasing the trace distance from the via to the turning point from 12 um to 18 um had a 57% reduction in trace stress.

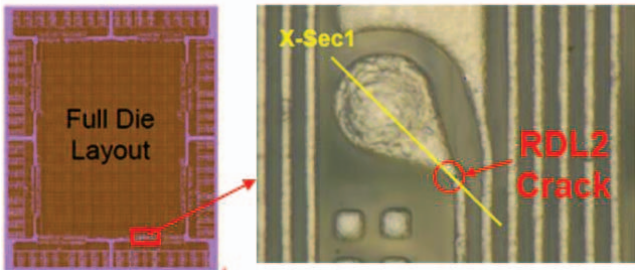


Figure 9. RDL trace crack

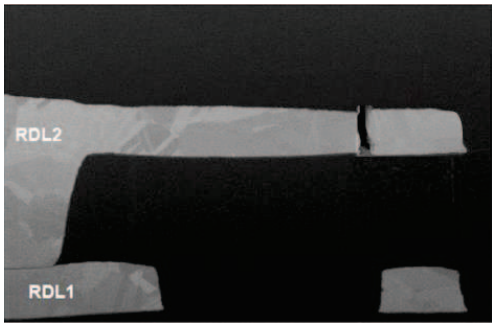


Figure 10. Cross section of RDL trace crack

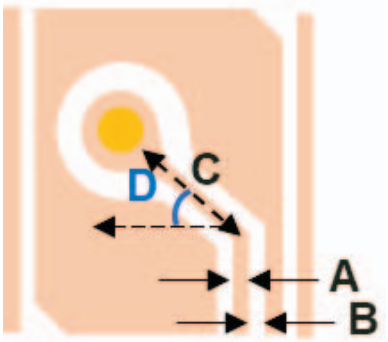


Figure 11. RDL Trace geometry: A is trace width, B is trace space, C is trace length from via to turning point, D is the trace angle

TABLE III. LINE DIMENSION EFFECT ON RDL CRACK RISK

Attribute	Leg 1	Leg 2	Leg 3	Leg 4
RDL Width (um)	2	2	1.5	2.2
RDL Thickness (um)	2	1.5	1.5	2.3
Stress Contour @ RDL Teardrop Area				
Normalized Stress	1.00X	1.14X	1.25X	0.85X

TABLE IV. TRACE GEOMETRY EFFECT ON RDL CRACK RISK

Attribute	Leg 5	Leg 6	Leg 7
RDL Width (um)	2	2	2
RDL Thickness (um)	2	2	2
Length from Via to turning Point (um)	12	18	20
Tear Drop Angle	45°	45°	60°
Stress Contour @ RDL Teardrop Area			
Normalized Stress	1.00X	0.43X	0.47X

After optimizing the RDL design by increasing the minimum trace width to 2.2 um and the trace thickness to 2.3 um and optimizing the pattern to increase the line length from via to the turning point to greater than 18 um, both packages successfully passed the multi-reflow tests. Figure 12 shows an example of the RDL trace design before and after trace optimization.

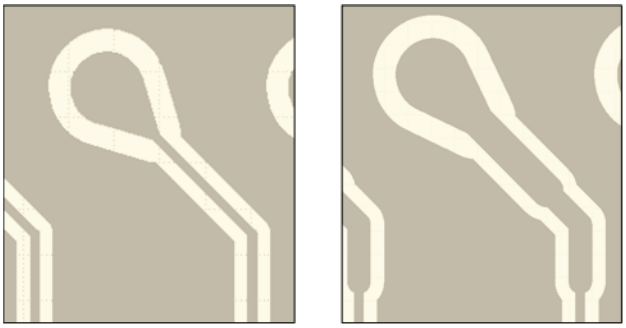


Figure 12. RDL layout a) before and b) after trace optimization

D. Reliability Performance

After optimizing the RDL design, the fan-out packages were subjected to the standard JEDEC reliability tests including moisture soaking level 4 (MSL4) as preconditioning, temperature cycling test (TCT) with -40°C to 125°C (condition G), unbiased high accelerated stress test (UHAST) with 110°C/85%RH, and high temperature storage test (HTS) at 150°C. Both packages passed 6X multi-reflow and the reliability tests without any failures as shown in Table V. After reliability testing, failure analysis was performed to check the integrity of the C4 joints and fine line patterns in the RDL layers. Cross-sectional analysis of the units showed no bump cracks or trace cracks as shown in Figures 13 and 14.

TABLE V. RELIABILITY TEST RESULTS

Reliability Test	Test Conditions	TV1	TV2
Multi-reflow (250°C)	6x	Passed	Passed
Component Level Test	MSL4	Passed	Passed
	uHAST 264 hrs (110°C/85%RH)	Passed	Passed
	TCG 850 cycles (-40 to 125°C)	Passed	Passed
	HTS 1000 hrs (150°C)	Passed	Passed

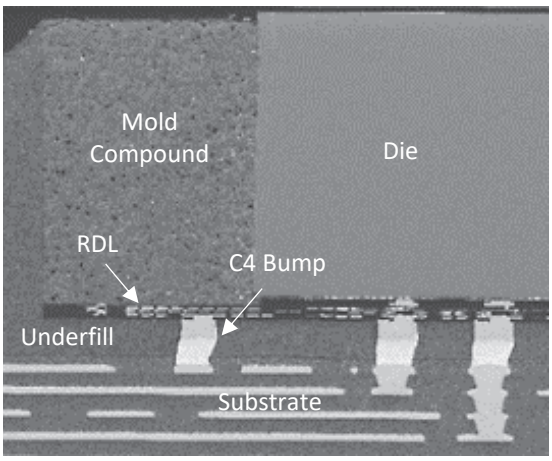


Figure 13. Cross-section showing good copper pillar C4 joint integrity

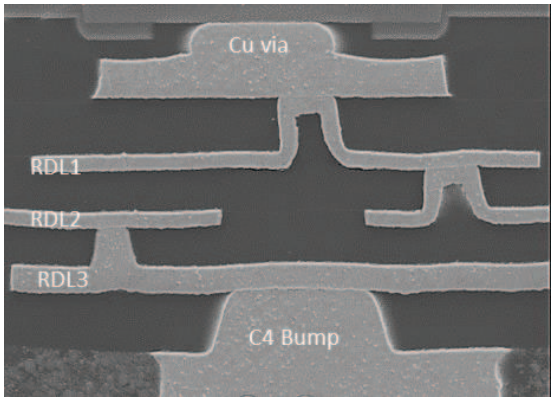


Figure 14. Cross-section of the RDL structure

IV. CONCLUSION

The reliability of large multi-chip fan-out packages was evaluated using the multi-reflow and component level stress tests. Our study showed that package stress from thermal loading could cause RDL cracking in the metal traces interconnecting the dies. The RDL trace locations near the gap between the SOC and I/O die are high stress concentration areas. RDL trace design and geometric dimensions are critical to interconnect reliability. Thicker and/or wider traces reduce the risk for RDL cracking. Increasing the distance between the trace via and the turning point in the line also reduces the RDL crack risk. By optimizing the RDL design and trace dimensions, RDL stress effects can be minimized enabling large format fan-out packages to pass the standard JEDEC reliability tests.

ACKNOWLEDGMENT

The authors would like to thank TSMC for their assistance with finite element stress simulations.

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