Embedded IPD Integration Solution for Large Chip Module Fan-Out Package

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I. Abstract

This paper will provide an overview of Si based capacitor/IPD integration evolution trends seen in the industry across different package platform, including 2.5D TSI DTC and embedded IPD on FO-EB and FO-MCM. From viewpoint of electrical performance, it figured out the comparison of 2.5D and FO EB (Embedded Bridge) with different IPD allocation respectively. We also indicated the difference of various IPD type (IPD in SOC, Stand-alone IPD, IPD in FO) Besides, the comparison of integrated capacitor technology (MLCC, 2D MiM, and TSI with DTC) are discussed accordingly. Finally, package level reliability of FO-EB with IPD integration be demonstrated successfully.

Keywords—TSI (Through Silicon Interposer); DTC (Deep Trench Capacitor); IPD (Integrated Passive Devices); Chip Module (CM); Fan-Out Multi-Chip Module (FO MCM); Fan-Out Embedded Bridge (FO EB)

II. Introduction

As showed in figure 1, data center with cloud computing through networking connection to provide the specific service for all of end application. Both cloud computing and network connection inquired extreme high computing performance and high data transmission to drive the requirement of those advanced package such as 2.5D, FO-EB and FO-MCM.

Based on the description of figure 2, from viewpoint of device level, it drove quantum computing and logic in memory technology on logic/memory industry respectively in the near future. On the other hand, from networking system interface's viewpoint, Co-Package Optics (CPO) is one of candidate to provide high link speed and high data transmission. In figure 3, just indicated the major difference between 2,5D package with silicon interposer and FO-EB package with alternative embedded bridge die. FO-EB package is one candidate of 2.5D alternative solution.

In table1, Actually, there are three different type of thin film IPD, with various function, and applied on those application (consumer product, industrial, network/server and automotive), especially on network and server application for the purpose of digital and mixed signal. However, from viewpoint of IPD type, we also listed down 3 approaches as showed in table 2, IPD on SOC processed by foundry, could provide high electrical performance with highly integration and customization design service. On the other hand, if IPD integrated on FO package, could gain the excellent performance, but major drawback are IPD/FO co-design need and long time-to-market compared to the other 2 types. Eventually, stand-alone IPD integration on package is the mainstream for all of IPD integration currently, even higher cost, but it exhibited more mature DSC (Die Side Cap)/LSC (Land Side Cap) assembly technology and fast time-to-market. That is why lots of players adopted/applied the integration technology at this moment.

However, from viewpoint of capacitance range and POD, traditional MLCC could provide high capacitance and low cost under the largest POD compared to both 2D MiM and TSI/DTC 3D structure. On the contrary, due to high electrical performance requirement, TSI with DTC and Si IPD are driving those advanced package with IPD integration. As indicated in table 3, TSI w/ DTC could provide good ESR (Equivalent Series Resistance) performance and good power decoupling compared to the other MLCC and 2D MiM (Metal Insulator Metal) structure, even with the middle range of capacitance. That is why more and more players keep an eye on the technology and adopted either TSI/DTC or Si IPD approach.

On the other hand, based on various product/application corresponded to different power consumption, including consumer product (smart phone, wearable, VRAR), edge computing product (ADAS, PC and graphic gaming) and cloud computing (server, router, switch). With higher and higher power consumption requirement on AI/HPC and network product, it is looking into high thermal conductivity TIM as typical silicone base TIM alternative solution to meet future demand as showed in figure 4. Regarding AI/HPC package solution, we could provide 2.5D, FO-MCM and FO-EB various package solution respectively to meet the power requirement. In shortly, advanced package platform with high thermal conductivity TIM integration plays a key role at this moment.

Figure 1: AI/HPC Eco-System

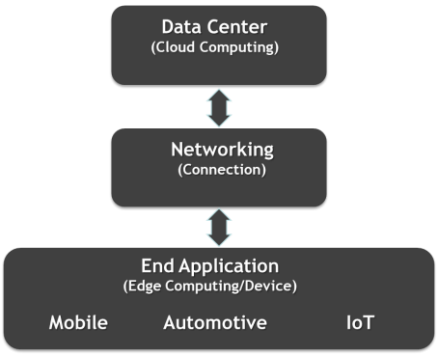


Figure2: AI/HPC Driving those Key Technologies

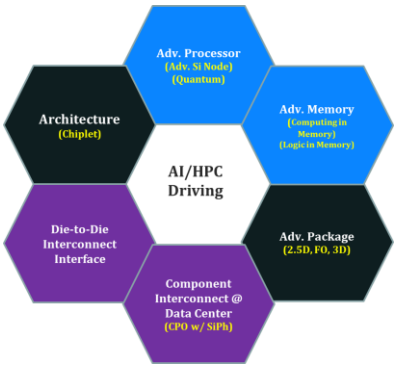


Figure 3: Advanced Fan-Out Package with 2.5D/FO-EB

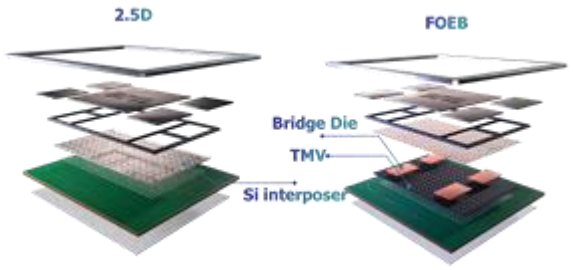


Table 1: Function of Thin Film IPD

Thin Film IPD	Type	1	2	3
Product	Function	ESD/ EMI Protection	Digital and Mixed Signal	RF Device
Application	Consumer Product			
	Industrial			
	Network/ Server			
	Automotive			

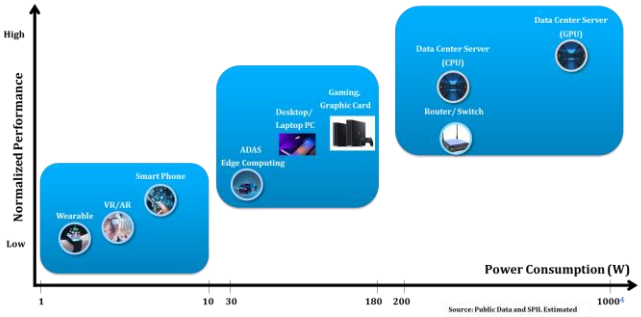
Table 2: IPD Type Comparison

Type (Thin Film IPD)	IPD in SOC	Stand Alone IPD	IPD in FO
Feature	Integrated IPD On RDL Process	Integrated IPD on PKG (DSC, LSC)	Integrated IPD on FO PKG Structure
Advantage	High Performance	IPD development independently Fast Time-to-Market	Highly Integration
Dis-Advantage	Customization (depended on SOC design)	High Cost	Co-Design, Long Time-to-Market

Table 3: Integrated Capacitor Technologies

		MLCC	2D MiM (Metal Insulator Metal)	TSI w/ DTC
		Ceramic Base	Si IPD	Si IPD
Capacitor	POD	Thick	Thinnest	Thin
Electrical Perf.	Capacitance Range	High (100X)	Low (0.001X)	Middle (1X)
	ESR (Equivalent Series Resistance)	Poor	Good	Good
	BDV (Breakdown Voltage)	Middle	High	Low
	Power Decoupling	Good	Poor	Good

Figure 4: Power Consumption Evolution Trend



III. Electrical Simulation

From viewpoint of electrical performance, closer path from IPD to main SOC die is preferred. It could provide more significant benefit due to the reduction of AC noise. With the comparison of 2.5D, FO-EB and FO-MCM on table 4, 2.5D with TSI DTC is more mature platform as the mainstream compared to both FO-EB and FO-MCM with IPD integration.

Among those package platform, TSI with DTC structure was mainly found in 2.5D platform at this moment. It is more mature platform in the industry. As we knew, no matter what kind of DTC allocation by different TSI supplier is applied, DTC inside TSI with 3D structure is much easier to achieve higher capacitance for product demand. However, as showed in table 5, either 2.5D w/ TSI DTC or FO-EB embedded IPD/ bridge die side by side could gain around 40% reduction of AC noise compared to no IPD inside. In other word, FO-EB with embedded IPD/bridge die side by side also could provide better electrical demand besides 2.5D.

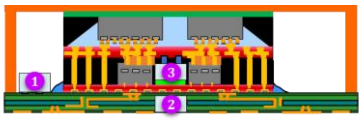
On the contrary, due to the limited C4 bump height (corresponded to C4 bump pitch), it got to either reduce original IPD thickness or increase C4 bump height if IPD landside of RDL as showed in figure 5. However, if increase C4 bump height, it represented to increase C4 bump pitch at the same time. There is a trade-off between more IO count demand and the increase of C4 bump height. In general, we should request IPD vendor to reduce IPD overall thickness and fit the limited room if possible.

Table 4: HPC Platform Comparison w/ IPD

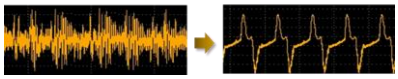
Platform		2.5D	FO-EB	FO-MCM
Structure	Interconnect	Si Interposer	Si Bridge Die + Organic RDL	Organic RDL
	Metal Layer	3L @ TSI	3L @ Bridge Die 1L @ FO	3~6L @ FO
	Cap. Integration	DTC (in Silicon Interposer)	IPD (Embedded in Bridge Area)	IPD (Landside of RDL)

DTC: Deep Trench Capacitor

Table 5: Electrical Performance by IPD Location

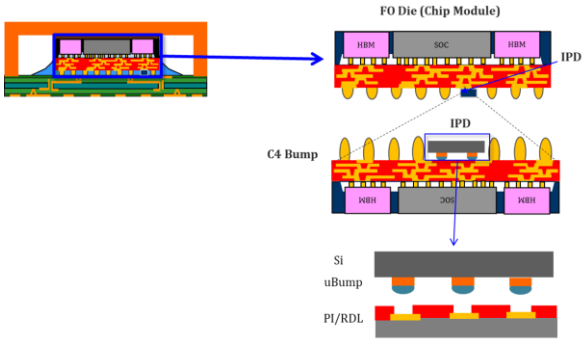


FO-EB



IPD Location		AC Noise /mV	
		P-P (mV)	Ratio
--	w/o IPD	195	1X
1	Chip Module Side	166	0.85X
2	Embedded in SBT	145	0.74X
3	Bridge Die Side / On Interposer(DTC)	115	0.59X

Figure 5: IPD Landside of RDL @ C4 Bump (FO-MCM)

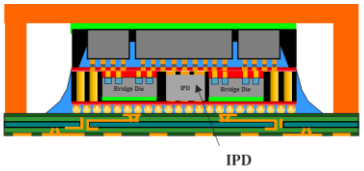


IV. Results and Discussion

As mentioned above for the benefit of IPD allocation, embedded IPD/ bridge die side by side at FO-EB platform, could gain better electrical performance. Therefore, integrated IPD/ Bridge die on the bottom and Chiplet SOC approach on the top is established as the verified TV as figure 6.

In conclusion, with the construction of FO-EB and embedded IPD integration, package level reliability verification is also demonstrated successfully by Pre-condition MSL4, unbiased highly accelerated stress test (uHAST) 264hrs, high temperature storage (HTS) 1000hrs and thermal cycle test (TCJ) 3000x in figure 7.

Figure 6: Package Level Reliability



No	Reliability Item	Result
1	Pre-con. MSL4 + uHAST 264h	Passed
2	Pre-con. MSL4 + TCJ 3000x	Passed
3	HTS 1000h	Passed

References

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