Proposed Standardization of Heterogenous Integrated Chiplet Models

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***Abstract*—With the economics of transistor scaling no longer universally applicable, the semiconductor industry faces an inflection point as higher cost, lower yield, and reticle size limitations drive the need for viable alternatives to traditional monolithic solutions. What we see is the move to innovative packaging technologies to support system-scaling demands and achieve lower system cost. This is driving an emerging trend to disaggregate what typically would be implemented as a single homogeneous, system-on-silicon (SOC) ASIC device into discrete, unpackaged ASIC devices, otherwise known as chiplets. These chiplets typically provide a specific function implemented in an optimal chip process node. Several of these chiplet devices are mounted and interconnected into a single package using high speed/bandwidth interfaces to deliver monolithic or greater performance at reduced cost, higher yield, and lower power with only a slightly larger area than a heterogeneous integrated advanced package.**

***As fabless semiconductor companies begin to bring these disaggregated chiplets to market, their successful adoption requires the industry to standardize on a set of interface protocols in order to offer plug-and-play compatibility between different suppliers' chiplets, creating a true open ecosystem and supply chain. Integrating these multi-vendor chiplets into a heterogeneous package assembly will also require chiplet vendors to provide their customers with a standardized set of design model deliverables in order to ensure operability in the end users EDA tool design workflows.**

***In this paper, we propose a set of standardized models that include thermal, physical, mechanical, IO, behavioral, power, signal and power integrity, electrical properties, and test models, as well as documentation to facilitate the integration of the chiplets into a design. Additionally, security traceability assurance is an emerging need to ensure trusted supply chain and operational security of the chiplets and the resulting packaged devices.**

It is strongly recommended that these models are electronically readable for use in the design work flows. The models should leverage available, existing industry standards, with extensions and/or new standards defined as necessary. The initial scope of these proposed models is currently targeted for 2.5D interposer-based designs. Note that these 2.5D structures may include silicon interposers, silicon bridges, or organic based fan-out/RDL packaging technologies, which can be referred to as "organic interposers." Additional or modified deliverables will be required to address the needs of 3D designs.

Keywords—chiplet, heterogeneous integrated (HI) package assembly, system in package (SiP), 2.5D interposer-based design, standard chiplet models, EDA

I. Introduction and Scope

A. Organization

The Chiplet Design Exchange (CDX) is a working group under the Open Domain-Specific Architecture (ODSA) sub-project under the direction of the Open Compute Project Foundation (OCP). The CDX group is comprised of members from EDA vendors, chiplet providers, and SiP end users charted to recommend standardized chiplet machine readable models and workflows to facilitate a chiplet ecosystem. The group is actively working on a whitepaper including these models and workflows. This paper summarizes the current proposed modeling chapter of the CDX whitepaper. Other ODSA working groups are also working on die-to-die (D2D) interface protocols and other related chiplet topics.

B. Definition and Characteristics of a Chiplet

A chiplet can be defined as a die specifically designed and optimized for operation within a package in conjunction with other chiplets. The interfaces used are the main differentiator. A chiplet differs from a conventional die in that a chiplet cannot typically be

packaged separately and still operate effectively; whereas a conventional die has powerful enough IO drivers to enable signaling over longer electrical distances. Optimizing a chiplet to operate within a package can be summarized according to the following key metrics on the chiplet-to-chiplet interface:

- Energy efficiency (pJ/bit)
- Bandwidth per beachfront (Gbps/mm)
- Area efficiency (Gbps/mm2)
- Latency (ns)
- Reach (mm)
- Pitch (μm)

This list is not exhaustive, as other metrics may be applicable. A chiplet will generally have considerably lower energy consumption per bit, given that it only needs to drive signals over a few millimeters or 10s of millimeters at most. The latency of these connections is also optimized for most applications, given the need to have these chiplets operate efficiently with one another.

II. The Need for Chiplet Models

As general purpose chiplet providers offer their devices for use in heterogeneous package designs, it is necessary that a standardized set of design models be provided to ensure operability in electronic design automation (EDA) design workflows. In this paper, we propose a set of standardized chiplet models to be provided by respective chiplet providers. It is strongly recommended that these models are electronically readable for use in design workflows. The models should leverage existing industry standards that are readily available, with extensions to these standards and the addition of new standards to be defined as necessary.

Table I. summarizes the proposed chiplet models to enable a usable chiplet ecosystem.

Table I. Models

Model	**Description**
Thermal	ECXML – JEDEC JEP181
Physical, Mechanical, and IO	Library Exchange Format (LEF) GDSII or OASIS SPICE JEDEC JEP30-P101 Optional: Verilog to Physical Pin Mapping File (CSV)
Behavioral	SystemVerilog IEEE – 1800-2017 Recommended: Verilog-AMS 2.4 Optional: SystemC IEEE – 1666-2011 Optional: Bus Functional Model (BFM)
Power	Liberty (.LIB) IEEE2416 Standard for Power Modeling to Enable System Level Analysis Optional: Unified Power Format (UPF) – IEEE 1801-2018 or Chip Power Format (CPF) Optional: Verilog-AMS 2.4 Optional: SystemC IEEE – 1666-2011
Signal Integrity Analysis	IBIS/IBIS-AMI Optional: SPICE Netlist (for the IO driver and/or receiver) Optional: Channel Model
Power Integrity Analysis	Chip Power Model (CPM)
Electrical Properties	JEDEC JEP30-E101
Test	Boundary Scan Description Language (BSDL) – IEEE 1149.1 BSDL – IEEE 1149.6/1149.7 ATPG Model - Primitive/UDP-based Verilog Recommended: Internal JTAG (IJTAG) IEEE 1687 Optional: IEEE-1500 Core Test Language (CTL) Description Optional: IP Firmware (if applicable) Recommended: Gray-Box Level Netlist Full-Chip ATPG Vectors – STIL (IEEE1450.1) or Parallel WGL Full-Chip Memory BIST/Repair Vectors – STIL (IEEE1450.1) or Parallel WGL Optional: Unified Power Format (UPF) – IEEE 1801 or Chip Power Format (CPM)
Security	Optional: Security Agent
Documentation and Guidelines	General Chiplet Documentation SiP Physical Integration Guidelines SiP Test Guidelines Optional: Firmware (if applicable) Optional: Security

Not all chiplets will require all of these models, but there must be a core set of deliverables provided to support design integration, verification, and testing of the chiplet IP into a SiP design. The scope of these models is currently targeted for 2.5D, interposer-based designs. Note that these 2.5D structures may include silicon interposers, silicon bridges, or organic based fan-out technologies — which can be considered as "organic interposers." Additional or modified deliverables will be required to address the needs of 3D designs.

III. Chiplet Models

A. Thermal

Thermal models are required for each chiplet in a SiP design to perform package-level thermal analysis. The information required by a thermal simulation tool for each chiplet component is provided in an industry standard, ECXML – JEP30-T181 JEDEC model. This model includes a 3D description of the chiplet, material thermal properties, and power maps summarizing the power profile of the device. A proposal to add support for arrays and spherical pins to the JEP30-T181 JEDEC standard has been submitted by the CDX working group. The current standard supports a steady state power/thermal model, but a time based, piecewise linear (PWL) power profile may be considered in future updates to the standard to support transient thermal behavior of the SiP device.

The power map should provide adequate granularity of the chiplet component for use in the SiP-level thermal analysis. This may include power estimates for each top-level block and/or a 2D grid of power estimates for each grid element. The minimum requirement is a single block power estimate for the entire chiplet. The standard also supports a two-resistor thermal model, but this mode is not recommended for SiP-level analysis. Separate models should be provided for different functional modes of operation if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

B. Physical, Mechanical, and IO

1) Library Exchange Format (LEF)

The LEF chiplet model defines the 2D physical dimensions, layer and electrical net names of each chiplet bump pin. This model is used for SiP-level physical design. LEF models have been historically provided to define abstract layout views of ASIC IP macros used by ASIC place and route (PNR) tools. LEF views may also be used to define abstract layout views of internal ASIC macros and SiP-level components, including chiplets used by package planning, design, and verification tools. The LEF views also include net signal information of the defined structures. PNR LEF views often include only the X/Y coordinates of the center of the pin connection point. PNR LEF views may also include additional information not required for package design, such as PNR blockages.

The design intent of LEF models used for package design differs from that of ASIC design and will generally require a different LEF model, which we can refer to as a "package" LEF model. A package LEF model should include all of the physical pin geometrical information required for the package design and verification process. A chiplet package LEF model should include the outline geometries of the chiplet die, including the scribe line and the outer-level geometrical boundary of the top-level metal layer. It should also include the top-level, 2D pin geometrical description of each pin, including micro-bumps, TSVs, and probe pads, along with the pin net name.

2) Graphical Design System/Open Artwork System Interchange Standard

The GDSII/OASIS chiplet model defines the 2D physical dimensions and layers of each chiplet pin. This model is used for SiP-level DRC, layout vs. schematic (LVS), and physical assembly. The GDSII format was established in the 1970s and remains a valid standard to this day. The OASIS format was established in the early 2000s and includes constructs to more efficiently represent the geometrical information of large databases, as compared to the GDSII format. Both formats are generally supported by most ASIC and package design tools, and the formats can be readily translated back and forth from each other. Either format or both can be provided for chiplet models.

A chiplet GDSII/OASIS model should include the outline geometries of the chiplet die, including the scribe line and the outer-level geometrical boundary of the top-level metal layers. It should also include the top-level, 2D pin geometrical description of each pin, including micro-bumps, through silicon vias (TSV), and may optionally include probe pads. If the assembler requires alignment keys for assembly purposes, these structures should also be included in the chiplet GDSII/OASIS model. Optionally, pin net names may also be defined by attaching text properties to the respective pins.

3) SPICE

The electrical connectivity of a SiP-level design is verified using a LVS design flow. Since the chiplet components of the design are fixed, only the connections to the top-level chiplet pins need to be defined and verified for the SiP design. To support this flow, a black box, SPICE level netlist model is provided for each chiplet, defining the top-level cell name and all the top-level external pins, including micro-bumps, TSVs, and optional probe pads. It is recommended that these pin names be consistent with the LEF, GDS, and functional SystemVerilog (SV) pin names.

4) JEDEC JEP30-P101

JEDEC JEP30-P101 is the model used to define the mechanical and IO properties, tolerances, and pertinent information for all chiplets and associated external pins for use in SiP-level connectivity and assembly. There are several different types of physical pin interconnect technologies used to connect the chiplet die to the interposer/bridge and/or substrate. For 2.5D applications, these pin types generally include micro-bump structures used to connect the die to the interposer or to the silicon bridge and TSVs used to connect the die through the interposer to the substrate. The micro-bump structures are process specific and may include copper pillar or solder ball interconnects. The TSV structures are also process specific. Additionally, probe pad structures are generally included on the chiplet die to support wafer-level testing of the die prior to package assembly. This model requires a 3D description as well as the material properties of the connectivity structures. This information is required for the design and verification of the SiP and by the chip assembler. The delivery mechanism of the actual chiplet devices should also be defined as either a wafer-level or singulated die. This information is used in the SiP assembly process.

The zGlue Exchange Format (ZEF) is an open-source format used to define mechanical, IO, and electrical information for packaged devices. The ZEF format is in the process of being migrated to an XML format and will be referred to as "ZEFXML". A variant of this format is being considered to define relevant mechanical, IO, and electrical information for unpackaged chiplet devices.

The mechanical and IO sections of the new ZEFXML open standard will be proposed as a new format for packaged and unpackaged chiplets. The mechanical information would be in JEP30-P101 and IO JEP30-E101 schemas.

5) Verilog to Physical Pin Mapping File/CSV Table (optional)

It is recommended that all pin names are consistent with the LEF, GDS, and functional SV pin names, where possible. If the chiplet functional pin names defined in the chiplet SV models are not identical to the pins defined in the LEF and/or GDS mapping file, a CSV table should be provided to map the associated functional pins in the SV model to the SPICE, LEF, and/or GDS pins.

C. Behavioral

Behavioral models for each chiplet component are required to support the SiP-level and optional system-level functional simulations. Verilog is an IEEE standard hardware description

language used to model the functionality of an electronic system. These models are used by functional simulators to simulate the component, SiP, and system-level behavior of the electronic system. For chiplets that contain analog functionality, the analog extension of Verilog, Verilog-AMS, should be considered. SystemC is another optional format that chiplet vendors may support for use in higher-level, system-level analysis and optimization.

SystemVerilog IEEE – 1800-2017

SystemVerilog (SV) is a superset of the Verilog HDL language and includes provisions to develop functional verification test benches. Chiplet vendors should provide accurate functional models for their device for use in SiP-level and system-level functional simulations. Chiplet vendors may optionally consider providing test benches written in SV for use in unit-level testing of a device in the context of the SiP and/or system-level functional verification.

Verilog-AMS 2.4 (recommended)

Verilog-AMS is an extension of the Verilog hardware description language (HDL) and includes constructs to model analog functionality and structural descriptions of mixed signal circuits and systems. It is now the standard language for device modeling (replacing C in SPICE). Chiplet vendors may optionally consider providing Verilog-AMS models of their device in addition to the SV model(s). This is generally recommended for chiplet components that include analog functionality. The models can be used with RTL and/or circuit-level simulation tools. Additional information such as analog behavior, thermal, and cost may also be included at the discretion of the chiplet vendor.

These models can be used to model the chiplet in the context of a SiP and/or system-level simulation. It can also be used for architectural exploration and performance modeling. The primary advantage of Verilog-AMS over other languages in the context of chiplets is that it uses "disciplines" to mark wire types, which include electrical, thermal, fluid, optical, and possibly RF at the level of stitching chips or chiplets into systems. While mixing disciplines on "wires" is illegal in Verilog-AMS, other HDLs consider everything as electrical, thus it's easier to make mistakes. Discipline information can easily be stripped out for Verilog compatibility.

SystemC IEEE – 1666-2011 (optional)

Optional functional models for the chiplet written in SystemC are used for electronic system-level or transaction-level modeling of the chiplet in the context of a SiP and/or system-level simulation. SystemC can also be used for architectural exploration, performance modeling, and software development. Chiplet vendors may optionally consider providing SystemC models of their devices in addition to the SV model(s). The models can be used with system-level design and analysis tools. Additional information such as analog behavior, thermal, and cost may also be included at the discretion of the chiplet vendor. These models can be used to model the chiplet in the context of a SiP and/or system-level simulation. It can also be used for architectural exploration, performance modeling, and software development.

Bus Functional Model (optional)

Some chiplet devices, such as processing devices, may include cycle accurate, bus functional models (BFM), which may be used for SiP and/or system-level functional verification. If the model is in the Verilog format, it can be used in addition or in lieu of an SV model.

D. Power Dissipation

1) Liberty (.LIB)

Liberty models include power models for the chiplet based on clock period and core/IO operating voltage levels. This model may be used to model the power of the chiplet in the context of a SiP and/or system-level simulation. Separate models should be provided for different functional modes of operation, if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

2) IEEE 2416

The IEEE 2416 power modeling standard analyzes chiplets based on equation, measured, or simulated data. A single model can capture power at different operating modes. Power should be provided for test modes if significantly different from the functional modes.

3) Unified Power Format – IEEE 1801-2018 or Chip Power Format

The Unified Power Format (UPF) or Chip Power Format (CPF) models are used to define the power intent and power implementation of the chiplet device, including all unique power domains and supplies. The chiplet UPF/CPF models can be used by the SiP package and/or system design teams to plan, implement, and verify the power delivery to each chiplet within the SiP package design. Separate models should be provided for different functional modes of operation, if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

E. Signal Integrity Analysis

1) IBIS/IBIS-AMI

Input/output buffer information specification (IBIS) models are a simplified model of I/O buffers run on a SPICE-like simulator for board and SiP-level signal integrity analysis. The traditional IBIS model is an ASCII, table-based current versus voltage (I-V) model and includes parasitic RC information of the buffers. IBIS-AMI models are a more complex model of I/O buffers run on a SerDes channel simulator for high-speed, board-level signal integrity analysis. These models include two ASCII files (.ibs and .ami) and a platform-specific executable model (.dll for Windows, .so for Linux). These models are generally required for multi-gigabit serial links. The IBIS models are a simplified model which allows an IP provider to hide the details of I/O buffer design. Alternatively, the chiplet vendor may provide a detailed or simplified SPICE netlist of the I/O buffers in addition to or in lieu of an IBIS model.

Chiplet vendors may provide optional channel models for the high speed, D2D interfaces to assist signal integrity engineers in the set up and analysis of these interfaces. The channel requirements on these D2D interfaces should be defined in a tool readable format by the respective chiplet and SOC-PHY vendors. Touchstone models are used to define insertion loss, return loss, and crosstalk specification. Eye diagram specifications (eye mask width and height) can be captured in an XML format. We will consider recommending adding an eye diagram specification to the JEP30-E101 JEDEC standard.

F. Power Integrity Analysis

1) Chip Power Model

Chip Power Model (CPM) is a de facto standard used to model the static and transient power profile of a full die, including the internal resistor-inductor-capacitor (RLC) parasitics of the chiplet power delivery network, through the power and ground pins of the chiplet. The models are used to perform SPICE level power integrity analysis at the board and SiP level. Separate CPM models should be provided for different functional modes of operation, if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

G. Electrical Properties

JEP30-E100 is a JEDEC standard that includes electrical and functional properties for parts and associated terminals. We propose using this standard to capture the electrical and functional properties for a chiplet part and its associated pins (i.e., terminals).

The property values can be specified with or without conditions. The JEP30 schema is a container where properties can be specified with values, conditions, and equations. Additional properties unique to chiplet devices may be added and/or removed to the existing standard. Chiplet vendors can adhere to the standard values and/or specify their own values.

ZEF is an open-source format used to define mechanical, IO, and electrical information for packaged devices. ZEF is defined in the CSV format. ZEFXML is an enhancement of ZEF in the XML format for better support in multiple-values data, grouping of data, and custom unit and data. It is schema based and described in XML Schema Definition (XSD) and easily extensible with backward compatibility to older versions.

There are three data exchange XML files as defined below. Each of them defined by the associated XSD file.

- Mechanical – All x, y, z, tolerance, solder type, and material properties
- IO – Pin location, functionality, mode of operation, electrical characteristics (EC), abs max values, operating conditions, allowable RLC, voltage references, temperate-based voltage and current (VI) pin characteristics
- Electrical – Contains overall absolute maximum ratings, recommended operating conditions, ESD ratings, and electrical characteristic such as root mean square (RMS) current limit

There is an XSD file defining the schema associated with each file type. The first line of each file consists of the file description followed by the name and value pair for each parameter.

- mech_zef.xsd
- io_zef.xsd
- elect_zef.xsd

The filenames follow a convention naming of <OPN>_<TYPE>_zef.xml where:

- OPN – Orderable part number which is a unique product identifier from the manufacturer
- TYPE – Represents the type of file, either MECH, IO, or ELECT

For example, a BQ27426YZFT chiplet would have:

- BQ27426YZFT_mech_zef.xml
- BQ27426YZFT_io_zef.xml
- BQ27426YZFT_elect_zef.xml

ZEF and ZEFXML information is available on github at https://github.com/zglue/zef.

Sample properties for chiplet safe operating areas (SOA) and conditions are summarized as follows:

- Voltage levels on pins
- Max RMS current limit on pins and bumps, when applicable
- Max capacitance (also defined in .LIB)
- Allowed voltage overdrive/underdrive
- ESD rating
  - Human Body Model (HBM)
  - Charge Device Model (CDM)
  - Machine Model (MM)
- Thermal limits
  - Min/max junction
  - Allow for equation
- Future considerations
  - Shock and vibration rating
  - RadHard rating
  - Power sequencing
  - Static voltage scaling map
  - Dynamic voltage scaling
  - RFI emission tolerance

H. Test

Integrating multiple ASIC (chiplet) devices into a single package presents several challenges in testing the individual chiplet devices as well as the D2D interfaces between the chiplets. Although chiplets are delivered by respective chiplet vendors as pre-tested, known-good-die (KGD) [1] devices, during the assembly process it is possible that a chiplet device and/or the D2D interconnect is damaged or defective. As such, there is still a requirement to test the individual chiplets. To facilitate this in-package testing, the chiplet vendors will need to provide the respective manufacturing test patterns to ensure the device is still operational after it is assembled into the SiP package. It is also necessary to test each of the D2D interfaces between all chiplets with slow and at-speed interconnect testing. Since many of the test pins of the individual chiplets may not be available through external package pins, advanced 2.5D and 3D test access [4] and methods [9].

Production testing of traditional ASIC devices utilize structured DFT tests as the primary test methods. Boundary Scan [2] is used for IO and interconnect testing, MBIST/repair for internal memory testing, and scan testing for internal digital logic. Analog or IP testing utilizes additional testing techniques including functional patterns, loopback, and other Built-In Self-Test (BIST) logic tests. The individual chiplet tests, D2D tests, and any top-level IP tests are combined into a complete ATE production test program for the multi-die, SiP device. The SiP integrator may also include some overall functional tests.

The BIST and IP-related ATE tests are accessed or initialized through a standard IEEE-1149.1 [2] TAP serial interface, which typically runs at a slow clock rate of 10 to 50 Mhz. IJTAG [3] is the preferred method of internal test access for DFT/BIST and IP testing. Chiplet scan testing will need to accommodate IO overrides at the package pins, as well as coordinated feedthroughs through the chiplets to support standard scan techniques and newer methods, such as packet-based scan [6]. In SiP designs with multiple chiplets, the TAP TDI/TDO test pins are serially connected from chiplet to chiplet, connected through the interposer. Since these serial pins are serially "daisy chained" in the SiP, the operational speed of the JTAG IO will be limited by the slowest chiplet BSCAN speed. Additionally, SiP designs with large interposers and many chiplets will have interposer routing parasitic delays which could further reduce the operational test speed of the SIP device. To minimize these delays, careful interposer test routing and SiP planning are required as well as static timing analysis and/or timing simulation to verify the SiP interconnect delays.

IP test methods may incorporate serial or parallel D2D functional interfaces. Techniques such as in-package SiP boundary scan and IO BIST with lane redundancy and repair [5] may be used during production test and functional operation to boost overall SiP yield. Serial D2D interconnect test techniques may include near-end/far-end and D2D SerDes loopback. These test techniques are typically provided in the purchased IP core itself. Chiplet vendors need to provide full documentation for IP test and integration, as well as supporting PDL/ICL files to simplify SiP level pattern generation and simulation.

The power of the chiplet devices operating in their respective test modes may be significantly higher than the functional mode power. Careful power planning, analysis, and control are required [7].

An additional challenge in testing SiP devices with multiple chiplets is debugging failing test patterns of an embedded chiplet. In traditional ASIC devices, IP vendors will provide test/diagnostic support as required to the ASIC test team for their respective IP. A chiplet vendor will provide test patterns and guidelines to assist the SiP test team in developing a SiP level test program. A chiplet may be very difficult to debug should it fail SiP level testing. The ownership and responsibility for chiplet debug and failure analysis is an issue that will need to be addressed between the chiplet vendors and SiP test teams. However, the chiplet vendor should provide enough models, netlists, and design information for the SiP assembler to easily debug D2D test failures and interconnect tests.

Several of the published test standards and chiplet deliverables are summarized in the following.

1) *Boundary Scan Description Language (BSDL) – IEEE 1149.1 [2]/IEEE-1149.6 [10]*
   Chiplet boundary scan model used for slow-speed IO and interconnect testing within the package and external to the package at the system and board levels. Supports DC and AC coupled interfaces, as required.

2) *Automatic Test Pattern Generation (ATPG) model – Primitive/User Datagram Protocol (UDP) based Verilog*
   Generic standard cell and IO models used to test logic and interconnect are required. EDA-vendor specific models for all major EDA vendors are optional.

Internal JTAG (IJTAG) IEEE 1687 [4]
Test patterns for chiplet IP and MBIST/repair tests.

- Instrument Connectivity Language (ICL): Used to describe the internal test structures of the device under test.
- Procedural Description Language (PDL): Used to create test patterns for IP, like SerDes, and specialized tests and to create chiplet test initialization sequences, like PLL initialization for D2D at-speed scan tests.

3) *IEEE-1500 Core Test Language (CTL) description [8] (optional)*
   Required for 2.5D chiplets that have HBM PHYs [5]

4) *IP Firmware (required, if applicable)*
   For test initialization of chiplet and/or IP PHYs that are embedded in a chiplet.

5) *Gray-box level netlist (recommended)*
   Gray-box level netlist of test logic interfaces to support functional and timing simulation of chiplet production test patterns.

- Scan
- Boundary scan
- 3D: All IEEE1838 logic including PTAP/STAP, DWR, 3DCR, etc.
- Min/Typ/Max SDF: timing files for all supplied netlists

6) *Full-chip ATPG vectors – STIL (IEEE1450.1) or parallel wgl*
   ATPG vectors generated by DFT test tools to test the internal logic of the chiplet device through the chiplet IO pins.

7) *Full-chip MBIST/repair vectors – STIL (IEEE1450.1) [11] or parallel waveform generation language (wgl) test patterns*
   MBIST vectors generated by DFT test tools to test the internal memories of the chiplet device through the chiplet IO pins.

8) *UPF – IEEE 1801 [12] or CPF (optional)*
   UPF/CPF models for the chiplet defining the power intent and implementation of the chiplet device including all unique power domains and supplies.

I. *Security Agent (optional)*

The security agent is hardware and/or software provided with the chiplet to enable the end user of the SIP to assure the trusted supply chain traceability of the respective chiplet. The security agent is optional but may be required for certain security-critical use cases.

The chiplet die is authenticated with a system-level root-of-trust device (for example: OpenTitan) using established cryptographic authentication techniques. Software images downloaded onto the chiplet die, or used to update embedded firmware on the chiplet die must be cryptographically signed. An example of such a technique are physically unclonable functions (PUF), as discussed in [13]. Once successfully authenticated, the SiP can access the chiplet and data transfers to the SiP are enabled. No data transfers to the chiplet should be allowed if the authentication method fails. The chiplet will silently ignore all data accesses by the SiP until the authentication is successful. Unsuccessful authentication attempts should be reported to the SiP, and the reason for the authentication failure should be recorded by the SiP.

J. *Documentation and Guidelines*

Although it is strongly recommended that all chiplet models and specifications are provided in a machine-readable format, it is still necessary to provide documentation to describe the functionality and operation of the chiplet as well as guidelines to facilitate the integration, functional/physical verification, analysis, and ATE production testing of the chiplet in a SiP design.

1) General Chiplet Documentation

An IC datasheet is provided for all ASIC components and generally includes a detailed description of the device, pinout, operating conditions, and electrical/mechanical specifications. A datasheet should be provided for a chiplet including similar information that would be provided in an ASIC data sheet. Since a chiplet is unpackaged, specific package information would not be applicable. However, information should be provided to describe the packaging technology that the chiplet can deploy for integration into a SiP design. Where applicable, the chiplet vendor should document the compatible package assembly vendors and processes. Detailed models should also be provided for the design and assembly of the chiplet into a SiP device, as outlined in the other modeling items included in this section.

Due to the size and complexity of information on datasheets that have to be manually transferred to software tools, the tendency for human error that can drive costly repairs at later stages in the design process is high. This paper recommends that the data stored in the datasheet be also stored in the JEDEC JEP30 PartModel files, so that consumers can auto load the relevant data directly into their software tools efficiently and without introducing errors.

2) SiP Physical Integration Guidelines

SOC IP vendors generally provide integration guidelines that are used by IC and package design teams to integrate their IP into a custom ASIC design. These guidelines include information on how to simulate and integrate the IP into an ASIC block or floorplan and verify the physical and electrical integrity of the IP. They also include checklists, package guidelines and requirements, and any other general information that would assist the design team to successfully integrate the IP. Some vendors provide optional consulting support and/or support a design review with design teams to ensure their IP is integrated and verified in compliance with guidelines. A similar set of guidelines for chiplet IP should be provided by the respective vendors to be used by IC and package design teams to integrate their IP into a custom SiP design. Optional consulting support and/or design review support should also be considered.

3) SiP Test Guidelines

SOC IP vendors generally provide test guidelines that are used by the DFT and test teams to support DFT insertion and ATE test program development of their associated IP. Additional guidelines may also be provided to support the end customer in bench testing and bring-up of the device. Similar test guidelines for chiplet IP should be provided by the respective vendors to be used by the DFT, ATE, and functional bring-up test teams to support the ATE and functional testing of the respective chiplet within the context of the SiP design.

4) Firmware (optional)

Some chiplets may include internal IP or logic that requires firmware to test and/or configure the IP for use in the end application. Where applicable, chiplet vendors should provide the firmware, detailed guidelines, documentation, and scripts as required to support the test and/or configuration of the respective chiplet within the context of the SiP design.

5) Security Guidelines (optional)

Chiplet vendors should provide documentation and guidelines for the hardware and/or software integration of security technology to support the end user of the SiP to implement and/or operate security agents, assuring the trusted supply chain traceability of the respective chiplet.

IV. Conclusion

The benefits provided by the heterogeneous integration of chiplet devices into a single, advanced package is dramatically driving demand into new markets and applications. The packaging technologies and associated EDA design workflows to support 2.5D designs with embedded HBM memories are relatively mature and have been deployed in production designs for several years. Successful deployment of chiplet-based devices requires the adoption of standardized chiplet models to establish this emerging ecosystem. The models proposed in this paper are targeted to be developed by the prospective chiplet providers and delivered to their end users. Although it will take some time before the newly proposed models are formally adopted as standards, most should be usable in their current state. EDA vendors will also need to support these models in their tools and workflows. In addition to the proposed chiplet models, new standards for 2.5 and 3D assembly rules require new standards and formats. EDA vendors and 2.5D/3D manufacturing vendors are currently collaborating on these new standards, which will hopefully be in place by the time the chiplet ecosystem becomes available to the broader market.

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