Slow Wave and Dielectric Quasi-TEM Modes of Metal-Insulator-Semiconductor (MIS) Structure Through Silicon Via (TSV) in Signal Propagation and Power Delivery in 3D Chip Package

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Abstract

The effects of slow wave and dielectric quasi-TEM modes due to MIS (Metal-Insulator-Semiconductor) structure TSV (Through-Silicon-Via) are analyzed by using the proposed MIS TSV model and the measured results. Since MIS TSV has larger surface, longer length, and smaller insulator thickness than those of conventional on-chip metal lines, the stronger effects of slow wave and dielectric quasi-TEM modes of MIS structure on electrical performance appear. After obtaining the MIS structure TSV model with the dimension variables based on the measurement and 3D full wave simulation, two slow wave and dielectric quasi-TEM modes effects on MIS TSV electrical characteristics are analyzed in the aspects of signal propagation and power delivery.

Introduction

Currently developed high performance and high density chip packages are having 3D stacked chip structure on account of flexible combination on a single chip package, short electrical delay path between chips, and small package size. [1] There are many 3D stacked chip package technologies such as bond wire, flip chip, and through silicon via (TSV). Even though bond wire and flip chip are very matured and cheap technology because of their long history and high yield, many chip and package companies are developing and searching for new 3D stacking technology such as TSV to overcome the limitations in electrical performance (long & high loading Input/Output (I/O) interconnections between chips in bond wire) and chip density (small number of stacked chips in flip chip).

TSV is well known as the most promising 3D stacked chip package technology because of its almost unlimited number of I/O interconnections, the shortest electrical delay path, and smaller loadings between chips enabling high speed, low power, and relatively large chip density on a single chip package. [2] [3]

However, since TSV is formed inside semiconducting silicon substrate with finite and nonzero resistivity and has MIS (metal-insulator-semiconductor) structure such as metal (TSV) – insulator (silicon dioxide around TSV: SiO_2) – semiconductor (silicon substrate: Si) as shown in Fig. 1 (Signal-Ground TSV pair; SG-TSV), there are silicon substrate effects on electrical characteristics of TSV such as slow wave and dielectric quasi-TEM modes appearing at signal propagation and power delivery. Usually, commercial silicon substrate has finite resistivity in the range of 5 to 40 (Ω·cm) or 2.5 to 20 (S/m), and electrical characteristics of MIS structure TSV are more strongly affected by the two modes.

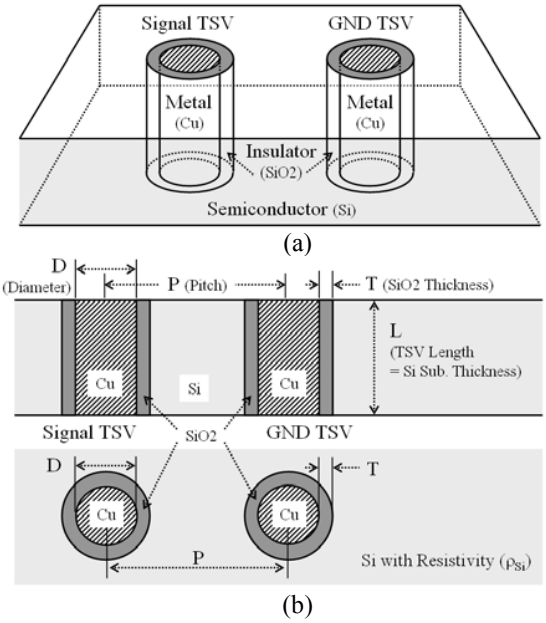


Figure 1. (a) MIS structure SG-TSV (b) Dimension definition of (a) for the proposed MIS structure SG-TSV model

Fig. 2 shows the resistivity-frequency domain chart, which defines signal propagation modes depending on resistivity of silicon substrate. As a resistivity of Si substrate is smaller owing to higher doping concentration (left direction of Fig. 2), dielectric quasi-TEM mode (upper-right region of Fig. 2; Si substrate acts as dielectric material) appears at higher frequency, which is decided by the dielectric relaxation frequency of Si substrate ($f_e = 1/(2 \cdot \pi \cdot \varepsilon_0 \cdot \varepsilon_{Si} \cdot \rho_{Si})$: ε_0=8.854 x 10^{-12} F/m, ε_{Si}=11.9, ρ_{Si}=resistivity of Si). Therefore a wave with a frequency of dielectric quasi-TEM mode region can run through MIS structure without an effect of Si substrate resistivity ideally. This means that a wave feels a shunt capacitance (C_d) of double layers of SiO_2 insulator (ε_{SiO2}=4)

and Si substrate (i.e. $C_d = (C_{SiO2} \cdot C_{Si})/(C_{SiO2} + C_{Si})$). Whereas in slow wave mode (lower-left region of Fig. 2), Si substrate acts as semiconductor neither dielectric nor metallic. Therefore Si substrate in slow-wave mode partly blocks electric field penetrating itself but fully accepts penetration of magnetic field, and consequently a wave of slow wave mode feels larger capacitance than that of dielectric quasi-TEM does and travels very slowly (larger relative dielectric constant than SiO2 and Si substrate). [4] [5]

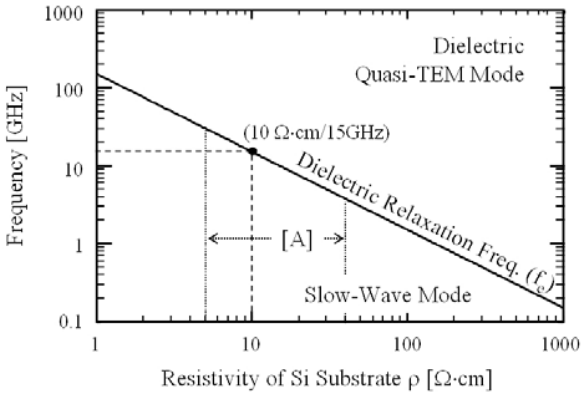


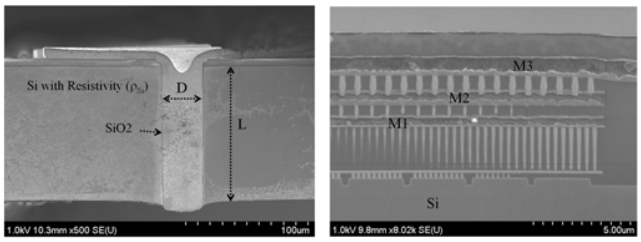
Figure 2. Resistivity – frequency domain chart showing dielectric relaxation frequency

As mentioned before, since SG-TSV has MIS structure and is formed in commercial silicon substrate with finite and moderate resistivity (range [A] of Fig. 2), a fast switching digital signal, which has very broadband and large amount of low frequency spectrum, on TSV is very strongly affected by two slow wave and dielectric quasi-TEM modes and non-linear frequency dependant insertion loss. [6] While in the aspect of power delivery system, TSV is very helpful to reduce power distribution network (PDN) impedance because slow wave mode means large capacitance or high effective dielectric constant. [7]

In this paper, the effects of slow wave and dielectric quasi-TEM modes due to MIS structure SG-TSV will be presented and analyzed by using the proposed models and the measured results. The test patterns for the simulations and measurements have MIS structure SG-TSVs for signal propagation, and meshed type on-chip power distribution networks (PDNs). Through the measurements, we will give you the confidence of the simulated results in case of the typically designed patterns on the test chips. After then, by showing the simulated results of various MIS structure SG-TSV conditions, we will analyze the effects of slow wave and dielectric quasi-TEM modes in accordance with SG-TSV design, silicon dioxide dimension, and resistivity of silicon substrate on signal propagation and PDN impedances in frequency domain.

Proposed MIS Structure TSV Model

In order to know Si substrate effect on MIS structure TSV, it is the best way to measure all possible cases depending on Si resistivity and TSV dimensions. However it is very difficult to do so due to the lack of equipments and matured technologies. Therefore it is very necessary to know how precisely and correctly 3D full wave simulation tool reflects the measured results of the limited number of test patterns and the proposed MIS structure SG-TSV and on-chip metal line models follow the 3D full simulation results.



(a) (b)

Figure 3. SEM pictures of (a) MIS structure TSV in the thinned Si substrate and (b) Three metal layers above Si substrate

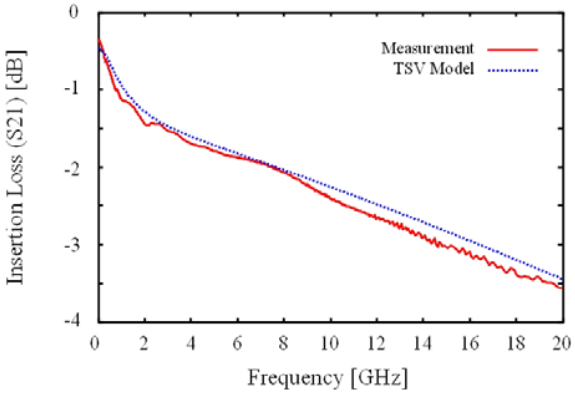


Figure 4. Insertion loss (S21 magnitude) comparison of the measurement and the proposed MIS structure SG-TSV model

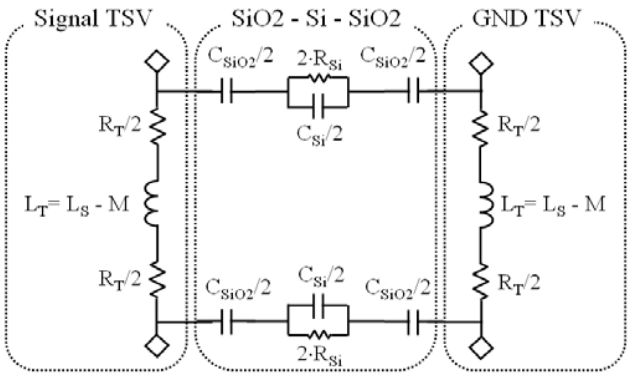


Figure 5. Proposed MIS structure SG-TSV model and parameters defined by Eqs. (1) ~ (6)

Fig. 3 shows the SEM pictures of a fabricated MIS structure SG-TSV in the thinned Si substrate, and three metal layers and micro-contact-vias for on-chip PDN structure, and Fig. 4 shows the insertion losses of a test pattern including 4 MIS structure TSVs (signal:ground = 2:2) and 2 on-chip metal lines (signal:ground=1:1) for TSV connections, and the proposed MIS structure SG-TSV and on-chip metal line models.

As shown in Fig. 4, the proposed models well reflect the measured result, and it has been proven that the proposed MIS structure SG-TSV model can well explain the electrical characteristics of MIS structure SG-TSV depending on Si resistivity and MIS structure SG-TSV dimensions.

Fig. 5 is the proposed MIS structure SG-TSV model and parameters. The model parameters are defined by dimensions such as D (TSV diameter [um]), L (TSV length [um]), P (Pitch [um]: distance between two TSV Centers), T (SiO2 insulator thickness [um]), and ρ_{Si} (Si substrate resistivity [Ω·cm]) as followings. (Fig. 1(b))

$$R_T = \frac{L}{5.8E7 \cdot \pi \cdot (D/2)^2} \cdot \sqrt{1 + 0.25 \cdot freq} \quad (1)$$

$$L_S = \left(0.8 \cdot \frac{P}{50} + 1\right) \cdot \frac{\mu_0 \cdot L}{2\pi} \cdot \left[\ln\left(\frac{2 \cdot L}{D/2}\right) - 1\right] \quad (2)$$

$$M = \left(0.8 \cdot \frac{P}{50} + 1\right) \cdot \frac{\mu_0 \cdot L}{2\pi} \cdot \left[\ln\left(\frac{L}{P} + \sqrt{1 + \left(\frac{L}{P}\right)^2}\right) - \sqrt{1 + \left(\frac{P}{L}\right)^2} + \frac{P}{L}\right] \quad (3)$$

$$C_{SiO2} = \frac{3.9 \cdot \varepsilon_0 \cdot L}{T} \cdot \left(2 \cdot \pi \cdot \frac{D}{2}\right) \quad (4)$$

$$C_{Si} = \frac{11.9 \cdot \varepsilon_0 \cdot \pi \cdot L}{\ln\left[\frac{P}{D} + \sqrt{\left(\frac{P}{D}\right)^2 - 1}\right]} \quad (5)$$

$$R_{Si} = \frac{11.9 \cdot \varepsilon_0 \cdot \rho_{Si}}{100 \cdot C_{Si}} = \frac{1}{G_{Si}} \quad (6)$$

where μ_0 and ε_0 are permeability and permittivity of free-space, respectively. 'freq' in Eq. (1) is frequency with GHz unit. Eqs. (1), (2), and (4) and Eqs. (3), (5), and (6) have units [Ω/TSV], [H/TSV], [F/TSV], [H/SG-TSV], [F/SG-TSV], and [Ω/SG-TSV], respectively.

In Eq. (1), $\sqrt{1 + 2.5 \cdot freq}$ reflects skin depth effect of TSV pillar. In Eqs. (2) and (3), $\left(0.8 \cdot \frac{P}{50} + 1\right)$ corrects self and mutual inductances of TSV pillar depending on TSV pitch. Eq. (4) can be obtained from MIM (metal-insulator-metal) capacitance between TSV pillar and Si substrate considering concentrated electric field distributions in SiO2 when waves are in slow-wave mode. Eqs. (5) and (6) come from capacitance of two wire transmission line in dielectric quasi-TSM mode and the relation of $G_{Si} = 2\pi \cdot f_e \cdot C_{Si}$, respectively. [5]

Electrical Characteristic of MIS structure SG-TSV

In this section, electrical characteristics of MIS structure SG-TSV is going to be analyzed by using the proposed MIS structure SG-TSV model and showing the frequency dependence of the insertion loss (S21), the slow wave factor (β/β_0), and the effective dielectric constant (ε_{eff}).

First of all, the reference MIS structure SG-TSV with the dimensions of D=30 um, L=100 um, P=100 um, and T=0.5 um is analyzed changing ρ_{Si} such as 5, 10, 20, and 40 Ω·cm. Based on the dielectric relaxation frequency of Fig. 2, it is well known that as ρ_{Si} goes up Si substrate more quickly goes to dielectric, and this phenomenon is well explained by Figs. 6 and 7, which show the slow wave factor and effective dielectric constant of SG-TSV, respectively.

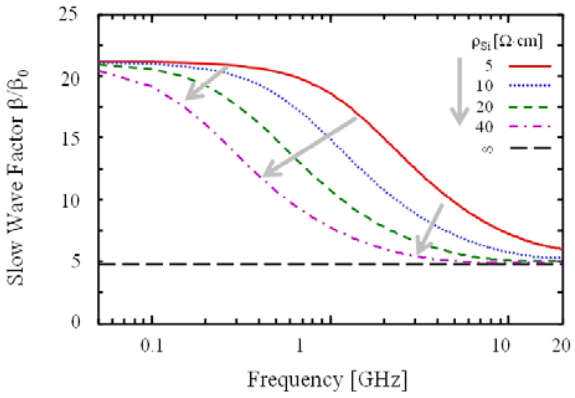


Figure 6. Slow wave factor (β/β_0) depending on ρ_{Si} in the reference MIS structure SG-TSV. (5 Ω·cm; solid line, 10 Ω·cm; dotted line, 20 Ω·cm; dashed line, 40 Ω·cm; dot-dash line, and ∞ Ω·cm; long dashed line: line notations are used in common from Fig. 6 to Fig. 9)

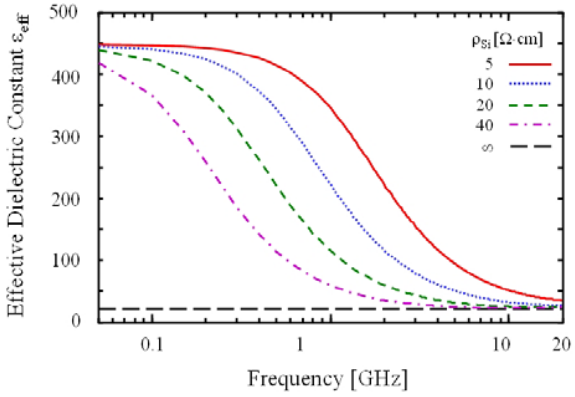


Figure 7. Effective dielectric constant (ε_{eff}) depending on ρ_{Si} in the reference MIS structure SG-TSV

As ρ_{Si} has larger value, the decreasing point of slow wave factor (start of a transition from slow wave mode to dielectric quasi-TEM mode) is shifted to lower frequency and the slow wave factor is closing to the infinity ρ_{Si} or the dielectric quasi-TEM mode, which is plotted on Figures with the long dashed lines. Since a slow wave factor is defined by $\beta/\beta_0 = \sqrt{\varepsilon_{eff}}$, the effective dielectric constant can be easily obtained. And we also know that slow wave mode due to finite resistivity of Si substrate causes very large capacitance of SG-TSV in low frequency (350 and 20 [fF/SG-TSV] at 50 MHz and 20 GHz of Fig. 7 respectively) and consequent very severe non-linear response of transmitted signals. These are very bad conditions to current high speed switching I/O drivers and should be minimized by increasing Si substrate resistivity.

Transmitted signal quality can be known by seeing insertion loss (S21) as shown in Fig. 8. A better flatness of S21 magnitude guarantees smaller jitter. However, as a wave

frequency is closing to dielectric quasi-TEM mode (high frequency), Si substrate effect is becoming larger and consequently the wave feels larger conductance G_{Si} and lost larger signal power. As a result, in order to keep a smaller capacitance and a better S21 magnitude flatness of SG-TSV, Si substrate resistivity should be larger.

Usually SG-TSV has very short length (L: 40 um ~ 100 um) and the effective dielectric constant at 20 GHz is 22.6 (Fig. 7). This means that TSV length is smaller than 5 % of 20 GHz wave length (λ_{20GHz}/20=158 um). Therefore characteristic impedance (Z0) of SG-TSV is not important and impedance mismatching is not shown in Fig. 8, but the real and imaginary parts of Z0 are plotted in Figs. 9 in order to improve your understandings.

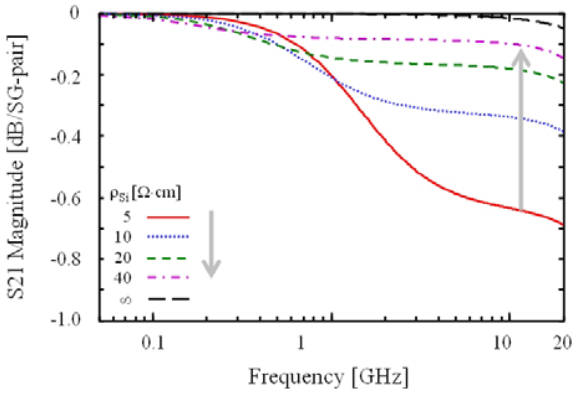


Figure 8. S21 Magnitude depending on ρ_{Si} in the reference MIS structure SG-TSV

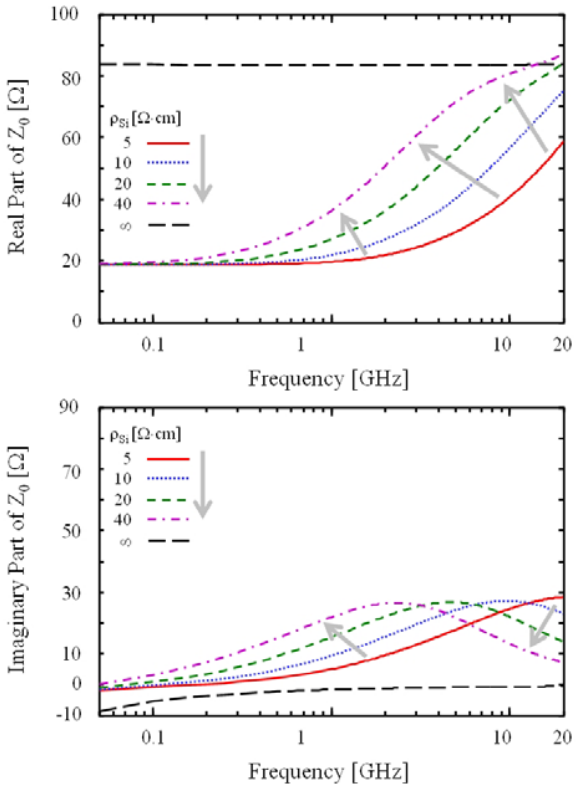


Figure 9. Real (upper) and imaginary (lower) parts of characteristic impedance (Z0) of the reference MIS structure SG-TSV depending on ρ_{Si}

Slow Wave and Dielectric Quasi-TEM Mode Effects depending on Design of MIS structure SG-TSV

Previously, the Si substrate resistivity effects have been analyzed. Slow wave mode induces large capacitance in low frequency range, and dielectric quasi-TEM mode induces large insertion loss in high frequency range and bad flatness of S21 magnitude. And larger Si substrate resistivity value was suggested to minimize the problems due to the two modes.

From now on, MIS structure SG-TSV design effects on slow wave and quasi-TEM modes are analyzed by showing slow wave factor (β/β_0) and S21 magnitude under the fixed Si substrate resistivity (ρ_{Si}) as 10 Ω·cm.

First of all, TSV diameter (D) is changed by ± 50% referenced to the design of the reference MIS structure SG-TSV with the dimensions of D=30 um, L=100 um, P=100 um, and T=0.5 um.

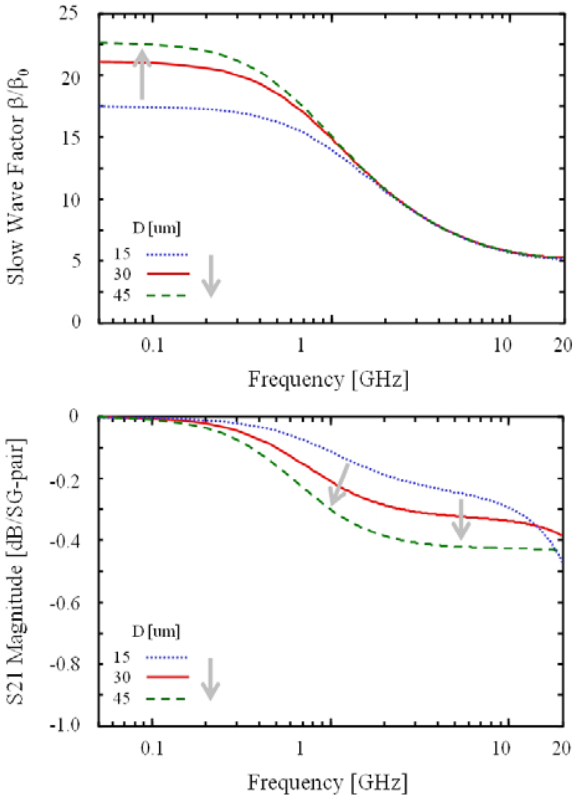


Figure 10. Slow wave factor (upper) and S21 magnitude (lower) when TSV diameters (D) are 15 um (dotted line), 30 um (solid line), and 45 um (dashed line)

As shown in Fig. 10, as TSV diameter increases, the slow wave factor increases in low frequency. This means effective dielectric constant, SG-TSV capacitance, and slow wave mode effect become higher, larger, and stronger, respectively. Therefore if Si substrate can not be controlled, smaller diameter TSV is better to keep smaller capacitance. Larger TSV diameter also increases Si substrate conductance (G_{Si}), and makes S21 magnitude flatness and signal loss worse and larger respectively.

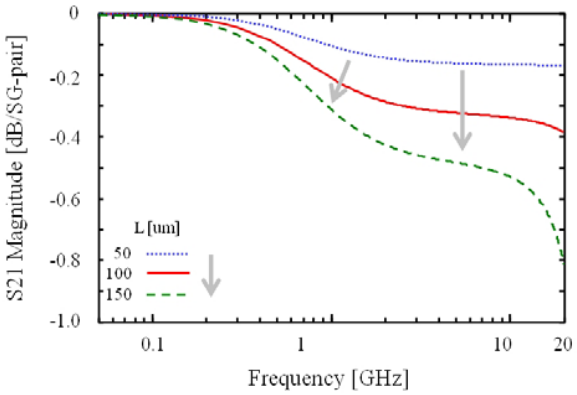


Figure 11. S21 Magnitude when TSV lengths (L) are 50 um (dotted line), 100 um (solid line), and 150 um (dashed line)

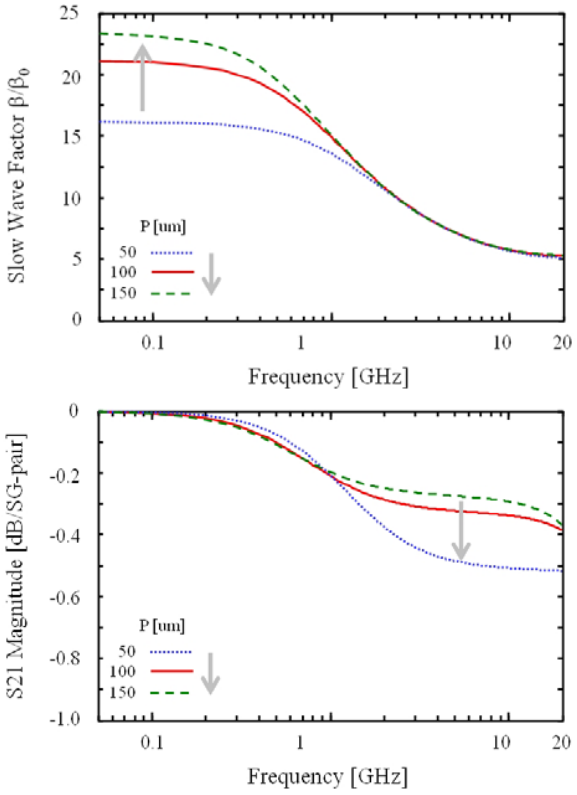


Figure 12. Slow wave factor (upper) and S21 magnitude (lower) when SG-TSV pitches (P) are 50 um (dotted line), 100 um (solid line), and 150 um (dashed line)

Then TSV lengths (L) are selected as 50, 100, 150 um under fixing D, P, and T as 30, 100, and 0.5 um. For this comparison, only S21 magnitudes are plotted in Fig. 11 because slow wave factor ($\beta/\beta_0 = \sqrt{\varepsilon_{eff}}$) is independent to transmission line length and the slow wave factors of three different lengths are same as the solid line of Fig. 10. As TSV length increases, the total G_{Si} and consequent signal loss of MIS structure SG-TSV rapidly increase. Another noticeable phenomenon is very large insertion loss of L=150 um case (dashed line) over 10 GHz. This high loss is also found in the dotted line of Fig. 10. These two large insertion losses at very high frequency come from TSV inductance, which becomes larger when D is smaller (Fig. 10) and L is longer (Fig.11).

Fig. 12 shows the slow wave factors and the S21 magnitudes of three SG-TSVs with different pitches such as 50 um, 100 um, and 150 um. Of course, other dimensions are fixed as the reference MIS structure SG-TSV. The smaller pitch means larger G_{Si} and induces larger insertion loss as shown in the upper figure of Fig. 12. Also larger pitch means larger slow wave mode effect due to SiO_2 effect, and consequently induces larger slow wave factor in low frequency as shown in the lower figure of Fig. 12.

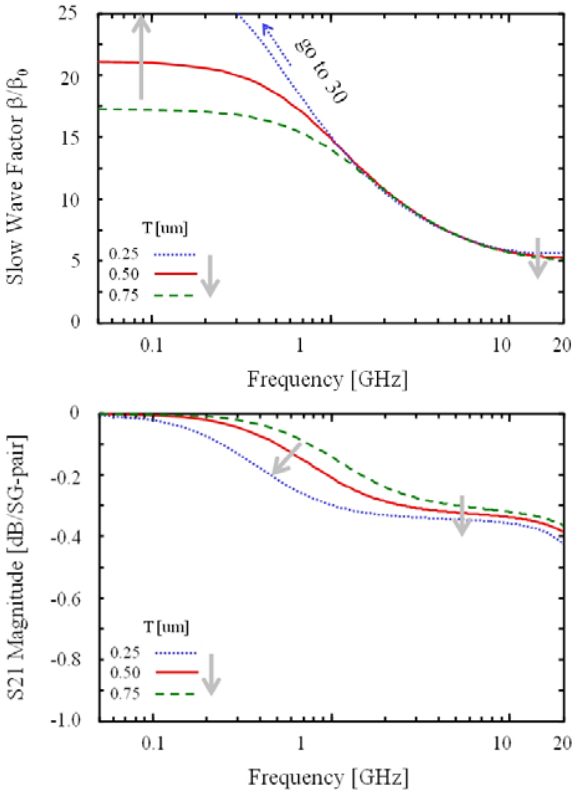


Figure 13. Slow wave factor (upper) and S21 magnitude (lower) when SiO2 thicknesses (T) are 0.25 um (dotted line), 0.5 um (solid line), and 0.75 um (dashed line)

The last part of SG-TSV design is SiO2 thickness. When SiO2 thickness is 0.25 um the slow wave factor goes up to 30, which means effective dielectric constant is almost 900. By comparing with from Figs. 10 to 12, the strongest slow wave mode effect appears at Fig. 13. Therefore SiO_2 thickness is the most important parameter to control slow wave mode effect of MIS structure SG-TSV. However the insertion loss variation due to G_{Si} in high frequency is small. This means that SiO_2 thickness only affects slow wave mode at low frequency.

From the previous figures, it has been understood that slow wave mode is related to effective dielectric constant and capacitance of MIS structure SG-TSV, and dielectric quasi-TEM mode governs S21 magnitude or insertion loss by controlling G_{Si}. And we have also known that the MIS structure SG-TSV dimensions such as D, L, and P affect two

slow wave and dielectric quasi-TEM modes simultaneously. But SiO_2 very strongly affects only slow wave mode.

Slow Wave Effect on 3D Stacked On-Chip PDNs with MIS structure SG-TSVs

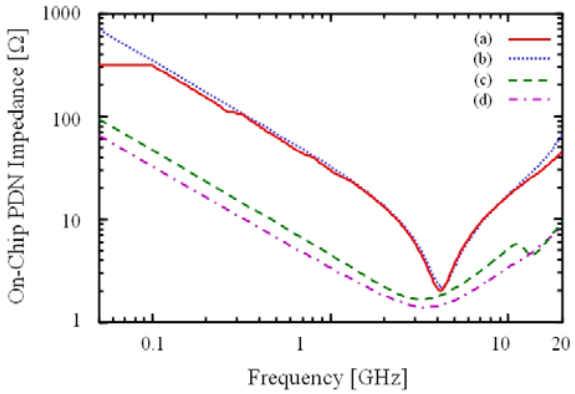


Figure 14. On-chip PDN impedance of (a) 1000 × 1000 um^2 single on-chip PDN (measurement; solid line) (b) 1000 × 1000 um^2 single on-chip PDN (Model; dotted line) (c) 1000 × 2000 um^2 single on-chip PDN (Model; dashed line) (d) Stacked two 1000 × 1000 um^2 single on-chip PDNs connected by 100 MIS structure TSVs (Model; dot-dash line)

Fig. 14 shows on-chip PDN impedances of 4 different on-chip PDNs. On-chip PDN has a meshed structure with 10 um line width and 15 um line space. The on-chip PDN model is composed with the on-chip metal line model based on the measurement. The solid and dotted lines are the measured and modeled on-chip PDN impedances of 1000 × 1000 um^2 single on-chip PDN. The on-chip PDN model well follows the measured result.

By using the well verified the on-chip PDN model, 1000 × 2000 um^2 single on-chip PDN (dashed line) and stacked two 1000 × 1000 um^2 single on-chip PDNs connected by 100 reference MIS structure TSVs (dot-dash line) are simulated. The two on-chip PDNs have same area as 1000 × 2000 um^2 but the stacked one shows lower PDN impedance. This comes from slow wave mode effect of MIS structure TSV in low frequency and small effective inductance of 100 TSVs (50 for the Power Net and 50 for the Ground Net) between two on-chip PDNs in high frequency. Therefore it can be known that the only slow wave mode effect of MIS structure TSV appears at power delivery.

Conclusions

The effects of slow wave and dielectric quasi-TEM modes due to MIS structure SG-TSV have been presented and analyzed by using the proposed models and the measured results. In low frequency range, when a signal propagates through SG-TSV, the effective dielectric constant and permeability determining the signal propagation velocity (β) are decided by the thickness of SiO2 around two TSVs and the pitch between two TSVs, and '1', respectively. As the SiO2 thickness is smaller and the pitch is larger, the effective dielectric constant becomes larger and slow wave mode effect appears strongly showing enlarged capacitance and severely distorted flatness of signal loss.

In high frequency range, the dielectric constant and permeability are same as those of silicon substrate acting like a dielectric. Therefore, the electrical characteristics of MIS structure SG-TSV show those of two wire transmission line embedded in lossy dielectric material.

Therefore MIS structure SG-TSV for signal transmission application should be designed with smaller diameter, smaller pitch, shorter length, and smaller SiO_2 thickness in larger Si substrate resistivity value to minimize capacitance. But if a signal loss in high frequency is important, a pitch of SG-TSV should be optimized because there is trade off between capacitance and insertion loss.

In power delivery application (on-chip PDN) of MIS structured TSV, the slow wave mode is always helpful to reduce PDN impedance by enlarged capacitance. But the dielectric quasi-TEM mode effect is not shown due to the very small multi-TSV and PDN inductance effects.

Acknowledgments

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References

1. S. Winkler, Advanced IC Packaging, 2007 Edition, Electronic Trend Publications (2007).
2. U. Kang, *et al*, "8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology," *IEEE Jorn. of Solid-State Circuit*, Vol. 45, No. 1, Jan. 2010.
3. J. S. Pak, *et al*, "Electrical Characterization of Through Silicon Via (TSV) depending on Structural and Material Parameters based on 3D Full Wave Simulation," *Proc. the 9th international symposium on Electronic Materials and Packaging* , Seoul, Korea, Nov. 2007.
4. H. Hasegawa, *et al*, "Properties of Microstrip Line on Si-SiO2 System," *IEEE Tans. on Microwave Theory and Techniques*, Vol. MTT-19, No. 11, Nov. 1971.
5. T. Shibata, *et al*, "Characterization of MIS Structure Coplanar Transmission Lines for Investigation of Signal Propagation in Integrated Circuits," *IEEE Tans. on Microwave Theory and Techniques*, Vol. 38, No. 7, July 1990.
6. J. Kim, *et al*, "Through Silicon Via (TSV) Equalizer," *Proc. 18th conference on Electrical Performance of Electronic Packaging and Systems*, Portland (Tigard), Oregon, Aug. 2009.
7. J. S. Pak, *et al*, "Sharing Power Distribution Networks for Enhanced Power Integrity by using Through-Silicon-Via," *Proc. the 2008 Electrical Design Advanced Packaging & Systems*, Seoul, Korea, Dec. 2008.