Team Project

Chiplet-Based Modular Computing Platform

Project Definition:

The Chiplet-Based Modular Computing Platform aims to develop a flexible, scalable, and high-performance computing solution utilizing chiplet technology. This innovative platform will empower companies to customize their hardware configurations tailored to specific workloads, thereby enhancing performance while reducing costs and development time.
Additionally, the project will focus on enhancing language proficiency and incorporating user objects, such as large groups, into the platform. This will involve conducting thorough cost and benefit analyses and feasibility studies to ensure that the system meets the diverse needs of its users effectively.

The design of Chiplet-Based Modular Computing Platform needs to ensure their flexibility and expandability, with the core being the realization of standardized interfaces, the use of appropriate packaging technologies and the provision of diverse modular design options. A standardized interface ensures seamless communication between modules and supports compatibility with different vendors and architectures; while suitable packaging technology addresses electrical connections and thermal management between chips to ensure system performance and stability. Diversified module design allows for flexible selection of modules with different functions based on specific application requirements, thus enabling system customization and scalability to meet the complex demands of high-performance computing.

Mission Statement

For companies or individuals who are seeking customizable, high-performance computing solutions and need flexible hardware configurations tailored to specific workloads, The Chiplet-Based Modular Computing Platform is a scalable and high-performance computing solution, That has the ability to enhance performance while reducing costs and development time. Unlike traditional hardware systems, Our product enables seamless hardware customization through chiplet technology, providing a modular, cost-efficient, and adaptable solution to meet diverse computational needs.

Potential Companies and Businesses for the Project(Target Users)

1. Semiconductor Manufacturers: AMD, Intel, NVIDIA

Develop and produce chiplets optimized for various workloads, contributing to the modular platform.

2. Cloud Service Providers：Amazon Web Services (AWS), Microsoft Azure, Google

Use the modular platform to offer customized computing solutions to clients, enhancing their cloud services.

3. AI and Machine Learning Companies：OpenAI, TensorFlow, DataRobot

Role: Leverage the chiplet architecture for high-performance AI processing, enabling faster model training and inference.

4. Gaming Companies：Epic Games, Unity Technologies

Role: Utilize the platform to create powerful gaming engines that can dynamically allocate resources based on user demands.

5. Telecommunications Companies: Qualcomm, Ericsson

Role: Integrate chiplet technology into networking hardware to enhance performance and scalability for 5G and IoT applications.

6. Research Institutions and Universities: MIT, Stanford University

Role: Collaborate on innovative research projects utilizing the modular platform for simulations and experiments in computing.

User Stories

1.Computer gamer

I am a computer gamer using a modular computing platform based on chiplet technology. As the demand for graphics performance in gaming continues to increase, you want to be able to upgrade only the GPU chiplet instead of replacing the entire computer. This will allow you to continue to maintain the high performance of your games while saving on upgrade costs.

I just purchased a newly released 3A title game and realized that the current GPU is no longer capable of achieving smooth frame rates. So you decide to fix the problem by upgrading your GPU chiplet.

The user opens the user control panel of the modular computing platform. Then the system detects the current GPU chiplet performance and displays its information:

A list of optional upgrade chipsets is displayed, including GPU chiplets of different models and prices. the user selects a GPU chiplet with higher performance and confirms the purchase. The platform guides the insertion of the new GPU chiplet and automatically uninstalls the old module. The system completes the connection with the new GPU through a standardized interface and updates the corresponding drivers and configurations.

After the upgrade is complete: The system reboots and the new GPU chiplet is loaded. Users re-run the game, the frame rate is greatly improved and the experience is significantly optimized.

2.IT administrator

As an IT administrator, I was responsible for maintaining the company's server and workstation infrastructure. The company has decided to introduce the chiplet platform to improve computing performance and flexibility. I would like to integrate the chiplet platform in the existing infrastructure. This will maximize the use of existing resources and will not require major changes to the existing system.

The company has decided to upgrade the computing performance of some of its servers, but has a limited budget so it cannot just replace all the hardware. The newly purchased chiplet platform needs to be integrated into the existing infrastructure, including the network configuration, storage system, and allocation of computing resources.

Through the management console, the system displays the current hardware architecture of the servers and the task loads that are running. The user has chosen to integrate the chiplet platform as a compute acceleration module into an existing server rack.

System Detection and Configuration: The system automatically detects the installed chiplet platform and displays its hardware information. The system guides the network configuration, connecting the chiplet platform's network interface to the existing LAN and ensuring that the chiplet module can access existing storage servers and resource pools.

The system recognizes the resources of existing servers and automatically assigns task loads to the chiplet platform. Users have the option of manually adjusting or automatically assigning compute tasks, allowing the chiplet platform to take on high-load tasks while the old servers continue to handle regular tasks.

3. Data scientist

As a data scientist in the analytics team at a biotech company, I need to run complex genomic simulations that require high computational power and fast data processing, so I want to leverage the modular capabilities of the chip-based modular computing platform because the current traditional computing systems cannot efficiently handle the large datasets and iterative processes needed for my analyses, resulting in delayed insights that hinder our research advancements.

Minimum Value Product (MVP)

Our team will validate the product's feasibility and market demand by delivering the smallest version of the core functionality with minimal investment of resources. During the product design process, we prioritize the implementation of core features. MVP contains the core features of the platform, such as modular design, standardized interfaces, and basic extensibility, without including all advanced features. This allows us to test and validate the chip at an early stage. The basic functionality of the chip platform is implemented for its interoperability, communication performance and scalability, without the need to fully implement a complex system.

Core elements of MVP:

1. Robust packaging:
Use a representative packaging technology that connects multiple chip modules and demonstrates stable electrical communication and thermal management capabilities between chips.The package solution needs to meet the basic electrical and thermal performance requirements to ensure the operational stability of the system.

2. Standardized interface:
Implement a standardized, flexible communication interface. Allow communication between at least two modules with different functionality through low latency and high bandwidth. The interface should be based on industry standards, verified for compatibility with multiple modules, and ensure future scalability.

3. Diverse module integration:
The project needs to provide a minimum of two modules with different functions. It should also demonstrate the pluggability or upgradability of the modules, while allowing users to combine and replace them according to application requirements. The selection and design of modules should demonstrate their initial optimization for different computing tasks, emphasizing the adaptability of the system.

Literature Review

Standardized Interfaces Analysis

The paper 'Proposed Standardization of Heterogeneous Integrated Chiplet Models' illustrates that establishing a standardized ecosystem has become essential, as the result of industry shifts toward chiplet architectures in order to improve performance and reduce costs and power consumption. Due to the limitations of monolithic semiconductor scaling, particularly in advanced packaging solutions, the industry's demand for heterogeneous integration is growing[1].

In this case, the paper provides 9 Chiplet models to build the Chiplet system. That is: a). Thermal; b).Physical, Mechanical, and IO; c).Behavioral; d).Power Dissipation; e).Signal Integrity Analysis; f).Power Integrity Analysis; g).Electrical Properties; h).Test; I). Security Agent (optional); j).Documentation and Guidelines. The full proposal can be found on that paper. As is shown in the table 1.1 below:

TABLE I. MODELS

Model	**Description**
Thermal	ECXML – JEDEC JEP181
Physical, Mechanical, and IO	Library Exchange Format (LEF) GDSII or OASIS SPICE JEDEC JEP30-P101 Optional: Verilog to Physical Pin Mapping File (CSV)
Behavioral	SystemVerilog IEEE – 1800-2017 Recommended: Verilog-AMS 2.4 Optional: SystemC IEEE – 1666-2011 Optional: Bus Functional Model (BFM)
Power	Liberty (.LIB) IEEE2416 Standard for Power Modeling to Enable System Level Analysis Optional: Unified Power Format (UPF) – IEEE 1801-2018 or Chip Power Format (CPF) Optional: Verilog-AMS 2.4 Optional: SystemC IEEE – 1666-2011

[1] A. Mastroianni et al., "Proposed Standardization of Heterogenous Integrated Chiplet Models," 2021 IEEE International 3D Systems Integration Conference (3DIC), Raleigh, NC, USA, 2021, pp. 1-8, doi: 10.1109/3DIC52383.2021.9687611.

Signal Integrity Analysis	IBIS/IBIS-AMI Optional: SPICE Netlist (for the IO driver and/or receiver) Optional: Channel Model
Power Integrity Analysis	Chip Power Model (CPM)
Electrical Properties	JEDEC JEP30-E101
Test	Boundary Scan Description Language (BSDL) – IEEE 1149.1 BSDL – IEEE 1149.6/1149.7 ATPG Model - Primitive/UDP-based Verilog Recommended: Internal JTAG (IJTAG) IEEE 1687 Optional: IEEE-1500 Core Test Language (CTL) Description Optional: IP Firmware (if applicable) Recommended: Gray-Box Level Netlist Full-Chip ATPG Vectors – STIL (IEEE1450.1) or Parallel WGL Full-Chip Memory BIST/Repair Vectors – STIL (IEEE1450.1) or Parallel WGL Optional: Unified Power Format (UPF) – IEEE 1801 or Chip Power Format (CPM)
Security	Optional: Security Agent
Documentation and Guidelines	General Chiplet Documentation SiP Physical Integration Guidelines SiP Test Guidelines Optional: Firmware (if applicable) Optional: Security

Table 1.1 models in paper

There are also some details shown in the paper when considering some parts of the model. For example, In the electrical properties part, the paper proposes using JEP30-E100 standard to capture the electrical and functional properties for a Chiplet part and its associated pins and ZEF is used to define mechanical, IO, and electrical information for packaged devices. Also the Github link is provided for the ZEF information https://github.com/zglue/zef.

This paper reveals the present situation of the standard of the Chiplet model. 'The newly proposed models will take some time to be formally adopted as standards, new standards and formats for 2.5D and 3D assembly rules also need to be developed, EDA vendors and 2.5D/3D manufacturers are collaborating on these new standards, with the hope that they will be officially implemented before the widespread adoption of the chiplet ecosystem.'

Modular High-Performance Computing Using Chiplets

One of our project's goals is to explore the feasibility of segmenting chips into different modules in order to improve the efficiency of chip products. Our project will explore the modules for specific application scenarios, such as computationally intensive tasks. At the same time, we compare the performance differences of different modularization schemes and evaluate their performance under different workloads.

The paper[2] by Vinnakota and Shalf explores the potential of chiplet technology to enable modular, customizable high-performance computing (HPC) systems. Inspired by the Fugaku supercomputer's A64FX processor[3], Vinnakota proposed a modular chiplet-based architecture. This builds on industry trends towards chiplet-based designs, as exemplified by AMD's use of chiplets to reduce manufacturing costs (Su et al., 2017). However, the authors extend this concept further, envisioning a more open and flexible ecosystem of interoperable chiplets for HPC.

A key aspect of the proposed architecture is its standardization of chiplet form factors and interfaces. This approach draws parallels with other successful modular standards in computing, such as the High Bandwidth Memory (HBM) specification. The authors propose two main chiplet types: square for compute-intensive functions and rectangular for I/O-intensive functions. This standardization enables a mix-and-match approach to system design, allowing HPC architects to customize systems for specific workloads more easily than monolithic designs.

The paper[4] by Yin and Lin points out that Chiplet-based architecture has emerged as a solution to the increasing complexity and cost of monolithic System-on-Chips (SoCs). As silicon technology becomes more advanced, the need for efficient, scalable, and cost-effective SoC designs has motivated the decomposition of large SoCs into smaller,

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[2] Vinnakota, B., & Shalf, J. M. (2023). Modular High-Performance Computing Using Chiplets. *Computing in Science and Engineering*, *25*(6), 39–48. https://doi.org/10.1109/MCSE.2023.3341749

[3] R. Okazaki et al., "Supercomputer Fugaku CPU A64fx realizing high performance, high-density packaging, and low power consumption," Fujitsu, Tokyo, Japan, 2020. [Online]. Available: https://www.fujitsu.com/ global/about/resources/publications/technicalreview/ 2020-03/article03.html

[4] Yin, J., Lin, Z., Kayiran, O., Poremba, M., Altaf, M. S. bin, Jerger, N. E., & Loh, G. H. (2018). Modular routing design for chiplet-based systems. Proceedings - International Symposium on Computer Architecture, 726–738. https://doi.org/10.1109/ISCA.2018.00066

reusable chiplets. These chiplets can be individually designed, optimized, and fabricated using appropriate technologies, allowing for a flexible and modular approach to system design.

In a Multi-Chip Module (MCM) system, deadlock is a state in which the modules are unable to continue execution because they are waiting for resources from each other, causing the system to come to a standstill.Yin and Lin explore a modular routing design methodology that effectively avoids the deadlock problem by placing steering restrictions at chip boundaries. The central mechanism behind this method is the introduction of turn restrictions, which limit certain routing decisions at module boundaries. This is critical for chip submodule implementations, as it reduces the complexity associated with cross-module communication.

Another part of the paper explores the usage of active silicon interposers in MCM systems. This technique allows part of the system functionality, such as memory interfaces, inter-chip interconnects, etc., to be relocated from the chip to the intermediary layer. The new design reduces the complexity of each module while increasing the scalability and cost-effectiveness of the system. This modular architecture significantly improves system scalability, allowing the chip to be more easily adapted and customized to different application requirements.

Further work is required to fully define the architecture. We need to explore the application performance and complexity tradeoffs for various parameters to define functional and physical modularity in detail.

Chiplets And Encapsulation Technology

Advanced packaging technology is the basic component of chiplets technology. Different packaging types also determine the characteristics, costs and uses of chiplets. This project will study the structural characteristics of several mature mass production packaging technologies, such as Cowos, EMIB and MCM, compare their applicable scenarios, and explore the future development direction of packaging technology.

Although the process node of the semiconductor industry is still improving, Moore's Law has gradually failed. The significant increase in chip design complexity and manufacturing cost does not bring linear increase in energy efficiency. As a modular design scheme, Chiplet technology can effectively reduce system complexity and improve production flexibility, which has become an important technology trend in high performance computing (HPC), artificial intelligence (AI) and data center. Integrated Design Ecosystem for Chiplets Heterogeneous Integration and Chip-to-Chip Interconnects in Advanced Packaging In this paper, we present a novel Chiplet based heterogeneous integration and chip interconnect scheme, which can optimize the scalability, cost effectiveness, and overall performance of Chiplet systems.

Heterogeneous Integration and Modular Design

The paper [5]shows that heterogeneous integration can maximize the utilization of different manufacturing processes by integrating Chiplet modules with different functions in a single package. For example, high-performance computing core modules can use advanced 7nm or 5 nm processes, while I/O or analog signal processing modules can use mature 28nm or larger processes. It can not only optimize the performance of each module, but also reduce the overall manufacturing cost.

The literature also proposes a concept of an "open modular chip ecosystem", where each Chiplet module achieves interoperability through standardized interfaces and packaging schemes, which greatly improves design flexibility. Chip designers are able to select and combine different Chiplet modules according to different application requirements. Fast customization of chip products without the need to design each module from scratch.

Interconnect Technology Between Chips

The main barrier to Chiplet architecture development is efficient inter-chip communication. While traditional soCs rely on complex internal interconnect design, Chiplet architecture implements inter-module communication through interconnect technology on the encapsulation layer. The example of this paper is an interchip interconnect technology based on silicon intermediate layer. Signal lines are embedded in the intermediate layer of the packaging substrate, which greatly reduces the delay and power consumption of signal transmission and supports up to TB/s inter-chip bandwidth. In addition, the mediation layer is able to support many different types of interfaces, such as memory, storage controllers, and network interfaces, thus achieving higher system integration and interoperability. This approach provides a more efficient design framework for future high performance computing systems that can meet the increasing computational demands.

The Role and Challenges of Packaging Technology

Encapsulation technology is the cornerstone of Chiplet technology. The advanced packaging techniques proposed in this paper, such as 2.5D and 3D packaging, can improve chip integration and performance by vertically stacking and horizontally integrating multiple chiplets. In 3D packaging, the vertical interconnection between modules can shorten the signal transmission path, reduce power consumption and improve system response speed.

However, with the development of packaging technology, the design and manufacturing complexity has increased. It is pointed out that package thermal management, power transfer and signal integrity are the main technical challenges. In order to solve these problems, researchers need to develop and use more advanced thermal management materials and

[5] *J. H. Lau et al., "Integrated Design Ecosystem for Chiplets Heterogeneous Integration and Chip-to-Chip Interconnects in Advanced Packaging Technology," in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*, 2024, pp. 1046-1052. [Online]. Available: https://ieeexplore.ieee.org/document/101668*

technologies, such as low resistance interconnects and efficient thermal interface materials, to ensure the stability of the system at high performance operation.

As advanced packaging technologies further mature and spread, the standardized Chiplet ecosystem is expected to become an industry standard, allowing modules from different vendors to work together in the same system. The heterogeneous integration in the encapsulation layer will be further extended to more application areas, such as smart terminals and edge computing, to meet diverse market requirements.

Future research may focus on how to optimize the thermal management and signaling efficiency of the encapsulation technology and how to accelerate the development and deployment of the Chiplet system through automated design tools. These developments will further promote the use of Chiplet technology in VLSI design and bring more innovative machines to the next generation of computing systems.

Yin, J., Lin, Z., Kayiran, O., Poremba, M., Altaf, M. S. bin, Jerger, N. E., & Loh, G. H. (2018). Modular routing design for chiplet-based systems. Proceedings - International Symposium on Computer Architecture, 726–738. https://doi.org/10.1109/ISCA.2018.00066

Vinnakota, B., & Shalf, J. M. (2023). Modular High-Performance Computing Using Chiplets. *Computing in Science and Engineering*, *25*(6), 39–48. https://doi.org/10.1109/MCSE.2023.3341749

R. Okazaki et al., “Supercomputer Fugaku CPU A64fx realizing high performance, high-density packaging, and low power consumption,” Fujitsu, Tokyo, Japan, 2020. [Online]. Available: https://www.fujitsu.com/ global/about/resources/publications/technicalreview/ 2020-03/article03.html

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