# COL215P Assignment 2.1

## Machine Vision Through Neural Network Hardware Component Design

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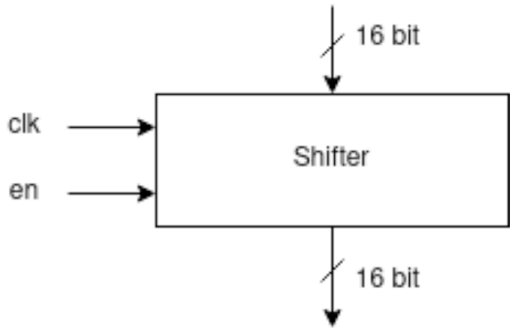
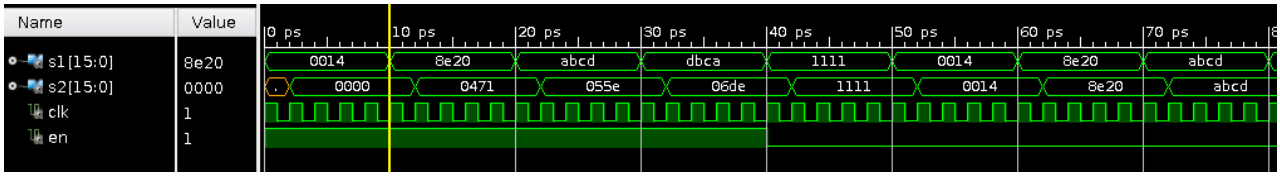
# Shifter

For the 32 bit shifter, we append 5 “0” bits to the left of the original std_logic_vector and drop the least significant 5 bits. The shift only happens when the enable signal “en” is set to 1. Otherwise it outputs the input signal.

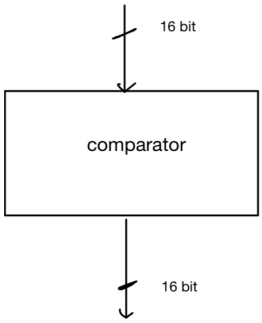
Testbench: As can be seen from the testbench, the shifter shifts the input signal s1 by 5 bits to the right in the output signal s2 on the rising edge of the clock when the enable signal is set to ‘1’. Otherwise, it just outputs the input signal.



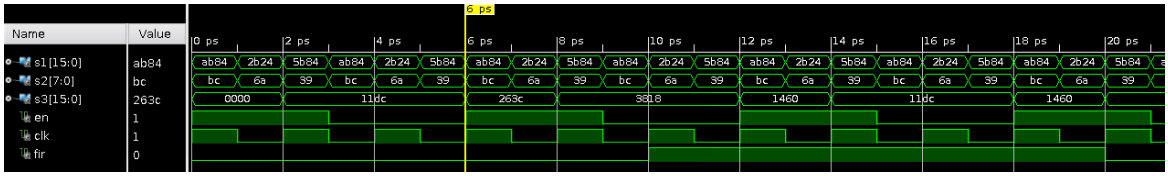

# Comparator

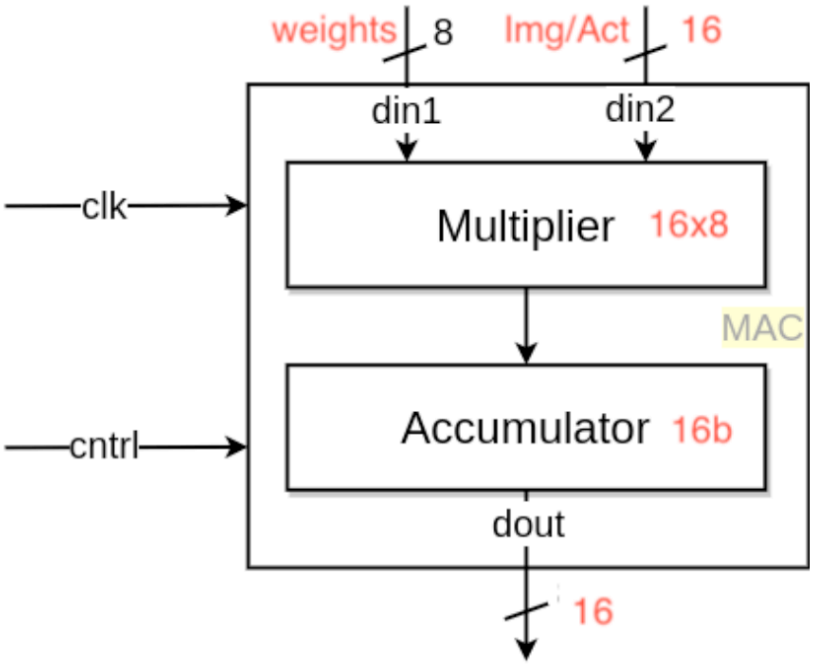
Comparator outputs the input signal if it is non-negative, otherwise it outputs 0. This can be checked by checking for the MSB (Most Significant Bit) of the input. MSB is ) for non-negative inputs and 1 for negative inputs. So it outputs the original input signal if thee MSB is 0 and outputs 0 if the MSB is 1.




# MAC

This component is as per the specifications specified in the assignment. There are two components which we have used, multiplier “mul” is a combinational circuit which multiplies two inputs of 16x8 bits and outputs a 16 bit number by dropping the less significant 8 bits. The accumulator “acc” is a sequential circuit which stores a value and adds the result of the multiplier to it with each clock cycle.

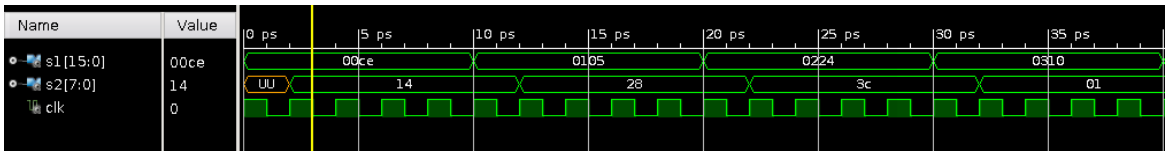


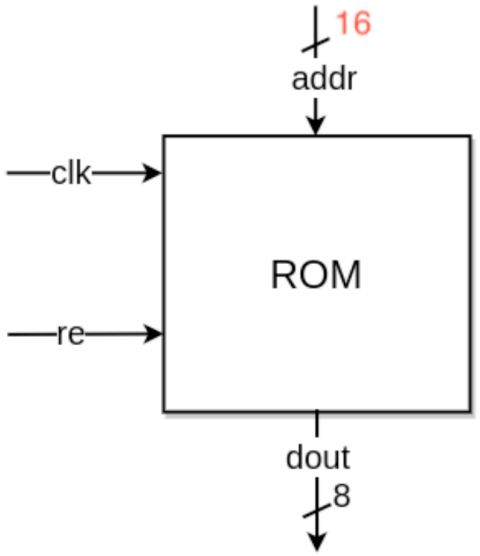



# ROM

The ROM consists of an array of size 51674 address locations of size 8 bits. The initialisation consists of reading 784 input file values from input file and then reading the remaining values from the weights and bias file.

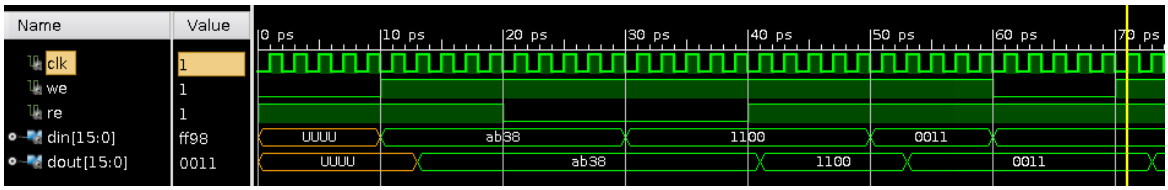
Output of the ROM is just the memory value at the location that is input at the rising edge of the clock.

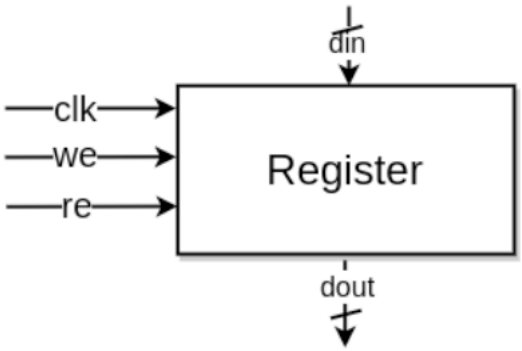



# Register

The register writes the input value at the rising edge of the clock if the write enable signal is set to '1'. This value is stored as a signal in the register. When the read enable signal is set to '1', this stored value is written to the output signal with the rising edge of the clock. The data width of the register has been kept generic.






# RAM

We have considered a generic RAM where the number of locations and the size of each location are flexible as we are considering to use multiple RAMs in our final project. The RAM works in a way similar to a register except it has an additional signal for address which specifies which address is being read from the RAM.