COL216 Assignment 2.3

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February 2022

1 Introduction

The single cycle design made in the previous stage will be changed to a multi-cycle design in this stage.

Memory

The Data Memory and the Program Memory are combined into one single component named the memory. The memory has been modelled as a 128*32 array. I have assumed that the program memory will occupy the starting addresses in the memory and is expected to be initialize in the memory itself.

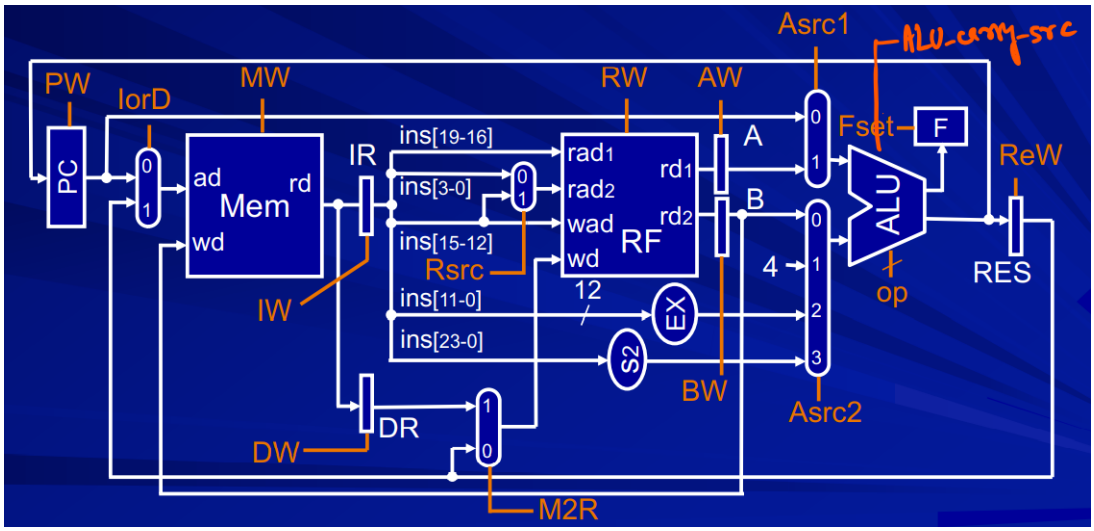
PC

PC is no longer handling computation for the next address, which is now be handled by the ALU and additional multiplexers logic. ALU computes word address which is changed to byte addressed before being stored into PC, which is now clocked and has a write enable signal PW.

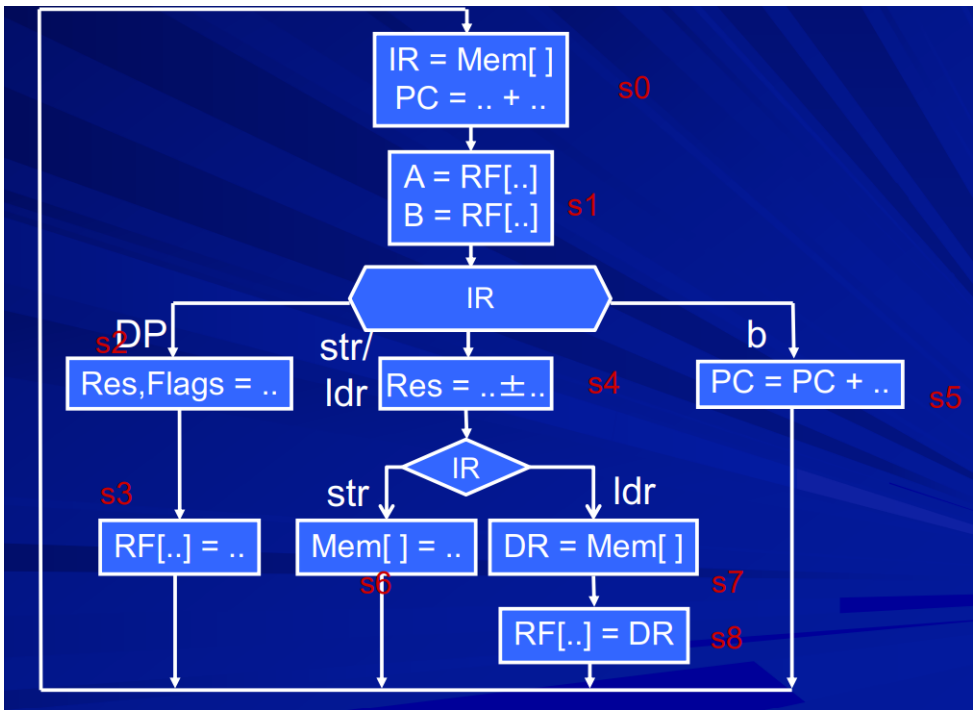
FSM

Separate component to handle the control logic for the multi-cycle design, receives information about the signal and produces the corresponding control signals dependent on the current state. The current state is maintained as a an enumerated datatype, which changes based on the instruction on the clock rising edge. An asynchronous reset is also present

Circuit Diagram



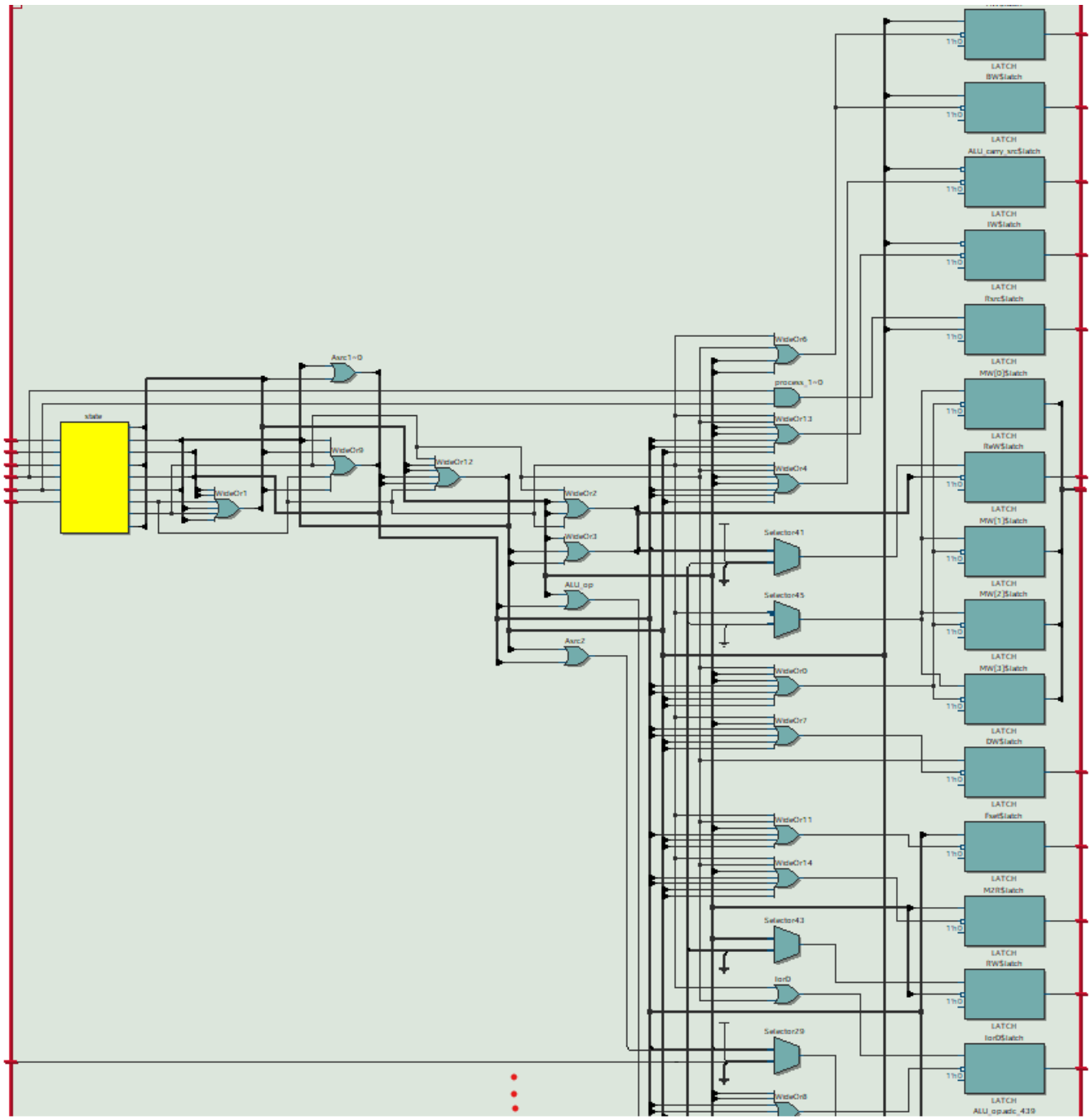
State Transition Diagram for FSM controller



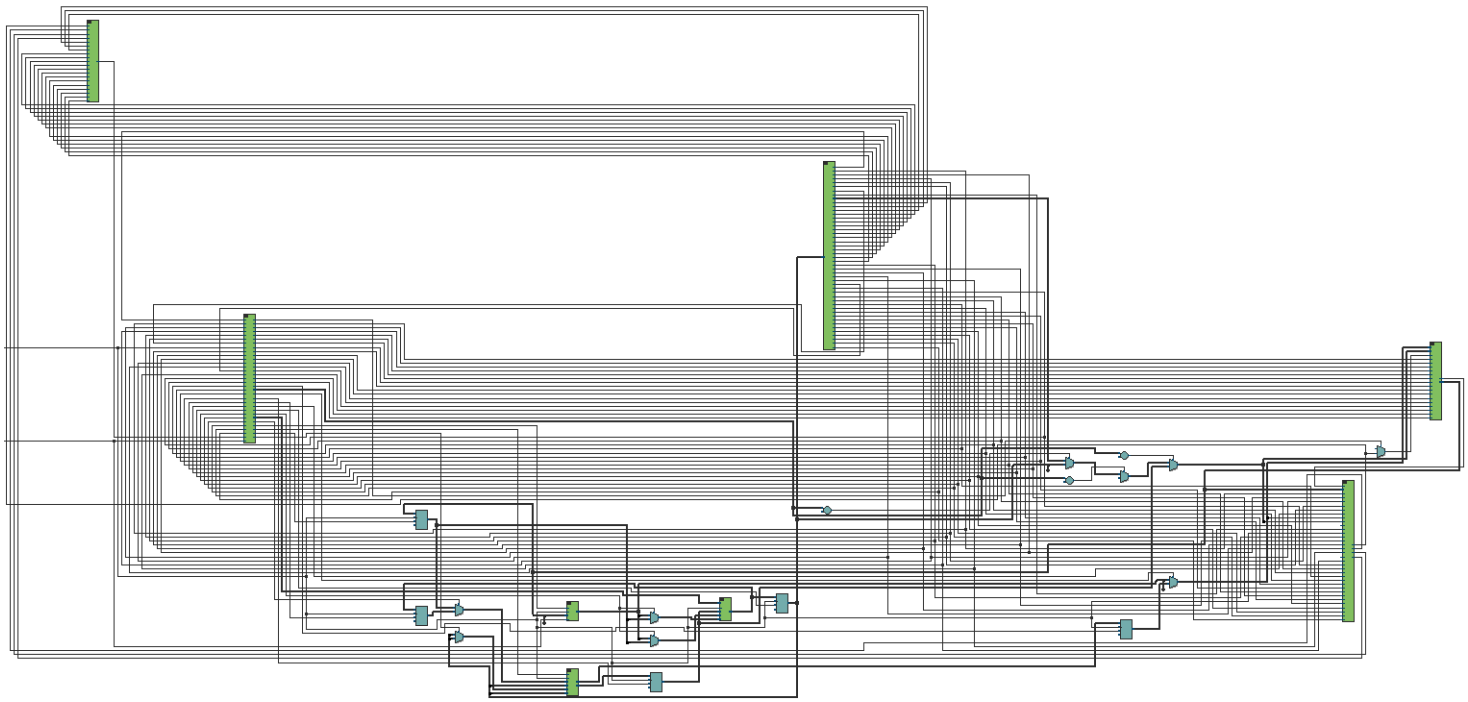
Design Choices

- A new enumerated data type is created to hold the state of the FSM ($s0 \ldots s8$)
- The FSM is separated into a component, which receives information about the instruction and produces control signals. The states change on the rising edge of the clock and also have an asynchronous reset to set the state to $s0$
- In each state appropriate control signals are set for the registers which means that the registers will be set and available at the rising edge of the next cycle.
- To produce next address ALU processes the PC has a word address and either adds (1) or the (branch offset and 1) , the later is achieved by setting the ALU operation to adc and setting the carry in to one.
- An additional Fset, signal has been added to the Flag module because Flags are not expected to be set in every iteration.

FSM circuit diagram

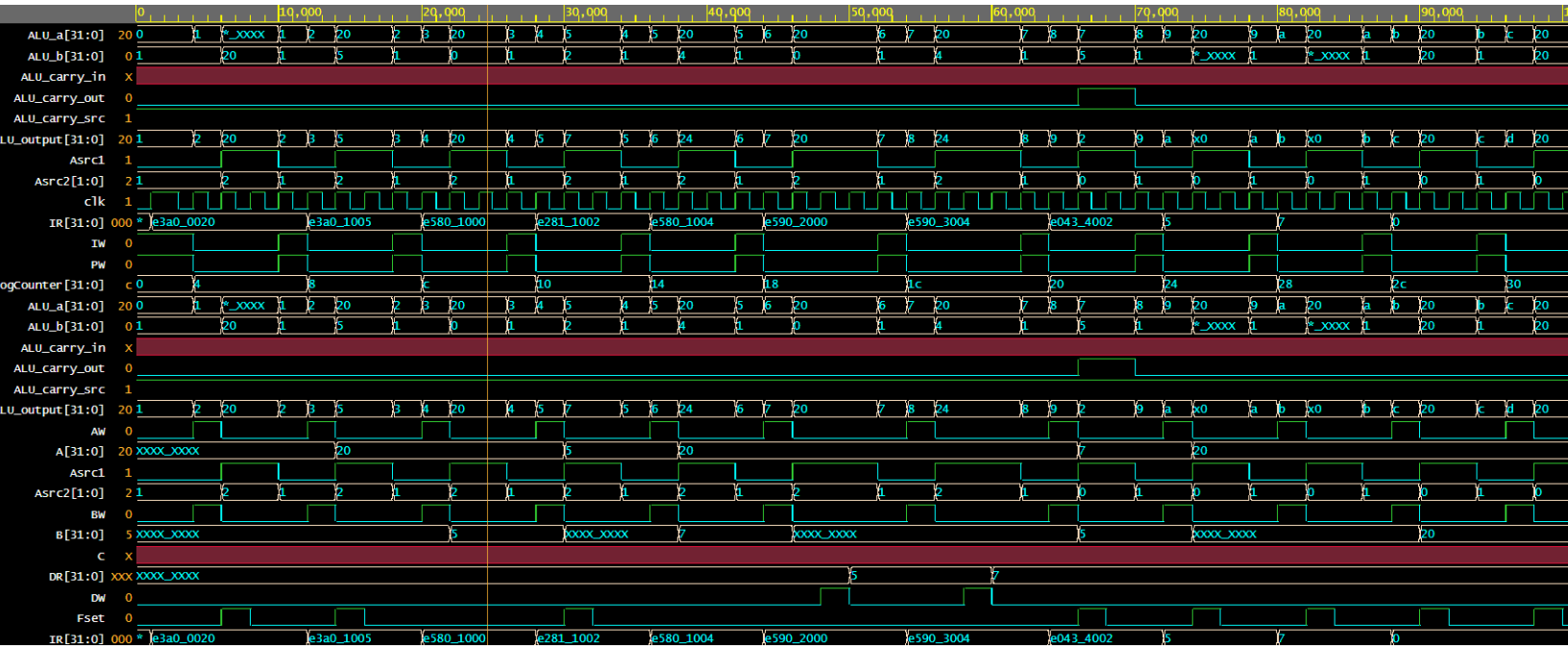


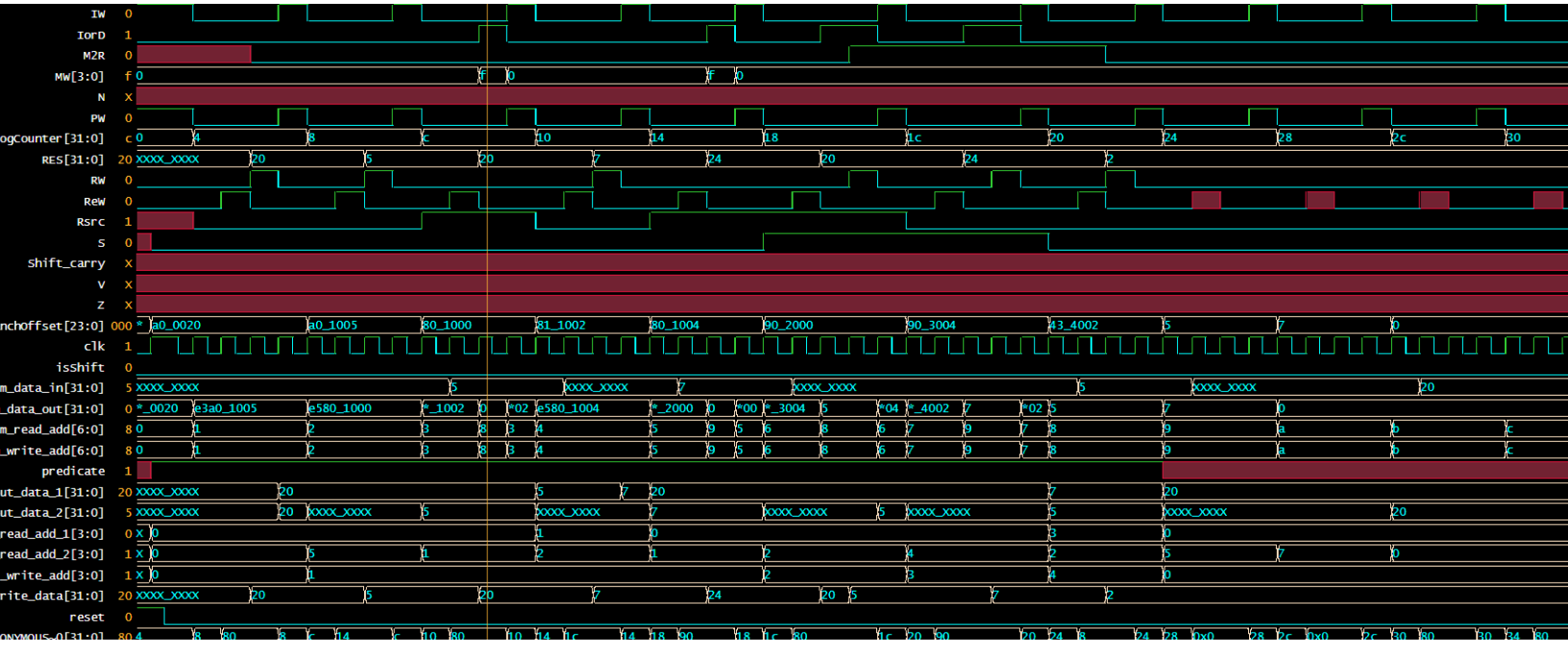
Processor circuit diagram



Program Testing 1

The two programs used in the previous assignment are used for testing but some modifications are made, in the first program the load/store address is changed to the 32 to avoid conflicting with the program instructions (both in the same memory) The EP wave generated is as follows and is tested for different signal values in the processor


ALU_a[31:0]
ALU_b[31:0]
ALU_carry_in
ALU_carry_out
ALU_carry_src
ALU_output[31:0]
Asrc1
Asrc2[1:0]
clk
IR[31:0]
IW
PW
ogCounter[31:0]
AW
A[31:0]
BW
B[31:0]
C
DR[31:0]
DW
Fset
e3a0_0020
e3a0_1005
e580_1000
e281_1002
e580_1004
e590_2000
e590_3004
e043_4002

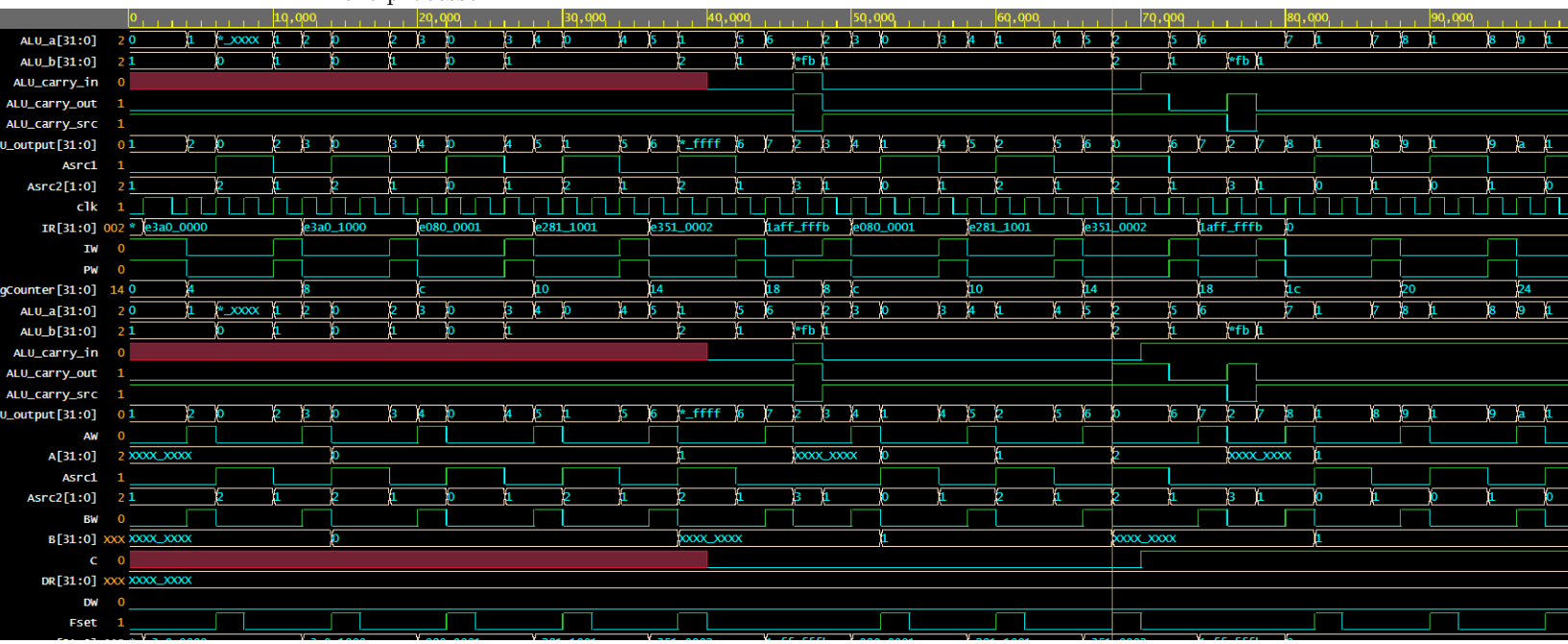

IW
IorD
M2R
MW[3:0]
N
PW
ogCounter[31:0]
RES[31:0]
RW
ReW
Rsrc
S
Shift_carry
V
Z
clk
isShift
reset
predicate
e3a0_0020
e3a0_1005
e580_1000
e281_1002
e580_1004
e590_2000
e590_3004
e043_4002

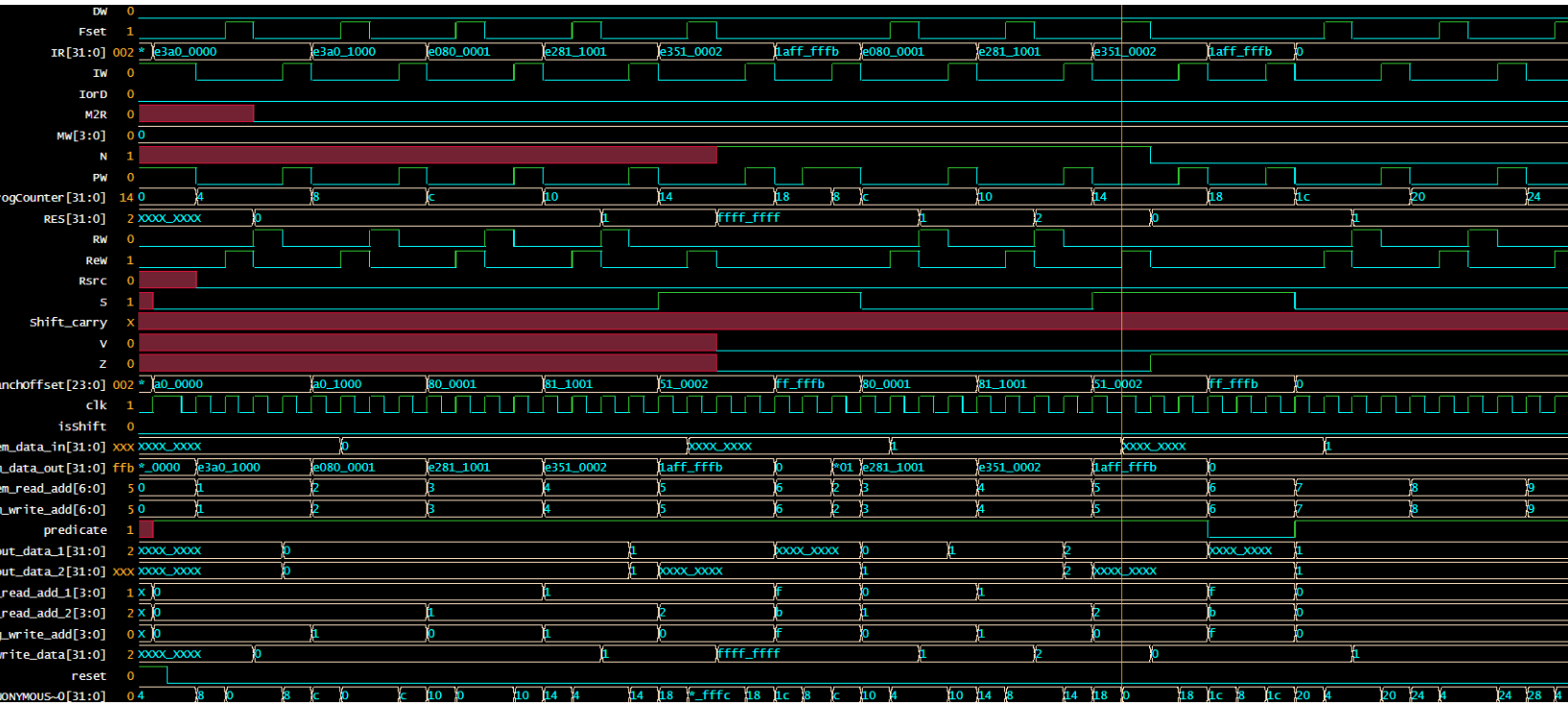
Program Testing 2

The second program is modified so that the loop runs for a smaller number of iterations by changing the compare instruction to (cmp r1 , #2) as follows,

```
22 signal MEMORY : MEM := ( 0 => X"E3A00000",
23 1 => X"E3A01000",
24 2 => X"E0800001",
25 3 => X"E2811001",
26 4 => X"E3510002",
27 5 => X"1AFFFFFB",
28 others => X"00000000"
```

The EP wave generated is as follows and is tested for different signal values in the processor





Resource Utilization for FSM

FSM

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               67      210      31.90%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              26      63400     0.04%
# Info: CLB Slices                        5       15850     0.03%
# Info: Dffs or Latches                   40      126800    0.03%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
```

Note

I forgot to mention in the last report, that the extra credit day was utilized in Assignment 2.2.