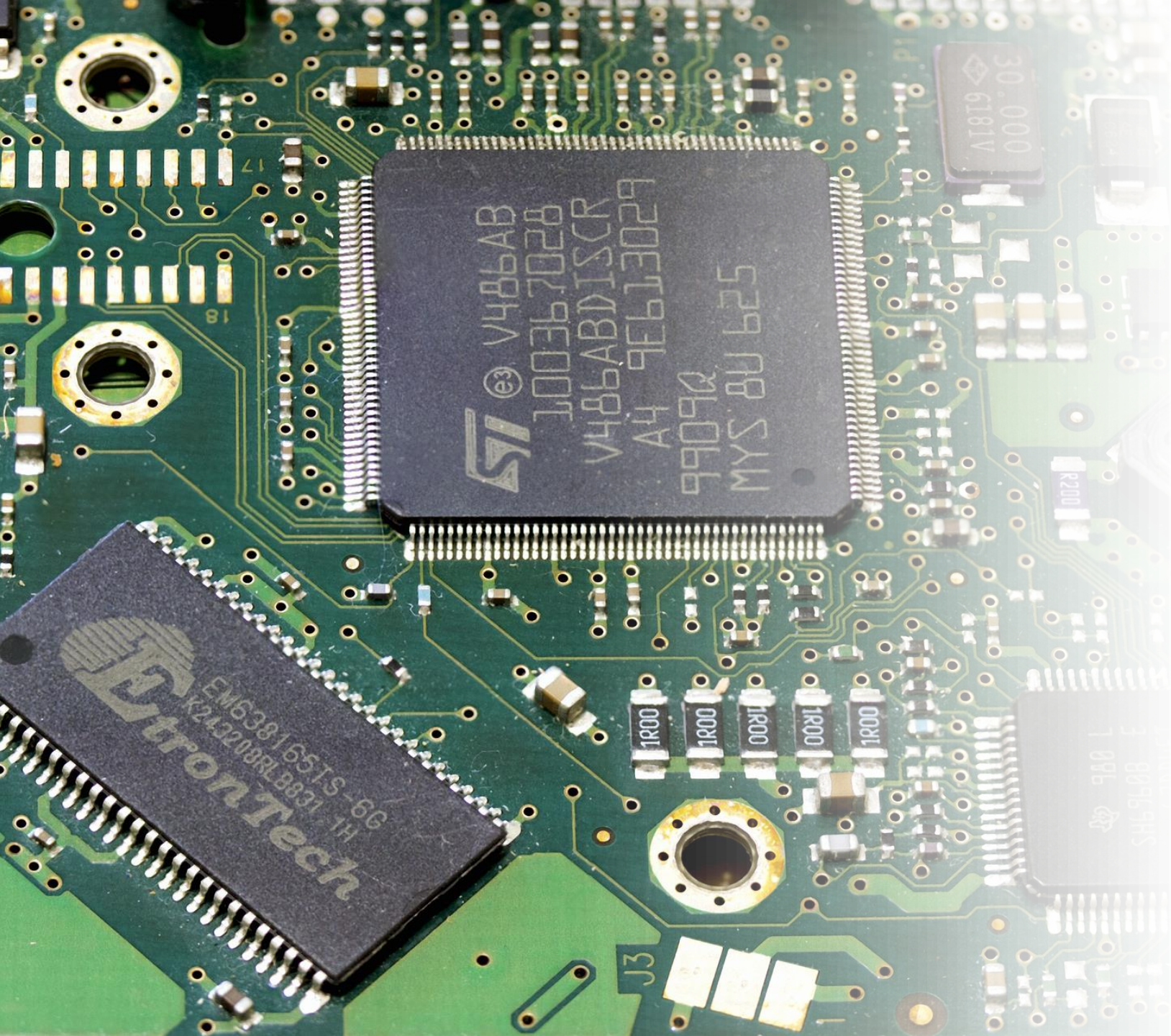

Digital Logic and System Design

9. FPGA

COL215, I Semester 2023-2024
Venue: LHC 111
'E' Slot: Tue, Wed, Fri 10:00-11:00

Instructor: Preeti Ranjan Panda
panda@cse.iitd.ac.in
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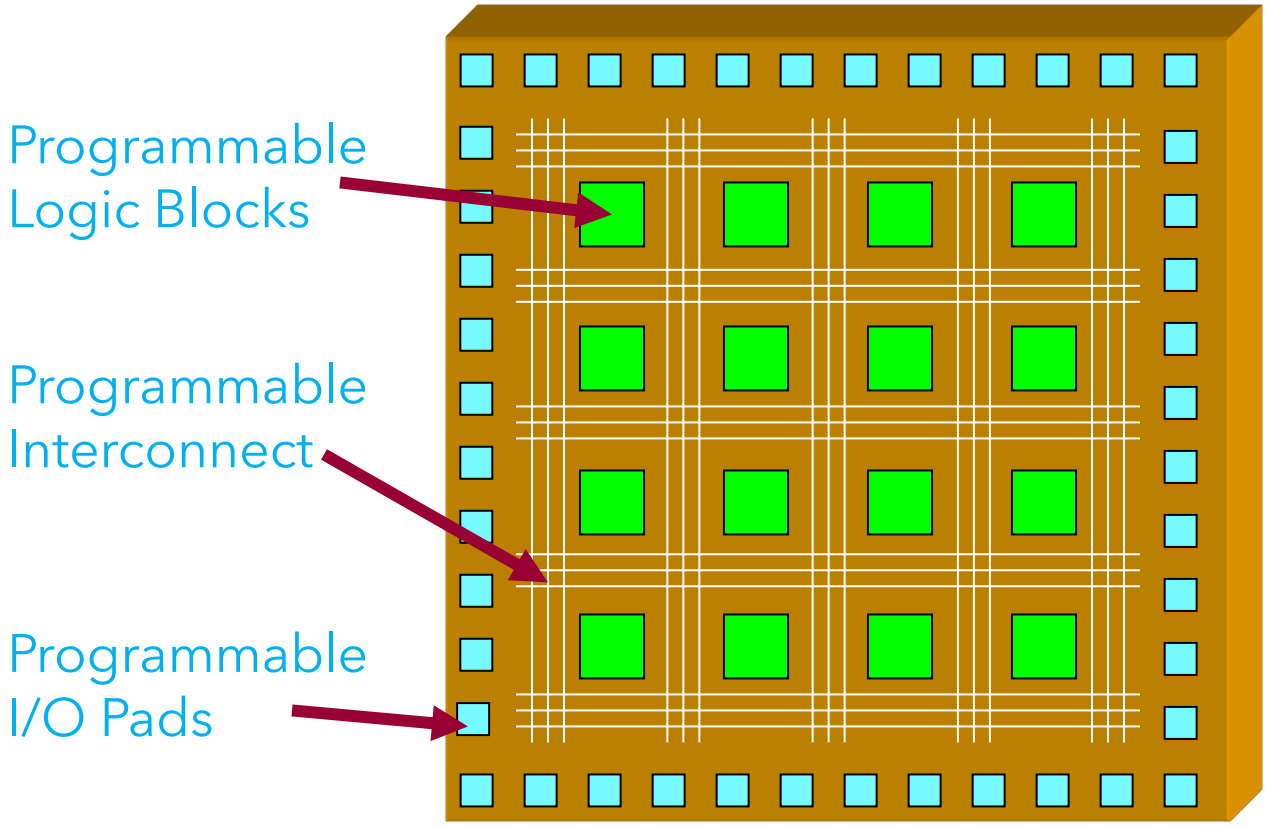
Dept. of Computer Science & Engg., IIT Delhi

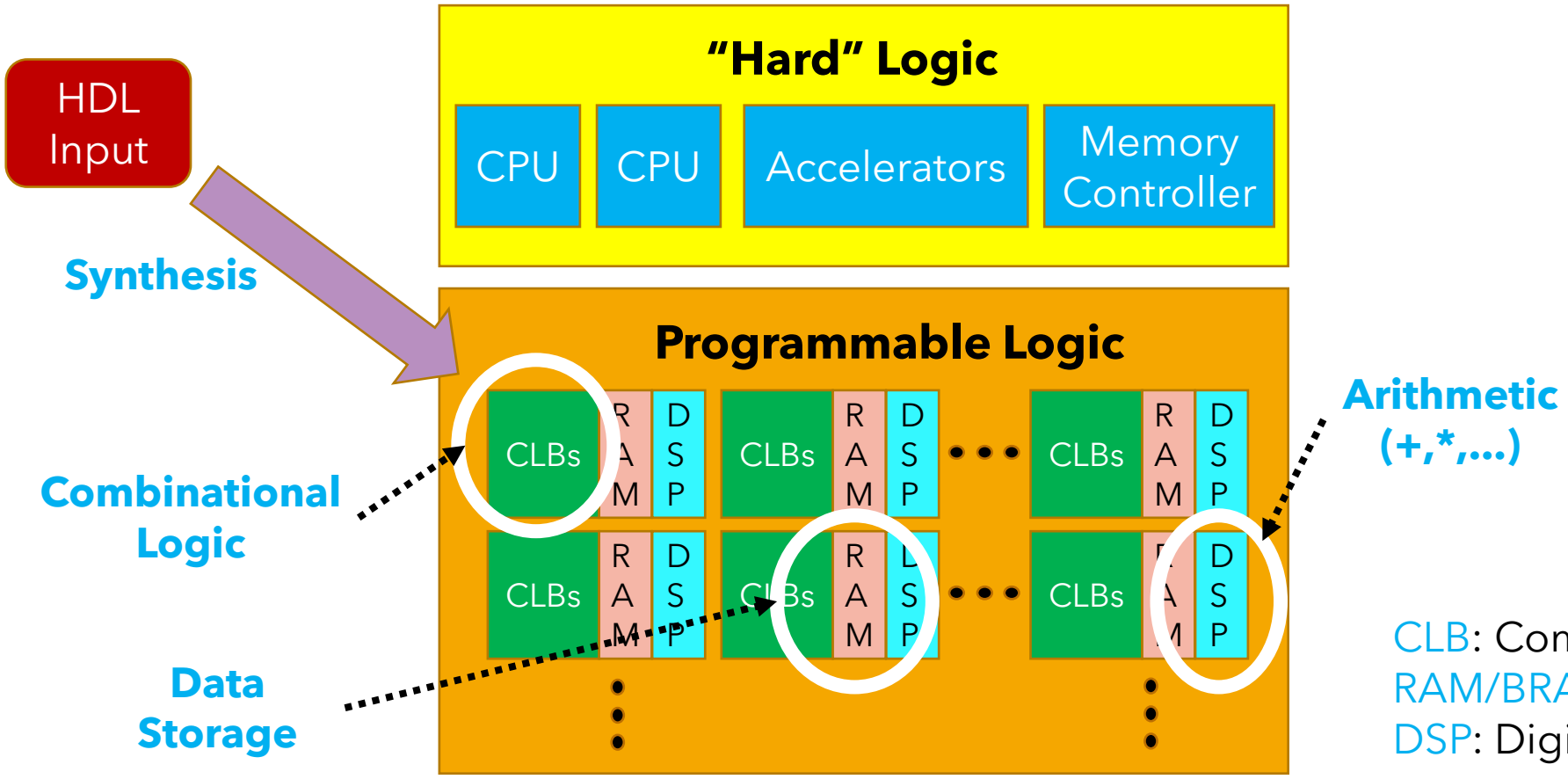
Field Programmable Gate Array

- **Field Programmable**
  - Customised/Programmed by designer
  - vs. "Mask Programmable": customised by foundry
- **Gate Array**
  - Design methodology: pre-fabricated gates, connected later
- Customisation/Programming process **simple/cheap**
  - Design turnaround time: minutes/hours
- FPGA chips **produced in bulk**
  - independent of functionality

Classical FPGA architecture

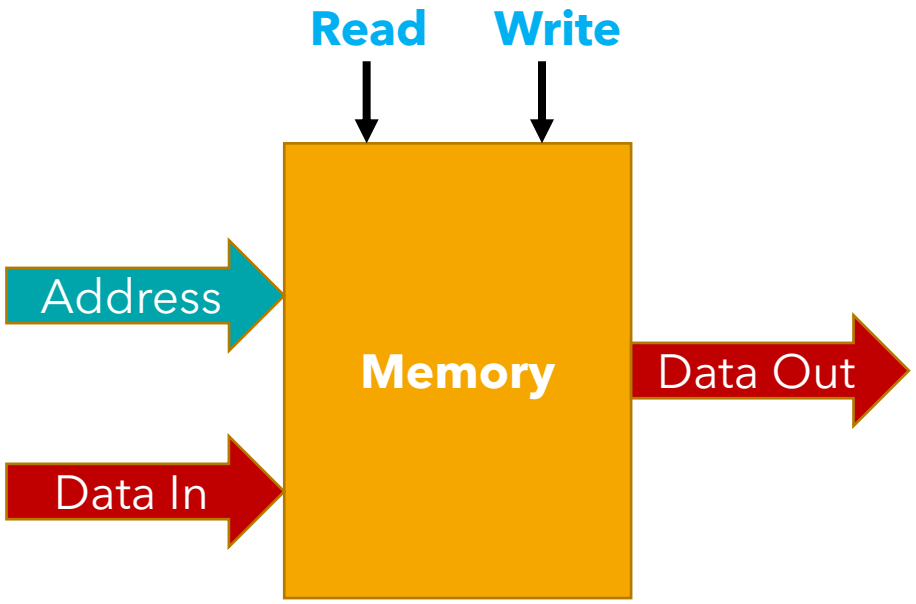


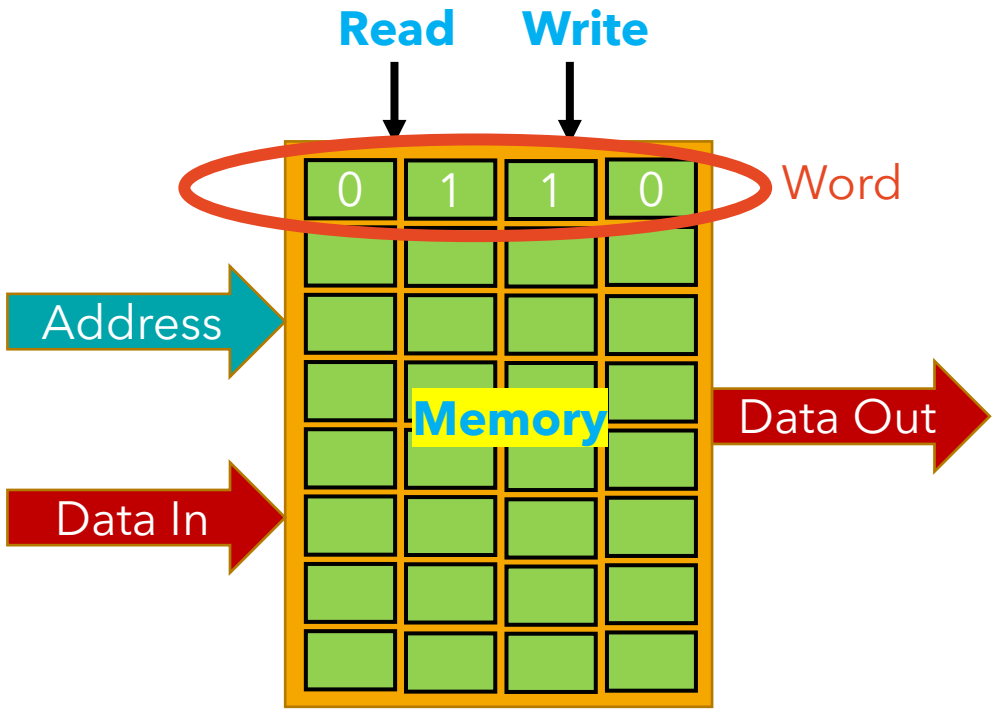
Modern FPGA Architecture: Xilinx Zynq 7000 Series



CLB: Combinational Logic Block
RAM/BRAM: Random Access Memory
DSP: Digital Signal Processing unit

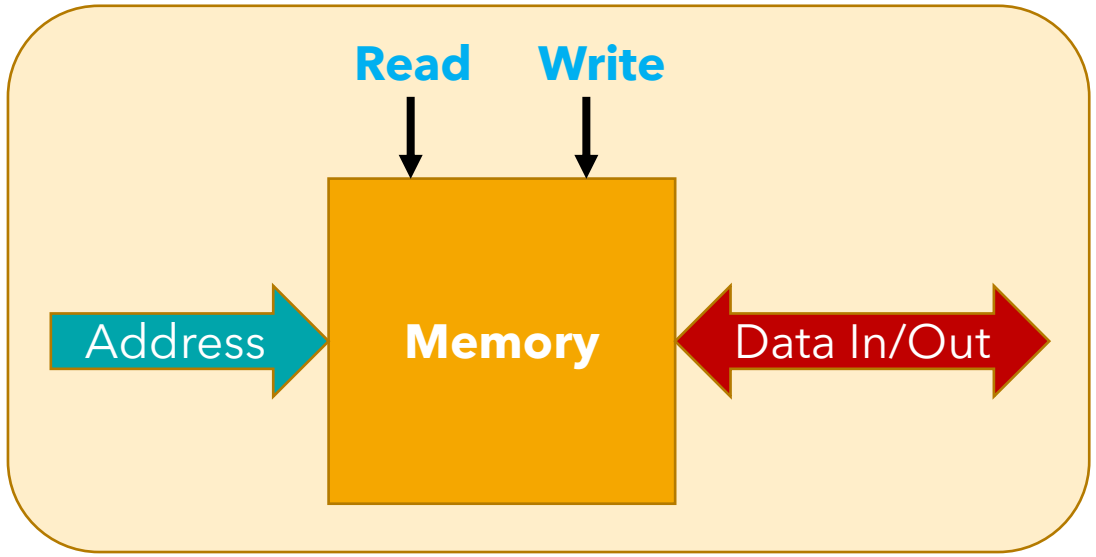
Memory



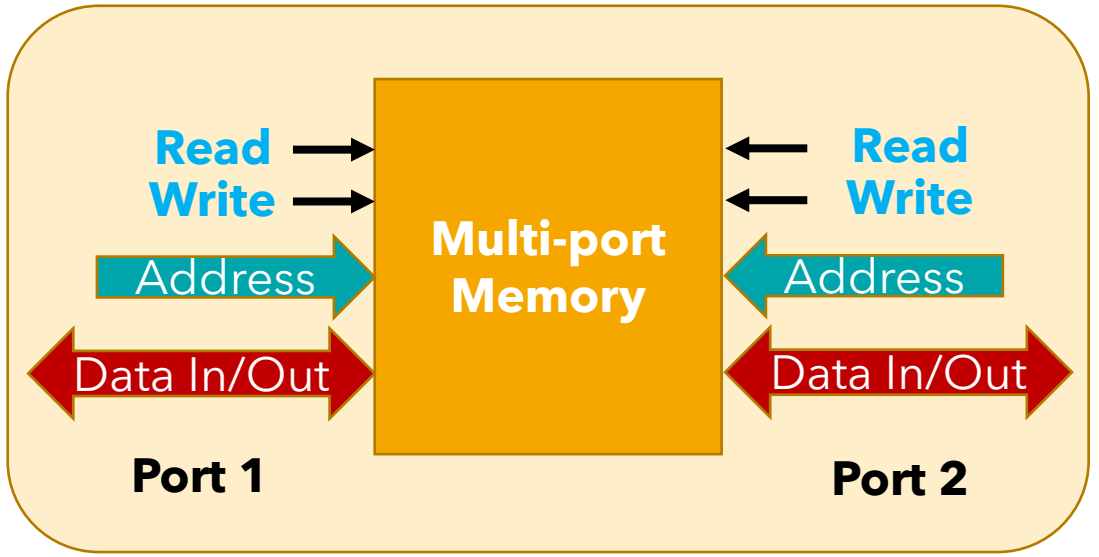


Word Size: 4 bits
Memory Size: 8 words

Memory: General Architectures



Bi-directional Data Bus

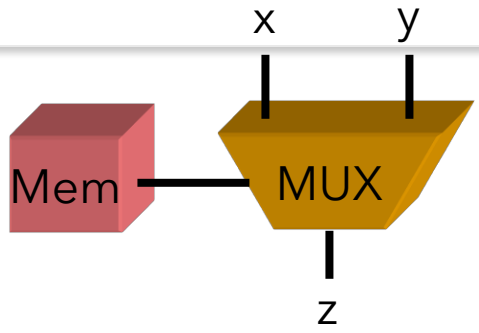


Multiple Simultaneous Accesses

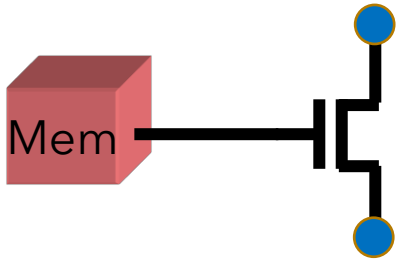
Read & Write on Same Address: ??

FPGA Programming: SRAM

- **SRAM**: Static Random Access Memory
  - Stores a bit (0/1)
- **Programming**:
  - writing 0 or 1 into SRAM cell
  - this, in turn, causes:
    - selections
    - connections



Programming the logic



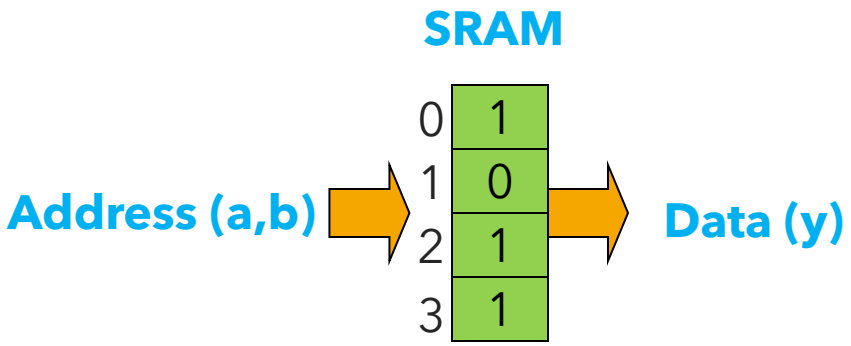
Programming the interconnection (short/open)

SRAM-based FPGA

- Each logic block consists of an SRAM
- An SRAM with 2^n bits can implement ANY function of n inputs
  - Use inputs as address
  - Store value in locations

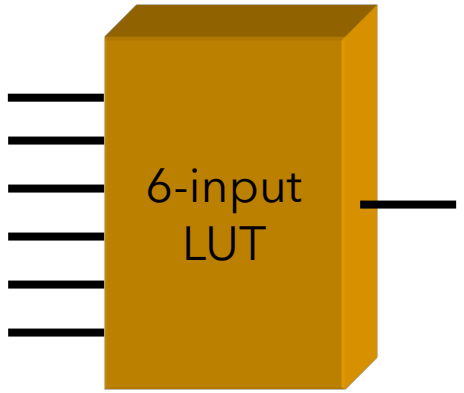
Truth Table of Function

a b	y
0 0	1
0 1	0
1 0	1
1 1	1



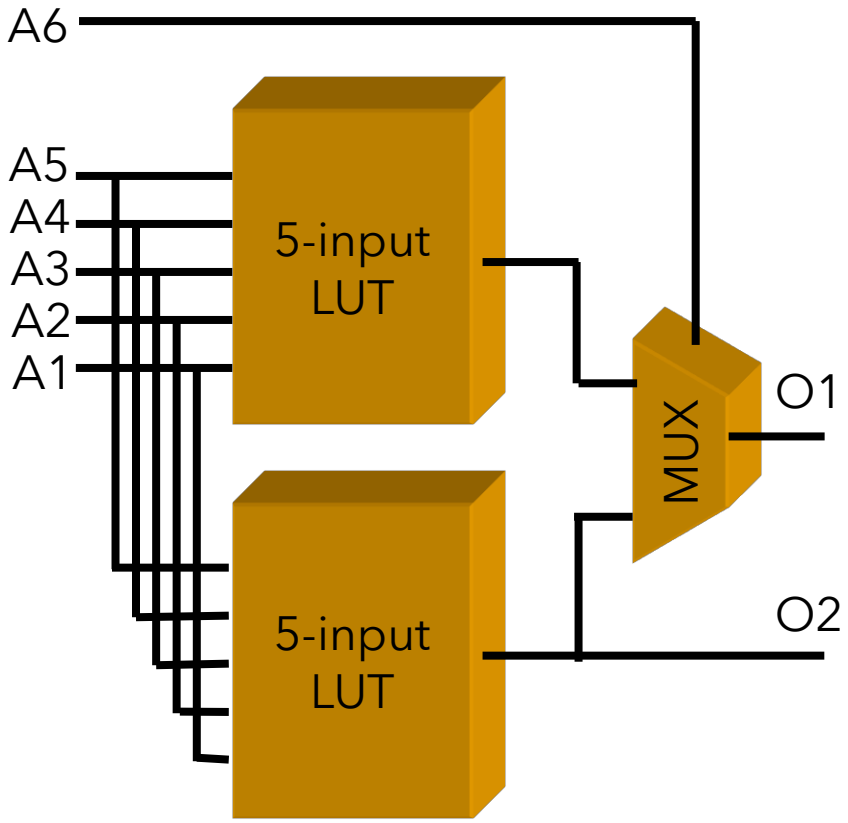
Xilinx 7-Series Architecture

- 64-bit Look-up Tables (LUT)
  - All functions of 6 inputs
- What if we wanted 2 functions of 5 inputs instead?

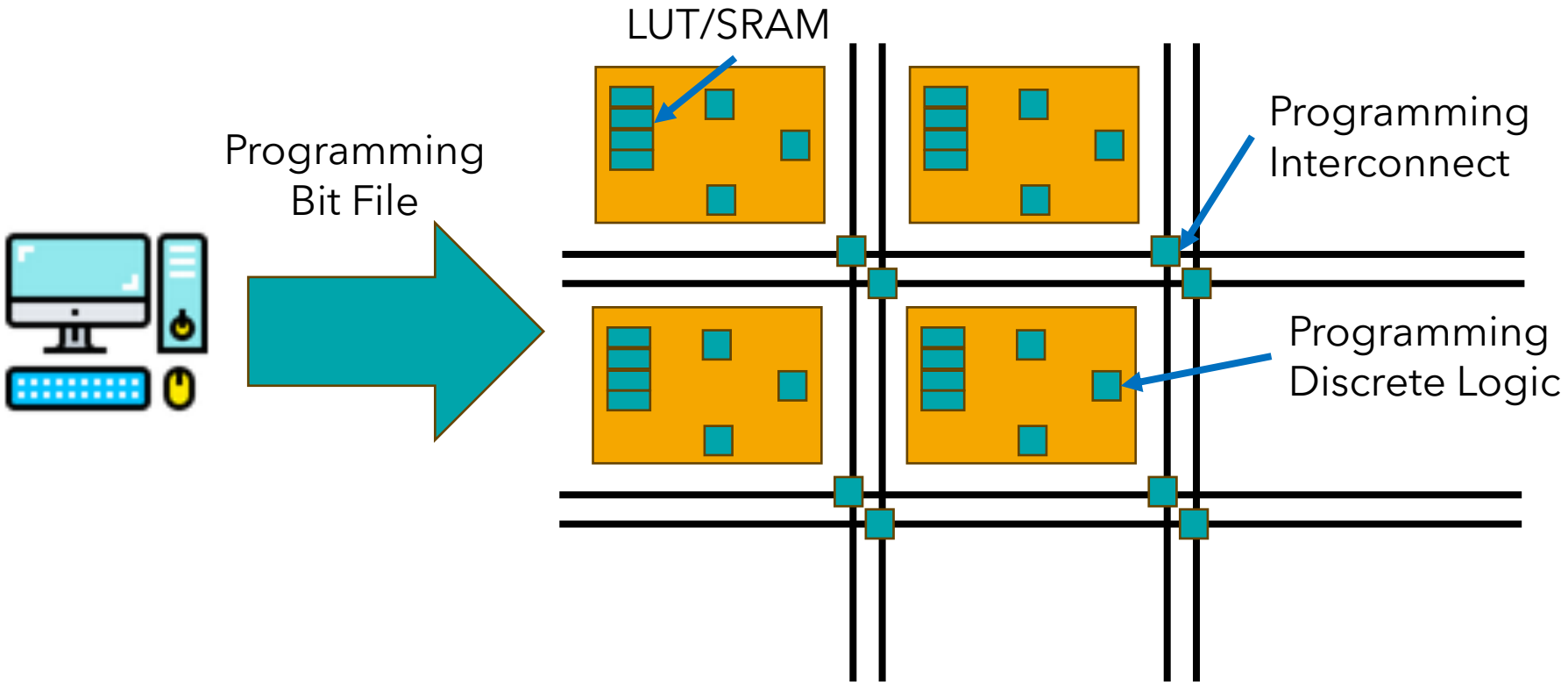


Xilinx 7-Series Architecture

- 2 Functions of 5 inputs
  - Split into 2 banks
    - 2 functions of 5 inputs



Programming the FPGA



Programming the FPGA