

2202-COL216 Major exam

UTKARSH SINGH 2021CS10558

TOTAL POINTS

43 / 60

QUESTION 1

1 Question 1 3 / 3

✓ + 3 pts Correct

+ 2 pts Partial correct 2 / No explanation

+ 1 pts Partial correct 1 / Explanation but incorrect ans

+ 0 pts Incorrect

QUESTION 2

2 Question 2 3 / 3

✓ + 3 pts Correct

+ 2 pts Partial Correct 2 (Calculated for 2 processors)

+ 1 pts Partial Correct 1 (Calculated for 1 processor1)

+ 0 pts Incorrect

- 0.5 pts Minor Mistake

QUESTION 3

3 Question 3 3.5 / 4

+ 4 pts Correct with explanation. Wrote proper relation based explanation and calculation for each subpart.

✓ + 3.5 pts Wrote only relations but no calculations included.

+ 3 pts Correct fillings without explanation.

- 0.5 pts per wrong filling.

+ 0 pts Blank

QUESTION 4

4 Question 4 3 / 3

✓ + 3 pts Correct with explanation. This include finding all the intermediate components before concluding the final answer

+ 1.5 pts few components are correct but wrong final answer or could not reach answer.

+ 1.5 pts Correct final answer without explanation (only answer written).

+ 1 pts Nothing is correct but tried.

+ 0 pts Blank

QUESTION 5

5 Question 5 6.5 / 7

Request-1

✓ + 1 pts Correct

+ 0.5 pts Partially Correct

+ 0 pts Incorrect

Request-2

✓ + 1 pts Correct

+ 0.5 pts Partially Correct

+ 0 pts Incorrect

Request-3

✓ + 1 pts Correct

+ 0.5 pts Partially Correct

+ 0 pts Incorrect

Request-4

✓ + 1 pts *Correct*

+ 0.5 pts *Partially Correct*

+ 0 pts *Incorrect*

Request-5

✓ + 1 pts *Correct*

+ 0.5 pts *Partially Correct*

+ 0 pts *Incorrect*

Request-6

+ 1 pts *Correct*

✓ + 0.5 pts *Partially Correct*

+ 0 pts *Incorrect*

Request-7

✓ + 1 pts *Correct*

+ 0.5 pts *Partially Correct*

+ 0 pts *Incorrect*

- 0.5 pts X and Y coexists

QUESTION 6

6 Question 6 10 / 10

✓ + 2 pts *correct miss rate for case 1.*

✓ + 2 pts *correct miss rate for case 2.*

✓ + 2 pts *correct miss rate for case 3*

✓ + 2 pts *answer with the correct reason for D.*

✓ + 2 pts *answer with the correct reason for E.*

+ 0 pts *not attempt or fully incorrect*

QUESTION 7

7 Question 7 0 / 10

+ 4 pts *A correct*

+ 3 pts *B correct*

+ 3 pts *C correct*

+ 2 pts *Partial marks for A*

+ 1.5 pts *Partial marks for B*

+ 1.5 pts *Partial marks for C*

✓ + 0 pts *Complete Wrong or missing*

QUESTION 8

Question 8 20 pts

8.1 (a) 0 / 3

+ 3 pts *Correct option with explanation*

+ 2 pts *Correct option but no explanation*

✓ + 0 pts *Incorrect*

8.2 (b) 2 / 2

✓ + 2 pts *Correct answer with explanation*

+ 1 pts *Correct answer but no explanation*

+ 0 pts *Incorrect*

8.3 (c) 2 / 2

✓ + 2 pts *True with Explanation*

+ 1 pts *True but no explanation*

+ 0 pts *Incorrect*

8.4 (d) 3 / 3

✓ + 3 pts *Correct with both points explained*

+ 1.5 pts *Only one point explained*

+ 0 pts *Incorrect*

8.5 (e) 0 / 3

+ 3 pts *Correct answer*

+ 2 pts *Correct bits calculation*

+ 1 pts *Partially correct bit calculation*

+ 1.5 pts *Correct Answer but no explanation*

✓ + 0 pts *Incorrect*

8.6 (f) 3 / 3

✓ + 3 pts *Correct*

+ 1.5 pts Partially Correct

+ 1.5 pts Correct answer but no explanation

+ 0 pts Incorrect

8.7 (g) 2 / 2

✓ **+ 2 pts** *Correct*

+ 1 pts Partial Correct

+ 0 pts Incorrect

8.8 (h) 2 / 2

✓ **+ 2 pts** *Correct*

+ 1 pts Partial Correct

+ 0 pts Incorrect

Name: Utkarsh Singh

Roll No: 2021CS10558

(COL 216) Computer Architecture

May 1, 2023

Major Exam

Duration: 120 minutes

(60 marks)

Beware: Be concise in your writing. You can use rough sheets for calculations. But you cannot submit any additional sheet for grading on Gradescope. So make sure you are certain when you write something (after rough work, or use a dark pencil). If you cheat, you will surely get an F in this course.

- Consider a processor with a 16 Kbyte unified L1 cache. The miss rate for this cache is 3% and the hit time is 2 clock cycles. The processor also has an 8 Mbyte, on-chip L2 cache. 95% of the time, data requests to the L2 cache are found. If data is not found in the L2 cache, a request is made to a 4 Gbyte main memory. The time to service a memory request is 100,000 clock cycles. On average, it takes 3.5 clock cycles to process a memory request. How often is data found only in main memory, and not in either of the two caches? [3 marks]

Let

$$\text{Miss rate of L1} = \frac{3}{100}$$

$$\text{Miss rate of L2} = \frac{5}{100}$$

Probability to miss in both L1 and L2 = $\frac{3}{100} \times \frac{5}{100} = \frac{15}{10000}$
 Probability to miss in L1 and find in L2 = $\frac{3}{100} \times \frac{95}{100} = \frac{285}{10000}$
 Probability to miss in L2 and find in L1 = $\frac{5}{100} \times \frac{95}{100} = \frac{475}{10000}$

Name: Utkarsh Singh

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2. Each instruction fetch means a reference to the instruction cache and 35% of all instructions reference data memory. Processor A has two 8 Kbyte, L1 caches – one for data and one for instructions. Computer B has a single, unified 16 Kbyte L1 cache that holds both instructions and data. For A, the average miss rate in the L1 instruction cache is 2%, the average miss rate in the L1 data cache is 10%, and the miss penalty for both data and instruction caches is 9 clock cycles. For B, the average miss rate is 3% for the cache as a whole, and the miss penalty is again 9 clock cycles. Which processor has better performance? [3 marks]

Soln) for A

$$\text{Miss rate of L1 (instruction)} = \frac{2}{100}$$

$$\text{Miss rate of L1 (data)} = \frac{10}{100}, \text{ Assume hit} = 1 \text{ clock cycle}$$

$$\text{Miss penalty} = 9$$

$$\text{Clock cycles per instruction} = 1 + \frac{2}{100} \times 9 + \frac{10}{100} \times \frac{35}{100} \times 9$$

$$= 1 + \frac{180}{1000} + \frac{315}{1000}$$

$$= 1 + \frac{495}{1000}$$

for B

$$\text{Clock cycles per instruction} = 1 + \frac{8}{100} \times 9 + \frac{35}{100} \times \frac{3}{100} \times 9$$

$$= 1 + \frac{2700 + 945}{10000}$$

$$= 1 + \frac{3645}{10000}$$

\therefore If we assume same hit time for both the processors, clock cycles per instruction of A is greater than B.

\therefore B performs better than A.

Name: Utkarsh Singh

Roll No: 2021CS10558

3. The following table gives the parameters for a number of different caches. Your task is to fill in the missing fields in the table. Recall that m is the number of physical address bits, C is the cache size (number of data bytes), B is the block size in bytes, E is the associativity, S is the number of cache sets, t is the number of tag bits, s is the number of set index bits, and b is the number of block offset bits. [4 marks]

Cache	m	C	B	E	S	t	s	b
1.	32	2048	8	1	256	21	8	3
2.	32	2,048	4	4	128	23	6	2
3.	32	1,024	2	8	64	25	6	1
4.	32	1024	32	2	16	23	4	5

Table 1: Cache organization

- 1) $S = 2^s = 2^8 = 256$, $C = BES = 2048$
- 2) $B = 2^b = 2^2 = 4$, $C = BES \Rightarrow E = 4$
- 3) $S = 2^s \Rightarrow s = 6$, $t + s + b = 32 \Rightarrow t = 25$
- 4) $C = BES \Rightarrow B = 32$, $b = \log B = 5$

4. A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing? [3 marks]

$$100 \text{ times refreshed} \rightarrow 10^{-3} \text{ sec}$$

$$1 \text{ times refreshed} \rightarrow 10^{-9} \text{ sec}$$

$$10^{-9} \text{ sec} \rightarrow 1 \text{ times refreshed}$$

$$\text{memory cycle time} = 64 \times 10^{-9} \text{ sec} \rightarrow 64 \times 10^{-4} \text{ times refreshed} = 64 \times 10^{-2} \text{ sec/nsec}$$

for refreshing

so out of total 64 nsec, 64×10^{-2} nsec is used for refreshing

$$\frac{64 \times 10^{-2}}{64} \times 100 = 1\% \quad (\text{Answer})$$

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5. Consider a symmetric shared-memory multiprocessor (3 processors sharing a bus) implementing a snooping cache coherence protocol (MSI). For each of the events below, explain the coherence protocol steps (does the cache flag a hit/miss, what request is placed on the bus, who responds, is a writeback required, etc.) and mention the eventual state of the data block in the caches of each of the 3 processors. Assume that X and Y are not in any of the caches at the start of the sequence, the caches are direct-mapped, and blocks X and Y map to the same set in each cache (X and Y cannot co-exist in a cache at any time). [7 marks]

Request	Cache hit/miss	Request on bus	Who responds/ Write Back happens?	Cache 1 state	Cache 2 state	Cache 3 state
P1: Write X	miss	Main memory sends X	Main memory sends X, no write back only P1 writes	M	I	I
P2: Write X	miss	to invalid X in P1 and send X to P2	P1 responds, no write back	I	M	I
P3: Read X	miss	P2 sends the value of X and gets shared	P2 responds, write back happens	I	S	S
P1: Read X	miss	Main memory sends X,	Main memory responds, no write back	S	S	S
P3: Write X	hit	invalidates P1, P2	P3, responds no write back	I	I	M
P3: Read Y	miss	Main memory gets write backed and sends Y	Main memory responds, write back happens	I	I	M
P2: Write Y	miss	P3 sends Y and invalidates	P2: responds no write back	I	M	I

Table 2: Snoop based Cache Coherence Table

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6. You are given the following code to analyze:

```
1 int x[2][128];
2 int i; int sum = 0;
3
4 for (i = 0; i < 128; i++) {
5     sum += x[0][i] * x[1][i];
6 }
```

Assume we execute this under the following conditions: (a) sizeof(int) = 4. (b) Array x begins at memory address 0x0 and is stored in row-major order. (c) In each case below, the cache is initially empty. (d) The only memory accesses are to the entries of the array x. All other variables are stored in registers. Given these assumptions, estimate the miss rates for the following cases: [10 marks]

A. Case 1: Assume the cache is 512 bytes, direct-mapped, with 16-byte cache blocks. What is the miss rate?

B. Case 2: What is the miss rate if we double the cache size to 1,024 bytes?

C. Case 3: Now assume the cache is 512 bytes, two-way set associative using an LRU replacement policy, with 16-byte cache blocks. What is the cache miss rate?

D. For case 3, will a larger cache size help to reduce the miss rate? Why or why not?

E. For case 3, will a larger block size help to reduce the miss rate? Why or why not?

A) +block size = $\frac{512}{16}$

No. of blocks = $\frac{512}{16} = 32$ = no. of sets 4 = no of index bits

block size = 16 bytes \Rightarrow 4 integers in 1 block.

address of $x[0][i]$	index no.
0	0
4	0
8	0
12	0
16	1
20	1
:	:
504	30
508	31

address of $x[1][i]$	index no.
512	0
516	0
520	0
524	1
528	1
:	:
532	1
536	1
540	1
544	1
548	1
552	1
556	1
560	1
564	1
568	1
572	1
576	1
580	1
584	1
588	1
592	1
596	1
600	1
604	1
608	1
612	1
616	1
620	1
624	1
628	1
632	1
636	1
640	1
644	1
648	1
652	1
656	1
660	1
664	1
668	1
672	1
676	1
680	1
684	1
688	1
692	1
696	1
700	1
704	1
708	1
712	1
716	1
720	1
724	1
728	1
732	1
736	1
740	1
744	1
748	1
752	1
756	1
760	1
764	1
768	1
772	1
776	1
780	1
784	1
788	1
792	1
796	1
800	1
804	1
808	1
812	1
816	1
820	1
824	1
828	1
832	1
836	1
840	1
844	1
848	1
852	1
856	1
860	1
864	1
868	1
872	1
876	1
880	1
884	1
888	1
892	1
896	1
900	1
904	1
908	1
912	1
916	1
920	1
924	1
928	1
932	1
936	1
940	1
944	1
948	1
952	1
956	1
960	1
964	1
968	1
972	1
976	1
980	1
984	1
988	1
992	1
996	1
1000	1

Total read operations = $128 \times 2 = 256$

We can observe that whenever we will access $x[0][i]$, it will surely be a miss, because either that index is preoccupied by $x[1][i-1]$ or it is empty.

Similar observation can be made for $x[1][i]$, so miss rate is 100%

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B) ~~No.~~ no. of indexes = $\frac{1024}{16} = 64$

in this case

address of $m[0][i]$	index no.	address of $m[i][0]$	index no.
0	0	512	32
4	0	516	32
8	0	520	32
12	1	;	{
16	1	;	
;	1	;	
504	31	;	
508	31	;	
		63	63
		63	63

- Q) In every 4 iteration: 8 reads are present. Out of which 6 are hits.
 $\therefore \text{miss rate} = \frac{2}{8} \times 100 = 25\%$

C) no of indexes = $\frac{512}{16 \times 2} = 16$

address of $m[0][i]$	index no.	address of $m[i][0]$	index no.
0	0	0	0
4	0	0	0
8	0	0	0
12	1	0	1
16	1	0	1
;	1	0	1
504	15	0	15
508	15	0	15
		15	15
		15	15

here, index of $m[0][i]$ and ~~$m[i][0]$~~ are same but no collision because 2-way associative. So out of 8, 6 hits, [25% miss rate]

- D) No, if we increase cache size, keeping block size constant we won't get an increase in hit rate because out of 4, miss ~~is~~ is inevitable (compulsory) infact all the misses in two way associative is compulsory misses. ~~so even if~~ so even if no of indexes gets increased no of misses will remain same.

- E) Yes, larger block size will help reduce miss rate, because new no. of compulsory misses will get reduced, ~~as~~ More integers can fit in a single block, \therefore No of hits increases and no of misses ~~as~~ decreases.

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7. You are writing a new 3D game. You are currently working on a function to blank the screen buffer before drawing the next frame. The screen you are working with is a 640×480 array of pixels. The machine you are working on has a 32 KB direct-mapped cache with 8-byte lines. The C structures you are using are as follows:

```
1 struct pixel{  
2     char r;  
3     char g;  
4     char b;  
5     char a;  
6 };  
7  
8 struct pixel buffer[480][640];  
9 int i, j;  
10 char *cptr;  
11 int *iptr;  
12 }
```

Assume the following: (a) $\text{sizeof(char)} = 1$ and $\text{sizeof(int)} = 4$ (b) buffer begins at memory address 0. The cache is initially empty. (c) The only memory accesses are to the entries of the array buffer. Variables i, j, cptr, and iptr are stored in registers.

(A) What percentage of writes in the following code will hit in the cache? [4 marks]

```
1 for (j = 639; j >= 0; j--) {  
2     for (i = 479; i >= 0; i--){  
3         buffer[i][j].r = 0;  
4         buffer[i][j].g = 0;  
5         buffer[i][j].b = 0;  
6         buffer[i][j].a = 0;  
7     }  
8 }
```

(B) What percentage of writes in the following code will hit in the cache? [3 marks]

```
1 char *cptr = (char *) buffer;  
2 for (; cptr < (((char *) buffer) + 640 * 480 * 4); cptr++)  
3     *cptr = 0;
```

(C) What percentage of writes in the following code will hit in the cache? [3 marks]

```
1 int *iptr = (int *) buffer;  
2 for (; iptr < ((int *) buffer + 640 * 480); iptr++)  
3     *iptr = 0;  
4 }
```

A) No of bytes in 1 block = $\frac{32 \times 10^3}{8} = 4000$ bytes

- ∴ 4000 characters are present in a block.
∴ buffer[i][j].r, buffer[i][j].g, buffer[i][j].b, buffer[i][j].a will be in a single block.
so after every ~~1000~~ iterations there will be ~~1000~~ misses approximately. Eg: ~~buffer[0][0] → 1~~

~~address(buffer)~~
~~index(buffer[0][0]) - index(buffer[0][0])~~
~~address(buffer[0][0]) - (address of buffer[1][0])~~
 $= 640$

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No of ~~misses~~ misses in filling whole cache atleast once ~~2000 bytes~~
~~(2 lines)~~

$$\frac{8000}{1000} \text{ (miss in every } 1000^{\text{th}} \text{ entry)}$$

Assume 50 iteration.

~~No of lines filled = 50~~

$$\text{No of misses} \xrightarrow{\text{miss rate}} = \frac{640 \times 50}{1000} = \frac{32000}{1000} = 32$$

No of misses
in 50 iterations

$$\therefore \text{miss rate} = \frac{32}{50 \times 4} \times 100 = 16\%$$

B)

~~640 × 480 × 4~~
We can see that 4000 characters are present
in a block, and ~~that~~ write operations are
performed sequentially.

$$\therefore \text{Miss rate} = \frac{1}{4000} \times 100 = \frac{1}{40} \%$$

C) Here, 1 miss will occur after 1000 ~~writes~~ writes

so

$$\text{Miss rate} = \frac{1}{1000} \times 100 = 0.1\%$$

Name: Utkarsh Singh

Roll No: 2021CS10558

8. Choose the correct answer or write short answers to the following questions. [20 marks]

- (a) Consider the IEEE-754 single precision floating point numbers $P = 0xC1800000$ and $Q = 0x3F5C2EF4$. Which one of the following corresponds to the product of these numbers represented in the IEEE-754 single precision format? [3 marks]

- (a) $0x404C2EF4$ ✓ (b) $0x405C2EF4$ (c) $0xC15C2EF4$ (d) $0xC14C2EF4$

- (b) Consider a 3-stage pipelined processor having a delay of 10 nanosecs, 20 nanosecs, and 14 nanosecs for the first, second, and the third stages, respectively. Assume that there is no other delay and the processor does not suffer from any pipeline hazards. Also assume that one instruction is fetched every cycle. The total execution time for executing 100 instructions on this processor is 2040 ns nanosecs. [2 marks]

$$\text{Clock cycle} = 20 \text{ ns}$$

$$\text{total clock cycles} = 102$$

$$\text{total time} = 102 \times 20 \text{ ns} = 2040 \text{ ns}$$

- (c) "False sharing occurs only if a cache block contains multiple words" - True or False? Why? [2 marks]

True, because false sharing means than one word is present in stale state, i.e. its updated value is somewhere else and other word in the same block is fresh, i.e. it contains its updated value. Therefore multiple words are required in false sharing.

- (d) In a MSI coherence protocol, when is a cache controller forced to write back a block, B? [3 marks]

In a MSI, cache controller is forced to write back in two cases:

- 1) When cache is present in modified state and a request to read that particular block comes.
- 2) When that block is present in modified state and it requests read of some other block of same index which replaces that particular block in modified state, in that case, write back is required.

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- (e) Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____. [3 marks]

- (f) Consider a 3 GHz processor with a three-stage pipeline and stage latencies τ_1 , τ_2 and τ_3 such that $\tau_1 = 3\tau_2/4 = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is 4 GHz, ignoring delays in the pipeline registers. [3 marks]

$$\tau_1 : \tau_2 : \tau_3 = 1 : \frac{4}{3} : \frac{1}{2}, \text{ after split } \neq 1 : \frac{2}{3} : \frac{2}{3} : \frac{1}{2}$$

so new latency = $\frac{3}{4}$ times previous
1 sec $\rightarrow 3 \times 10^9$ operations
no of operations will be $\frac{4}{3} \times 3 \times 10^9 = 4 \times 10^9 = 4 \text{ G Hz}$

- (g) Tick all that apply. Concepts taught in class to improve program performance are: [2 marks]
 (a) pipelining (b) branch prediction (c) pipeline stalls (d) caching (e) cache coherence

- (h) Tick all that apply. Concepts taught in class to maintain program correctness are: [2 marks]
 (a) pipelining (b) branch prediction (c) pipeline stalls (d) caching (e) cache coherence