

Lab Exercise 4: Seven Segment Display

Design and implement a Seven Segment Display with the functional description given below.

The aim of this exercise is to learn how to use 4-digit seven segment display available on the BASYS3 board. It involves designing and implementing a circuit to display 16-bit binary number set on the slide switches as a 4 digit hexadecimal number (number with base 16).

Let the 16-bit binary number be $b_{15} b_{14} \dots b_1 b_0$ and its hexadecimal equivalent be $h_3 h_2 h_1 h_0$. Then these are related as follows.

$$h_0 = b_3 b_2 b_1 b_0$$

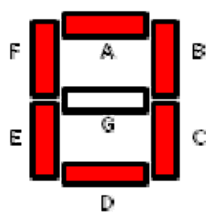
$$h_1 = b_7 b_6 b_5 b_4$$

$$h_2 = b_{11} b_{10} b_9 b_8$$

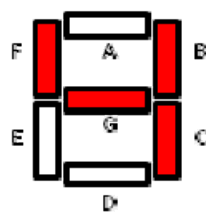
$$h_3 = b_{15} b_{14} b_{13} b_{12}$$

Instructions on how to use the display are given in section 8 of the BASYS3 board reference manual (available on Moodle). Patterns to be used for displaying hexadecimal digits are shown in the figure below.

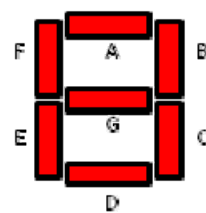
Bin: 0000 Hex: 0



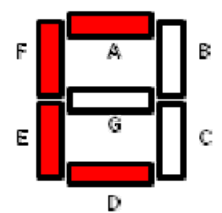
Bin: 0100 Hex: 4



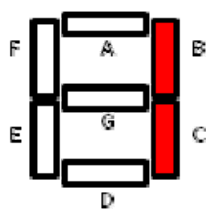
Bin: 0100 Hex: 8



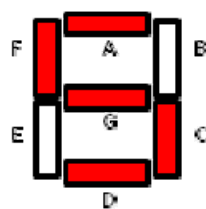
Bin: 1100 Hex: C



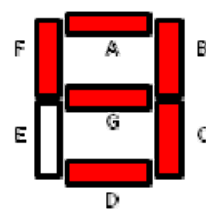
Bin: 0001 Hex: 1



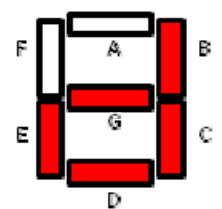
Bin: 0101 Hex: 5



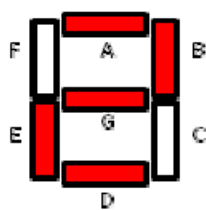
Bin: 1001 Hex: 9



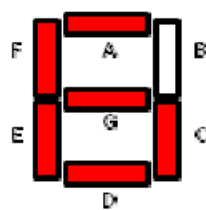
Bin: 1101 Hex: d



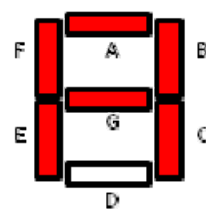
Bin: 0010 Hex: 2



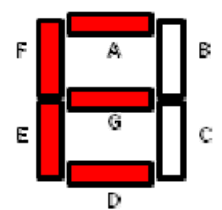
Bin: 0110 Hex: 6



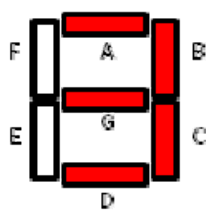
Bin: 1010 Hex: A



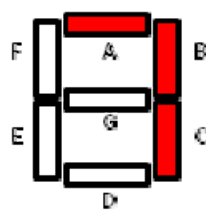
Bin: 1110 Hex: E



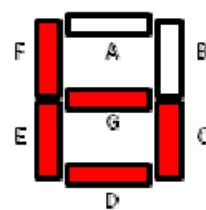
Bin: 0011 Hex: 3



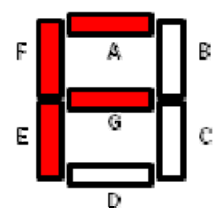
Bin: 0111 Hex: 7



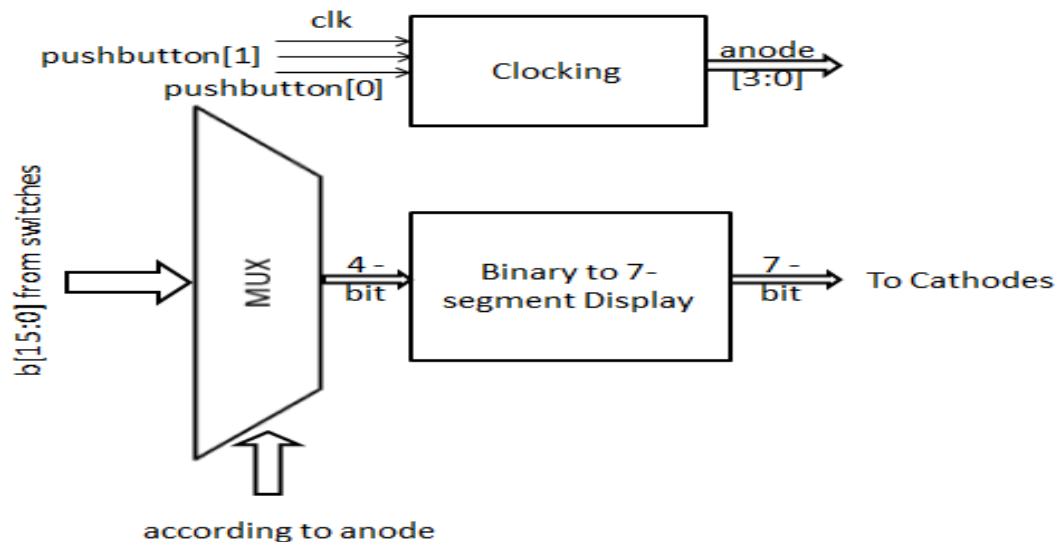
Bin: 1011 Hex: b



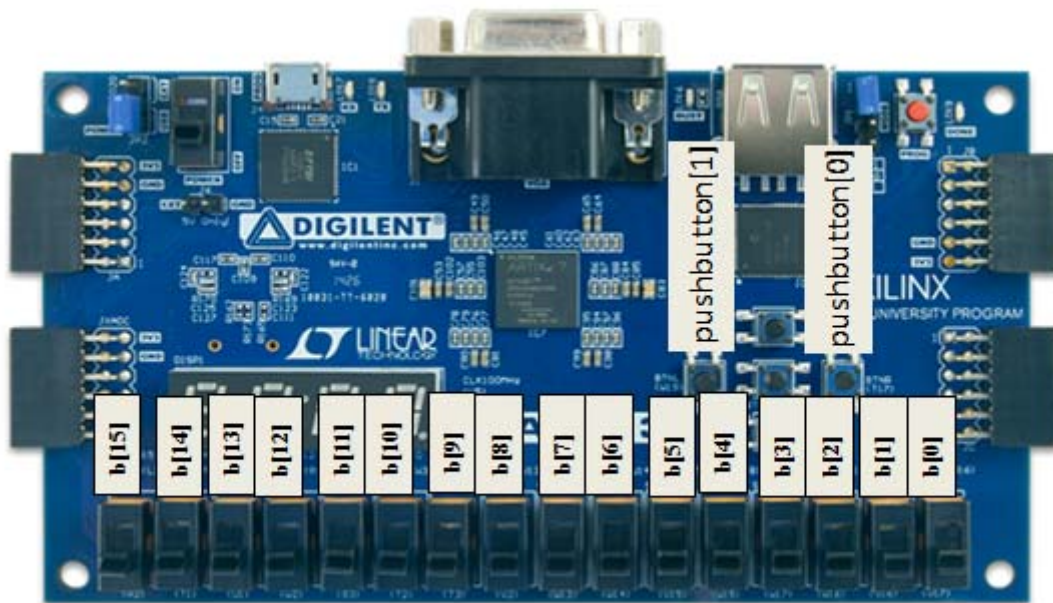
Bin: 1111 Hex: F



A rough sketch of the circuit is shown below. The 4 digits are displayed in a time multiplexed manner with refresh rate in the range of 60 Hz to 1 KHz. The clock available on the FPGA board has a frequency of 100 MHz which needs to be suitably divided to get a clock in the required range (4 times the refresh rate, that is, from 240 Hz to 4 KHz). However, during simulation, it is convenient to work directly with the clock without dividing it. Therefore, the circuit should provide two modes – one where the clock is divided (slow clock mode) and the other where it is not (fast clock mode).



Refer Basys 3 Document (part 8) for enabling cathodes and anodes.



$b[15:0]$ is the bit vector for 16 bit input.
 $pushbutton [1:0]$ is used to select clock rate.

Pressing $pushbutton[1]$ selects the fast clock mode
 Pressing $pushbutton[0]$ selects the slow clock mode

For Simulation, press pushbutton[1] and for verifying the synthesized circuit board, press pushbutton[0] to “01”.

Pin Name	Description	Purpose
clk	Input (from Basys 3 Internal clock)	clocking
b[15:0]	Input	Binary input from switches
Pushbutton[1:0]	Input	Selects clock rate
anode[3:0]	Output	To enable the digit on Display
cathode[6:0]	Output	To display the Hex Digit

Top Level Module Name : lab4_seven_segment_display