CMOS CIRCUIT DESIGN

REPORT

8 Bit Asynchronous Up Counter using Master Slave JK Flip-Flop

Problem Statement: A food factory has items manufactured and transported from one part to another part in their making stage and items are transported using a conveyor belt in ones or in pairs (that is either there will be one item or two items) design a counter to calculate the number of items. (In the design 2 counters of 4 bits to calculate up to 100 numbers using asynchronous clock will be required).

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Objective: To design an 8 Bit Up counter using Asynchronous Clock.

Software: Microwind Software.

Logic Gates:

- Three input Nand Gate
- Two Input Nand gate
- Not gate
- Five input And Gate
-

Mini Circuits: Master Slave JK Flip-Flop.

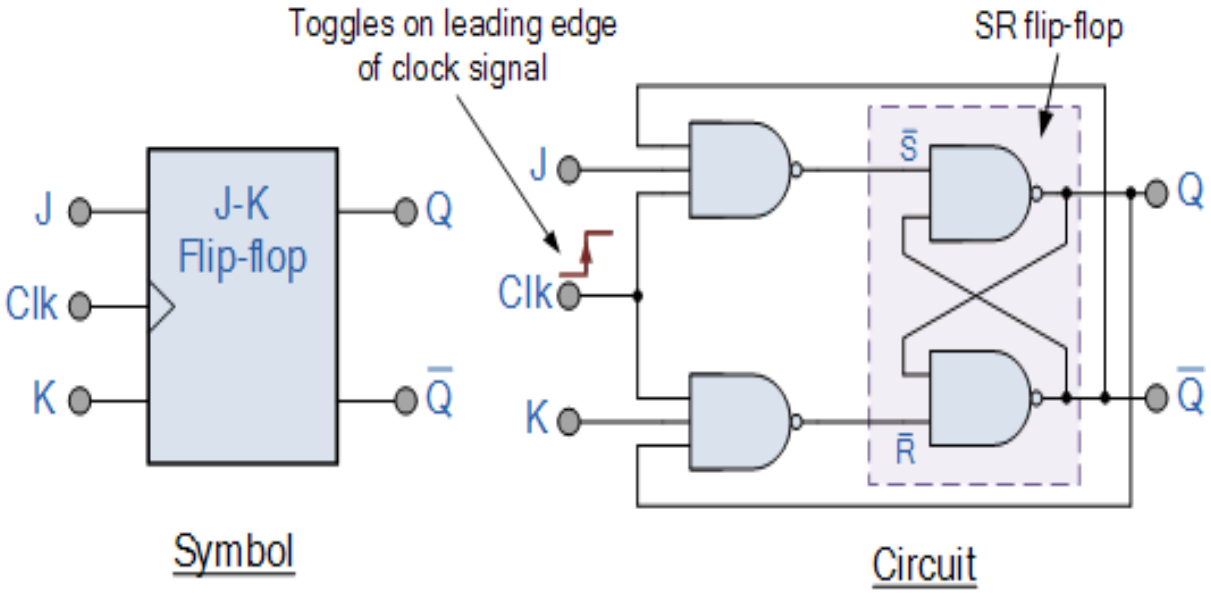
Construction: The construction started with JK Flip- Flop arrangement, the JK Flip Flop is made using Two Three input NAND gate and 2 Two input NAND gate in which the arrangement is made like the figure. The extra metal contacts required in the connections were metal-2 to polysilicon, metal-3 to polysilicon and metal 1- metal 3 contact.

The Master Slave JK Flip-Flop arrangement is needed to avoid the discrepancy faced in JK Flip-Flop that is when the clock frequency is lower and J=1 and K=1 the output toggles with each of clock pulse and the output needed for the further connection can get disrupted. The master slave arrangement consist of two clock pulse in which one pulse is not of the other master arrangement has positive edge triggered as master will always be the first to be triggered and the slave will follow the master. The Slave is a SR Flip flop the whole arrangement consists of 2 Three input NAND gates and 6 Two input NAND Gates.

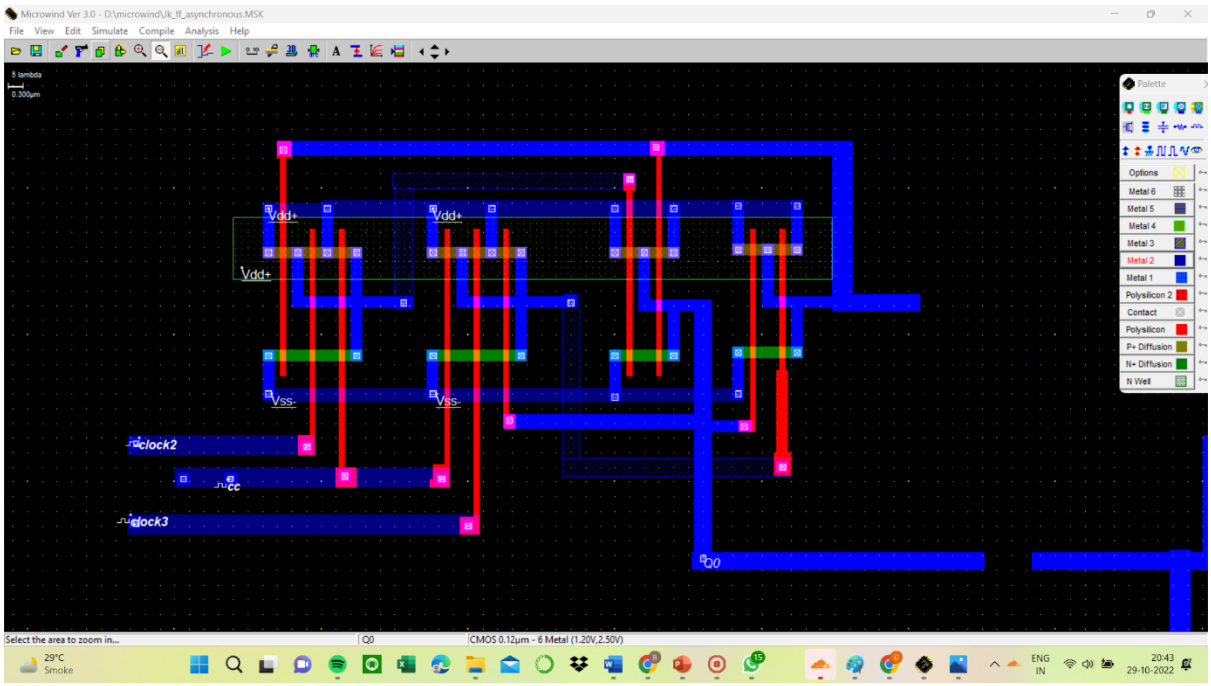
The 8-bit Asynchronous counter is made by using 8 Master Slave JK Flip Flop in which J=1 and K=1, and the clock pulse for each of the flip flop is taken from the not output of the previous Flip Flop. After 4 Flip Flop a five input NAND Gate is Connected to give the required output. The extra metal contacts used are metal-4 to polysilicon, metal-4 to metal1 and metal 4- metal1 connection. The output of the counter is taken from nQ terminal.

Microwind Diagrams and their Output:

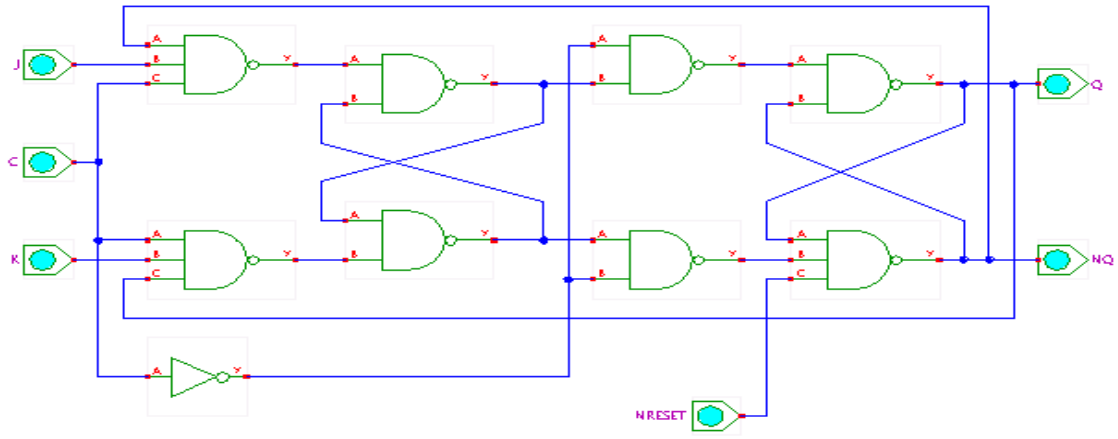
JK FLIP- FLOP



JK FLIP- FLOP MICROWIND DIAGRAM

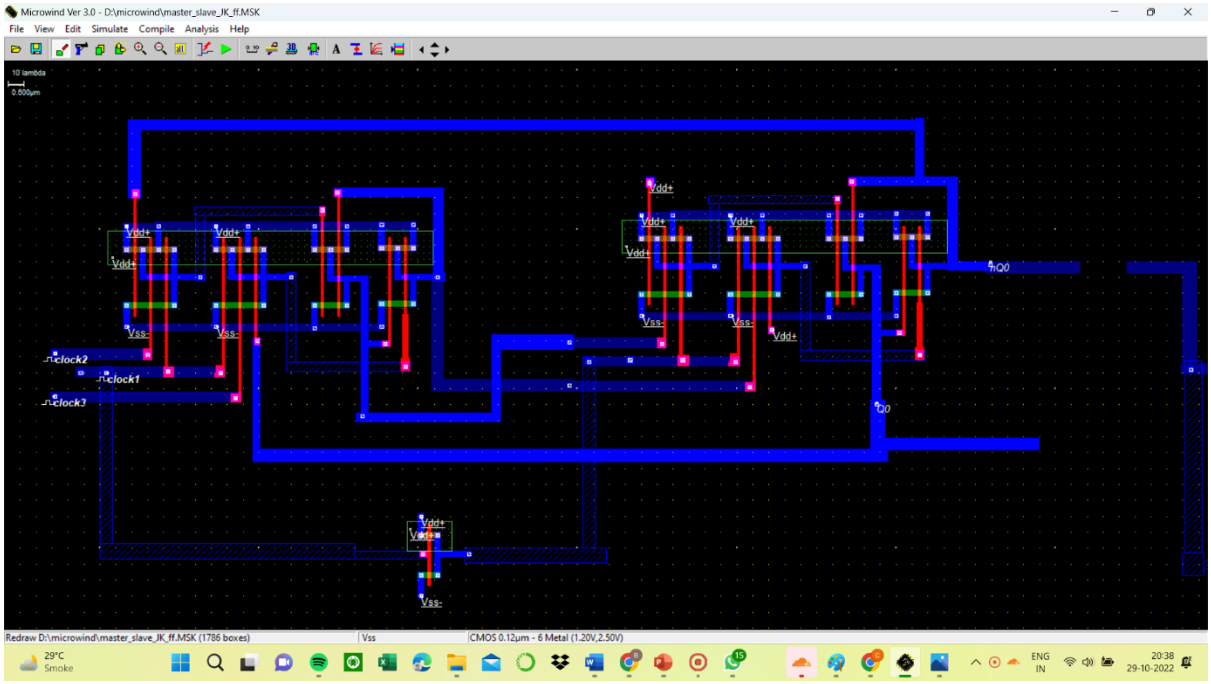


MASTER SLAVE JK FLIP-FLOP

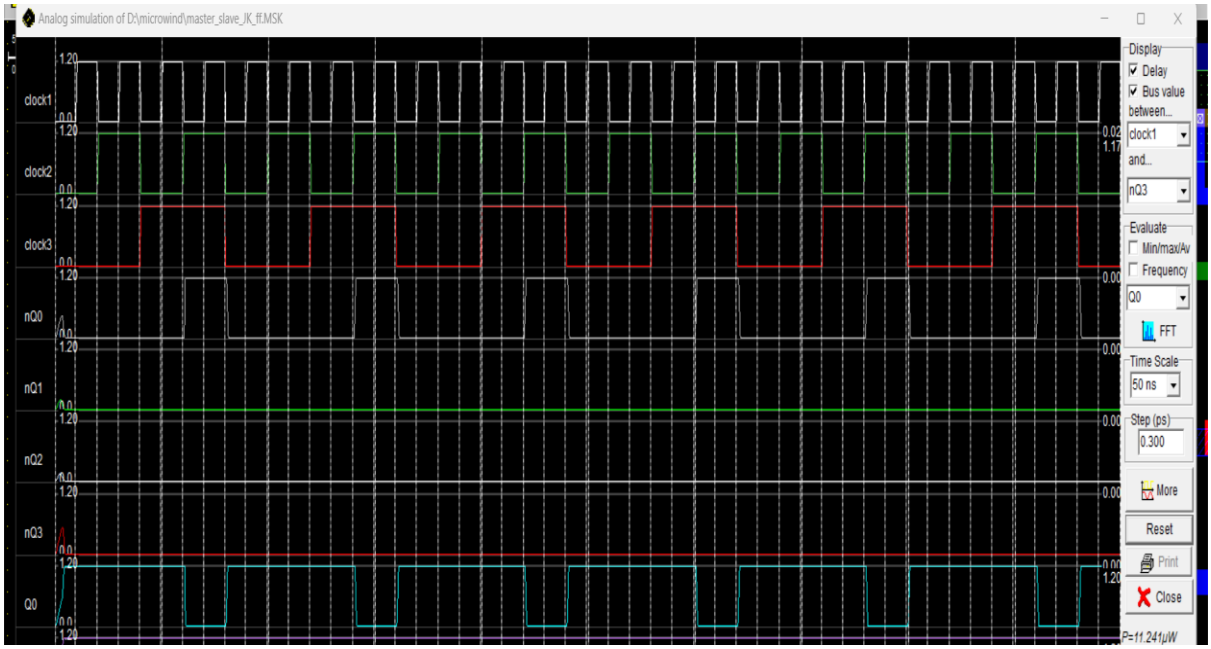


Note: initialization of this circuit is tricky. Use the NRESET switch. See the documention for help.

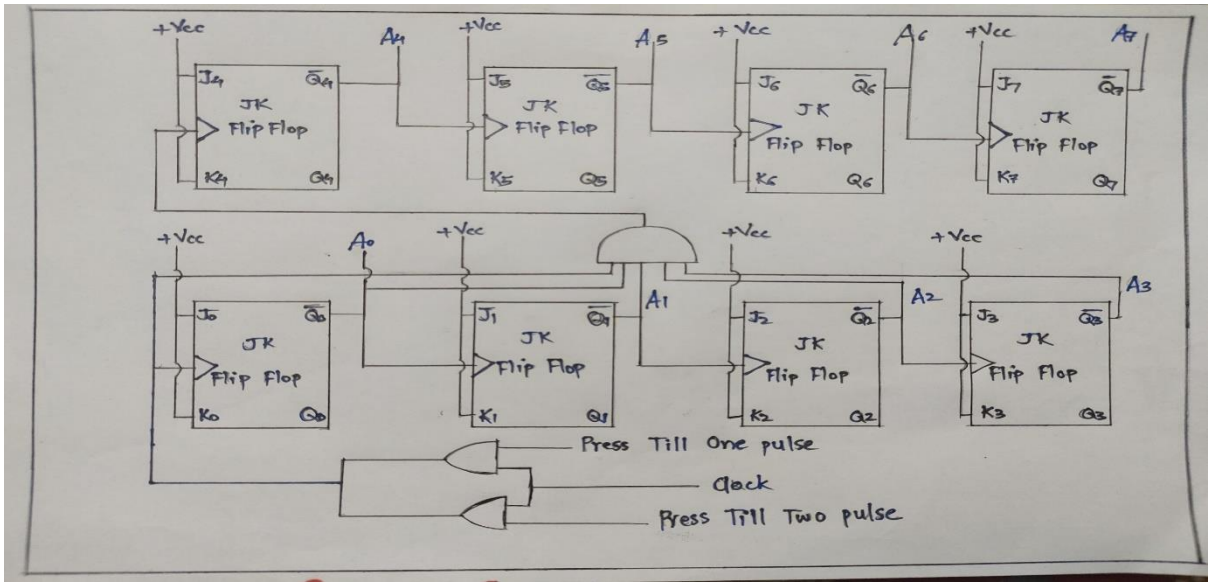
CMOS DIAGRAM



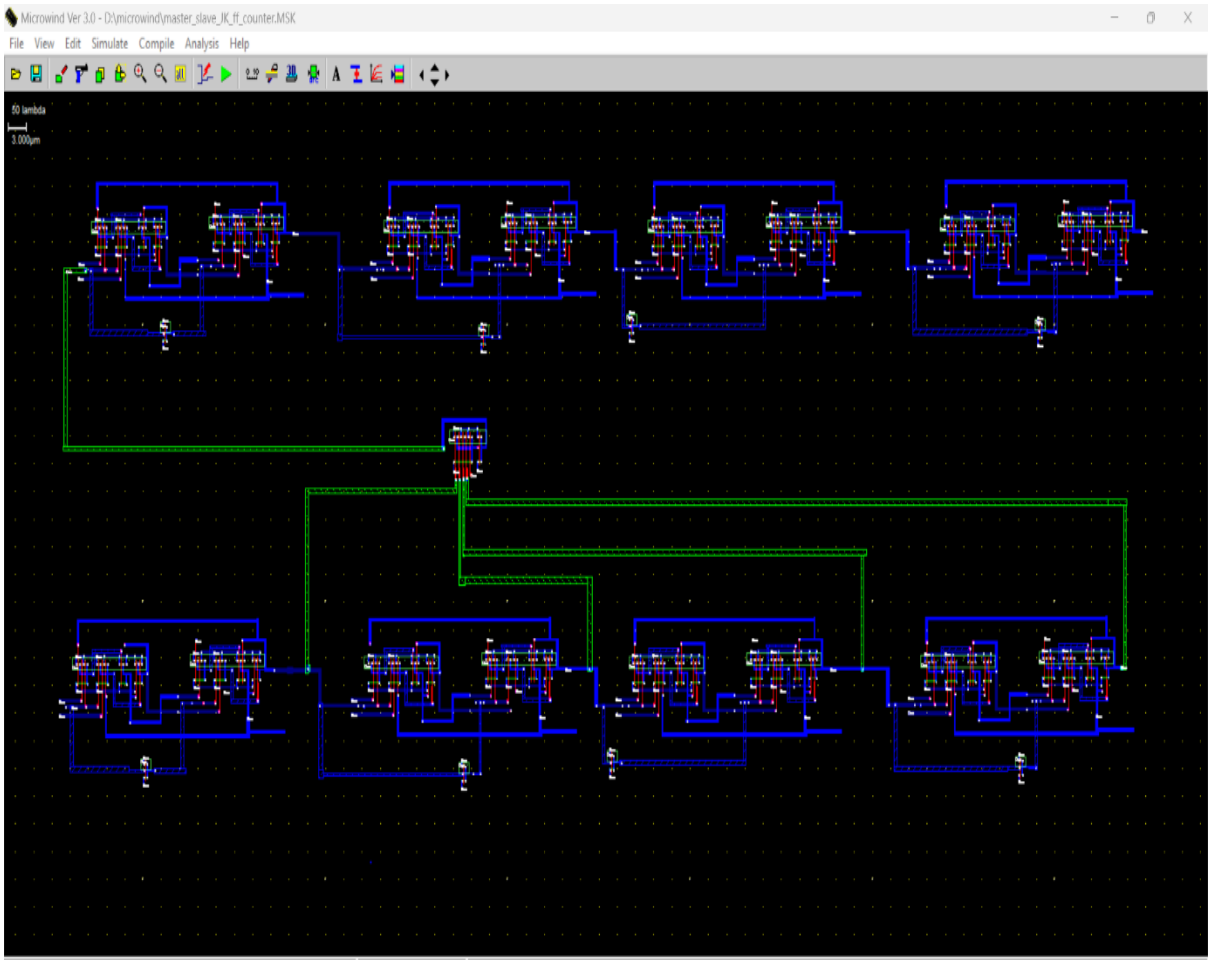
OUTPUT OF MASTER SLAVE JK FLIP- FLOP



LOGIC DIAGRAM



MICROWIND DIAGRAM OF UPCOUNTER



OUTPUT OF UP-COUNTER

Problems Faced: The construction of using a synchronous clock was difficult and use of D Flip Flop increases the space as well as construction complexity of the circuit. The use of Flip flop like SR and JK without slave arrangement gives error in the final output due to their invalid state and propagation delay. The construction can be simpler without NAND gate also. The simulation of the circuit with one pulse and two pulse was not possible in the same software as it also requires a timer operation as the button are to be pressed for a particular time but the main motive to create a up- counter is accomplished.

Conclusion: The up counter is designed and is working fine.