DAY-1

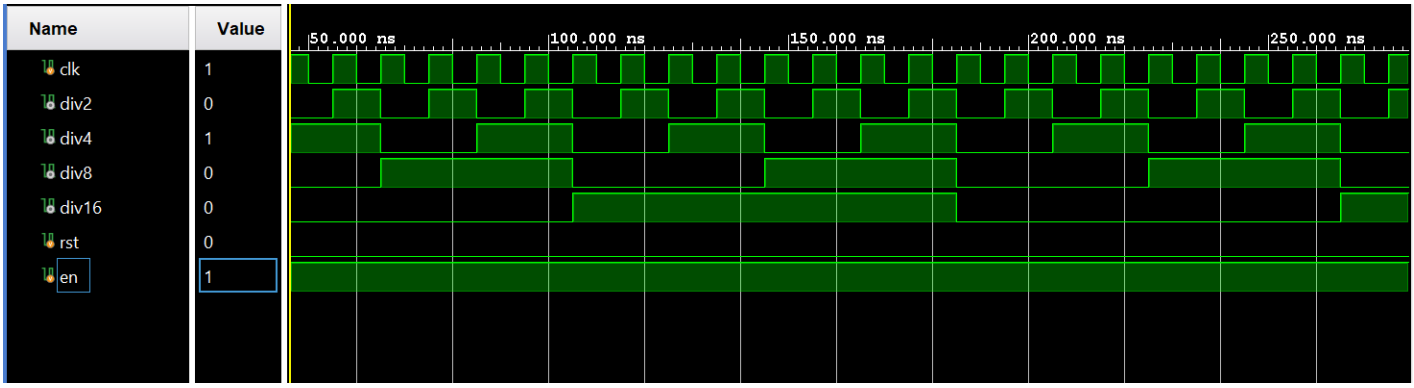
#100DAYSRTL

Aim:- To design the Clock divider (by clk/2n)

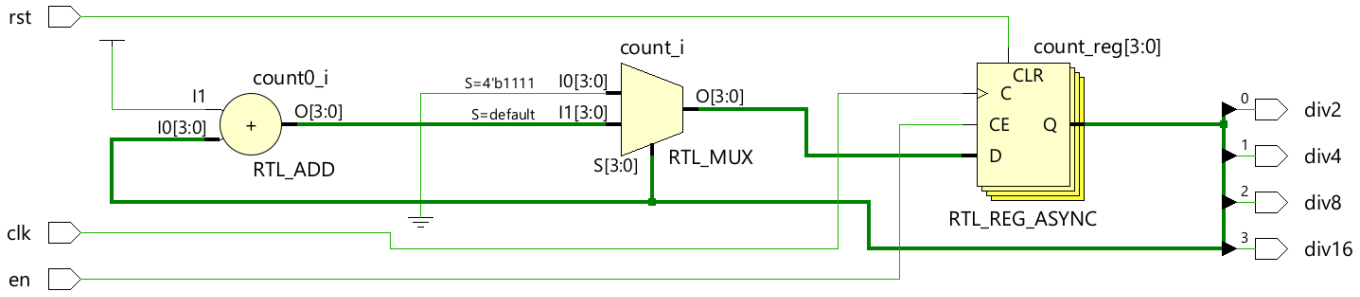
Verilog Code:-

```
1  //Author:- Chinna Venkata Narayana Reddy
2  //Date:-28/08/2023
3  module ClockDividerBy2n(
4      input rst, clk, en,
5      output  div2, div4, div8, div16
6  );
7      reg [3:0] count;
8
9      always @(posedge clk or posedge rst) begin
10         if (rst)
11             count <= 0;
12         else if (en) begin
13             if (count == 4'd15)
14                 count <= 0;
15             else
16                 count <= count + 1;
17         end
18     end
19     assign div2 = count[0];
20     assign div4 = count[1];
21     assign div8 = count[2];
22     assign div16 = count[3];
23 endmodule
```

Waveforms:-



Schematics:-


rst
clk
en
count0_i
I1
I0[3:0]
+
O[3:0]
RTL_ADD
count_i
S=4'b1111
I0[3:0]
S=default
I1[3:0]
O[3:0]
S[3:0]
RTL_MUX
count_reg[3:0]
CLR
C
CE
Q
D
RTL_REG_ASYNC
0
div2
1
div4
2
div8
3
div16