DAY-27

#100DAYSRTL

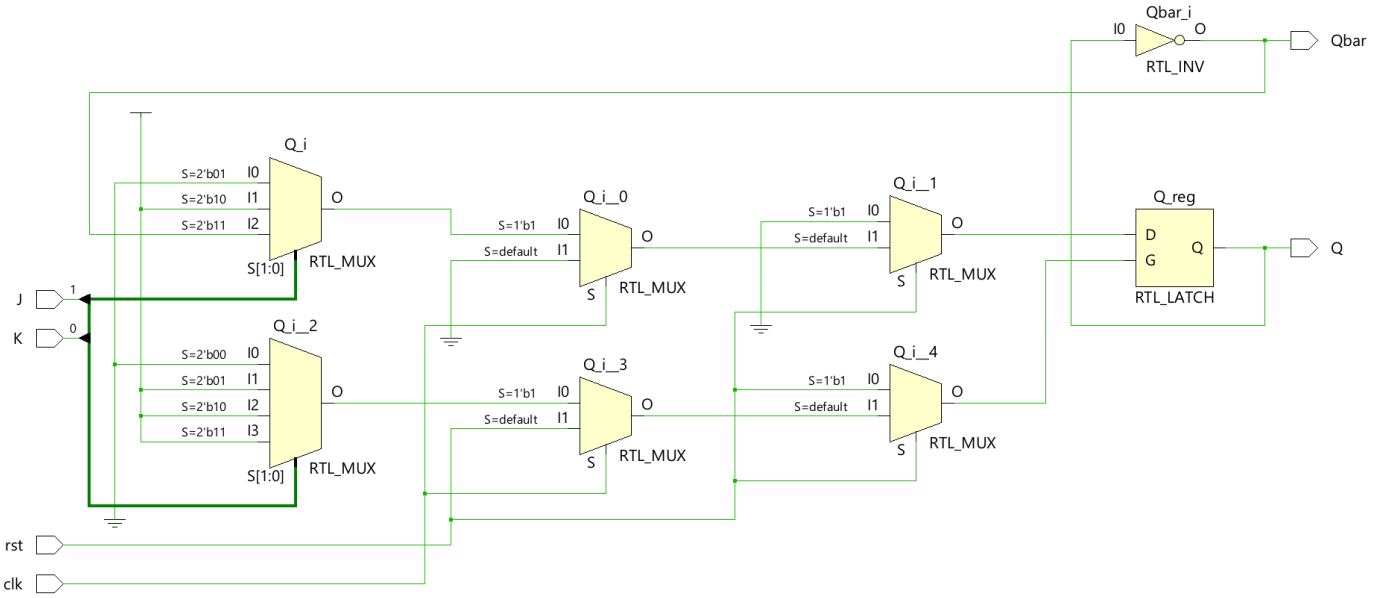
“Aim”:-To design JK Latch and D latch

“JK latch” :-

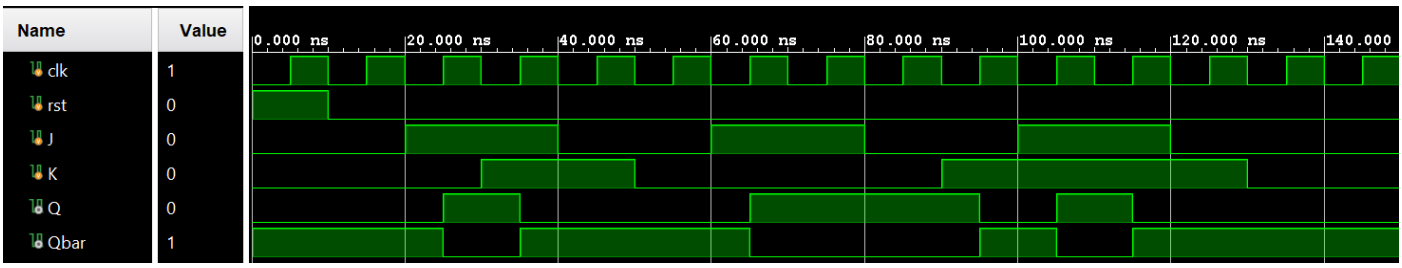
“Design Code”:-

```
`timescale 1ns/1ps
module JK_Latch (
  input clk, rst,
  input J, K,
  output reg Q,
  output Qbar
);
  always_latch  begin
  if (rst) Q=0;
    else if(clk) begin
      case ({J, K})
        2'b00: Q <= Q;     // No change
        2'b01: Q <= 1'b0; // Reset
        2'b10: Q <= 1'b1; // Set
        2'b11: Q <= ~Q;    // Toggle
        default : begin ; end
      endcase
    end
  end
  assign Qbar = ~Q;
endmodule
```

“Schematics”:-



“Waveforms”:-



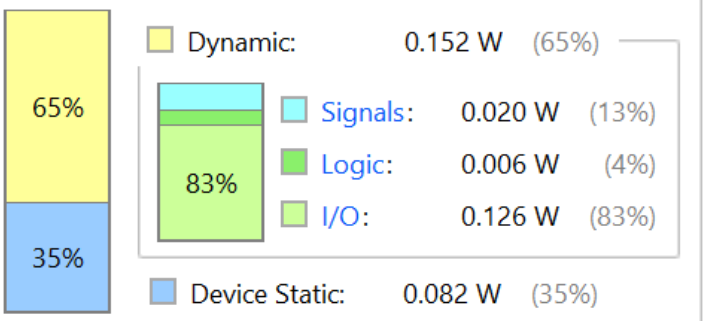
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.233 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (31.4 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

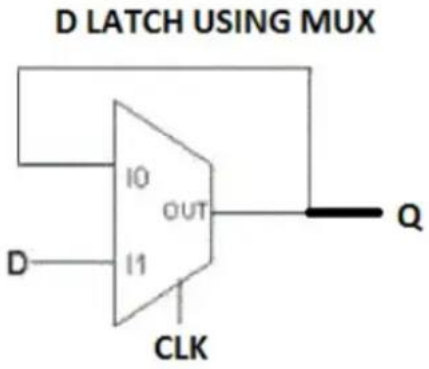
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



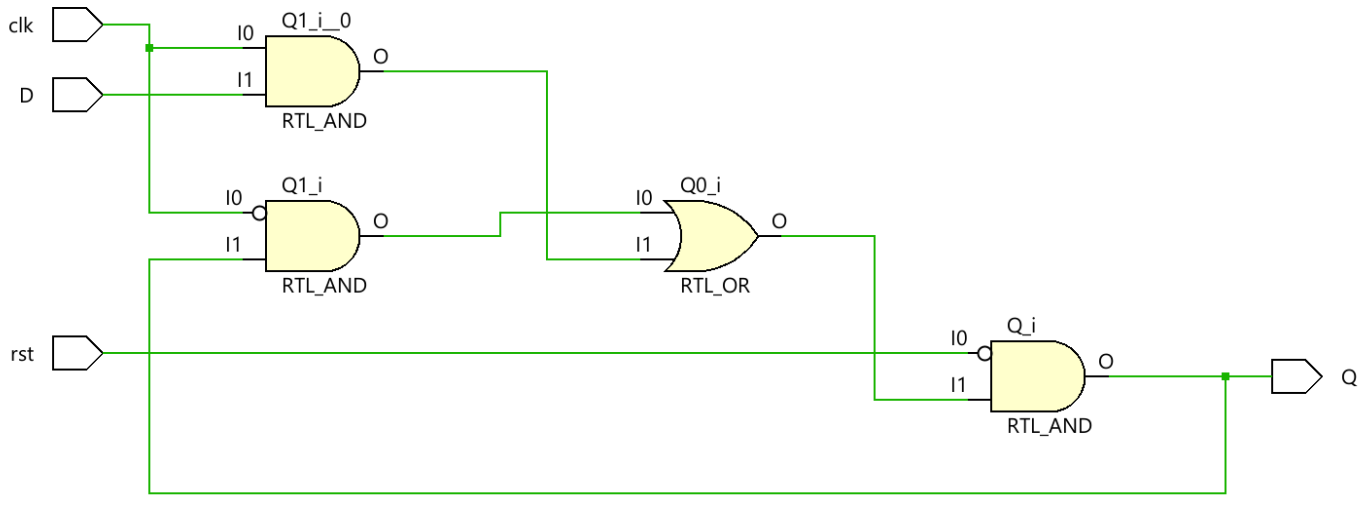
“D Latch” :-

“Design Code”:-

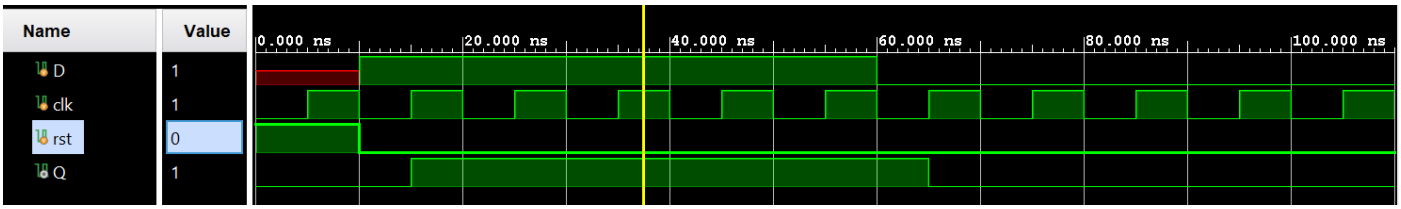



```
`timescale 1ns/1ps
module D_Latch (
  input clk,rst,
  input D,
  output Q
);
assign Q=(~rst)&(((~clk)&Q) |( clk & D ));
endmodule
```

“Schematics”:-



“Waveforms”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.275 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	59.5°C (31.4 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power