DAY-32

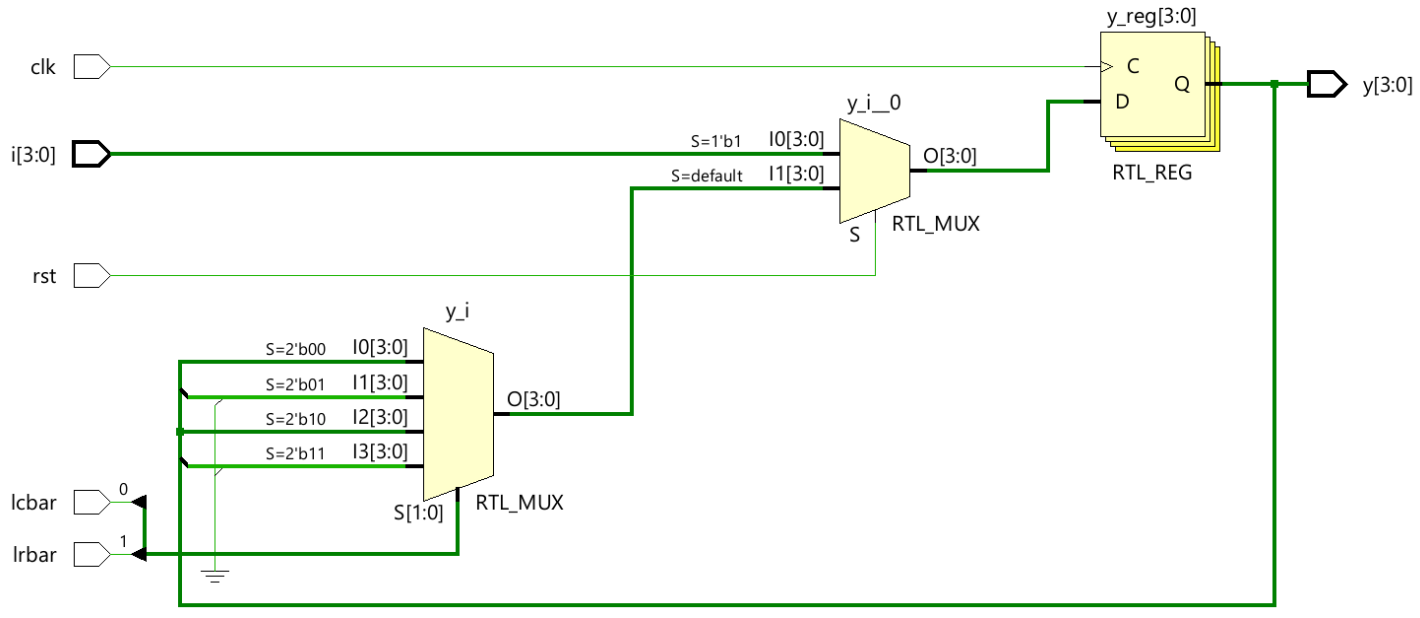
#100DAYSRTL

"Aim":-To Design Universal Shift register which performs linear circular left and right shift operations

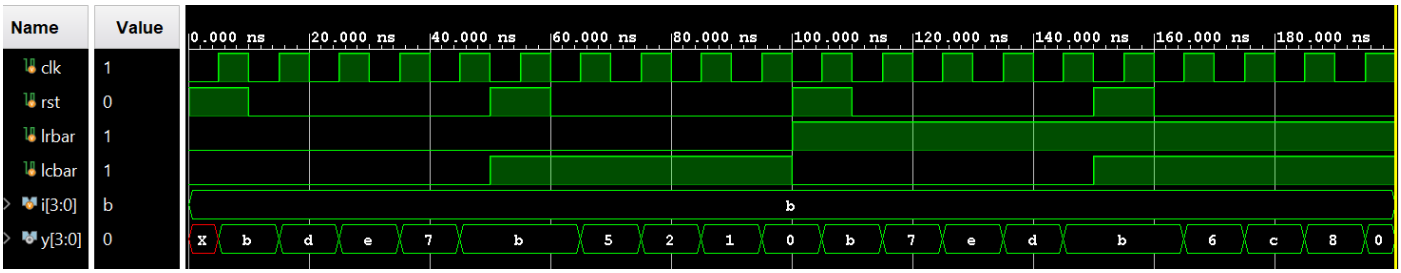
"Design Code":-

```
module usr_shift_reg_bl(input clk,rst,lrbar,lcbar,input [3:0]i,output reg [3:0]y);
always @ (posedge clk)begin
if(rst) y<=i;
else
begin
case({lrbar,lcbar})
2'b00:begin y<={y[0],y[3:1]};  end
2'b01: begin y<={1'b0,y[3:1]}; end
2'b10: begin y<={y[2:0],y[3]}; end
2'b11: begin y<={y[2:0],1'b0}; end
default: begin end
endcase
end
end
endmodule
```

"Schematics":-



“Waveforms”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.003 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.8°C**
Thermal Margin:	56.2°C (29.7 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity