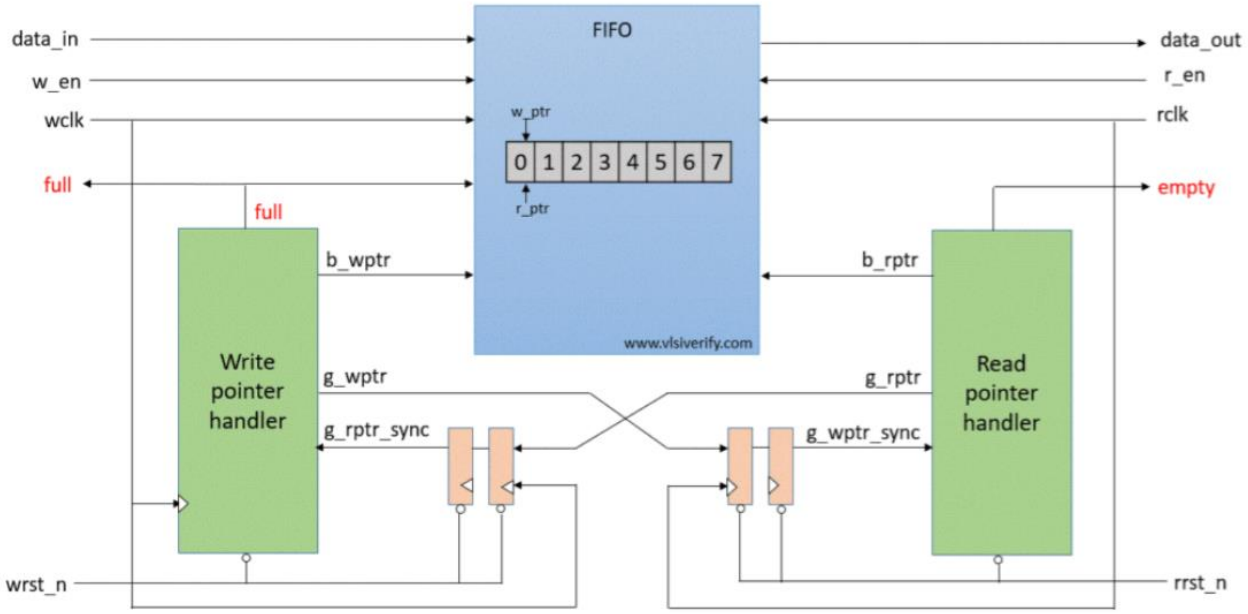
DAY-45

#100DAYSRTL

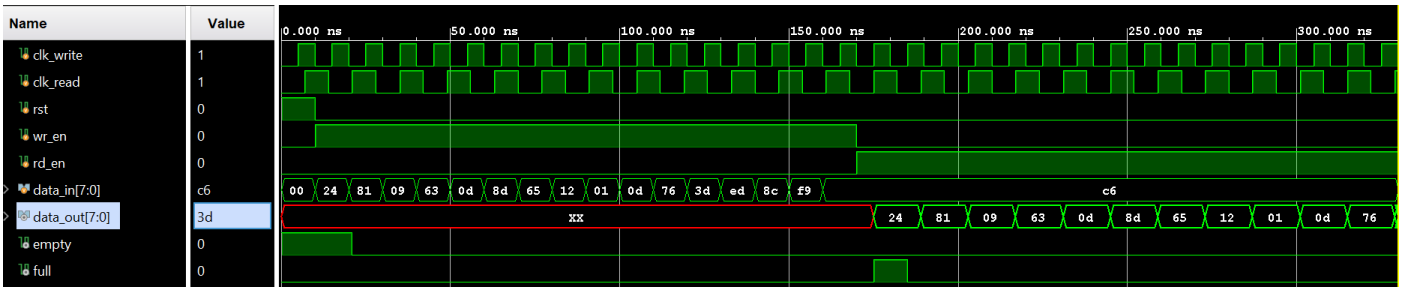
“Aim”:-To design a 16 bit depth Asynchronous FIFO

“Design Code”:-

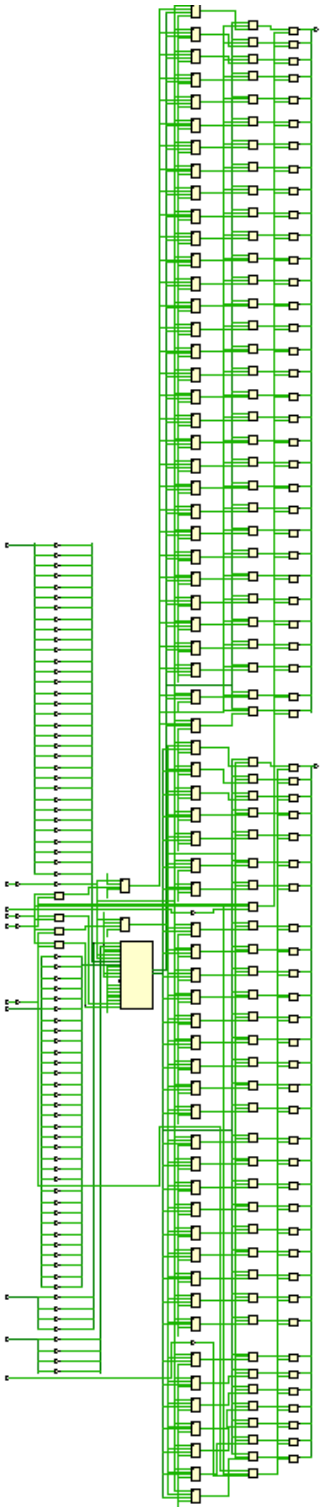



```
module async_fifo ( input clk_write,clk_read,rst,wr_en,rd_en,input [7:0] data_in,output reg [7:0] data_out,output reg empty,output reg full );
  parameter DEPTH = 16; // Depth of the FIFO
  reg [7:0] memory [0:DEPTH-1];reg [4:0] wr_ptr = 0; // Write pointer
  reg [4:0] rd_ptr = 0; // Read pointer
  reg [4:0] count = 0;  // Number of elements in the FIFO
  // Write process (synchronized to write clock)
  always @(posedge clk_write or posedge rst) begin
    if (rst) begin
      wr_ptr <= 0;
      count <= 0;
    end else if (wr_en && !full) begin
      memory[wr_ptr] <= data_in;
      wr_ptr <= (wr_ptr == DEPTH-1) ? 0 : wr_ptr + 1;
      count <= count + 1;
    end
  end
  // Read process (synchronized to read clock)
  always @(posedge clk_read or posedge rst) begin
    if (rst) begin
      rd_ptr <= 0;
      count <= 0;
    end else if (rd_en && !empty) begin
      data_out <= memory[rd_ptr];
      rd_ptr <= (rd_ptr == DEPTH-1) ? 0 : rd_ptr + 1;
      count <= count - 1;
    end
  end
  // Flags to indicate empty and full conditions
  assign  empty = (count == 0);
  assign  full = (count == DEPTH);
endmodule
```

“Waveforms”:-



“Implemented Design”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**4.795 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**34.0°C**
Thermal Margin:	51.0°C (26.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity