DAY-12

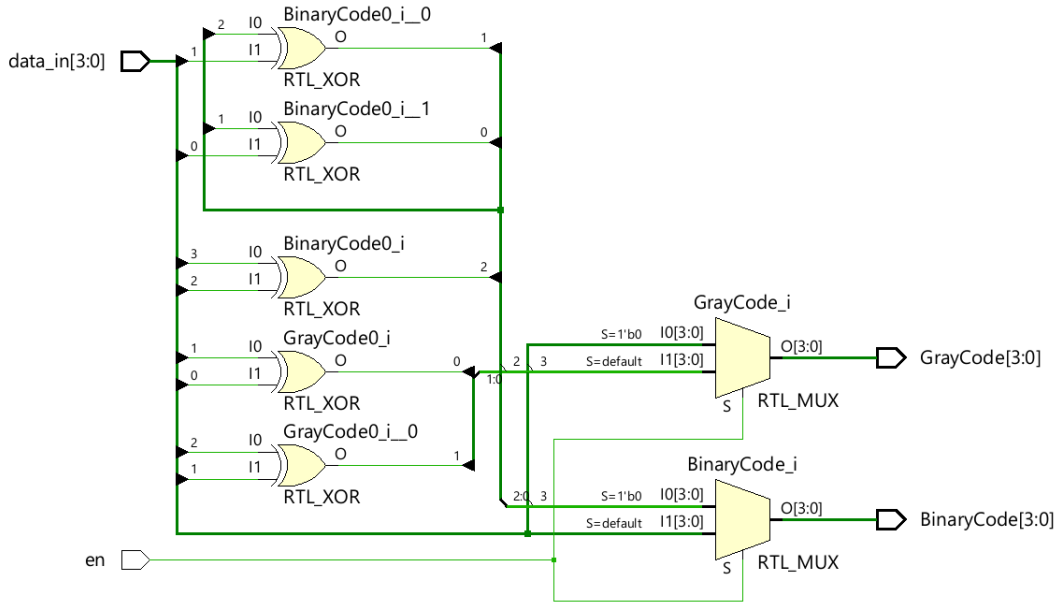
#100DAYSRTL

"Aim":- To Design the 4bit Gray to Binary converter and Binary to Gray converter Verilog

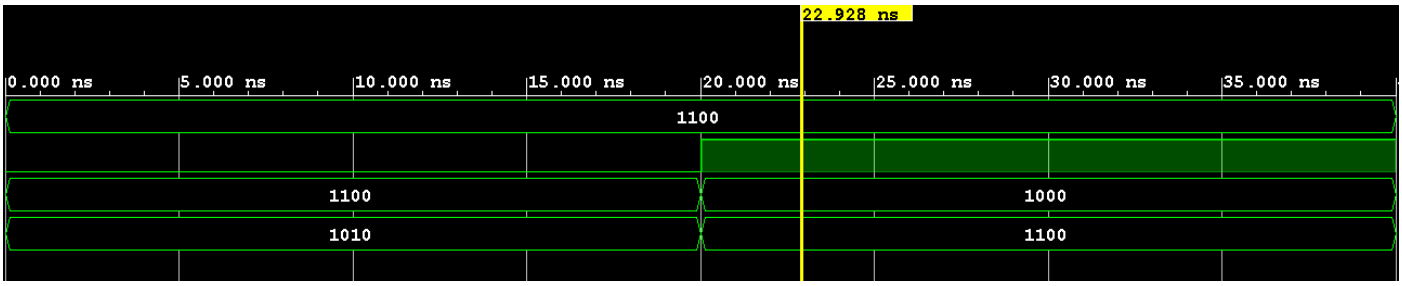
"Verilog Code":-

```
module B_G(
input [3:0] data_in,
input en,
output reg [3:0] BinaryCode,GrayCode
);
always @(*) begin
if(en)begin //Gray to Binary Converter
 BinaryCode[3]=data_in[3];
 BinaryCode[2]=BinaryCode[3]^data_in[2];
 BinaryCode[1]=BinaryCode[2]^data_in[1];
 BinaryCode[0]=BinaryCode[1]^data_in[0];
 GrayCode=data_in;
end
else begin //Binary to Gray converter
 GrayCode[3]=data_in[3];
 GrayCode[2]=data_in[3]^data_in[2];
 GrayCode[1]=data_in[2]^data_in[1];
 GrayCode[0]=data_in[1]^data_in[0];
 BinaryCode=data_in;
end
end
endmodule
```

"Schematics":-



“Waveforms”:-


22.928 ns
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
1100
1100
1000
1010
1100