DAY-40

#100DAYSRTL

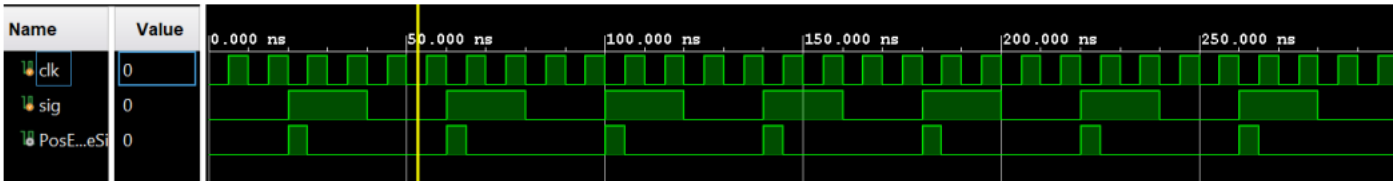
"Aim":-To design Positive Edge detector Circuit and Negative Edge detector Circuit

"Positive Edge detector Circuit"

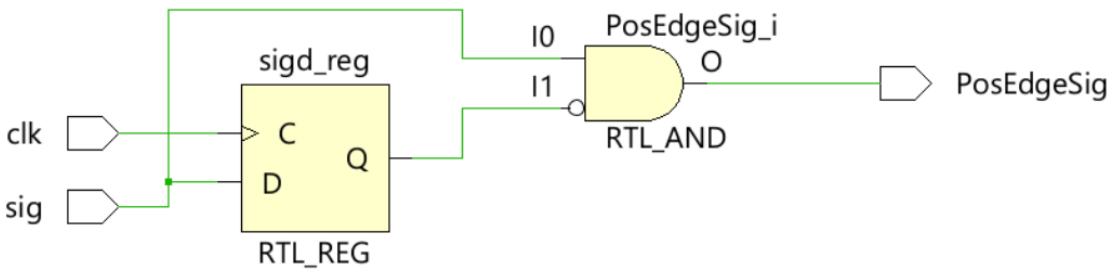
"Design Code":-

```
module PositiveEdgeDetector(
input clk,
input sig,//Sample signal which we want to detect the posedge
output PosEdgeSig
);
reg sigd;
always @(posedge clk) begin  // To delay the signal
sigd<=sig;
end
assign PosEdgeSig=(sig && ~sigd);
endmodule
```

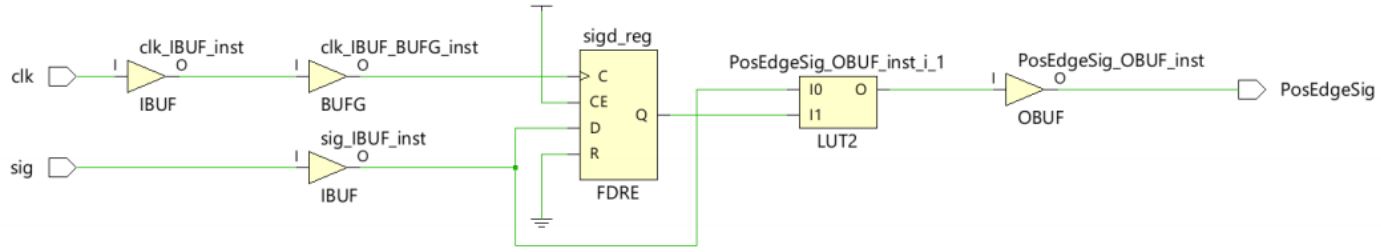
"Waveforms":-



"Elaborated Design":-



“Implemented Design”:-

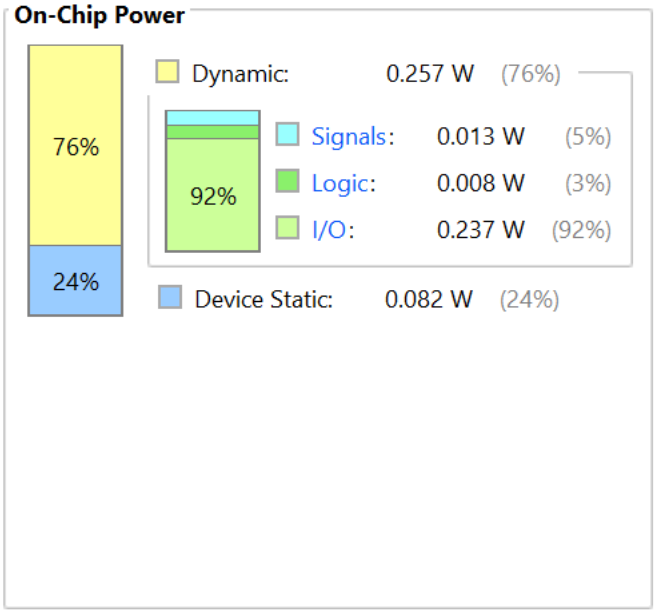


Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.339 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.6°C**
Thermal Margin:	59.4°C (31.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

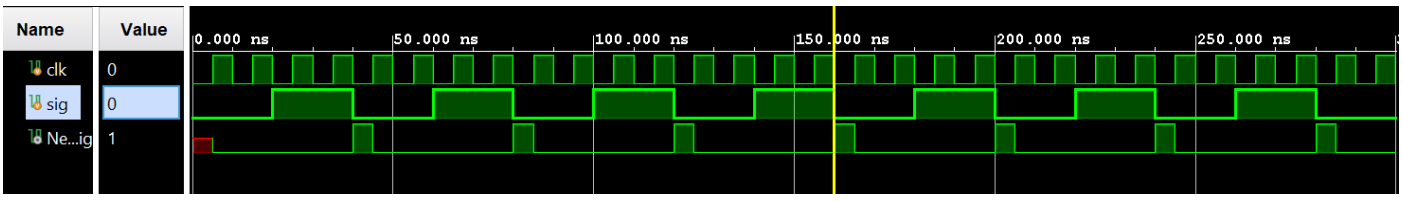


“Negative Edge detector Circuit”

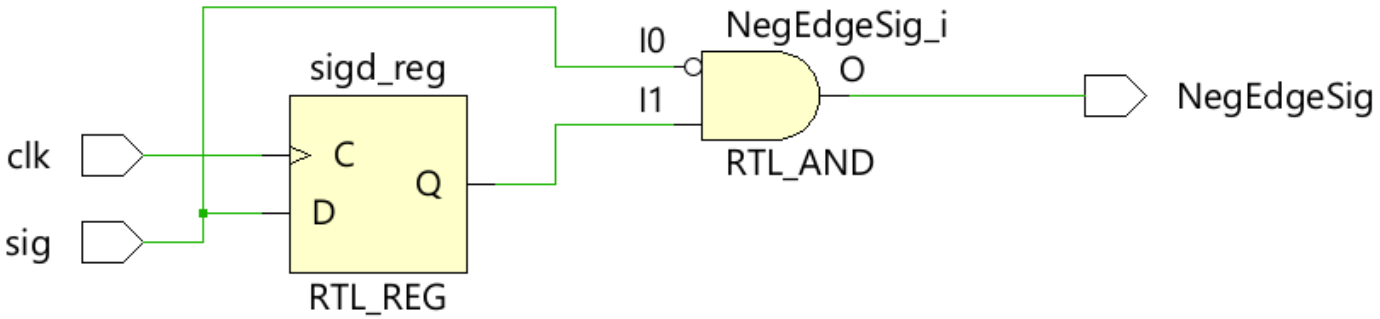
“Design Code”:-

```
module NegativeEdgeDetector(
input clk,
input sig,//Sample signal which we want to detect the negativeedge
output NegEdgeSig
);
reg sigd;
always @(posedge clk) begin  // To delay the signal
sigd<=sig;
end
assign NegEdgeSig=(~sig && sigd);
endmodule
```

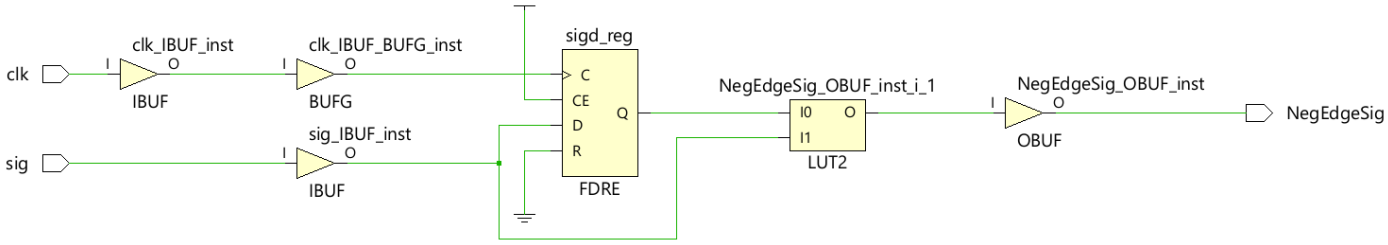
“Waveforms”:-



“Elaborated Design”:-



“Implemented Design”:-



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Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power