



DAY-6

#100DAYSRTL

“Aim”:- To Verify the 4-bit ripple carry adder using System Verilog Layered Testbenches

“System Verilog Testbenches”:-

Design:-

```
1 module FA(  
2     input a,b,cin,  
3     output c,s  
4 );  
5     assign {C,S}=a+b+cin;  
6 endmodule  
7 module RCA(  
8     input [3:0] A,B,  
9     input Cin,  
10    output [4:0] result  
11 );  
12     wire carry;  
13     wire [3:0] sum;  
14     wire carry1,carry2,carry3,carry4;  
15     FA FA1(A[0],B[0],Cin,carry1,sum[0]);  
16     FA FA2(A[1],B[1],carry1,carry2,sum[1]);  
17     FA FA3(A[2],B[2],carry2,carry3,sum[2]);  
18     FA FA4(A[3],B[3],carry3,carry4,sum[3]);  
19  
20     assign result={carry,sum};  
21 endmodule
```

Interface:-

```
interface RC_IF vif;  
    logic [3:0] A,B;  
    logic Cin;  
    logic [4:0] Result;  
endinterface
```

Transaction:-

```
class transaction;  
    rand bit [3:0] A;  
    rand bit [3:0] B;  
    rand bit Cin;  
    bit [4:0] result;  
  
    function new();  
        A = $random;  
        B = $random;  
        Cin = $random;  
    endfunction  
  
    function void display();  
        $display("Transaction: A=%h, B=%h, Cin=%b, Result=%h", A, B, Cin, result);  
    endfunction  
endclass
```

Generator:-

```
class generator;
mailbox #(transaction) mbx;
event done;

function new(mailbox #(transaction) mbx);
    this.mbx = mbx;
endfunction

task run(int count);
    repeat (count) begin
        transaction tr = new();
        tr.result = tr.A + tr.B + tr.Cin;
        mbx.put(tr);
        tr.display();
    end
    ->done;
endtask
endclass
```

Driver:-

```
class driver;
mailbox #(transaction) mbx;
virtual RCA_IF vif;

function new(mailbox #(transaction) mbx);
    this.mbx = mbx;
endfunction

task run();
    transaction tr;
    forever begin
        mbx.get(tr);
        vif.A = tr.A;
        vif.B = tr.B;
        vif.Cin = tr.Cin;
        #1;
        tr.result = vif.result;
        tr.display();
    end
endtask
endclass
```

Monitor:-

```
1 class monitor;
2     transaction tr;
3     mailbox (transaction) mbx;
4     virtual RC_Vif vif;
5     function new(mailbox (transaction) mbx);
6         this.mbx=mbx;
7     endfunction
8     task run();
9         tr=new();
10        forever begin
11            tr.Result<=vif.Result;
12            mbx.put(tr);
13            tr.display("Mon");
14        end
15    endtask
16 endclass
```

Scoreboard:-

```
class scoreboard;
mailbox #(transaction) mbx;
mailbox #(transaction) mbxref;
event sconext;

function new(mailbox #(transaction) mbx, mailbox #(transaction) mbxref);
    this.mbx = mbx;
    this.mbxref = mbxref;
endfunction

task run();
    forever begin
        transaction tr;
        transaction trref;
        mbx.get(tr);
        mbxref.get(trref);
        tr.display();
        trref.display();
        if (tr.result == trref.result)
            $display("[SCO] : DATA MATCHED");
        else
            $display("[SCO] : DATA MISMATCHED");
        ->sconext;
    end
endtask
endclass
```

Environment:-

```
1 class environment;
2   generator gen;
3   scoreboard sco;
4   monitor mon;
5   driver drv;
6   event next;
7   mailbox #(transaction) gdmbx; ///gen - drv
8   mailbox #(transaction) msmbx; /// mon - sco
9   mailbox #(transaction) mbxref; ///// gen -> sco
10  virtual clk_Div_if vif;
11  function new(virtual clk_Div_if vif);
12    gdmbx=new();
13    msmbx=new();
14    mbxref=new();
15    gen=new(gdmbx,mbxref);
16    sco=new(msmbx,mbxref);
17    this.vif=vif;
18    drv.vif=this.vif;
19    mon.vif=this.vif;
20    gen.sconext=next;
21    sco.sconext=next;
22  endfunction
23  task pre_test();
24    drv.reset();
25  endtask
26  task test();
27  fork
28    gen.run();
29    drv.run();
30    mon.run();
31    sco.run();
32  join_any
33  endtask
34  task post_test();
35    wait(gen.done.triggered);
36    $finish();
37  endtask
38  task run();
39    pre_test();
40    test();
41    post_test();
42  endtask
43 endclass
```

TopModule:-

```
module tb;
  RCA_IF vif();
  RCA dut (vif);
  environment env;
  initial begin
    env = new(vif);
    env.gen.count = 30;
    env.run();
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
endmodule
```