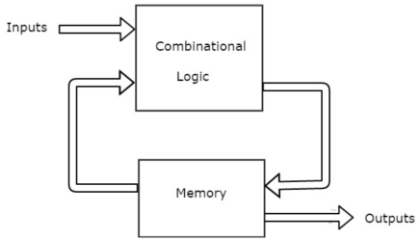
DAY-47

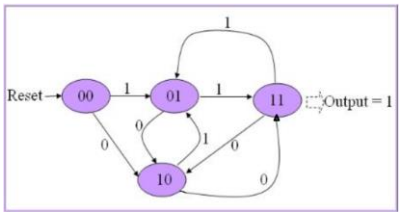
#100DAYSRTL

"Aim":- To design a Moore FSM sequence detector to detect the sequence 11 or 00 (Non Overlapping)

"Theory":-



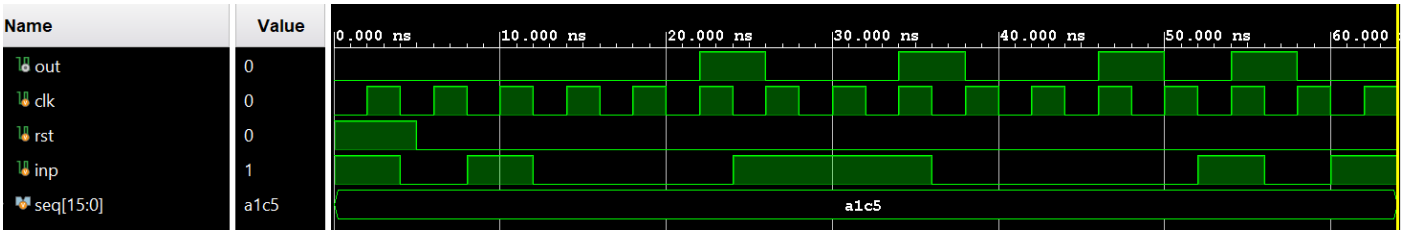
- Moore FSM depends on the present state only



"Design Code":-

```
module moore(clk, rst, inp, out);
  output out;
  input clk, rst, inp;
  reg out;
  reg [1:0] state;
  always @(posedge clk, posedge rst) begin
    if (rst) begin state <= 2'b00 ; out <= 0; end
    else begin
      case(state)
        2'b00: begin if (inp) state <= 2'b01;
                     else state <= 2'b10;
               end
        2'b01: begin if (inp) state <= 2'b11;
                     else state <= 2'b10;
               end
        2'b10: begin if (inp) state <= 2'b01;
                     else state <= 2'b11;
               end
        2'b11: begin if (inp) state <= 2'b01;
               else state <= 2'b10;
               end
        default:state <= 2'b00;
      endcase
    end
  end
  always @(posedge clk) begin
    if (state == 2'b11)  out <= 1;
    else out <= 0;
  end
endmodule
```

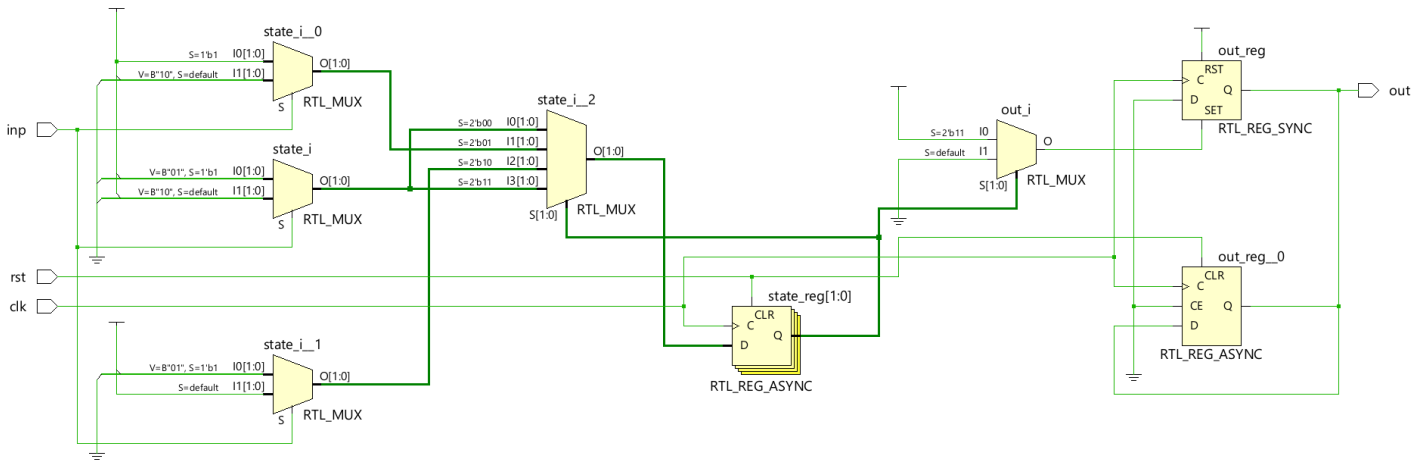
“Waveforms”:-



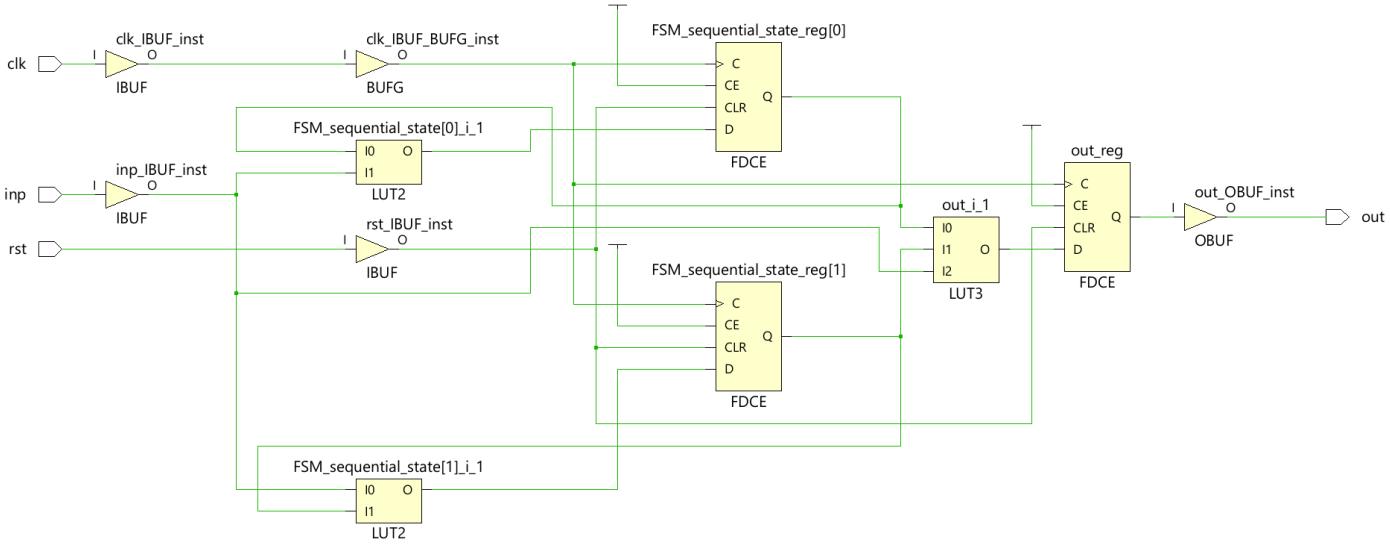
“Console”:-

```
state = 0| input = 1| output = 0
state = 2| input = 0| output = 0
state = 1| input = 1| output = 0
state = 2| input = 0| output = 0
state = 3| input = 0| output = 0
state = 2| input = 0| output = 1
state = 1| input = 1| output = 0
state = 3| input = 1| output = 0
state = 1| input = 1| output = 1
state = 2| input = 0| output = 0
state = 3| input = 0| output = 0
state = 2| input = 0| output = 1
state = 3| input = 0| output = 0
state = 1| input = 1| output = 1
state = 2| input = 0| output = 0
state = 1| input = 1| output = 0
```

“Elaborated design”:-



“Implemented design”:-



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.859 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.6°C**
Thermal Margin:	58.4°C (30.8 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power