DAY-41

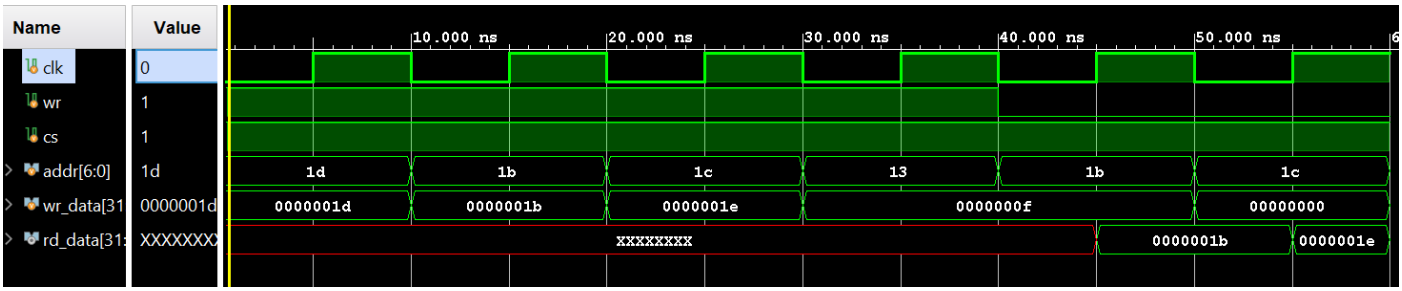
#100DAYSRTL

“Aim”:-To design a Memory of Size 1 MB 32 bit .

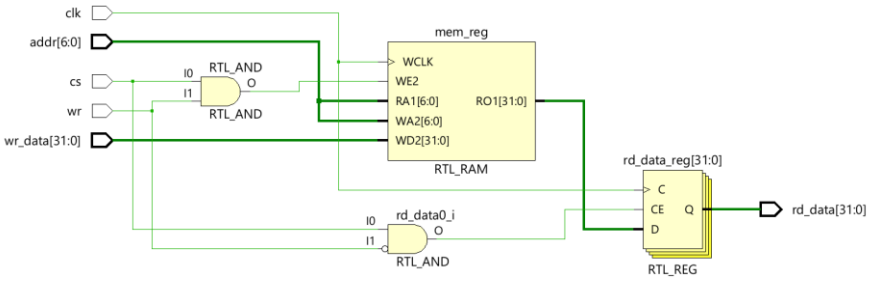
“Design Code”:-

```
module mem_1MB_32bit(
input clk,wr,cs,
input [6:0] addr,
input [31:0] wr_data,
output reg [31:0] rd_data);
reg [31:0] mem[0:127];
always @(posedge clk) begin
if(cs&wr)
mem[addr]<=wr_data;
end
always @(posedge clk)
begin
if(cs&(~wr))
rd_data<=mem[addr];
end
endmodule
```

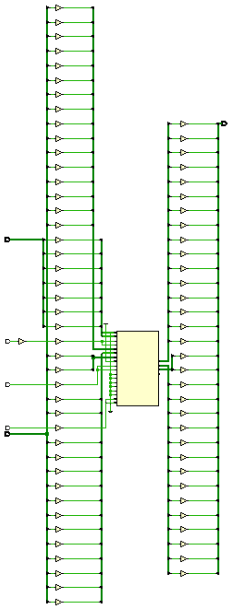
“Waveforms”:-



“Elaborated Design”:-



“Implemented Design”:-



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**8.381 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**40.8°C**
Thermal Margin:	44.2°C (23.3 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity