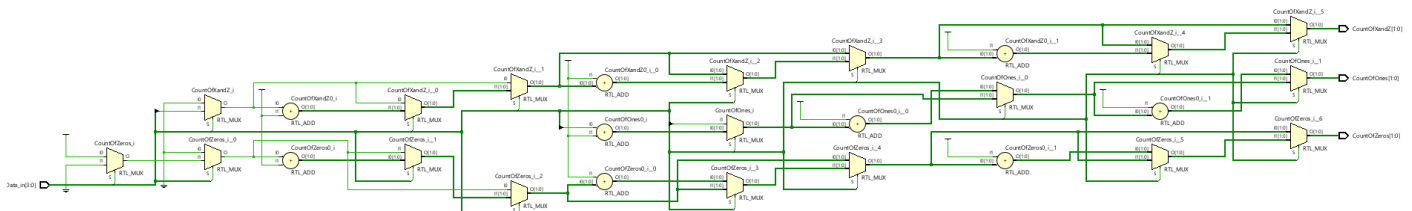# DAY-19

#100DAYSRTL

"Aim":- To Design the Binary Digit Counter Which Counts the occurrence of ones and zeros.

"Design Code":-

```verilog
module BinaryDigitCounter(
  input [3:0] Data_in,
  output reg [1:0] CountOfOnes,
  output reg [1:0] CountOfZeros,
  output reg [1:0] CountOfXandZ
);
  always @(*) begin
    CountOfOnes = 0;
    CountOfZeros = 0;
    CountOfXandZ=0;
    for (int i = 0; i < 4; i = i + 1) begin
      if (Data_in[i]) // To count the occurence of ones
        CountOfOnes = CountOfOnes + 1;
      else if (~Data_in[i])  // To count the occurence of Zeros
        CountOfZeros = CountOfZeros + 1;
      else if (Data_in[i]==1'bX) // To count the occurence of Unknowns
        CountOfXandZ=CountOfXandZ+1;
    end
  end
endmodule
```

"Schematics":-

"Waveforms":-

Name	Value	0.000 ns	20.000 ns	40.000 ns	60.000 ns	80.000 ns	100.000 ns	120.000 ns
Data_in[3:0]	XXXX	0100	0001	1001	0011	1101	0101	0010	0001	1101	1X20	XZXX	2X20	XXXX
CountOfOnes[1:0]	0	1	2	3	2	1	3	1	0			
CountOfZeros[1:0]	0	3	2	1	2	3	1	0	1	0		
CountOfXandZ[1:0]	0	0						2	0	3	0	