

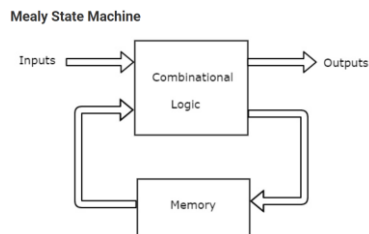


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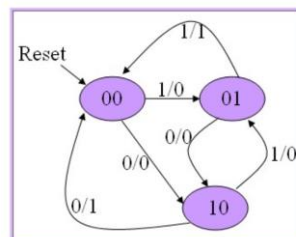
#100DAYSRTL

“Aim”:- To design a Mealy FSM sequence detector to detect the sequence 11 or 00 (Non Overlapping)

“Theory”:-



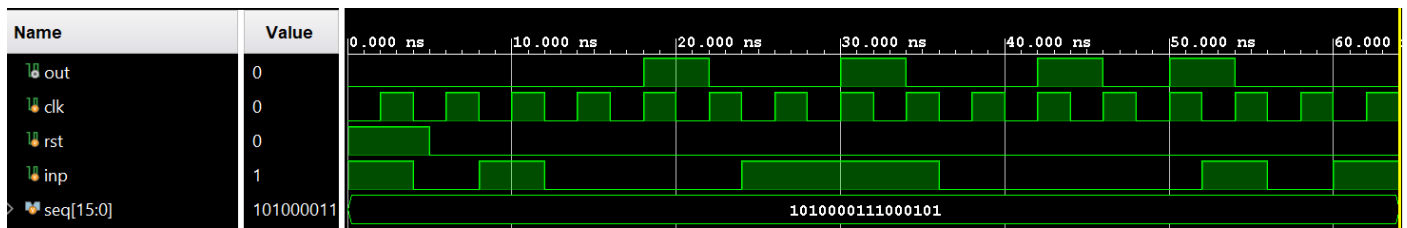
- Mealy machine depends on present state and present input



“Design Code”:-

```
module mealy(clk,rst,inp,out);
input clk, rst, inp;
output reg out;
reg [1:0] state;
always @(posedge clk, posedge rst) begin
if(rst) begin
out <= 0;
state <= 2'b00;
end
else begin
case (state)
2'b00:begin if (inp) begin state <=2'b01;out <=0; end
else begin state <=2'b10;out <=0; end
end
2'b01:begin if(inp) begin state <= 2'b00;out <= 1; end
else begin state <= 2'b10;out <= 0; end
end
2'b10:begin if(inp) begin state <= 2'b01;out <= 0; end
else begin state <= 2'b00;out <= 1; end
end
default:begin state <= 2'b00; out <= 0; end
endcase
end
end
endmodule
```

“Waveforms”:-



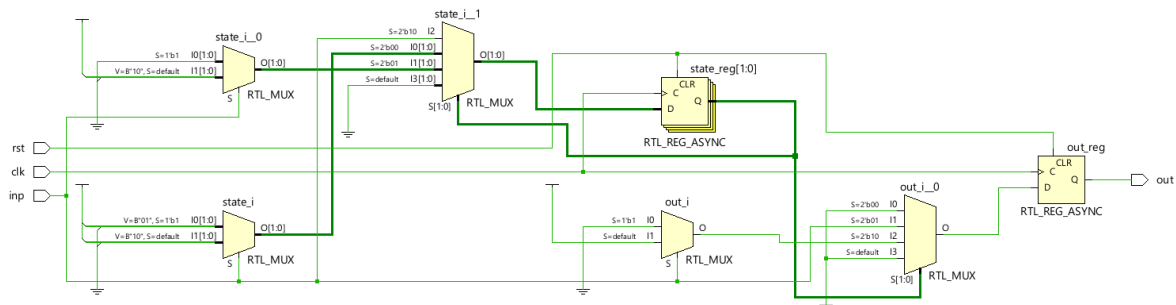
“Console”:-

```

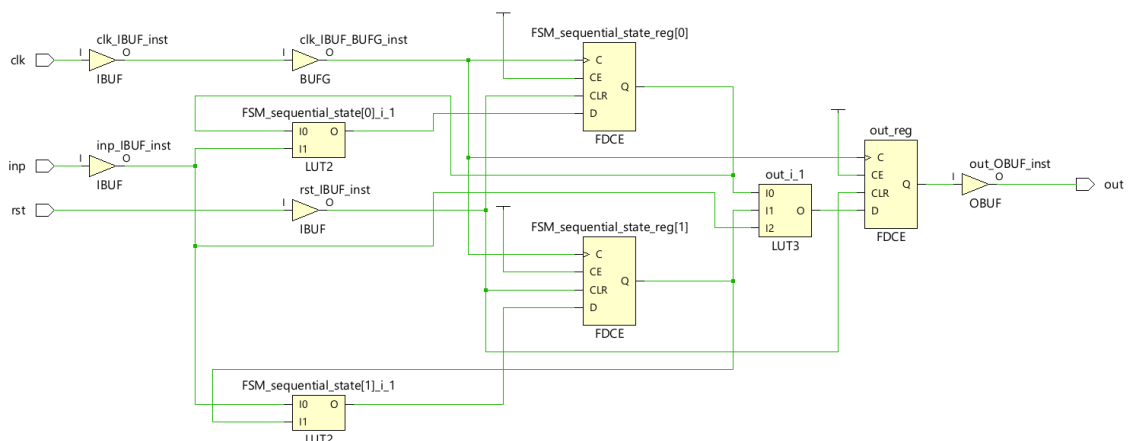
state = 0 | input = 1 | output = 0
state = 2 | input = 0 | output = 0
state = 1 | input = 1 | output = 0
state = 2 | input = 0 | output = 0
state = 0 | input = 0 | output = 1
state = 2 | input = 0 | output = 0
state = 1 | input = 1 | output = 0
state = 0 | input = 1 | output = 1
state = 1 | input = 1 | output = 0
state = 2 | input = 0 | output = 0
state = 0 | input = 0 | output = 1
state = 2 | input = 0 | output = 0
state = 0 | input = 0 | output = 1
state = 1 | input = 1 | output = 0
state = 2 | input = 0 | output = 0
state = 1 | input = 1 | output = 0

```

“Elaborated Design”:-



“Implemented Design”:-



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.859 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.6°C
Thermal Margin:	58.4°C (30.8 W)
Effective θ JA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

