



DAY-18

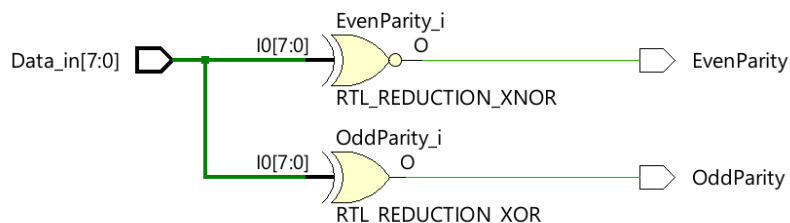
#100DAYSRTL

“Aim”:- To Design the Parity Checker

“Verilog Code”:-

```
module ParityChecker(  
input [7:0]Data_in,  
output EvenParity,OddParity  
);  
assign OddParity=^(Data_in);  
assign EvenParity=~^(Data_in);  
endmodule
```

“Schematics”:-



“Waveforms”:-

0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns	60.000 ns	70.000 ns	80.000 ns	90.000 ns
00100100	10000001	00001001	01100011	00001101	10001101	01100101	00010010	00000001	00001101

“Console Results”:-

```
Data_in=00100100,EvenParity=1,OddParity=0  
Data_in=10000001,EvenParity=1,OddParity=0  
Data_in=00001001,EvenParity=1,OddParity=0  
Data_in=01100011,EvenParity=1,OddParity=0  
Data_in=00001101,EvenParity=0,OddParity=1  
Data_in=10001101,EvenParity=1,OddParity=0  
Data_in=01100101,EvenParity=1,OddParity=0  
Data_in=00010010,EvenParity=1,OddParity=0  
Data_in=00000001,EvenParity=0,OddParity=1  
Data_in=00001101,EvenParity=0,OddParity=1
```