DAY-21

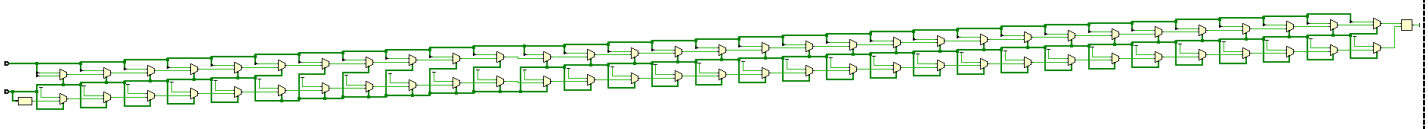
#100DAYSRTL

“Aim”:-To Design a MUX that acts as an Asynchronous PISO

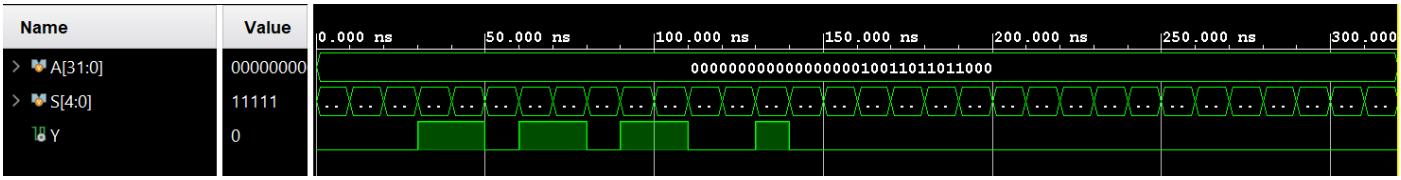
“Design Code”:-

```
module Mux #(parameter N = 32, M = 5) ( //M=log2(M)
    input [N-1:0] A, //Parallel Data  as input
    input [M-1:0] S,
    output reg Y // Serial Data as output
);
always @(*) begin
for(int i=0;i<N;i++) begin
case (S)
i:Y=A[i];
endcase
end
end
endmodule
```

“Schematics”:-



“Waveforms”:-



“Console”:-

```
A=00000000000000000010011011011000,S=00000,Y=0
A=00000000000000000010011011011000,S=00001,Y=0
A=00000000000000000010011011011000,S=00010,Y=0
A=00000000000000000010011011011000,S=00011,Y=1
A=00000000000000000010011011011000,S=00100,Y=1
A=00000000000000000010011011011000,S=00101,Y=0
A=00000000000000000010011011011000,S=00110,Y=1
A=00000000000000000010011011011000,S=00111,Y=1
A=00000000000000000010011011011000,S=01000,Y=0
A=00000000000000000010011011011000,S=01001,Y=1
A=00000000000000000010011011011000,S=01010,Y=1
A=00000000000000000010011011011000,S=01011,Y=0
A=00000000000000000010011011011000,S=01100,Y=0
A=00000000000000000010011011011000,S=01101,Y=1
A=00000000000000000010011011011000,S=01110,Y=0
A=00000000000000000010011011011000,S=01111,Y=0
A=00000000000000000010011011011000,S=10000,Y=0
A=00000000000000000010011011011000,S=10001,Y=0
A=00000000000000000010011011011000,S=10010,Y=0
A=00000000000000000010011011011000,S=10011,Y=0
A=00000000000000000010011011011000,S=10100,Y=0
A=00000000000000000010011011011000,S=10101,Y=0
A=00000000000000000010011011011000,S=10110,Y=0
A=00000000000000000010011011011000,S=10111,Y=0
A=00000000000000000010011011011000,S=11000,Y=0
A=00000000000000000010011011011000,S=11001,Y=0
A=00000000000000000010011011011000,S=11010,Y=0
A=00000000000000000010011011011000,S=11011,Y=0
A=00000000000000000010011011011000,S=11100,Y=0
A=00000000000000000010011011011000,S=11101,Y=0
A=00000000000000000010011011011000,S=11110,Y=0
A=00000000000000000010011011011000,S=11111,Y=0
Completed
```

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.441 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.8°C**
Thermal Margin:	59.2°C (31.2 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity