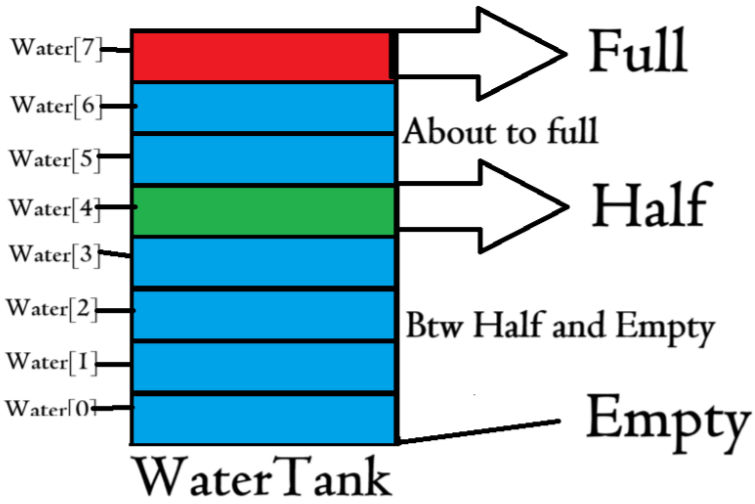
# DAY-17

# #100DAYSRTL

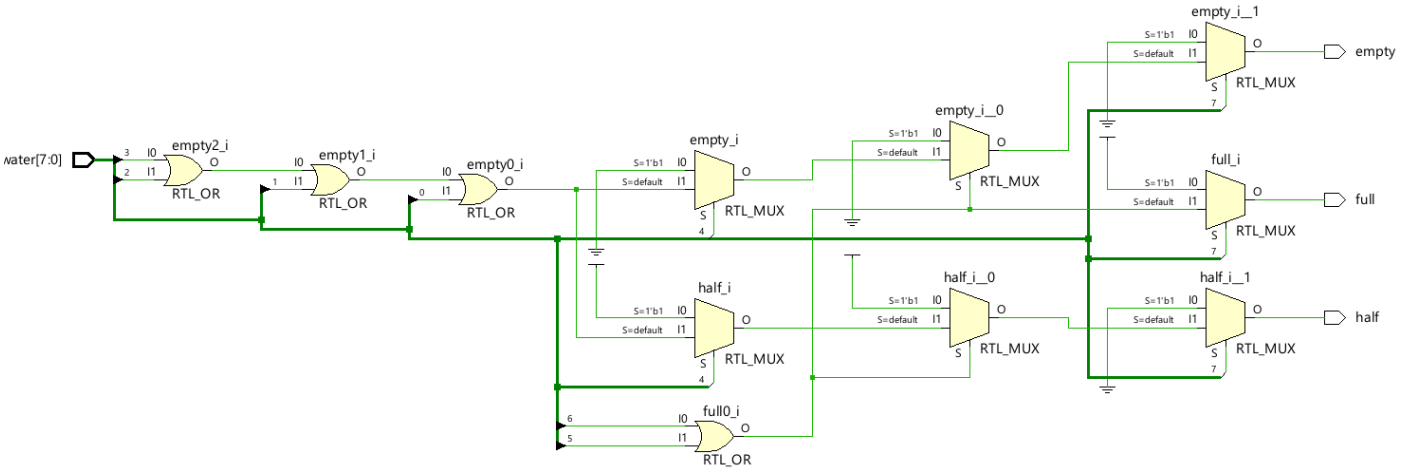
**"Aim":-** To Design the water level indicator using 8X3 encoder

## "Verilog Code":-

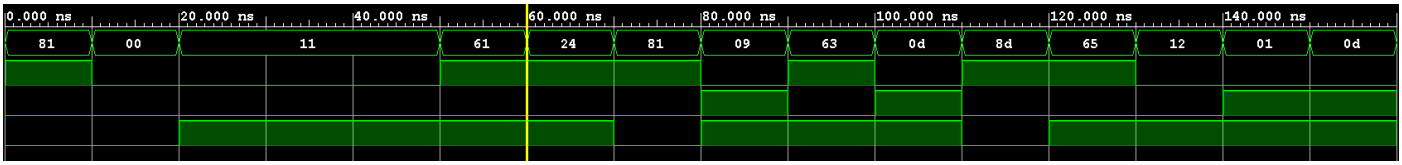



```
module TankLevelIndicator(input [7:0] water,
output reg full,empty,half);
always @(*) begin
if(water[7]) begin  // Tank level is Full
full=1;empty=0;half=0;
end
else if (water[6]|water[5]) begin  // Tank level is about to full
full=1;empty=0;half=1;
end
else if (water[4]) begin  // Tank is half
full=0;empty=0;half=1;
end
else if (water[3]|water[2]|water[1]|water[0]) begin // Tank level is between Half or Empty
full=0;empty=1;half=1;
end
else begin //Tank level is empty
full=0;empty=0;half=0;
end
end
endmodule
```

# “Schematics”:-




# “Waveforms”:-




# “Console Results”:-

```
water=10000001,full=1,empty=0,half=0
water=00000000,full=0,empty=0,half=0
water=00010001,full=0,empty=0,half=1
water=01100001,full=1,empty=0,half=1
water=00100100,full=1,empty=0,half=1
water=10000001,full=1,empty=0,half=0
water=00001001,full=0,empty=1,half=1
water=01100011,full=1,empty=0,half=1
water=00001101,full=0,empty=1,half=1
water=10001101,full=1,empty=0,half=0
water=01100101,full=1,empty=0,half=1
water=00010010,full=0,empty=0,half=1
water=00000001,full=0,empty=1,half=1
water=00001101,full=0,empty=1,half=1
```