DAY-38

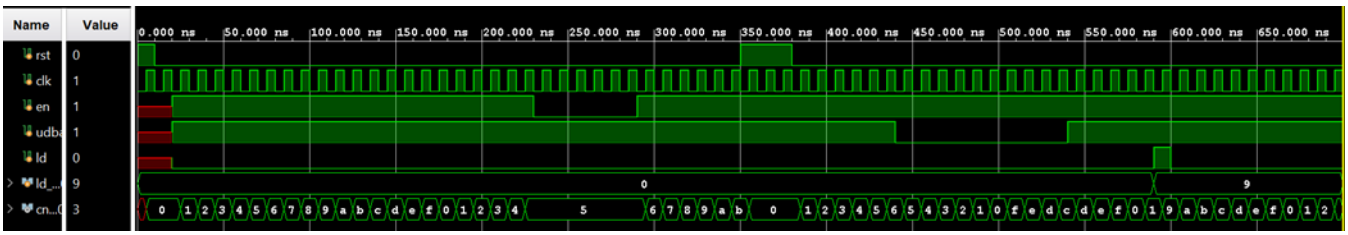
#100DAYSRTL

“Aim”:-To Design a Universal Counter (Down & Up)

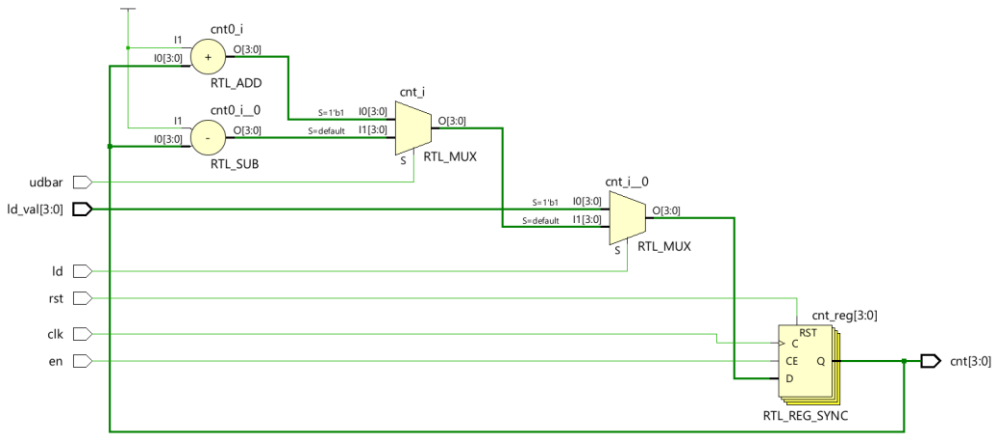
“Design Code”:-

```
module Counter(input rst,clk,en,udbar,ld,input [3:0] ld_val,output  reg [3:0]  cnt);
always @(posedge clk)
begin
if (rst) cnt<=0;
else
begin
if(en) begin
if (ld) cnt<=ld_val;
else begin
if (udbar) cnt<=cnt+1;
else cnt<=cnt-1;
end
end
end
end
endmodule
```

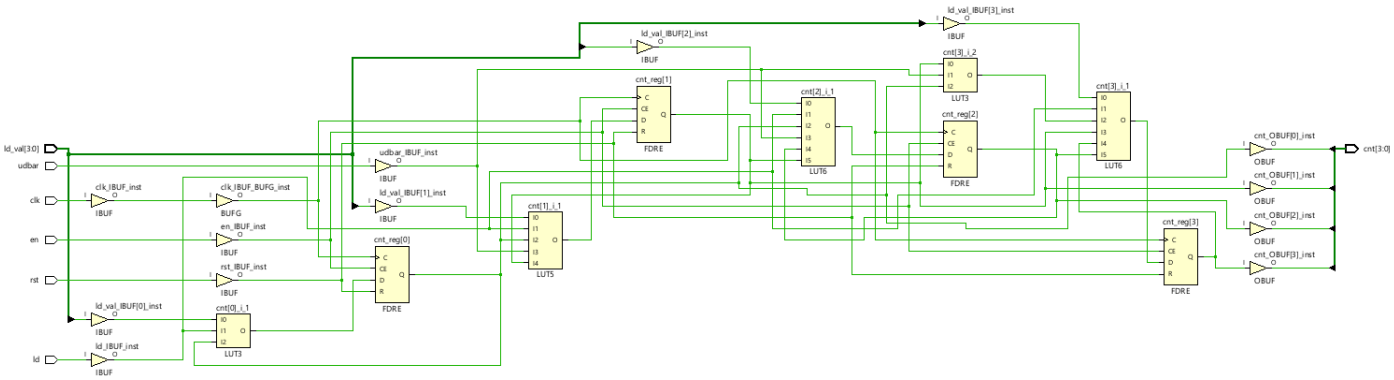
“Waveforms”:-



“Elaborated Design”:-



“Implemented Design”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.816 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.3°C**
Thermal Margin:	54.7°C (28.8 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power