DAY-36

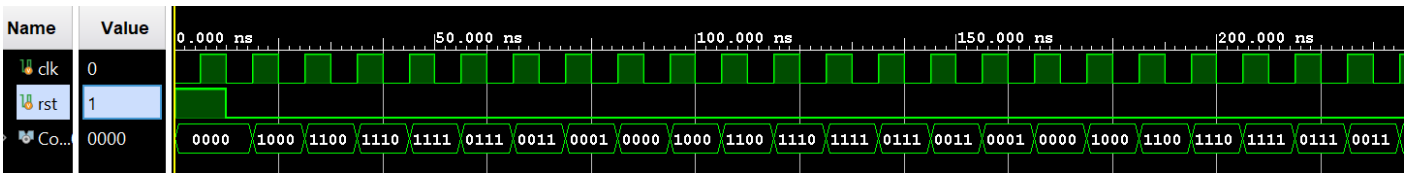
#100DAYSRTL

"Aim":-To Design JhonSonCounter (SwitchTailRing counter)

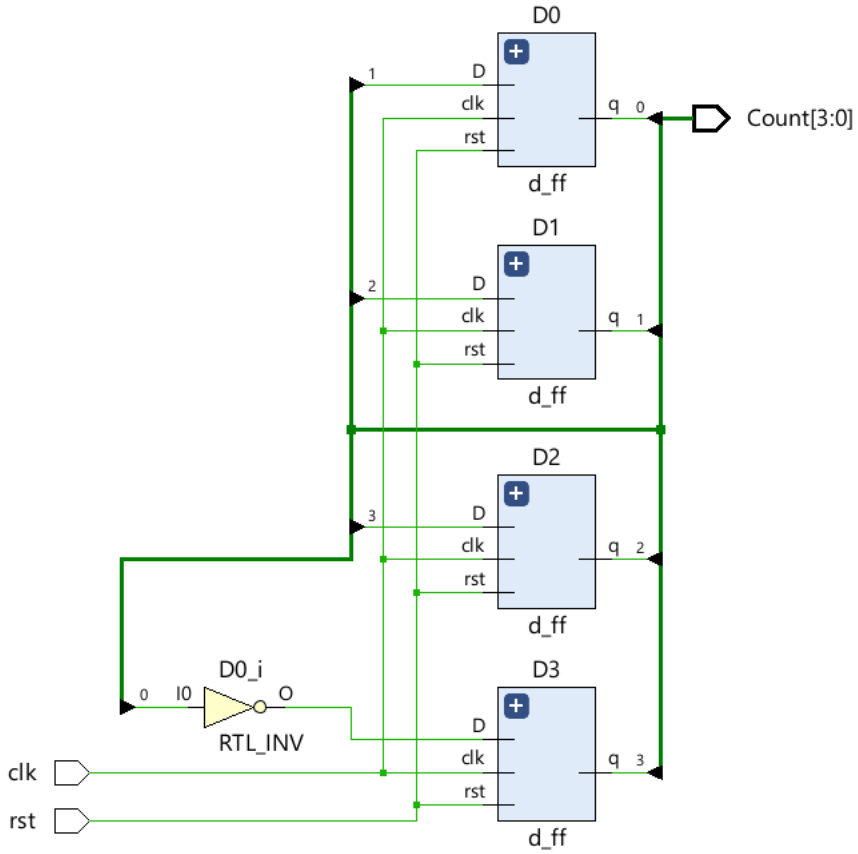
"Design Code":-

```
module JhonSoncounter(Count,clk,rst);
input clk,rst;
output [3:0] Count;
wire [3:0] temp ;
d_ff D3(temp[3],clk,~temp[0],rst);
d_ff D2(temp[2],clk,temp[3],rst);
d_ff D1(temp[1],clk,temp[2],rst);
d_ff D0(temp[0],clk,temp[1],rst);
assign Count=temp;
endmodule
module d_ff(q,clk,D,rst);
input clk,rst,D;
output reg q;
always @ (posedge clk or posedge rst) begin
if (rst) q<=0;
else q<=D ;
end
endmodule
```

"Waveforms":-



“Schematics”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.099 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power