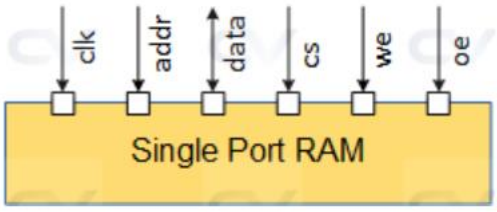
DAY-43

#100DAYSRTL

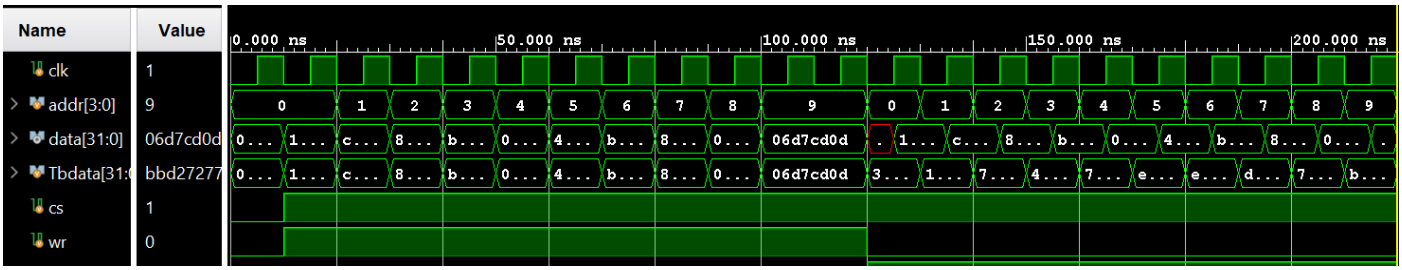
“Aim”:-To design a 32-bit Single Port RAM

“Design Code”:-

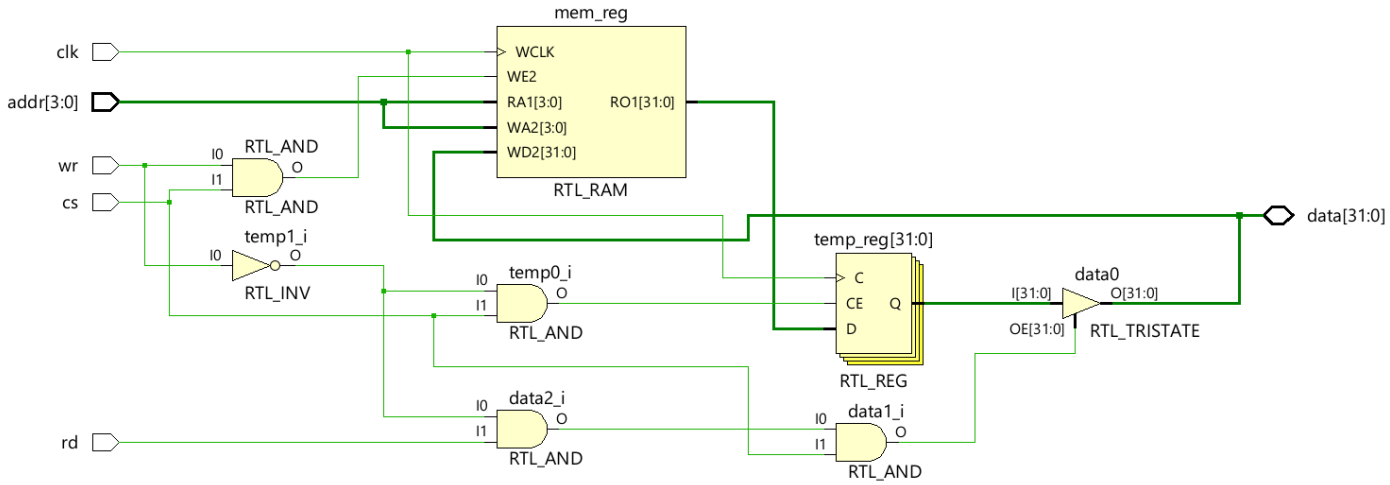



```
module SPRAM #(parameter AddrWidth=4,DataWidth=32,Depth=16)(clk,addr,data,cs,wr,rd);
input clk;
input [AddrWidth-1:0] addr;
inout [DataWidth-1:0] data;
input cs,wr,rd;
reg [DataWidth-1:0] temp;
reg [DataWidth-1:0] mem [Depth];
always @(posedge clk) begin
if(wr&&cs) mem[addr]<=data;
end
always @(posedge clk) begin
if(~wr&&cs) temp<= mem[addr];
end
assign data=((~wr)&&rd&&cs)?temp:'hz;
endmodule
```

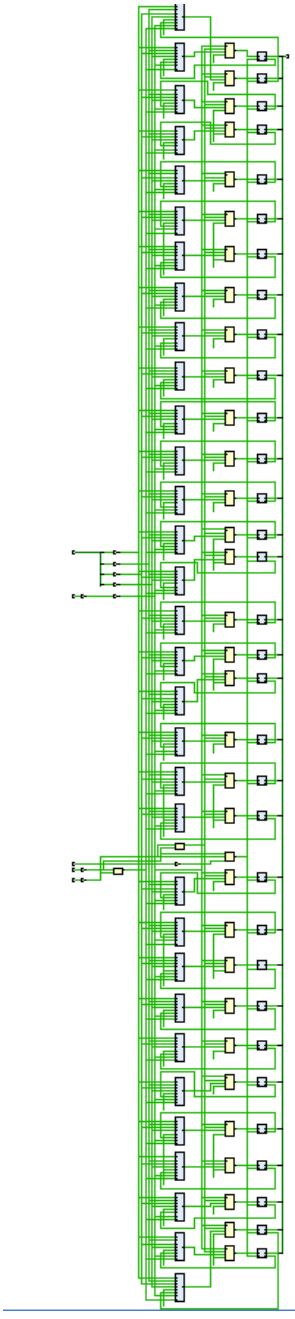
“Waveforms”:-



“Elaborated Design”:-



“Implemented Design”:-



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.277 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.4°C**
Thermal Margin:	57.6°C (30.4 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity