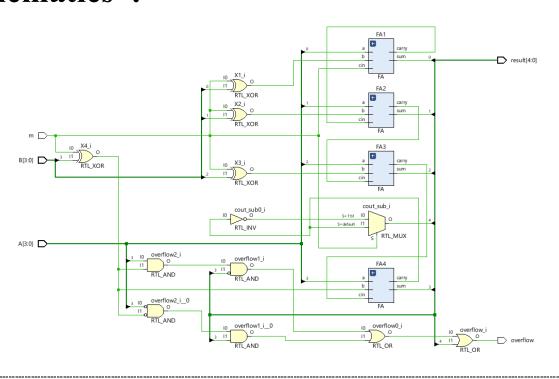


DAY-9 #100DAYSRTL

"Aim":- To Design the 4 bit Adder-Subtractor using Verilog "Verilog Code":-

```
module FA(input a, b, cin, output sum, carry);
 assign {carry, sum} = a + b + cin;
endmodule
module A S(
 input [3:0] A, B,
 input m,
 output [4:0] result,
 output overflow
wire [3:0] Y;
wire [3:0] C;
wire [3:0] S;
wire cout sub;
xor X1(Y[0],m,B[0]);
xor X2(Y[1],m,B[1]);
xor X3(Y[2].m.B[2]);
xor X4(Y[3],m,B[3]);
FA FA1(A[0], Y[0], m, S[0], C[0]);
FA FA2(A[1], Y[1], C[0], S[1], C[1]);
FA FA3(A[2], Y[2], C[1], S[2], C[2]);
FA FA4(A[3], Y[3], C[2], S[3], C[3]);
assign overflow = ((A[3] & Y[3] & ~S[3]) | (~A[3] & ~Y[3] & S[3])) | cout_sub;
assign cout sub = (m == 1'b1) ? ~C[3] : C[3];
assign result = {cout_sub, S};
endmodule
```

"Schematics":-



"Waveforms":-

For Addition

					40.000 ns	
10.000 ns	15.000 ns	20.000 ns	25.000 ns	30.000 ns	35.000 ns	
11	1100		1111		1011	
1110		1100		1101		
11010		11011		11000		
	11	1100	1100 11 1110 11	1100 1111 1110 1100	1100 1111 1 1110 1100 1	

For Subtraction

