DAY-22

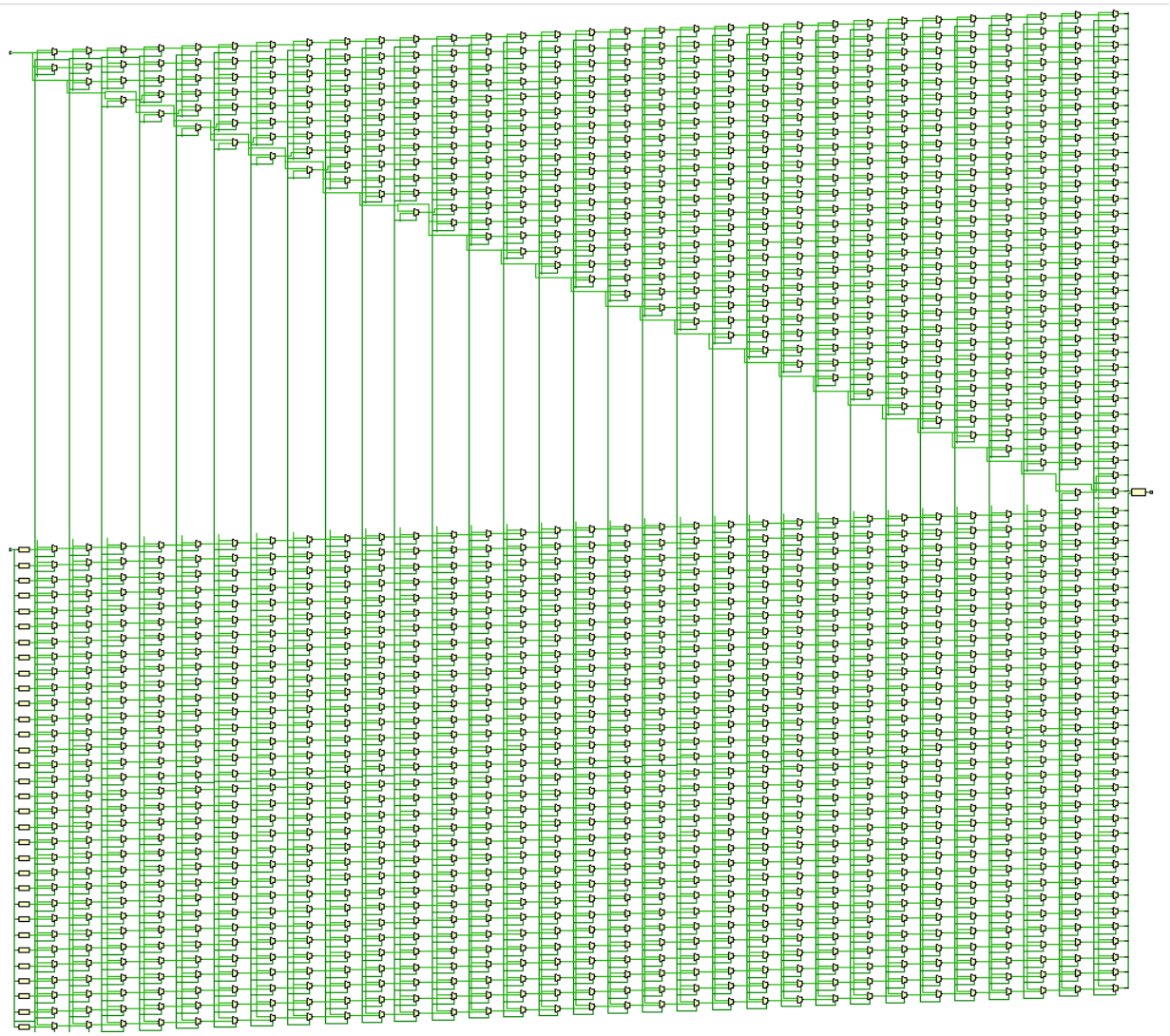
#100DAYSRTL

"Aim":-To Design a DEMUX that acts as an Asynchronous SIPO using System Verilog Design style

"Design Code":-

```
module Mux #(parameter N = 32, M = 5) ( //M=log2(M)
    input  A, //Parallel Data  as input
    input [M-1:0] S,
    output reg [N-1:0] Y // Serial Data as output
);
always @(*) begin
for(int i=0;i<N;i++) begin
for (int j=0;j<N;j++) begin
case(S)
i:begin
        Y[j]=0;
        if(i==j) Y[i]=A;
  end
endcase
end
end
end
endmodule
```

“Schematics”:-



“Console”:-

```
A=1,S=00000,Y=00000000000000000000000000000001
A=1,S=00001,Y=00000000000000000000000000000010
A=1,S=00010,Y=00000000000000000000000000000100
A=1,S=00011,Y=00000000000000000000000000001000
A=1,S=00100,Y=00000000000000000000000000010000
A=1,S=00101,Y=00000000000000000000000000100000
A=1,S=00110,Y=00000000000000000000000001000000
A=1,S=00111,Y=00000000000000000000000010000000
A=1,S=01000,Y=00000000000000000000000100000000
A=1,S=01001,Y=00000000000000000000001000000000
A=1,S=01010,Y=00000000000000000000010000000000
A=1,S=01011,Y=00000000000000000000100000000000
A=1,S=01100,Y=00000000000000000001000000000000
A=1,S=01101,Y=00000000000000000010000000000000
A=1,S=01110,Y=00000000000000000100000000000000
A=1,S=01111,Y=00000000000000001000000000000000
A=1,S=10000,Y=00000000000000010000000000000000
A=1,S=10001,Y=00000000000000100000000000000000
A=1,S=10010,Y=00000000000001000000000000000000
A=1,S=10011,Y=00000000000010000000000000000000
A=1,S=10100,Y=00000000000100000000000000000000
A=1,S=10101,Y=00000000001000000000000000000000
A=1,S=10110,Y=00000000010000000000000000000000
A=1,S=10111,Y=00000000100000000000000000000000
A=1,S=11000,Y=00000001000000000000000000000000
A=1,S=11001,Y=00000010000000000000000000000000
A=1,S=11010,Y=00000100000000000000000000000000
A=1,S=11011,Y=00001000000000000000000000000000
A=1,S=11100,Y=00010000000000000000000000000000
A=1,S=11101,Y=00100000000000000000000000000000
A=1,S=11110,Y=01000000000000000000000000000000
A=1,S=11111,Y=10000000000000000000000000000000
Completed
```

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.292 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.4°C**
Thermal Margin:	57.6°C (30.4 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity