



## DAY-23

### #100DAYSRTL

**“Aim”:-** To Design the input majority circuit in Mixed modeling (Gate & Data Flow).

**“Design Code”:-**

A0	A1	A2	A3	A4	A5	Y
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	1
0	0	0	0	1	1	1
0	0	0	1	0	0	1
0	0	0	1	0	1	1
0	0	0	1	1	0	1
0	0	0	1	1	1	1
0	0	1	0	0	0	1
0	0	1	0	0	1	1
0	0	1	0	1	0	1
0	0	1	0	1	1	1
0	0	1	1	0	0	1
0	0	1	1	0	1	1
0	0	1	1	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	1
0	1	0	1	0	1	1
0	1	0	1	1	0	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	0	0	1	1
0	1	1	0	1	0	1
0	1	1	0	1	1	1
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	1

The min-terms notation for the 5-input majority function is:

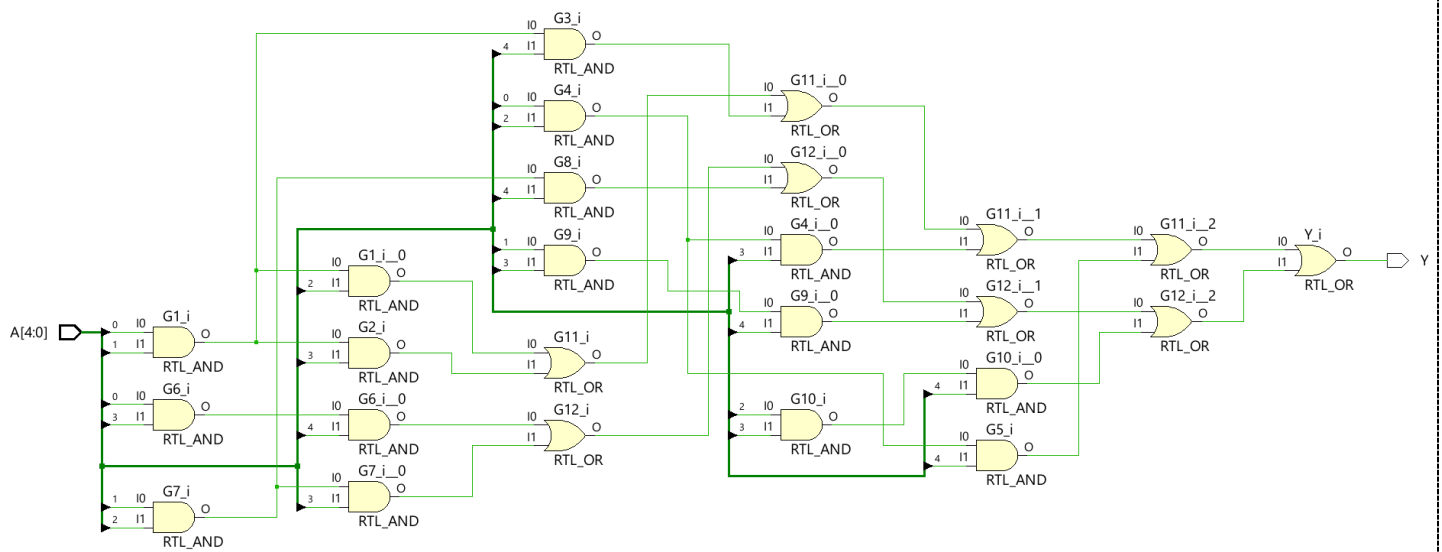
$\Sigma(1, 3, 5, 7, 9, 11, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31)$

```

module MajorityInputCircuit(
input [4:0] A,
output Y
);
wire [11:0]W;
and G1(W[0],A[0],A[1],A[2]);
and G2(W[1],A[0],A[1],A[3]);
and G3(W[2],A[0],A[1],A[4]);
and G4(W[3],A[0],A[2],A[3]);
and G5(W[4],A[0],A[2],A[4]);
and G6(W[5],A[0],A[3],A[4]);
and G7(W[6],A[1],A[2],A[3]);
and G8(W[7],A[1],A[2],A[4]);
and G9(W[8],A[1],A[3],A[4]);
and G10(W[9],A[2],A[3],A[4]);
or G11(W[10],W[0],W[1],W[2],W[3],W[4]);
or G12(W[11],W[5],W[6],W[7],W[8],W[9]);
assign Y=W[10] | W [11];
endmodule

```

## “Schematics”:-



## “Console”:-

A=00100, Y=0  
A=00001, Y=0  
A=01001, Y=0  
A=00011, Y=0  
A=01101, Y=1  
A=01101, Y=1  
A=00101, Y=0  
A=10010, Y=0  
A=00001, Y=0

### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.486 W  
**Design Power Budget:** Not Specified  
**Power Budget Margin:** N/A  
**Junction Temperature:** 25.9°C  
Thermal Margin: 59.1°C (31.2 W)  
Effective  $\theta_{JA}$ : 1.9°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power

