DAY-26

#100DAYSRTL

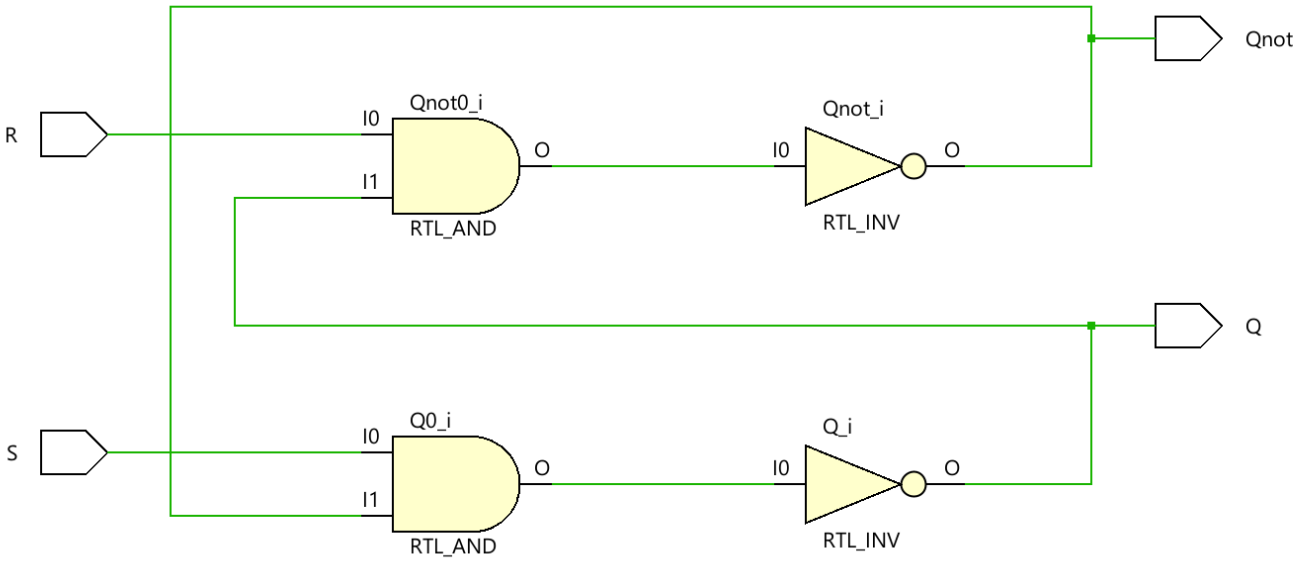
"Aim":-To design SR Latch using Nand Gates or Nor Gates

"SR latch Using Nand Gates" :-

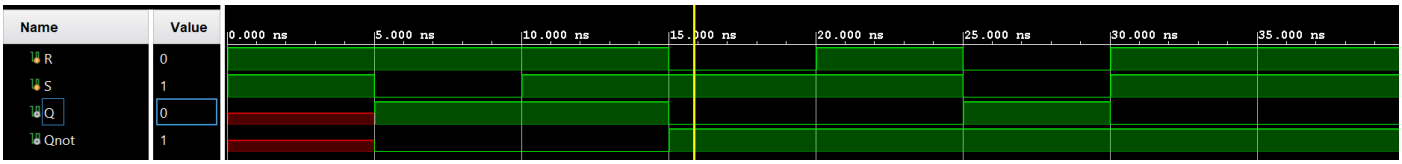
"Design Code":-

```
module NANDSR_latch(
  input  R, S,
  output Q, Qnot);
  nand(Qnot, R, Q);
  nand(Q, S, Qnot);
endmodule
```

"Schematics":-



"Waveforms":-



“Console”:-

S	R	!Q	Q
1	1	x	x
0	1	0	1
1	1	0	1
1	0	1	0
1	1	1	0
0	0	1	1
1	1	1	0

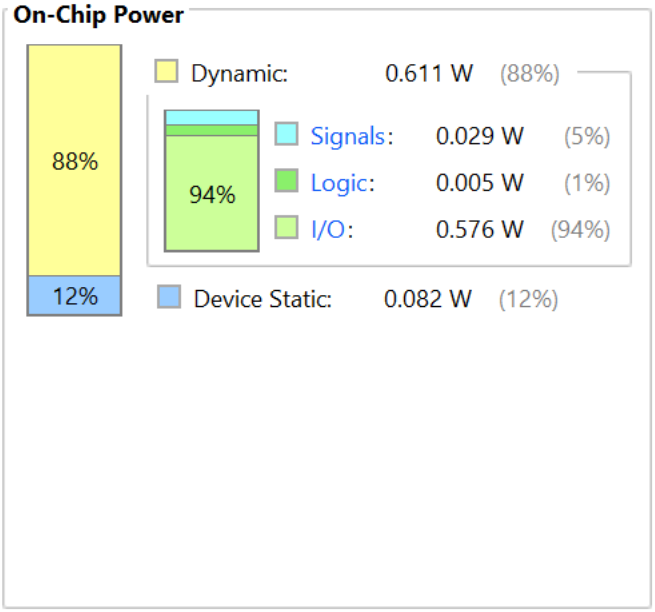
When !Q=Q , Then it is invalid condition

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.693 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	58.7°C (31.0 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

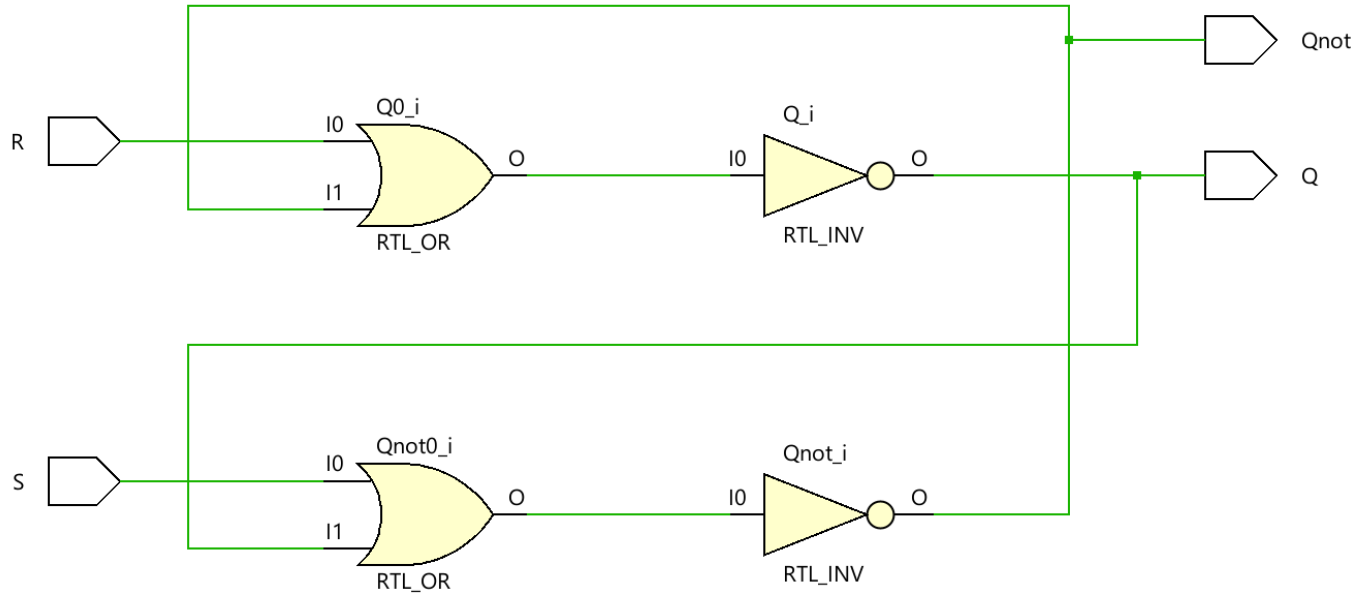


“SR Latch Using Nor Gates” :-

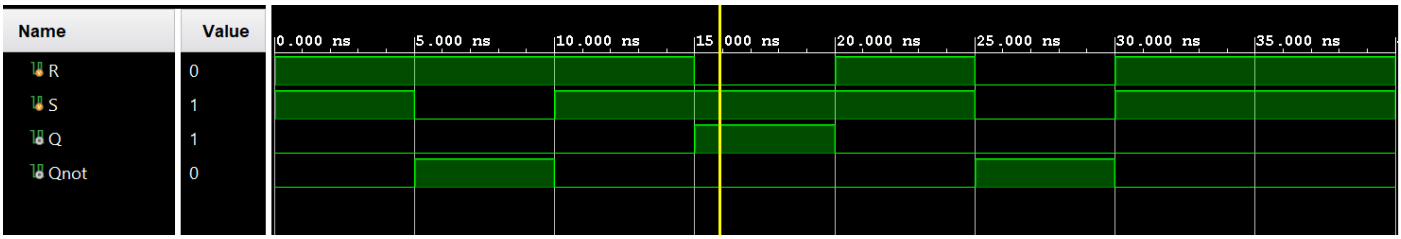
“Design Code”:-

```
module NORSR_latch(
  input  R, S,
  output Q, Qnot);
  nor(Qnot, S, Q);
  nor(Q, R, Qnot);
endmodule
```

“Schematics”:-



“Waveforms”:-



“Console”:-

```
S R !Q Q
1 1 0  0
0 1 1  0
1 1 0  0
1 0 0  1
1 1 0  0
0 0 1  0
1 1 0  0
```

When !Q=Q , Then it is invalid condition

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