DAY-31

#100DAYSRTL

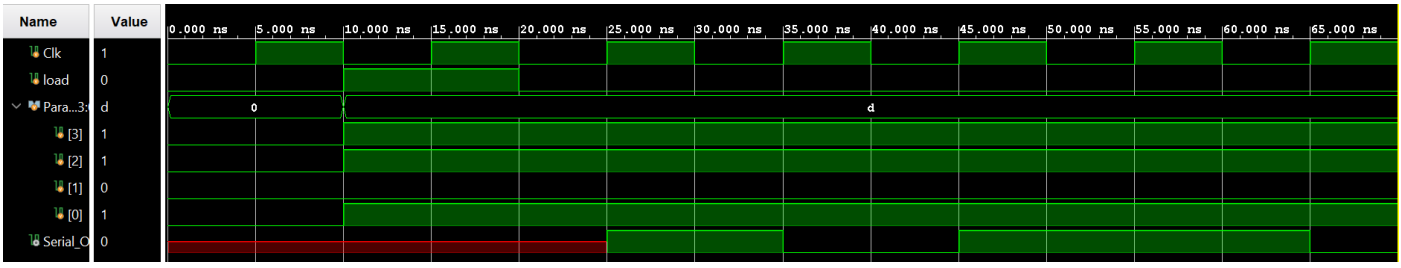
“Aim”:-To Design Parallel Input and Serial output & Parallel input and Parallel output

“PISO”

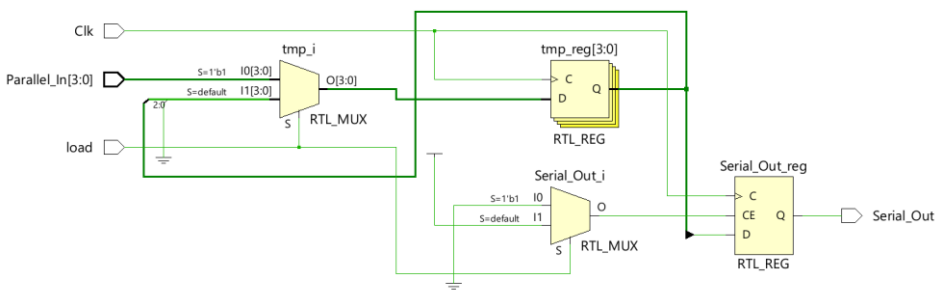
“Design Code”:-

```
module Shiftregister_PISO(Clk, Parallel_In,load, Serial_Out);
input Clk,load;
input [3:0]Parallel_In;
output reg Serial_Out;
reg [3:0]tmp;
always @(posedge Clk)
begin
if(load)
tmp<=Parallel_In;
else
begin
Serial_Out<=tmp[0];
tmp<={1'b0,tmp[3:1]};
end
end
endmodule
```

“Waveforms”:-



“Schematics”:-

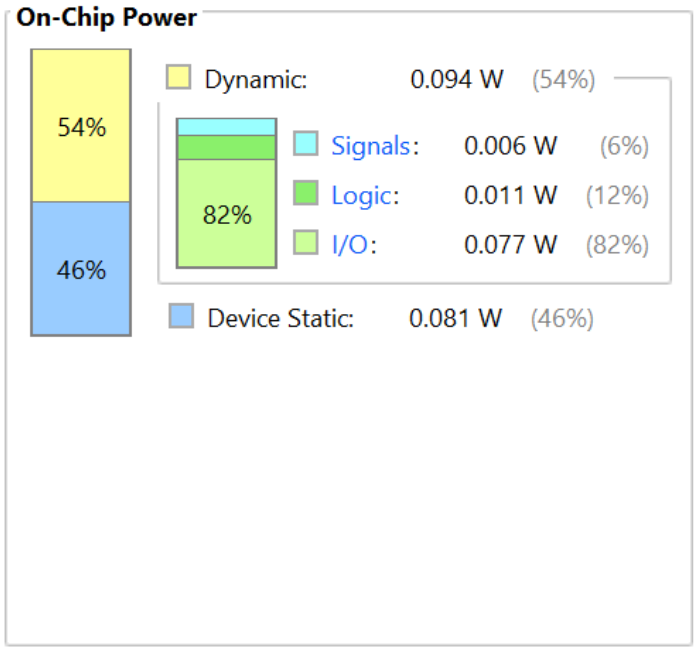


Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.176 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	59.7°C (31.5 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

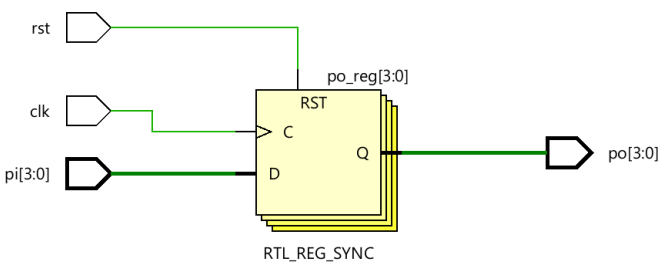


"PIPO"

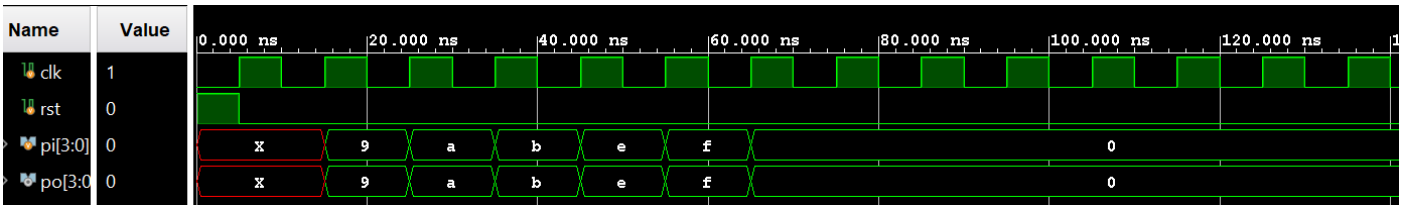
"Design Code":-

```
module pipomod(clk,rst, pi, po);
input clk,rst;
input [3:0] pi;
output reg [3:0] po;
always @(posedge clk)
begin
if (rst)
po<= 4'b0000;
else
po <= pi;
end
endmodule
```

"Schematics":-



“Waveforms”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.106 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power