DAY-29

#100DAYSRTL

“Aim”:-To Specify the differences between a Multi bit flip flop and a register.

Multi-bit Flipflop vs Register :-

Differences between Multi-bit flip-flops and registers:

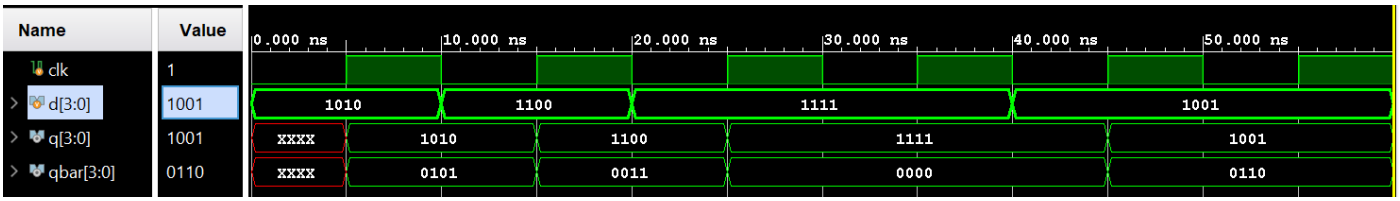
Feature	Multi-bit flip-flop	Register
Definition	A multi-bit flip-flop is a single flip-flop that can store multiple bits of data.	A register is a group of flip-flops that are connected together to store multiple bits of data.
Common uses	Multi-bit flip-flops are typically used to reduce the area and power consumption of digital circuits.	Registers are typically used to store data temporarily, such as the data that is being processed by a microprocessor or the data that is being transmitted between two devices.
Reset signal	Multi-bit flip-flops may or may not have a reset signal.	Registers typically have a reset signal.
Verilog coding	The Verilog code for a multi-bit flip-flop is similar to the Verilog code for a single-bit flip-flop, except that it has multiple D and Q pins.	The Verilog code for a register is simply a group of multi-bit flip-flops that are connected together. The D and Q pins of the flip-flops are connected together in a chain.

D-4bitFlipFlop

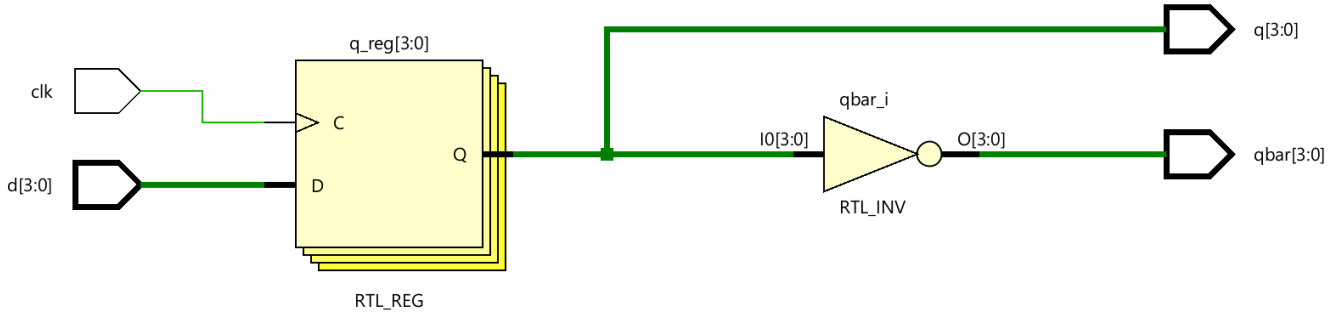
“Design Code”:-

```
module d_flip_flop_4bit (
  input clk,
  input [3:0] d,
  output reg [3:0] q
);
  always @(posedge clk) begin
    q <= d;
  end
endmodule
```

“Waveforms”:-



“Schematics”:-

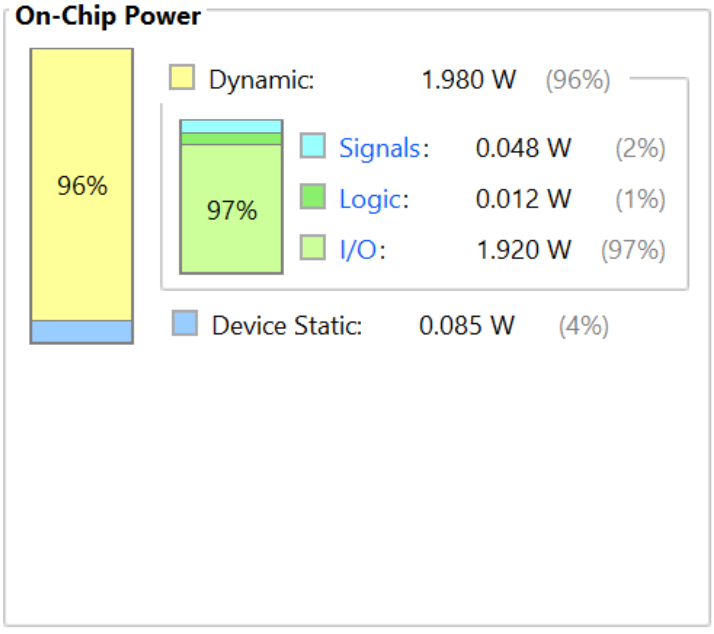


Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.065 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.9°C**
Thermal Margin:	56.1°C (29.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

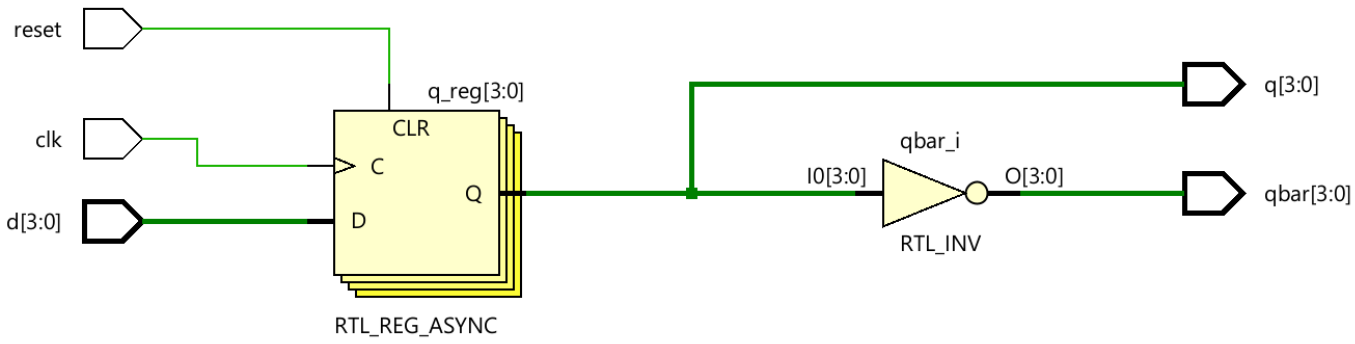


“4bitRegister” :-

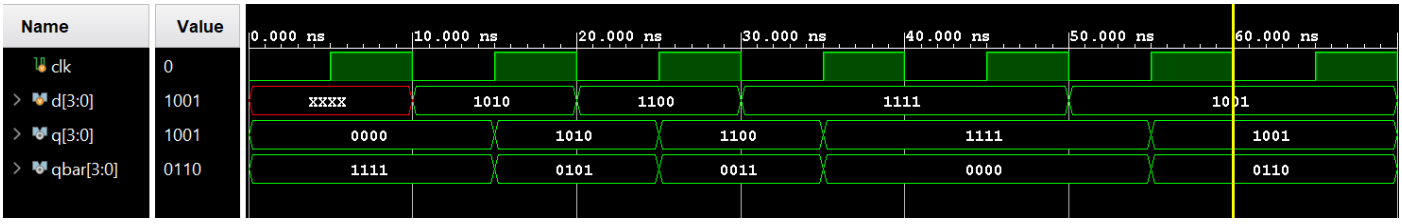
“Design Code”:-

```
module register_4bit (
  input clk,
  input [3:0] d,
  input reset,
  output reg [3:0] q,
  output [3:0] qbar
);
  always @(posedge clk or posedge reset) begin
    if (reset) begin
      q <= 4'b0;
    end else begin
      q <= d;
    end
  end
assign qbar=~q;
endmodule
```

“Schematics”:-



“Waveforms”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.111 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.0°C**
Thermal Margin:	56.0°C (29.6 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity