

DAY-30 #100DAYSRTL

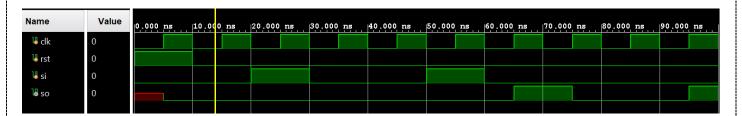
"Aim":-To Design Serial Input and Serial output & Serial input and Parallel output

"SISO"

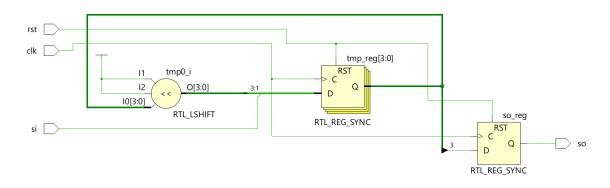
"Design Code":-

```
module sisomod(clk,rst,si,so);
input clk,si,rst;
output reg so;
reg [3:0] tmp;
always @(posedge clk)
begin
if (rst) begin
tmp <= 4'b0000;
so<=0;
end
else begin
tmp <= tmp << 1;
tmp[0] <= si;
so <= tmp[3];
end
end
end
end
endmodule</pre>
```

"Waveforms":-



"Schematics":-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.356 W

Design Power Budget: Not Specified

Power Budget Margin: N/A

Junction Temperature: 25.7°C

Thermal Margin: 59.3°C (31.3 W)

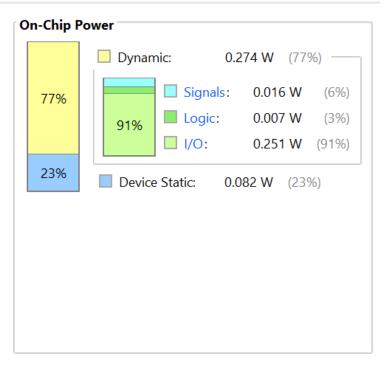
Effective ϑJA : 1.9°C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Launch Power Constraint Advisor to find and fix

invalid switching activity

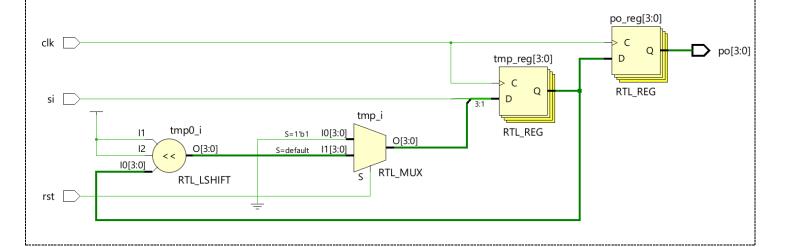


"<u>SIPO</u>"

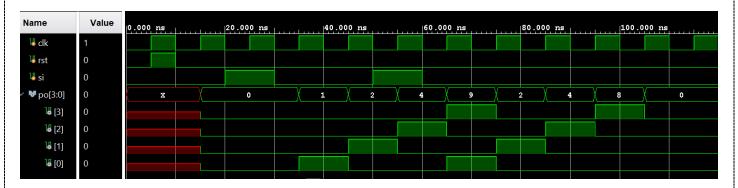
"Design Code":-

```
module sipomod(clk,rst, si, po);
input clk, si,rst;
output reg [3:0] po;
reg [3:0] tmp;
always @(posedge clk) begin
if (rst)
tmp <= 4'b0000;
else
tmp <= tmp << 1;
tmp[0] <= si;
po = tmp;
end
endmodule</pre>
```

"Schematics":-



"Waveforms":-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.875 W

Design Power Budget: Not Specified

Power Budget Margin: N/A

Junction Temperature: 26.6°C

Thermal Margin: 58.4°C (30.8 W)

Effective ϑJA : 1.9°C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

Launch Power Constraint Advisor to find and fix

invalid switching activity

