DAY-37

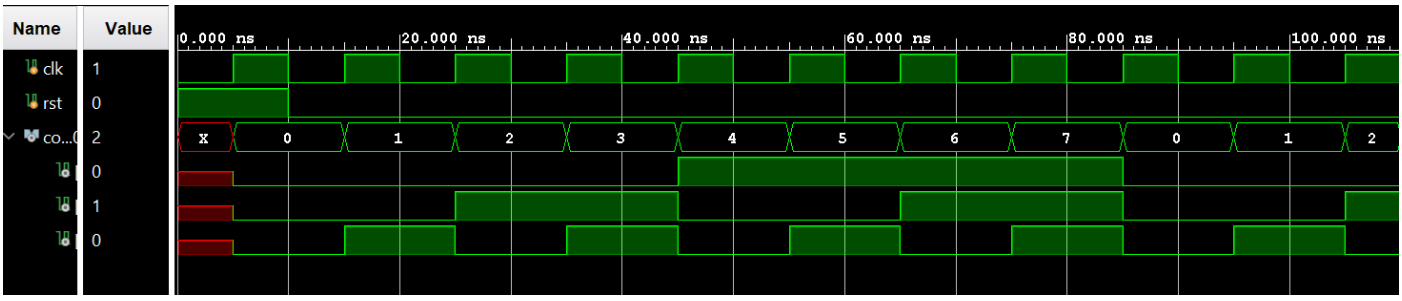
#100DAYSRTL

“Aim”:-To Design a Synchronous series counter

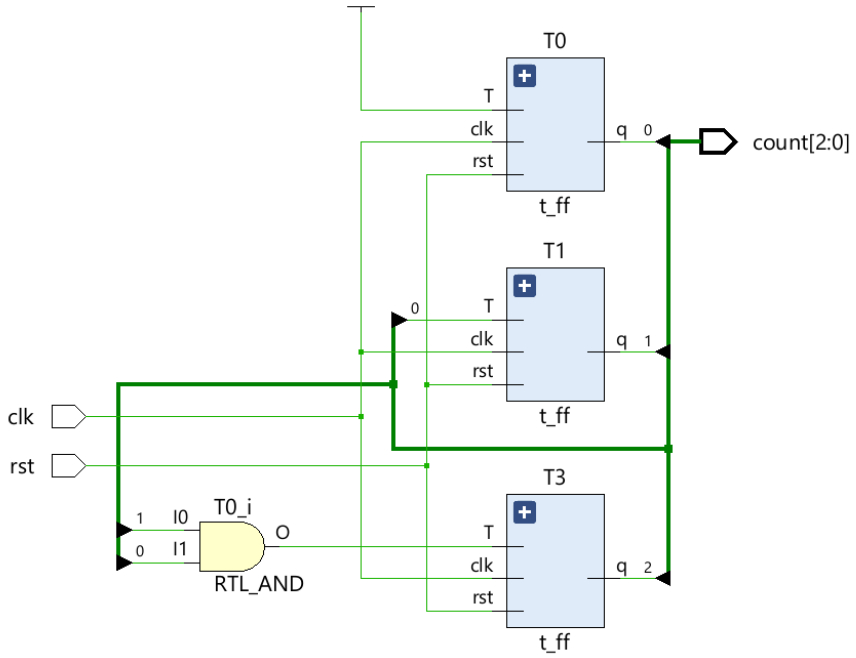
“Design Code”:-

```
module SSC(input clk,rst,output [2:0] count);
wire [2:0] q;
t_ff T0(1'b1,rst,clk,q[0]);
t_ff T1(q[0],rst,clk,q[1]);
t_ff T3((q[1]&q[0]),rst,clk,q[2]);
assign count=q;
endmodule
module t_ff(input T,rst,clk,output reg q);
always @(posedge clk) begin
if(rst) q<=1'b0;
else begin
case (T)
1'b0:q<=q;
1'b1:q<=~q;
default : begin ; end
endcase
end
end
endmodule
```

“Waveforms”:-



“Schematics”:-



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.581 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**28.0°C**
Thermal Margin:	57.0°C (30.1 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power