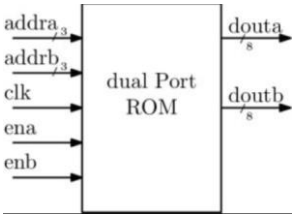
DAY-44

#100DAYSRTL

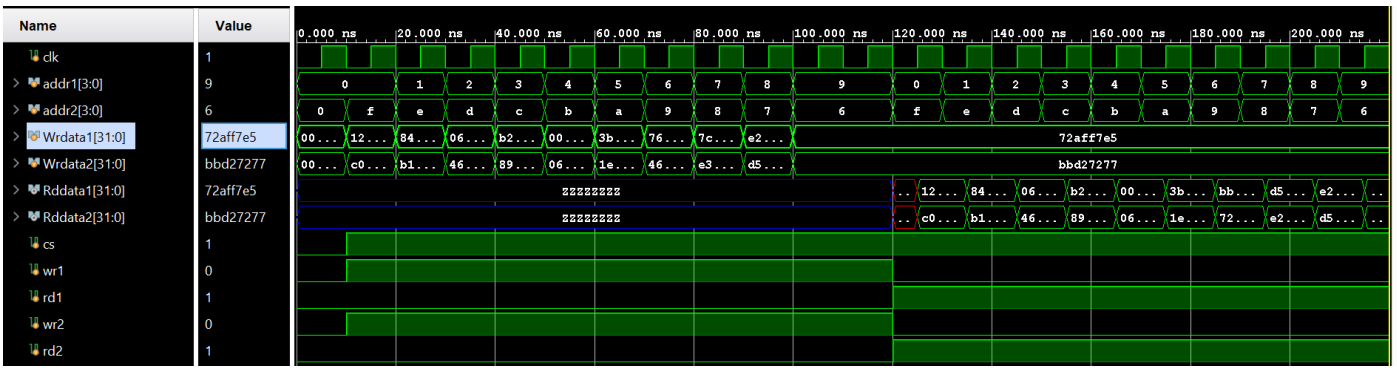
“Aim”:-To design a 32-bit Dual Port RAM

“Design Code”:-

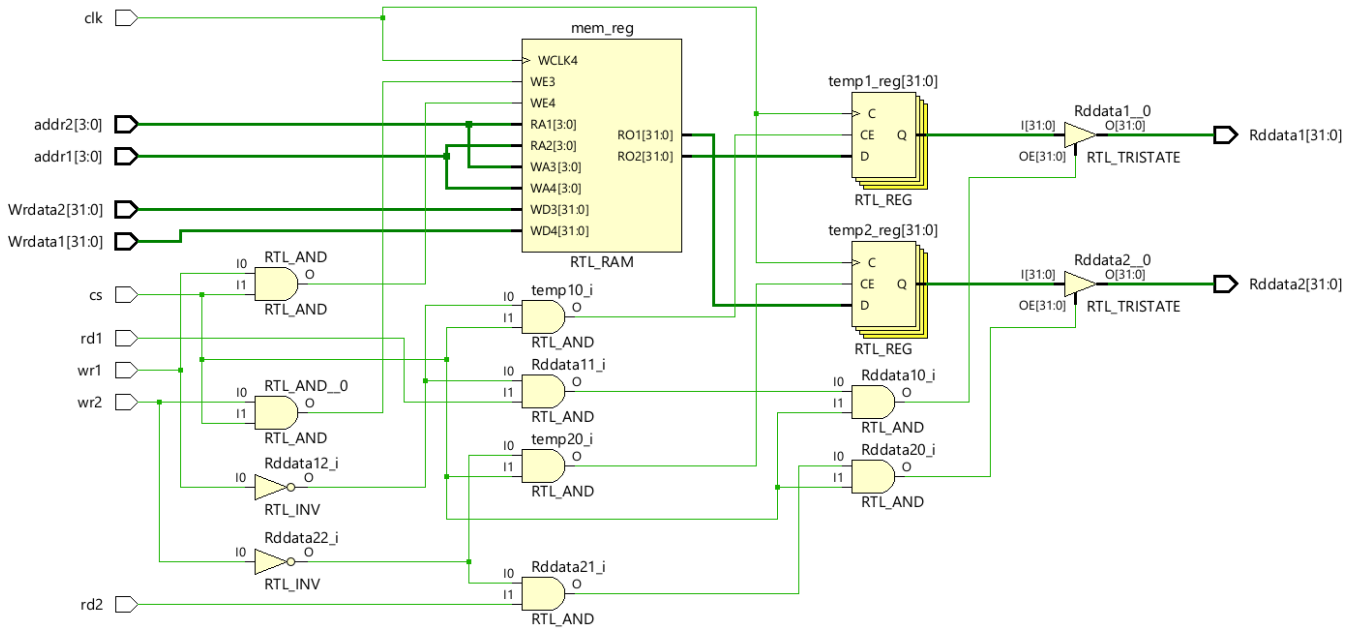



```
module SPRAM #(parameter AddrWidth=4,DataWidth=32,Depth=16)(clk,addr1,addr2,Wrdata1,Wrdata2,Rddata1,Rddata2,cs,wr1,rd1,wr2,rd2);
input clk;
input [AddrWidth-1:0] addr1;
input [AddrWidth-1:0] addr2;
input [DataWidth-1:0] Wrdata1;
input [DataWidth-1:0] Wrdata2;
output [DataWidth-1:0] Rddata1;
output [DataWidth-1:0] Rddata2;
input cs,wr1,rd1,wr2,rd2;
reg [DataWidth-1:0] temp1;
reg [DataWidth-1:0] temp2;
reg [DataWidth-1:0] mem [Depth];
always @(posedge clk) begin
if(wr1&&cs) mem[addr1]<=Wrdata1;
end
always @(posedge clk) begin
if(wr2&&cs) mem[addr2]<=Wrdata2;
end
always @(posedge clk) begin
if(~wr1&&cs) temp1<= mem[addr1];
end
always @(posedge clk) begin
if(~wr2&&cs) temp2<= mem[addr2];
end
assign Rddata1=((~wr1)&&rd1&&cs)?temp1:'hz;
assign Rddata2=((~wr2)&&rd2&&cs)?temp2:'hz;
endmodule
```

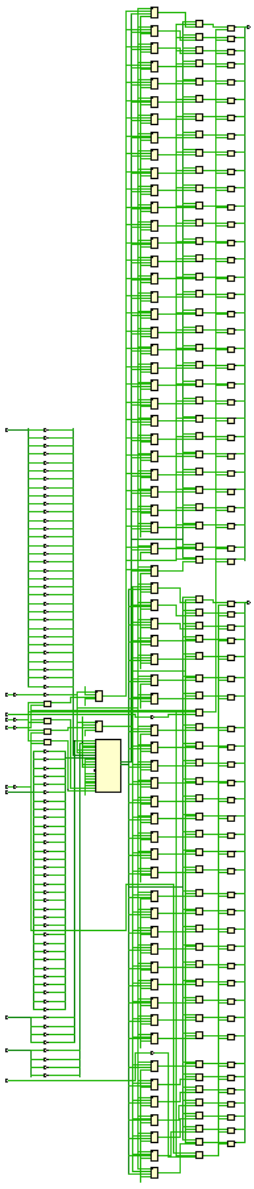
“Waveforms”:-



“Elaborated Design”:-



“Implemented Design”:-



Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**7.743 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**39.6°C**
Thermal Margin:	45.4°C (23.9 W)
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity