DAY-99
#100DAYSRTL

"UVM: Project-1"

"Aim":-To Verify the Combinational Adder using UVM testbenches

"Design Code":-

```
module add(input [3:0] a,b,output [4:0] y);
assign y = a + b;
endmodule
```

"Interface":-

```
interface add_if();
logic [3:0] a;
logic [3:0] b;
logic [4:0] y;
endinterface
```

"Transaction":-

```
`include "uvm_macros.svh"
import uvm_pkg::*;
class transaction extends uvm_sequence_item;
rand bit [3:0] a;
rand bit [3:0] b;
bit [4:0] y;
  function new(input string path = "transaction");
    super.new(path);
  endfunction
`uvm_object_utils_begin(transaction)
`uvm_field_int(a, UVM_DEFAULT)
`uvm_field_int(b, UVM_DEFAULT)
`uvm_field_int(y, UVM_DEFAULT)
`uvm_object_utils_end
endclass
```

"Generator":-

```
class generator extends uvm_sequence #(transaction);
`uvm_object_utils(generator)
transaction t;
integer i;
  function new(input string path = "generator");
    super.new(path);
  endfunction
virtual task body();
  t = transaction::type_id::create("t");
  repeat(10)
    begin
    start_item(t);
    t.randomize();
    `uvm_info("GEN",$sformatf("Data send to Driver a :%0d , b :%0d",t.a,t.b), UVM_NONE);
    finish_item(t);
    end
endtask
endclass
```

“Driver”:-

```
class driver extends uvm_driver #(transaction);
`uvm_component_utils(driver)
    function new(input string path = "driver", uvm_component parent = null);
      super.new(path, parent);
     endfunction
transaction tc;
virtual add_if aif;
    virtual function void build_phase(uvm_phase phase);
      super.build_phase(phase);
      tc = transaction::type_id::create("tc");
      if(!uvm_config_db #(virtual add_if)::get(this,"","aif",aif))
      `uvm_error("DRV","Unable to access uvm_config_db");
    endfunction
    virtual task run_phase(uvm_phase phase);
    forever begin
    seq_item_port.get_next_item(tc);
    aif.a <= tc.a;
    aif.b <= tc.b;
       `uvm_info("DRV", $sformatf("Trigger DUT a: %0d ,b :  %0d",tc.a, tc.b), UVM_NONE);
    seq_item_port.item_done();
    #10;
    end
    endtask
endclass
```

“Monitor”:-

```
class monitor extends uvm_monitor;
`uvm_component_utils(monitor)
uvm_analysis_port #(transaction) send;
  function new(input string path = "monitor", uvm_component parent = null);
    super.new(path, parent);
    send = new("send", this);
  endfunction
  transaction t;
  virtual add_if aif;
  virtual function void build_phase(uvm_phase phase);
   super.build_phase(phase);
    t = transaction::type_id::create("t");
   if(!uvm_config_db #(virtual add_if)::get(this,"","aif",aif))
   `uvm_error("MON","Unable to access uvm_config_db");
  endfunction
    virtual task run_phase(uvm_phase phase);
    forever begin
    #10;
    t.a = aif.a;
    t.b = aif.b;
    t.y = aif.y;
    `uvm_info("MON", $sformatf("Data send to Scoreboard a : %0d , b : %0d and y : %0d", t.a,t.b,t.y), UVM_NONE);
    send.write(t);
    end
    endtask
endclass
```

“Scoreboard”:-

```
class scoreboard extends uvm_scoreboard;
`uvm_component_utils(scoreboard)
uvm_analysis_imp #(transaction,scoreboard) recv;
transaction tr;
  function new(input string path = "scoreboard", uvm_component parent = null);
    super.new(path, parent);
    recv = new("recv", this);
  endfunction
  virtual function void build_phase(uvm_phase phase);
  super.build_phase(phase);
    tr = transaction::type_id::create("tr");
  endfunction
  virtual function void write(input transaction t);
   tr = t;
  `uvm_info("SCO",$sformatf("Data rcvd from Monitor a: %0d , b : %0d and y : %0d",tr.a,tr.b,tr.y), UVM_NONE);
    if(tr.y == tr.a + tr.b)
        `uvm_info("SCO","Test Passed", UVM_NONE)
   else
        `uvm_info("SCO","Test Failed", UVM_NONE);
   endfunction
endclass
```

“Agent”:-

```
class agent extends uvm_agent;
`uvm_component_utils(agent)
function new(input string inst = "AGENT", uvm_component c);
super.new(inst, c);
endfunction
monitor m;
driver d;
uvm_sequencer #(transaction) seqr;
virtual function void build_phase(uvm_phase phase);
super.build_phase(phase);
  m = monitor::type_id::create("m",this);
  d = driver::type_id::create("d",this);
  seqr = uvm_sequencer #(transaction)::type_id::create("seqr",this);
endfunction
virtual function void connect_phase(uvm_phase phase);
super.connect_phase(phase);
  d.seq_item_port.connect(seqr.seq_item_export);
endfunction
endclass
```

“Environment”:-

```
class env extends uvm_env;
`uvm_component_utils(env)
function new(input string inst = "ENV", uvm_component c);
super.new(inst, c);
endfunction
scoreboard s;
agent a;
virtual function void build_phase(uvm_phase phase);
super.build_phase(phase);
  s = scoreboard::type_id::create("s",this);
  a = agent::type_id::create("a",this);
endfunction
virtual function void connect_phase(uvm_phase phase);
super.connect_phase(phase);
a.m.send.connect(s.recv);
endfunction
endclass
```

“Test”:-

```
class test extends uvm_test;
`uvm_component_utils(test)
function new(input string inst = "TEST", uvm_component c);
super.new(inst, c);
endfunction
generator gen;
env e;
virtual function void build_phase(uvm_phase phase);
super.build_phase(phase);
  gen = generator::type_id::create("gen");
  e = env::type_id::create("e",this);
endfunction
virtual task run_phase(uvm_phase phase);
   phase.raise_objection(this);
   gen.start(e.a.seqr);
   #50;
   phase.drop_objection(this);
endtask
endclass
```

“Tb Top”:-

```
module add_tb();
add_if aif();
add dut (.a(aif.a), .b(aif.b), .y(aif.y));
initial begin
$dumpfile("dump.vcd");
$dumpvars;
end
initial begin
uvm_config_db #(virtual add_if)::set(null, "uvm_test_top.e.a*", "aif", aif);
run_test("test");
end
endmodule
```

“Result”:-

```
UVM_INFO @ 0: reporter [RNTST] Running test test...
UVM_INFO /home/runner/testbench.sv(30) @ 0: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :3 , b :14
UVM_INFO /home/runner/testbench.sv(56) @ 0: uvm_test_top.e.a.d [DRV] Trigger DUT a: 3 ,b :  14
UVM_INFO /home/runner/testbench.sv(85) @ 10: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 3 , b : 14 and y : 17
UVM_INFO /home/runner/testbench.sv(106) @ 10: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 3 , b : 14 and y : 17
UVM_INFO /home/runner/testbench.sv(108) @ 10: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 10: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :0 , b :7
UVM_INFO /home/runner/testbench.sv(56) @ 10: uvm_test_top.e.a.d [DRV] Trigger DUT a: 0 ,b :  7
UVM_INFO /home/runner/testbench.sv(85) @ 20: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 0 , b : 7 and y : 7
UVM_INFO /home/runner/testbench.sv(106) @ 20: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 0 , b : 7 and y : 7
UVM_INFO /home/runner/testbench.sv(108) @ 20: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 20: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :10 , b :9
UVM_INFO /home/runner/testbench.sv(56) @ 20: uvm_test_top.e.a.d [DRV] Trigger DUT a: 10 ,b :  9
UVM_INFO /home/runner/testbench.sv(85) @ 30: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 10 , b : 9 and y : 19
UVM_INFO /home/runner/testbench.sv(106) @ 30: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 10 , b : 9 and y : 19
UVM_INFO /home/runner/testbench.sv(108) @ 30: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 30: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :1 , b :4
UVM_INFO /home/runner/testbench.sv(56) @ 30: uvm_test_top.e.a.d [DRV] Trigger DUT a: 1 ,b :  4
UVM_INFO /home/runner/testbench.sv(85) @ 40: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 1 , b : 4 and y : 5
UVM_INFO /home/runner/testbench.sv(106) @ 40: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 1 , b : 4 and y : 5
UVM_INFO /home/runner/testbench.sv(108) @ 40: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 40: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :5 , b :8
UVM_INFO /home/runner/testbench.sv(56) @ 40: uvm_test_top.e.a.d [DRV] Trigger DUT a: 5 ,b :  8
UVM_INFO /home/runner/testbench.sv(85) @ 50: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 5 , b : 8 and y : 13
UVM_INFO /home/runner/testbench.sv(106) @ 50: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 5 , b : 8 and y : 13
UVM_INFO /home/runner/testbench.sv(108) @ 50: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 50: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :6 , b :5
UVM_INFO /home/runner/testbench.sv(56) @ 50: uvm_test_top.e.a.d [DRV] Trigger DUT a: 6 ,b :  5
UVM_INFO /home/runner/testbench.sv(85) @ 60: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 6 , b : 5 and y : 11
UVM_INFO /home/runner/testbench.sv(106) @ 60: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 6 , b : 5 and y : 11
UVM_INFO /home/runner/testbench.sv(108) @ 60: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 60: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :4 , b :11
UVM_INFO /home/runner/testbench.sv(56) @ 60: uvm_test_top.e.a.d [DRV] Trigger DUT a: 4 ,b :  11
UVM_INFO /home/runner/testbench.sv(85) @ 70: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 4 , b : 11 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 70: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 4 , b : 11 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 70: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 70: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :15 , b :10
UVM_INFO /home/runner/testbench.sv(56) @ 70: uvm_test_top.e.a.d [DRV] Trigger DUT a: 15 ,b :  10
UVM_INFO /home/runner/testbench.sv(85) @ 80: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 15 , b : 10 and y : 25
UVM_INFO /home/runner/testbench.sv(106) @ 80: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 15 , b : 10 and y : 25
UVM_INFO /home/runner/testbench.sv(108) @ 80: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 80: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :7 , b :2
UVM_INFO /home/runner/testbench.sv(56) @ 80: uvm_test_top.e.a.d [DRV] Trigger DUT a: 7 ,b :  2
UVM_INFO /home/runner/testbench.sv(85) @ 90: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 7 , b : 2 and y : 9
UVM_INFO /home/runner/testbench.sv(106) @ 90: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 7 , b : 2 and y : 9
UVM_INFO /home/runner/testbench.sv(56) @ 80: uvm_test_top.e.a.d [DRV] Trigger DUT a: 7 ,b :  2
UVM_INFO /home/runner/testbench.sv(85) @ 90: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 7 , b : 2 and y : 9
UVM_INFO /home/runner/testbench.sv(106) @ 90: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 7 , b : 2 and y : 9
UVM_INFO /home/runner/testbench.sv(108) @ 90: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(30) @ 90: uvm_test_top.e.a.seqr@@gen [GEN] Data send to Driver a :12 , b :3
UVM_INFO /home/runner/testbench.sv(56) @ 90: uvm_test_top.e.a.d [DRV] Trigger DUT a: 12 ,b :  3
UVM_INFO /home/runner/testbench.sv(85) @ 100: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 100: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 100: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(85) @ 110: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 110: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 110: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(85) @ 120: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 120: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 120: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(85) @ 130: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 130: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 130: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/runner/testbench.sv(85) @ 140: uvm_test_top.e.a.m [MON] Data send to Scoreboard a : 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(106) @ 140: uvm_test_top.e.s [SCO] Data rcvd from Monitor a: 12 , b : 3 and y : 15
UVM_INFO /home/runner/testbench.sv(108) @ 140: uvm_test_top.e.s [SCO] Test Passed
UVM_INFO /home/build/vlib1/vlib/uvm-1.2/src/base/uvm_objection.svh(1271) @ 140: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /home/build/vlib1/vlib/uvm-1.2/src/base/uvm_report_server.svh(869) @ 140: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :   65
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[DRV]     10
[GEN]     10
[MON]     14
[RNTST]     1
[SCO]     28
[TEST_DONE]     1
[UVM/RELNOTES]     1
```