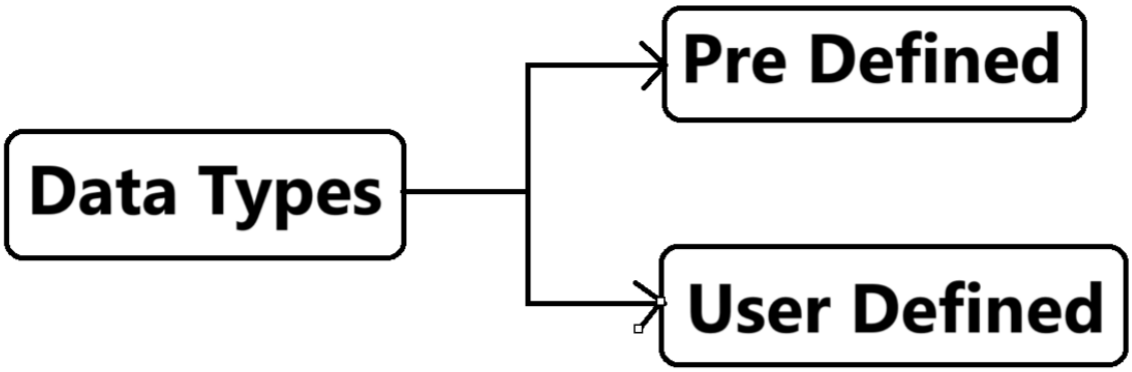
DAY-52
#100DAYSRTL

"System Verilog : Data Types "



Predefined Datatypes:-

2 valued data type	
bit:	1 bit (packed array)
byte:	8 bit (character)
shortint:	16 bit
int:	32 bit

4 valued data type	
logic:	1 bit (packed array)
integer:	32 bit
time:	64 bit unsigned

- 2 Valued :- Digits : 0 or 1
- 4 Valued :- Digits : 0 or 1 or X or Z

Code Practising:-

- 2 Valued Data Type:-

```
module tb;
//Way of defining the 2 valued data types
bit a;
byte b;
shortint c;
int c;
initial begin
//Displaying the default values of 2 valued data types
$display("The default value of bit data type:-%b",a);
$display("The default value of byte data type:-%b",b);
$display("The default value of shortint data type:-%b",c);
$display("The default value of int data type:-%b",d);
end
endmodule
```

4 Valued Data Type:-

```
module tb;
//Way of defining the 4 valued data types
logic a;
integer b;
time c;
initial begin
//Displaying the default values of 4 valued data types
$display("The default value of logic data type:-%b",a);
$display("The default value of integer data type:-%b",b);
$display("The default value of time data type:-%t",c);
end
endmodule
```

Console:-

2 Valued Data Type:-

```
The default value of bit data type:-0
The default value of byte data type:-0
The default value of shortint data type:-0
The default value of int data type:-0
```

4 Valued Data Type:-

```
The default value of logic data type:-x
The default value of integer data type:-xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
The default value of time data type:-                    0
```

Integer Data Types:-

shortint	2-state (1, 0), 16 bit signed
int	2-state, 32 bit signed
longint	2-state, 64 bit signed
byte	2-state, 8 bit signed
bit	2-state, user-defined vector size
logic	4-state (1,0,x,z) user-def
reg	4-state user-defined size
integer	4-state, 32 bit signed
time	4-state, 64 bit unsigned

Signed/Unsigned Integers:-

- byte, shortint, int, integer and longint defaults to signed
  - Use unsigned to represent unsigned integer value
    Example: int unsigned a;
- bit, reg and logic defaults to unsigned

- To create vectors, use the following syntax:
  - ✓Eg:- logic [1:0] L; // Creates 2 bit logic vector
- To use these types as unsigned, user has to explicitly declare it as unsigned.
  - ✓Eg:-int unsigned a;

String Data Types:-

- In Verilog, string literals are packed arrays of a width that is a multiple of 8 bits which hold ASCII values.
- In Verilog, if a string is larger than the destination string variable, the string is truncated to the left, and the leftmost
- characters will be lost.
- System Verilog adds new keyword "string" which is used to declare string data types unlike verilog.
- String data types can be of arbitrary length and no truncation occurs.

Code Practising:-

```
module tb;
//Way of defining the string data type
string a;
initial begin
//Displaying the default values of string data types
$display("The default value of logic data type:-%s",a);
end
endmodule
```

Console:-

Name	Value	Data...
a	""	String

; Default value :Null

User defined Datatypes:-

Systemverilog allows the user to define datatypes.
There are different ways to define user defined datatypes.

1. Class
2. Enumarations.
3. Struct
4. Union.
5. Typedef