DAY-85
#100DAYSRTL

"System Verilog:- TestBench Components"

"Transaction":-

It contains

- ✓ variables for all ports (DUT) except Global Signals
- ✓ modifiers for input ports
- ✓ Constrains for variables
- ✓ Methods→Printing Values, Copy

"Generator":-

- ✓ It performs Randomization for transaction method
- ✓ It Sends transactions to the driver
- ✓ It Sense event from Scoreboard and Driver

"Driver":-

- ✓ It Receives transactions from the generator
- ✓ It applies reset to DUT
- ✓ It applies transactions to DUT with an interface

"Monitor":-

- ✓ It Capture DUT response
- ✓ It Sends a response transaction to the scoreboard
- ✓ It also controls data to be sent for a specific operation

"Scoreboard":-

- ✓ It Receives transactions from the monitor
- ✓ Store transaction: array, Queue, Associative Array, etc
- ✓ Compare with expected result

“Environment Class”:-

- ✓It holds all classes together
- ✓It Schedules different process
- ✓It connects Mailbox, Events

“Transaction”:-

- ✓It has all the ports of DUT defined with logic
- ✓It is dynamic in nature