DAY-51
#100DAYSRTL

"Introduction to System Verilog"

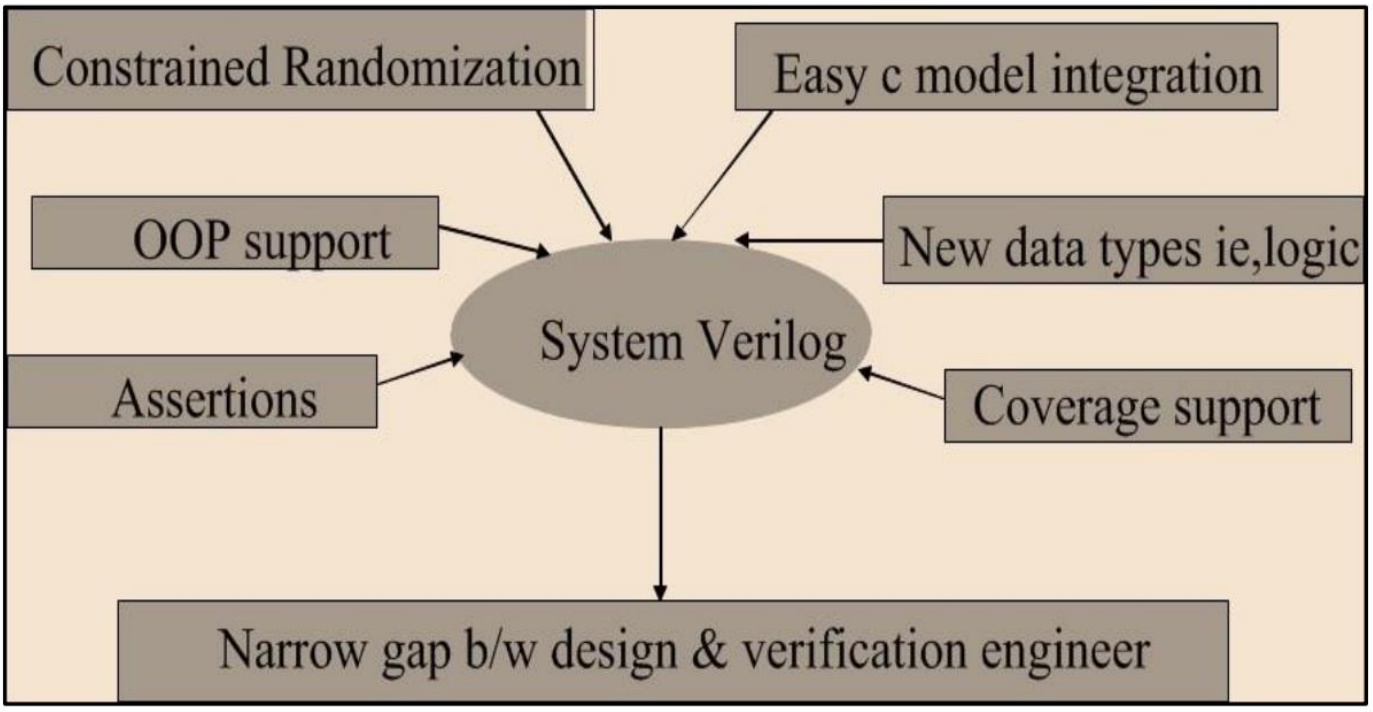
What is System Verilog:-

- System Verilog is a combined hardware description language and Hardware verification language
- System Verilog is an extensive set of enhancements to the IEEE
- 1364 Verilog-2001 standards
- It has features inherited from Verilog HDL, VHDL, C, C++

History and Evolution of System Verilog:-

- Verilog (IEEE standard 1364)
  - ✓ Began in 1983 as a proprietary language
  - ✓ Opened to the public in 1992
  - ✓ Became an IEEE standard in 1995 (updated in 2001 and 2005)
  - ✓ Between 1983 and 2005 design sizes increased dramatically
- System Verilog (IEEE standard 1800)
  - ✓ Originally intended to be the 2005 update to Verilog
  - ✓ Contains hundreds of enhancements and extensions to Verilog
  - ✓ Published in 2005 as a separate document
  - ✓ Officially superseded Verilog in 2009
  - ✓ Updated with more features in 2012 (IEE 1800 2012 standard)

Why is System Verilog:-



System Verilog-User View:-

System Verilog has 5 major parts

1. SVD – System Verilog for Design:-Features supporting Design
2. SVTB – System Verilog for Test benches:- Test bench specific Features
3. SVA – System Verilog Assertions:- Features for temporal and concurrent assertions
4. SVDPI – SV Direct Programming Interface:- For better C/C++ Integration
5. SVAPI – SV Application Programming Interface:-For better Coverage/Assertion integration

Verilog Vs System Verilog :-

VERILOG	SYSTEMVERILOG
Verilog is a Hardware Description Language (HDL).	SystemVerilog is a combination of both Hardware Description Language (HDL) and Hardware Verification Language (HVL).
Verilog language is used to structure and model electronic systems.	SystemVerilog language is used to model, design, simulate, test and implement electronic system.
It supports structured paradigm.	It supports structured and object oriented paradigm.
Verilog is based on module level testbench.	SystemVerilog is based on class level testbench.
It is standardized as IEEE 1364.	It is standardized as IEEE 1800-2012.
Verilog is influenced by C language and Fortran programming language.	SystemVerilog is based on Verilog, VHDL and c++ programming language.
It has file extension .v or .vh	It has file extension .sv or .svh
It supports Wire and Reg datatype.	It supports various datatypes like enum, union, struct, string, class.
It is based on hierarchy of modules.	It is based on classes.
It was began in 1983 as proprietary language for hardware modelling.	It was originally intended as an extension to Verilog in the year 2005.

Why not VHDL ? :-

VHDL Lacks

- ✓ Constrained Random Generation
- ✓ Functional Coverage
- ✓ Assertions

Specman E/Vera

- ✓ Used with VHDL and Verilog for Constrained Random generation and Functional Coverage

PSL (Property Specification Language)

- ✓ Used for Assertions

- Learning 1 language (System Verilog) is better than learning 2 languages (Specman E/Vera and PSL)

System Verilog Testbench Architecture:-