DIGITAL CLOCK USING SYSTEM VERILOG:-

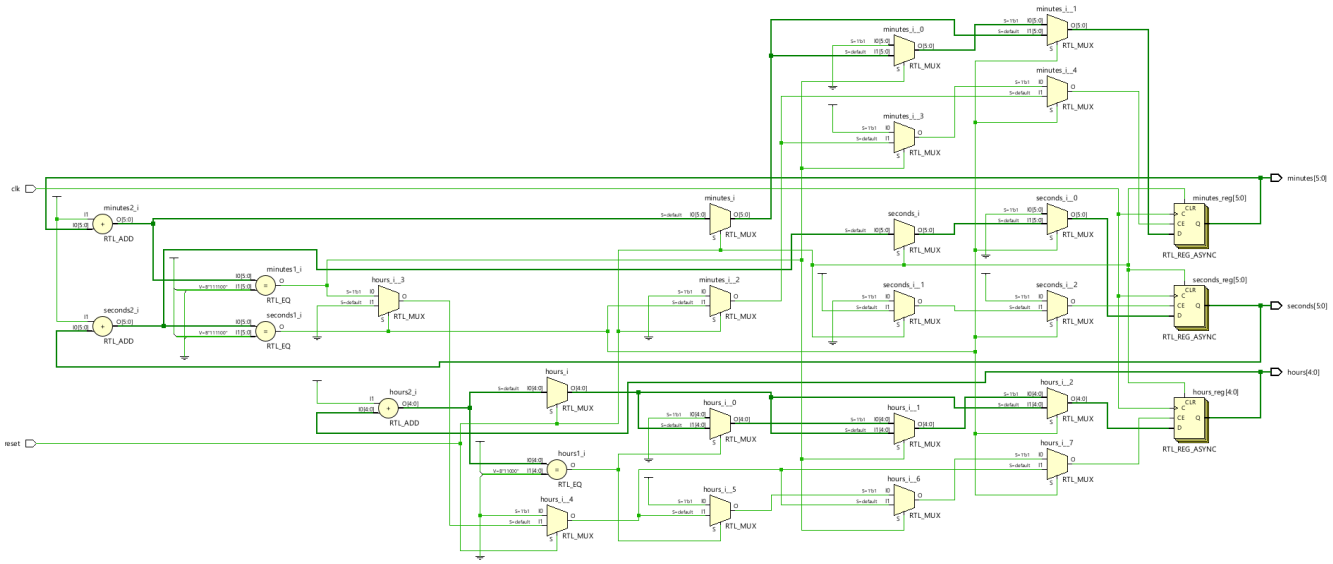
CODE:-

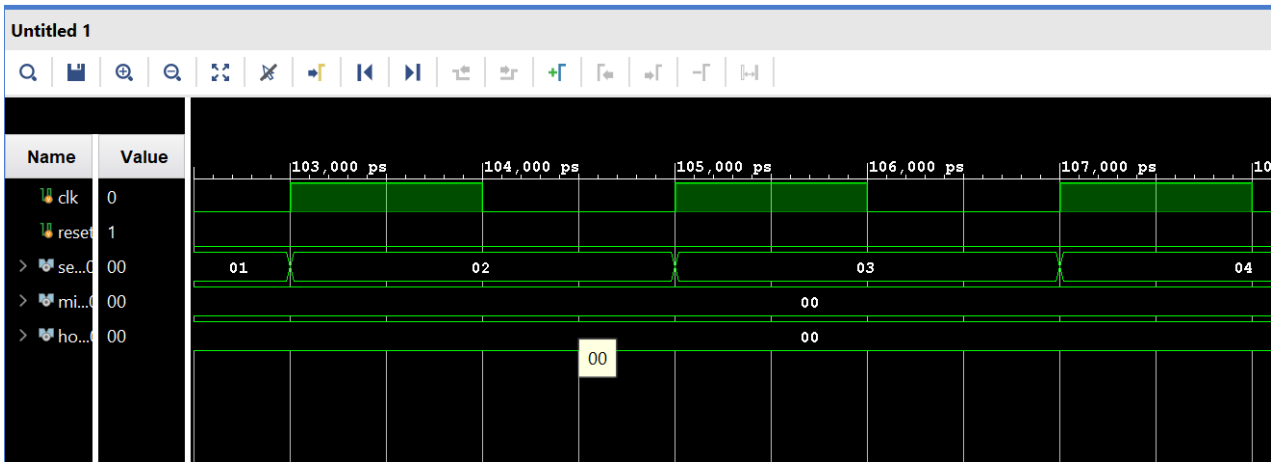
```
module Digital_Clock (
 input clk,reset,
 output [5:0] seconds,[5:0] minutes,[4:0] hours);
 reg [5:0] seconds;
 reg [5:0] minutes;
 reg [4:0] hours;
 always @(posedge clk or posedge reset)
  if (reset==1'b1) begin
    seconds<=0;
    minutes<=0;
    hours<=0;
  end
 else if (clk==1) begin
  seconds=seconds+1;
  if (seconds==60) begin
    seconds<=0;
    minutes=minutes+1;
    if(minutes==60) begin
      seconds<=0;
      minutes<=0;
      hours=hours+1;
      if(hours==24) begin
        seconds<=0;
        minutes<=0;
        hours<=0;
      end
    end
    end
```

```
end
end module
```

TestBench Code:-

```
module tb_clock;
   reg clk;
   reg reset;
   wire [5:0] seconds;
   wire [5:0] minutes;
   wire [4:0] hours;
   Digital_Clock uut (
     .clk(clk),
       .reset(reset),
       .seconds(seconds),
       .minutes(minutes),
       .hours(hours)
   );
   initial clk = 0;
   always #1 clk = ~clk;
   initial begin
      reset = 1;
      #100;
      reset = 0;
      end
      initial begin
      #8543986;
      $display("%0d:%0d:%0d",hours,minutes,seconds);
      $finish();
      end
   endmodule
```


clk
reset
minutes[5:0]
seconds[5:0]
hours[4:0]
RTL_ADD
RTL_EQ
RTL_MUX
RTL_REG_ASYNC


Untitled 1
Name
Value
clk
0
reset
1
00
00
00
103,000 ps
104,000 ps
105,000 ps
106,000 ps
107,000 ps
01
02
03
04
00
00
00