RDA8955L Datasheet

GSM 850/900/1800/1900 Quad-Band

SOC Processor

Preliminary

Product Specification

Revision 1.0.2

Content

1. Product Description

1.1 Overview

RDA8955L is a high performance, highly integrated system-on-chip solution for low cost, low power, GSM/GPRS application.

Integrating all essential electronic components, including baseband, quad band RF transceiver, power management onto a single system on chip.

Built around a cost effective 32-bit XCPU RISC core running at up to 312MHz with 4k of Instruction cache and 4k of Data cache, RDA8955L offers plenty of processing power for multimedia applications. A high-performance proprietary 16/32-bit digital signal processing engine can further improve overall performance and user experience when performing complex multimedia tasks.

It is also packed with impressive connectivity for easy scalability of the system, allowing glue less interfaces to camera and multimedia companion chips, SDMMC Memory Cards and SPI devices, LCD modules and USB (slave, full speed).

RDA8955L is GPRS Class 12 enabled, and supports Full Rate (FR), Half Rate (HR), Enhanced Full Rate (EFR) voice coders. It also supports simultaneous dual network operation and integrates a SIM controller with integrated level shifters that can support two SIM cards.

It is available in a small footprint, fine pitch, 7.5 X7.0 TFBGA package.

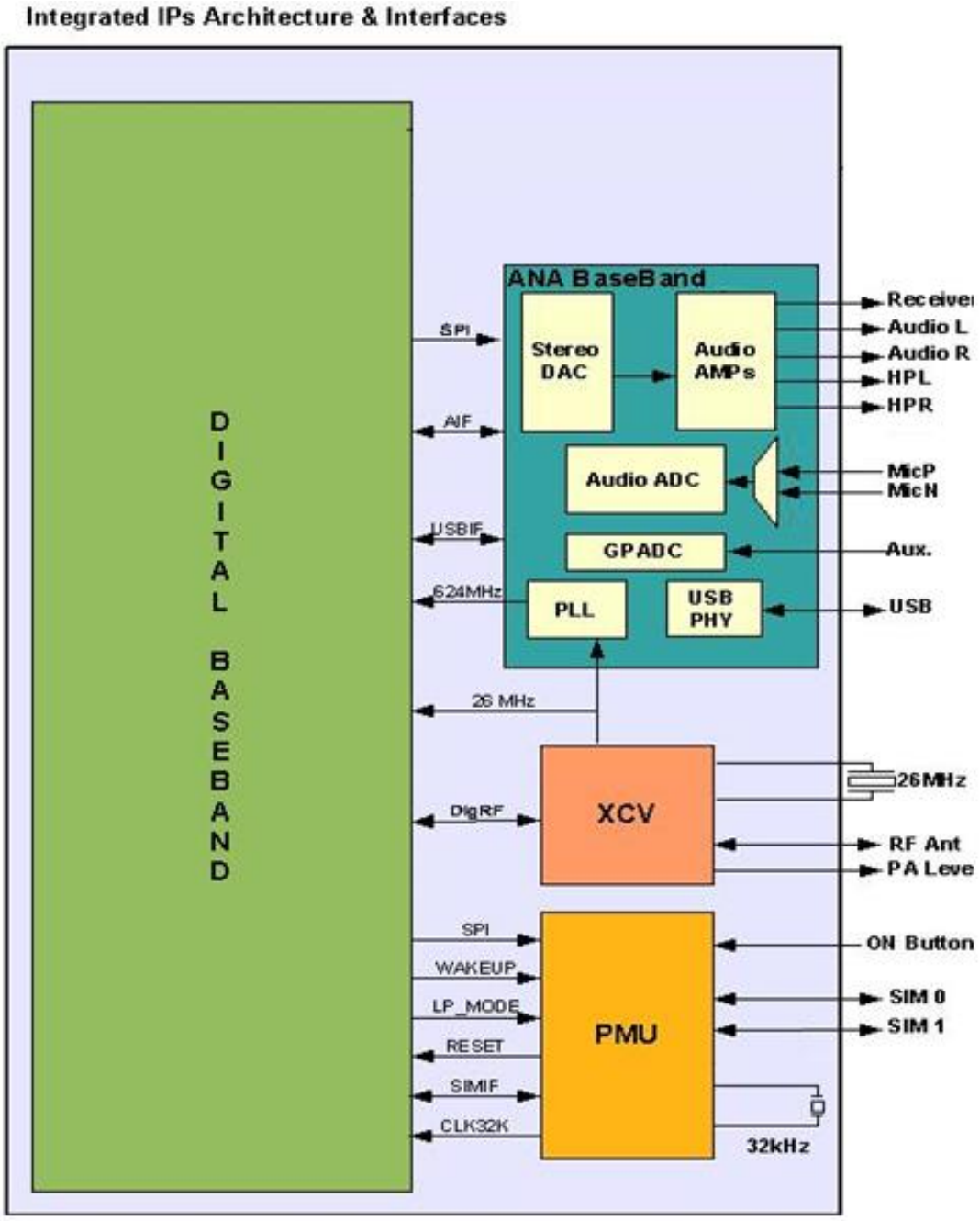
1.2 Features

- **General**
  - Integrated power management unit, base-band, GSM transceiver, and audio module
- **MCU subsystem**
  - RDA RISC Core
  - 4 kByte Instruction Cache
  - 4 kByte Data Cache with write back policy
  - High-performance multi-layer AHB bus
- **User Interface and Connectivity**
  - 5-row x 5-column keypad controller with hardware scanner
  - Pulse Width Modulator
  - Up to 37 GPIOs with interrupt function

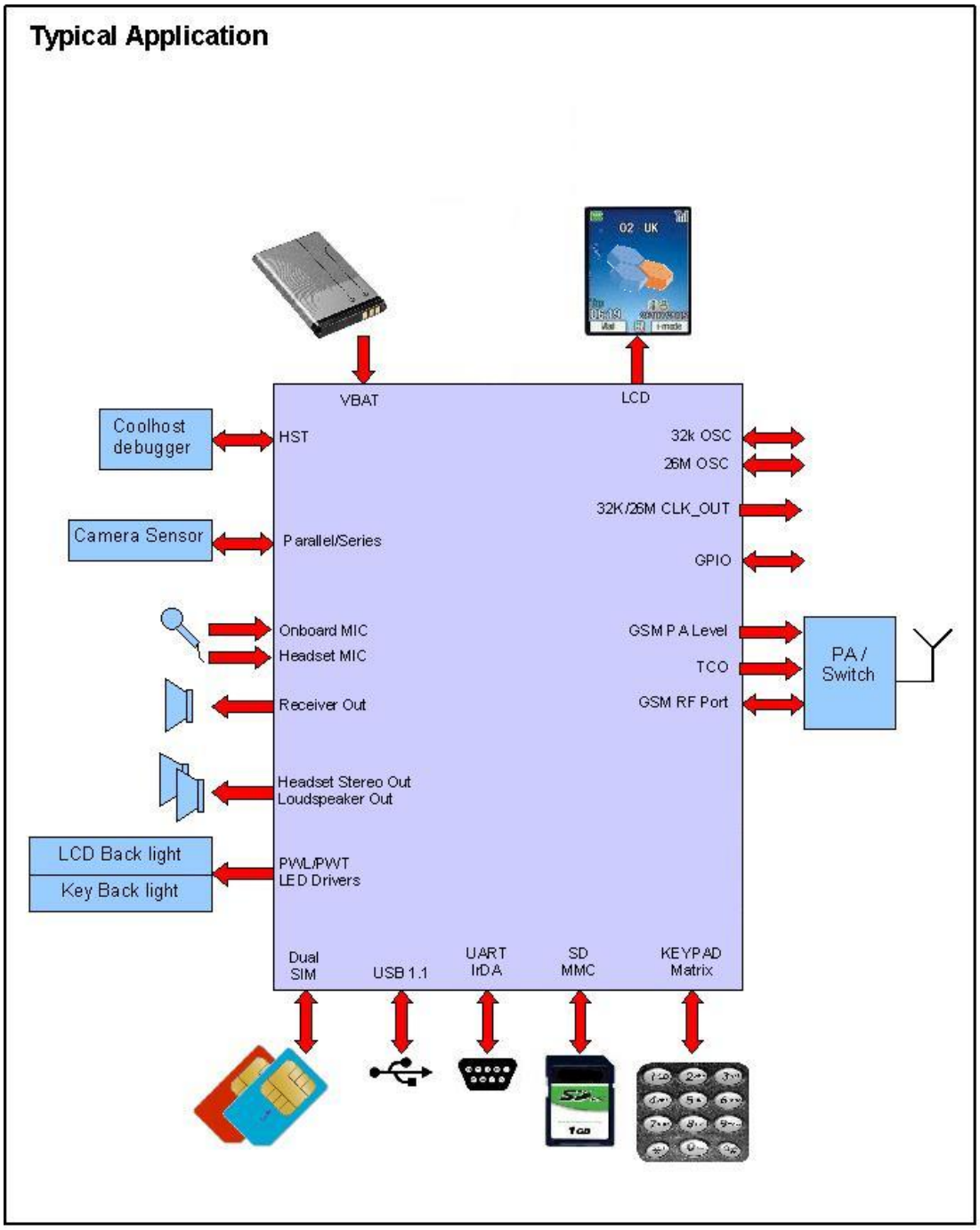
- Calendar (Real Time Clock) with alarm
- USB 1.1 device interface
- Two (2) UART interface
- Two (2) SPI interface
- Three (3) I2C interface
- One (1) SDMMC controller
- Two (2) GPADC, 10bits

- **Memory Interface**
  - Integrated 32Mb 1.8V SPI NOR Flash
  - Integrated 32Mb 1.8V DDR PSRAM
- **GSM/GPRS**
  - Dual single-ended LNAs support quad band receiver
  - Fully integrated channel filter
  - High dynamic range ADC
  - Transmitter support quad band
  - Programmable fractional-N synthesizer
  - On die wide range VCO and integrated loop filter
  - Fast settling time suitable for multi-slot GPRS applications
  - Low power mode support 32KHz crystal removal
  - GPRS Class 12
  - Support HR/FR/EFR voice codec
- **Audio**
  - 2 channels voice ADC, 8kHz, 13 bits/sample for headset and on-board microphone
  - Voice DAC, 8kHz, 13 bits/sample for receiver
  - High fidelity Stereo DAC, up to 48kHz, 16 bits per sample
  - Stereo Audio speaker driver
- **Power Management**
  - Li-ion battery charger
  - Complete integrated DC-DC and LDOs solution deriving from VBAT
  - Flexible I/O voltage
  - 4 open-drain output switches to supply/control the LED
  - LDO type vibrator
  - Internal 32KHz OSC
- **Debug**
  - Host debug interface allowing non-intrusive in depth investigation
  - GDB debugger
  - Execution logger and profiling through debug port
  - High level text based debugging using Host debug or USB
- **Package**
  - 7.5mm x 7mm, TFBGA package
  - 0,5mm pitch

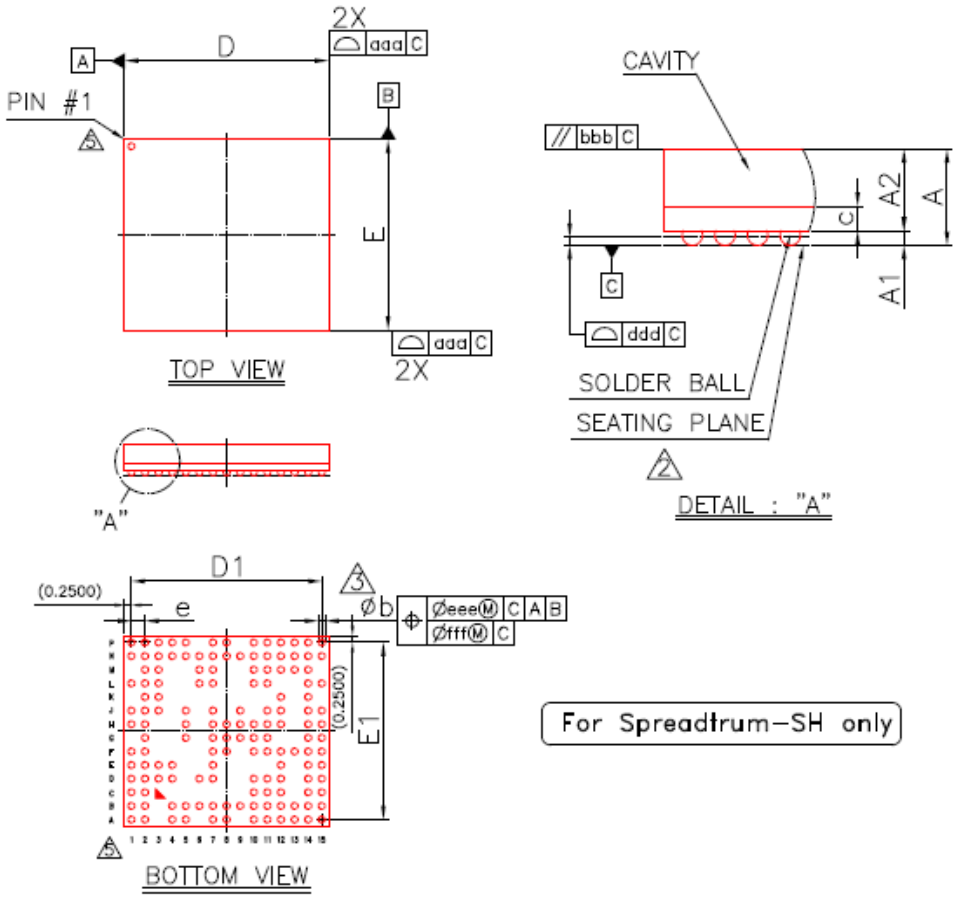
1.3 Functional Block Diagram



1.4 Application



1.5 Package Outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.0690	1.1400	1.2110	0.0421	0.0449	0.0477
A1	0.1300	0.1800	0.2300	0.0051	0.0071	0.0091
A2	0.9100	0.9600	1.0100	0.0358	0.0378	0.0398
c	0.2200	0.2600	0.3000	0.0087	0.0102	0.0118
D	7.4000	7.5000	7.6000	0.2913	0.2953	0.2992
E	6.9000	7.0000	7.1000	0.2717	0.2756	0.2795
D1	---	7.0000	---	---	0.2756	---
E1	---	6.5000	---	---	0.2559	---
e	---	0.5000	---	---	0.0197	---
b	0.2000	0.2500	0.3000	0.0079	0.0098	0.0118
aaa	0.1500			0.0059		
bbb	0.2000			0.0079		
ddd	0.0800			0.0031		
eee	0.1500			0.0059		
fff	0.0500			0.0020		
MD/ME	15 / 14					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

2. Package Pin Out

2.1 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	SW_GND	SW_BUCK		VBAT_PMU	VBAT_PMU		AU_LSL_N	AU_LSL_P		POWERKEY	V_MMC	V_CAM	GPIO_23	GPIO_22	GPIO_19	A
B	SW_GND	SW_BUCK		VBAT_PMU	VBAT_PMU	V_MEM	V_SPIMEM	GPADC_IN_0	GPADC_IN_1	SSD_CLK	SSD_CMD	GPIO_24	GPIO_21	GPIO_20	AVDD_2V4	B
C	V_ASW	PROG_EFUSE								SDAT_0	SDAT_2	RESETB_TEST		XVR_BS2	XVR_BS1	C
D	LED1	LED2	AC_R	GDRV		SPK_GND	SPK_GND			SDAT_1	SDAT_3	ANA_TEST_EN		XVR_BS0	PAON	D
E	V_RTC	V_BAT_RTC	VBAT_SENSE	IS_CHG			V_CORE					TST_H		RAMPOUT	RF_OUT_H	E
F	KP_LED_B	KP_LED_R					V_CORE	CORE_GND		CORE_GND	CORE_GND	XVR_GND	XVR_GND	XVR_GND	RF_OUT_L	F
G		KP_LED_G			V_VIB		PMU_GND	CORE_GND	CORE_GND	CORE_GND	CORE_GND			XVR_GND	RF_IN_L	G
H	V_LCD	V_USB			GPIO_15		PMU_GND	CORE_GND	CORE_GND	CORE_GND	CORE_GND	QN		XVR_GND	RF_IN_H	H
J	GPIO_14	GPIO_17	GPIO_18		GPIO_16		IO_GND		CORE_GND		CORE_GND	QP		IP	XVR_GND	J
K		GPIO_27	GPIO_25									IN		GPIO_0		K
L	GPIO_29	GPIO_26	GPIO_28			GPIO_33	GPIO_34			SIM_DIO_1	BBPLL_TEST			GPIO_1	GPIO_2	L
M		FM_GND	GPIO_30			GPIO_32	GPIO_31			SIM_CLK_0	SIM_CLK_1	GPIO_4	AUXCLK_OUT	GPIO_3		M
N	NC1	NC2	AU_MIC_P	AU_AUXMIC_P	AU_GND	V_MIC	AU_RCV_N	USB_DM	SIM_DIO_0	SIM_RST_0	SIM_RST_1	HST_TXD	GPIO_5	GPIO_7	XVR_XTAL1	N
P	V_ANA	AU_MIC_N	AU_AUXMIC_N	AU_HPL	AU_HPR		AU_RCV_P	USB_DP		V_SIM_0	V_SIM_1	HST_RXD	GPIO_6	V_PAD	XVR_XTAL2	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

2.2 Pin Definition and Function

PIN NO.	PIN Name	Power Domain	Type	Description
K14	GPIO_0	V_PAD	I/O	General purpose input /output
L14	GPIO_1	V_PAD	I/O	General purpose input /output
L15	GPIO_2	V_PAD	I/O	General purpose input /output
M14	GPIO_3	V_PAD	I/O	General purpose input /output
M12	GPIO_4	V_PAD	I/O	General purpose input /output
N13	GPIO_5	V_PAD	I/O	General purpose input /output
P13	GPIO_6	V_PAD	I/O	General purpose input /output
N14	GPIO_7	V_PAD	I/O	General purpose input /output
K3	GPIO_25	V_PAD	I/O	General purpose input /output
L2	GPIO_26	V_PAD	I/O	General purpose input /output
K3	GPIO_27	V_PAD	I/O	General purpose input /output
L3	GPIO_28	V_PAD	I/O	General purpose input /output
L1	GPIO_29	V_PAD	I/O	General purpose input /output
M3	GPIO_30	V_PAD	I/O	General purpose input /output
M7	GPIO_31	V_PAD	I/O	General purpose input /output
M6	GPIO_32	V_PAD	I/O	General purpose input /output
L6	GPIO_33	V_PAD	I/O	General purpose input /output
L7	GPIO_34	V_PAD	I/O	General purpose input /output

PIN NO.	PIN Name	Power Domain	Type	Description
B10	SSD_CLK	V_MMC	I/O	SD serial clock
B11	SSD_CMD	V_MMC	I/O	SD command output
C10	SDAT_0	V_MMC	I/O	SD serial data IO
D10	SDAT_1	V_MMC	I/O	SD serial data IO
C11	SDAT_2	V_MMC	I/O	SD serial data IO
D11	SDAT_3	V_MMC	I/O	SD serial data IO
J1	GPIO_14	V_LCD	I/O	General purpose input /output
H5	GPIO_15	V_LCD	I/O	General purpose input /output
J5	GPIO_16	V_LCD	I/O	General purpose input /output
J2	GPIO_17	V_LCD	I/O	General purpose input /output
J3	GPIO_18	V_LCD	I/O	General purpose input /output
A15	GPIO_19	V_CAM	I/O	General purpose input /output
B14	GPIO_20	V_CAM	I/O	General purpose input /output
B13	GPIO_21	V_CAM	I/O	General purpose input /output
A14	GPIO_22	V_CAM	I/O	General purpose input /output
A13	GPIO_23	V_CAM	I/O	General purpose input /output
B12	GPIO_24	V_CAM	I/O	General purpose input /output
P12	HOST_RXD	V_PAD	I	Debug port
N12	HOST_TXD	V_PAD	I/O	Debug port
N8	USB_DM	V_USB	I/O	D- data input/output
P8	USB_DP	V_USB	I/O	D+ data input/output
C12	RESETB_TEST	V_PAD	I	Inner test pin
E12	TST_H	V_PAD	I	Inner test pin
D12	ANA_TSET_EN	V_PAD	I	Inner test pin

PIN NO.	Ball Name.	Power Domain	Type	Describtion
J12	QP	AVDD2V4	I/O	Inner test pin
H12	QN	AVDD2V4	I/O	Inner test pin
K12	IN	AVDD2V4	I/O	Inner test pin
J14	IP	AVDD2V4	I/O	Inner test pin
N1	NC	N/A	N/A	NC
N2	NC	N/A	N/A	NC
N4	AU_AUXMIC_P	V_ANA	I	MIC input
P3	AU_AUXMIC_N	V_ANA	I	MIC input
N3	AU_MIC_P	V_ANA	I	AUX MIC input
P2	AU_MIC_N	V_ANA	I	AUX MIC input
P4	AU_HPL	V_ANA	O	Audio head phone output (L channel)
P5	AU_HPR	V_ANA	O	Audio head phone output (R channel)
P7	AU_RCV_P	V_ANA	O	Audio receiver output
N7	AU_RCV_N	V_ANA	O	Audio receiver output
A8	AU_LSL_P	V_BAT	O	Audio speaker output
A7	AU_LSL_N	V_BAT	O	Audio speaker output
L11	BBPLL_TEST	AVDD2V4	O	LDO output for SIM1
P11	V_SIM_1	SIM1	O	LDO output for SIM1
N11	SIM1_RST_1	SIM1	O	SIM1 card reset output
M11	SIM1_CLK_1	SIM1	O	SIM1 card clock output
L10	SIM1_DIO_1	SIM1	I/O	SIM1 data input/outputs
P10	V_SIM_0	SIM0	O	LDO output for SIM0
N10	SIM0_RST_0	SIM0	O	SIM0 card reset output
M10	SIM0_CLK_0	SIM0	O	SIM0 card clock output
N9	SIM0_DIO_0	SIM0	I/O	SIM0 data input/outputs

PIN NO.	PIN Name	Power Domain	Type	Description
B8	GP_ADC_IN_0		I	AUX ADC input 0
B9	GP_ADC_IN_1		I	AUX ADC input 1
D1	LED1		O	LED driver
D2	LED2		O	LED driver
G2	KP_LED_G		O	LED driver
F1	KP_LED_B		O	LED driver
F2	KP_LED_R		O	LED driver
A2,B2	SW_BUCK		O	DCDC output
C1	V_ASW		O	LDO output for ASW
C2	PROG_EFUSE		I	Inner test pin
D3	AC_R		I	Connecting to the Source(S) of the charger device
D4	GDRV		O	Connecting to the gate(G) of the charger device
E1	V_RTC		O	LDO output for RTC
E2	V_BAT_RTC		O	LDO output for BAT RTC
E3	VBAT_SENSE		I	VBAT sensing
A4,A5,B4,B5	VBAT_PMU		I	VBAT/Power input
E4	IS_CHG		I	Connecting to the cathode(K) of the charger device
E7,F7	V_CORE		I	Power input for digital circuit, from DCDC output
P1	V_ANA		O	LDO output for ANA
B7	V_SPIMEM		O	LDO output for nor flash
B6	V_MEM		O	LDO output for pSRAM
A12	V_CAM		O	LDO output for CAM
H1	V_LCD		O	LDO output for LCD
A11	V_MMC		O	LDO output for MMC
G5	V_VIB		O	LDO output for VIB
H2	V_USB		O	LDO output for inner USB circuit
N6	V_MIC		O	LDO output for MIC

PIN NO.	PIN Name	Power Domain	Type	Description
A10	POWKEY		I	Power key
P14	V_PAD		O	LDO output for PAD
E14	RAMPOUT		O	Ramping output
F15	RF_OUT_L		O	GSM RF output low band
E15	RF_OUT_H		O	GSM RF output high band
G15	RF_IN_L		I	GSM RF input low band
H15	RF_IN_H		I	GSM RF input high band
D15	PAON		O	RF hard-wire control bus bit
C14	XVR_BS2		O	RF hard-wire control bus bit
C15	XVR_BS1		O	RF hard-wire control bus bit
D14	XVR_BS0		O	RF hard-wire control bus bit
M13	AUXCLK_OUT		O	AUX 26MHz clock output
N15	XVR_XTAL1		I/O	Input 1 for DCXO crystal
P15	XVR_XTAL2		I/O	Input 2 for DCXO crystal
B15	AVDD_2V4		O	LDO output for GSM Transceiver
F8,F10,F11,G8,G9,G10,G11, H8,H9,H10,H11,J9,J11	CORE_GND			Connect to GND net
J7	IO_GND			Connect to GND net
H7,G7	PMU_GND			Connect to GND net
A1,B1	SW_GND			Connect to GND net
N5	AU_GND			Connect to GND net
D6,D7	SPK_GND			Connect to GND net
M2	FM_GND			Connect to GND net
F12,F13,F14,G14,H14,J14	XVR_GND			Connect to GND net

3. Electrical Specification

Table 1. Absolute Rating

Symbol	Description	MIN	TYP	MAX	Unit
VBAT	Power supply input			5	V
DC Charger	For charger circuit			7	V

Table 2. Operating Rating

Symbol	Description	Min	Typ	Max	Unit
VBAT	Power supply Input	3.4	3.8	4.2	V

Table 3. Temperature Characteristics

Parameter	*Min*	*Typ*	*Max*	*Unit*
Work Temperature	-20	25	70	°C
Storage Temperature	-40	/	125	°C

Table 4. RF Characteristics

(Vbatt = 3.8 V, T_A = 27 °C)

TX

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
fout	RF output frequency	GSM850 band	824		849	MHz
		GSM900 band	880		915	MHz
		DCS1800 band	1710		1785	MHz

		PCS1900 band	1850		1910	MHz
Pout	TX Output Power	GSM850 band		6		dBm
		GSM900 band		6		dBm
		DCS1800 band		5		dBm
		PCS1900 band		5		dBm
PE_rms	RMS Phase Error	GSM850 band			3	Degree
		GSM900 band			3	Degree
		DCS1800 band			4	Degree
		PCS1900 band			4	Degree
PE_peak	Peak Phase Error	GSM850 band			10	Degree
		GSM900 band			10	Degree
		DCS1800 band			12	Degree
		PCS1900 band			12	Degree
MASK	Output spectrum(200kHz)			-32		dBc
	Output spectrum(400kHz)			-62		dBc
	Output spectrum(1.8MHz)			-65		dBc

RX

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN}	RF input frequency	GSM850 band	869		894	MHz
		GSM900 band	925		960	MHz
		DCS1800 band	1805		1880	MHz
		PCS1900 band	1930		1990	MHz
Srx	RX sensitivity	GSM850 band		-109	-104	dBm
		GSM900 band		-109	-104	dBm
		DCS1800 band		-108	-104	dBm
		PCS1900 band		-108	-104	dBm
ACS200	±200k Block	GSM850 band	-9			dBc
		GSM900 band	-9			dBc
		DCS1800 band	-9			dBc
		PCS1900 band	-9			dBc
ACS400	±400k Block	GSM850 band	-41			dBc
		GSM900 band	-41			dBc
		DCS1800 band	-41			dBc
		PCS1900 band	-41			dBc

Table 5. Current Consumption

(Vbatt = 3.8 V, T_A = 27 °C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_idle_avg	average idle current	UART all on		9	10	mA
I_sleep_avg	average sleep current	UART all off		1.5	2	mA

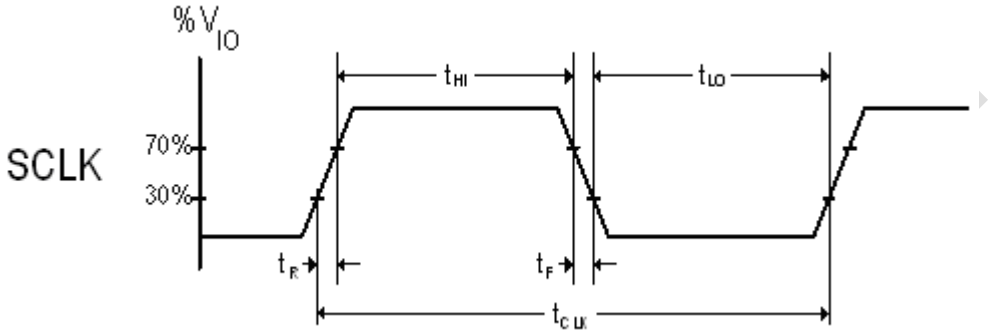
Table 6. Digital IO DC Characteristics

Symbol	*Description*	*Min.(V)*	*Typical(V)*	*Max.(V)*
VDD	All of power for digital usage	VDD-0.2	1.8/2.8	VDD+0.2
VIL	CMOS Low Level Input Voltage	0	-	0.3*VDD
VIH	CMOS High Level Input Voltage	0.7*VDD	-	VDD
VTH	CMOS Threshold Voltage	-	0.5*VDD	-

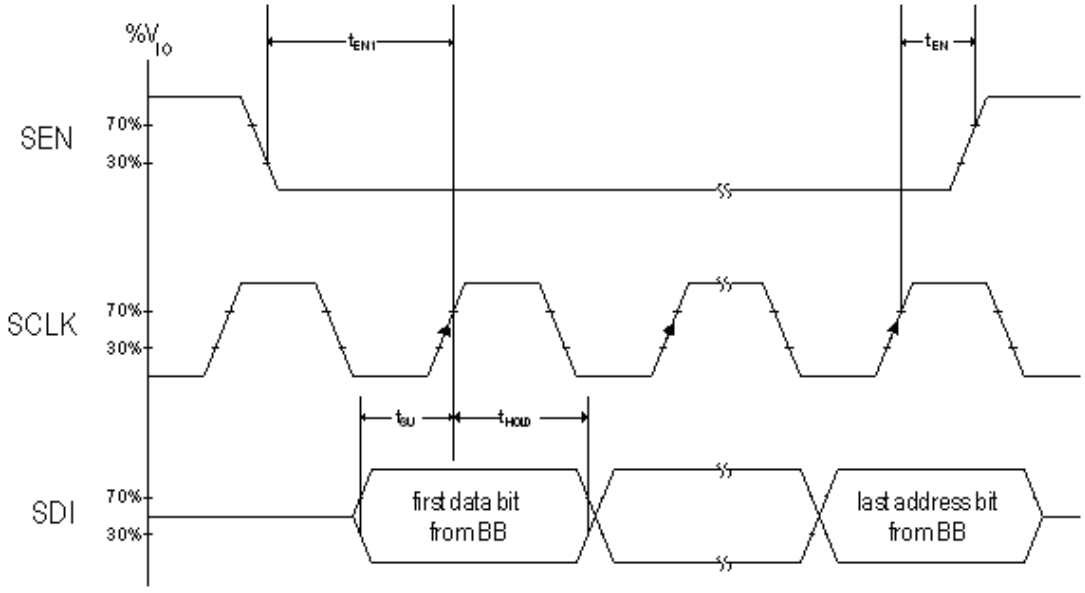
Table 7. Digital IO AC Characteristics (SPI Interface Timing)

Symbol	*Description*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{CLK}	SCLK Cycle Time	35	-	-	ns
t_R	SCLK Rise Time	-	-	50	ns
t_F	SCLK Fall Time	-	-	50	ns
t_{HI}	SCLK High Time	10	-	-	ns
t_{LO}	SCLK Low Time	10	-	-	ns
t_{SU}	SDI Setup Time to SCLK↑	15	-	-	ns
t_{HOLD}	SDI Hold Time to SCLK↑	10	-	-	ns
t_{EN1}	SEN↓ to SCLK↑ Delay Time	10	-	-	ns

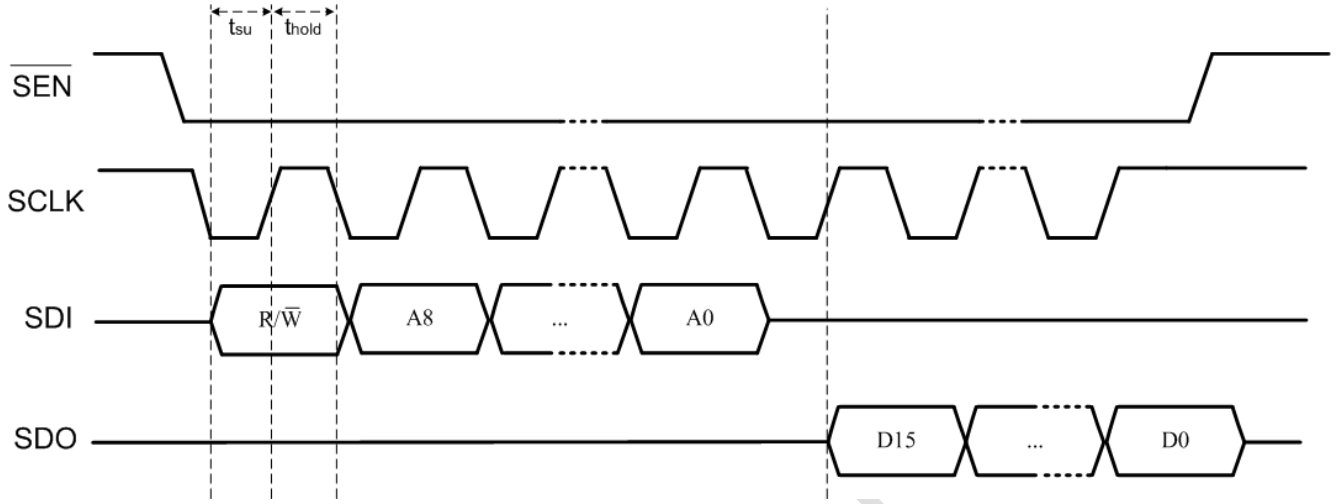
Symbol	*Description*	*Min.*	*Typ.*	*Max.*	*Unit*
t_{EN2}	SCLK↑ to SEN↑ Delay Time	12	-	-	ns
t_{EN3}	SEN↑ to SCLK↑ Delay Time	12	-	-	ns
t_W	SEN Pulse Width	10	-	-	ns
t_{CA}	SCLK↑ to SDO Delay Time	-	-	27	ns
C_{load}	Digital Input Pin Capacitance	-	-	5	pF
f_{REF}	Crystal Reference Frequency	-	26	-	MHz



SCLK Timing Diagram



SPI Write Timing Diagram



SPI Read Timing Diagram

Table 8. DCDC Characteristics

The brief specifications of the DCDC

Parameters	Conditions	Min	Typical	Max	Unit
Output Voltage	VBAT=4.2V Active mode	0.75	1.2	1.48	V
	VBAT=4.2V LP mode	0.91	1.427	1.75	V

Table 9. LDOs Characteristics

Low Drop-out Linear Regulators(LDO)

All LDOs have their own power down logic. Their main specifications are blow.

Parameter	Condition	Min	Typical	Max		Unit
V_A24						
Status after reset	On					
Output Voltage	Va24_vsel=1	1.88	2.05	2.45		V
	Va24_vsel=0	2.13	2.35	2.91		V
Output Current capacity	Va24_vsel=1			500		mA
	Va24_vsel=0			500		mA
V_PAD						
Status after reset	On					
Output Voltage	Vio_vsel=1	1.74	1.81	1.88		V
	Vio_vsel=0	2.78	1.81	2.98		V
Output Current	Vio_vsel=1	110				mA

capacity	Vio_vsel=0	140				mA
V_ANA						
Status after reset	On					
Output Voltage		2.25	2.48	2.75		V
Output Current capacity	VBAT=4.2v			250		mA
V_SPIMEM						
Status after reset	On					
Output Voltage		1.71	1.82	1.93		V
Output Current capacity	VBAT=4.2v			240		mA
V_MEM						
Status after reset	On					
Output Voltage		1.72	1.82	1.94		V
Output Current capacity	VBAT=4.2v			220		mA
V_CAM						
Status after reset	On					
Output Voltage	Vcam_vsel=1	1.71	1.82	1.93		V
	Vcam_vsel=0	2.53	2.81	3.10		V
Output Current capacity	Vcam_vsel=1			200		mA
	Vcam_vsel=0			220		mA
V_MMC						
Status after reset	Off					
Output Voltage	Vmmc_vsel=1	1.80	1.92	2.04		V
	Vmmc_vsel=0	2.95	3.20	3.29		V
Output Current capacity	Vmmc_vse=1			210		mA
	Vmmc_vsel=0			250		mA
V_LCD						
Status after reset	Off					
Output Voltage	Vlcd_vsel=1	1.72	1.82	1.94		V
	Vlcd_vsel=0	2.54	2.82	3.12		V
Output Current capacity	Vlcd_vse=1			200		mA
	Vlcd_vsel=0			260		mA
V_ASW						
Status after reset	Off					
Output Voltage	Vasw_vsel=1	1.74	1.82	1.88		V
	Vasw_vsel=0	2.60	2.80	2.98		V
Output Current capacity	Vasw_vse=1			80		mA
	Vasw_vsel=0			140		mA
V_SIM1						
Status after reset	Off					
Output Voltage	Vsim1_vsel=1	1.73	1.83	1.88		V

	Vsim1_vsel=0	2.59	2.78	2.96		V
Output Current capacity	Vsim1_vse=1			110		mA
	Vsim1_vsel=0			150		mA
V_SIM2						
Status after reset	Off					
Output Voltage	Vsim2_vsel=1	1.74	1.82	1.88		V
	Vsim2_vsel=0	2.60	2.79	2.98		V
Output Current capacity	Vsim2_vse=1			110		mA
	Vsim2_vsel=0			150		mA
V_VIB						
Status after reset	Off					
Output Voltage	VBAT=4.2v	2.94	3.18	3.40		V
Output Current capacity	VBAT=4.2v			430		mA
	VBAT=3.4v			170		mA
V_USB						
Status after reset	On					
Output Voltage		2.92	3.3	3.68		V
Output Current capacity	VBAT=4.2v			320		mA
	VBAT=3.4v			220		mA
V_backup						
Status after reset	On					
Output Voltage		2.66	2.8	2.92		V
Output Current capacity	VBAT=4.2v			1.9		mA
	VBAT=3.4v			1.6		mA
V_RTC						
Status after reset	On					
Output Voltage		1.32	1.50	1.62		V
Output Current capacity	VBAT=4.2v			1.3		mA
V_MIC						
Status after reset	Off					
Output Voltage		1.62	1.86	2.0		V
Output Current capacity	VBAT=4.2v			0.5		mA

4. Change List

Rev	Date	Author	Change Description
1.0.0	2017-07-01	Miao Xian	Original draft
1.0.1	2017-09-09	Miao Xian	Add DCDC and LDOs Characteristics
1.0.2	2017-09-09	Miao Xian	Fix VMMC output voltage in the LDOs Characteristics