ALU Verilog Code

```
module ALU (
    input [3:0] A, B,
    input [2:0] ALU_Sel,
    output reg [3:0] ALU_Out,
    output reg Zero
);
always @(*) begin
    case (ALU_Sel)
        3'b000: ALU_Out = A + B;
        3'b001: ALU_Out = A - B;
        3'b010: ALU_Out = A & B;
        3'b011: ALU_Out = A | B;
        3'b100: ALU_Out = ~A;
        default: ALU_Out = 4'b0000;
    endcase
    Zero = (ALU_Out == 4'b0000) ? 1'b1 : 1'b0;
end
endmodule
```