FIR Filter Verilog Code

```
module FIR_Filter(input clk, rst, input signed [7:0] x_in,
                  output reg signed [15:0] y_out);
    reg signed [7:0] h[0:3] = '{8'd1, 8'd2, 8'd3, 8'd4};
    reg signed [7:0] x[0:3];
    integer i;
    always @(posedge clk) begin
        if (rst) begin
            for (i = 0; i < 4; i = i + 1)
                x[i] <= 0;
        end else begin
            x[0] <= x_in;
            for (i = 1; i < 4; i = i + 1)
                x[i] <= x[i-1];
            y_out <= h[0]*x[0] + h[1]*x[1] + h[2]*x[2] + h[3]*x[3];
        end
    end
endmodule
```