

EE126Lab 3

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/pipelinecpu0/cik	0														
/pipelinecpu0/rst	0														
/pipelinecpu0/DEBUG_PC	32'h00000034	(00000000)	(00000004)	(00000008)	(0000000C)	(00000010)	(00000014)	(00000018)	(0000001C)	(00000020)	(00000024)	(00000028)	(0000002C)	(00000030)	(00000034)
/pipelinecpu0/DEBUG_PCPUs4_ID	32'h00000034	(00000000)	(00000004)	(00000008)	(0000000C)	(00000010)	(00000014)	(00000018)	(0000001C)	(00000020)	(00000024)	(00000028)	(0000002C)	(00000030)	(00000034)
/pipelinecpu0/DEBUG_PCPUs4_EX	32'h00000030	(00000000)	(00000004)	(00000008)	(0000000C)	(00000010)	(00000014)	(00000018)	(0000001C)	(00000020)	(00000024)	(00000028)	(0000002C)	(00000030)	(00000030)
/pipelinecpu0/DEBUG_PCPUs4_MEM	32'h0000002C	(00000000)	(00000004)	(00000008)	(0000000C)	(00000010)	(00000014)	(00000018)	(0000001C)	(00000020)	(00000024)	(00000028)	(0000002C)	(00000028)	(0000002C)
/pipelinecpu0/DEBUG_PCPUs4_WB	32'h00000028	(00000000)	(00000004)	(00000008)	(0000000C)	(00000010)	(00000014)	(00000018)	(0000001C)	(00000020)	(00000024)	(00000028)	(0000002C)	(00000028)	(00000028)
/pipelinecpu0/DEBUG_MemWrite	0														
/pipelinecpu0/DEBUG_MemWrite_EX	0														
/pipelinecpu0/DEBUG_MemWrite_MEM	0														
/pipelinecpu0/DEBUG_RegWrite	1														
/pipelinecpu0/DEBUG_RegWrite_EX	1														
/pipelinecpu0/DEBUG_RegWrite_MEM	1														
/pipelinecpu0/DEBUG_RegWrite_WB	0														
/pipelinecpu0/DEBUG_Branch	0														
/pipelinecpu0/DEBUG_Jump	0														
/pipelinecpu0/DEBUG_INSTRUCTION	32'hXXXXXXXXXX	(01095020)	(AC0A'0000)	(01095822)	(AC0A'0000)	(AD68'0004)		(02119025)	(00000000)		(AC12000C)	(00000000)			XXXXXXXX
/pipelinecpu0/DEBUG_TMP_REGS	128'h00000000000000000400000000C000000004	(00000008)00000040000000002000000000					(00000008)0000004000000000C000000000		(00000008)0000004000000000C000000004						
/pipelinecpu0/DEBUG_SAVED_REGS	128'hCEA4126C1009AC83DEADBEEF00000000	(CEA4126C1009AC83D00000000000000000000)										CFA4126C1009AC83DEADBEEF00000000			
/pipelinecpu0/DEBUG_MEM_CONTENTS	128'h00000000C000000000000000004DEADBEEF	(00000010)00000020000000000000000004					(00000000)00000020000000000000000004		(0000000C)00000000000000000000000004						(0000000C)00000000
128'h0000000C000000020000000300000004 128'h0000000C00000000000000000300000004															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	The pipeline is reset, all units are set to initial value. It fetches the 1 st instruction. ID of nop makes RegWrite become 1.														
2	The 1 st instruction goes to the ID stage. It is an ADD instruction so the RegWrite goes to 1. It fetches the 2 nd instruction at the meantime.														
3	The 1 st instruction goes to the EX stage. The 2 nd instruction goes to the ID stage. It is a SW instruction so MemWrite goes to 1. It fetches the 3 rd instruction.														
4	The 1 st instruction goes to the MEM stage. The 2 nd instruction goes to the EX. The 3 rd instruction goes to ID stage. It is a SUB instruction so RegWrite goes to 1. It fetches the 4 th instruction at the meantime.														
5	The 1 st instruction goes to the WB stage (finally with its RegWrite_WB is 1). So \$t2 changes to 0xC. The 2 nd instruction goes to MEM stage. But it stores a wrong value due to \$t2 has been updated. The 3 rd instruction goes to the EX stage. The 4 th instruction gets the right value of \$t2. The 5 th instruction is fetched.														
6	The 2 nd instruction changes the value of MEM(0). The 3 rd instruction goes to MEM stage. The 4 th instruction goes to EX stage. The 5 th instruction goes to the ID stage. Got the wrong value cause right value of \$t3 is still in MEM stage. It fetches the 6 th instruction.														
7	The 3 rd instruction goes to WB stage. Write the value of \$t3. The 4 th instruction write good value to DMEM. The 5 th instruction goes the EX stage. The 6 th instruction goes the ID stage. Read a good value from \$t3. It fetches the 7 th instruction.														
8	The 4 th instruction make the right value of \$t2 write to MEM(0). The 5 th instruction with wrong value goes to MEM stage. The 6 th instruction goes the EX stage. The 7 th instruction goes the ID stage. It fetches 8 th nop instruction.														
9	The 5 th instruction writes the wrong value to MEM. The 6 th instruction goes to MEM stage. Will write a good value. The 7 th instruction goes to EX stage. The 8 th instruction goes to ID stage. It fetches the 9 th nop instruction.														
10	The 6 th instruction writes good value to MEM.														

	<p>The 7th instruction goes MEM stage.</p> <p>The 8th instruction nop goes to EX stage.</p> <p>The 9th instruction nop goes to ID stage.</p> <p>The 10th instruction is fetched.</p>
11	<p>The 7th instruction writes good value to \$t2.</p> <p>The 8th instruction nop goes to MEM stage.</p> <p>The 9th instruction nop goes to EX stage.</p> <p>The 10th instruction goes to ID stage. Reads a good value due to 7th instruction has written back.</p> <p>The 11th instruction nop is fetched.</p>
12	<p>The 8th instruction nop goes to WB stage.</p> <p>The 9th instruction nop goes to MEM stage.</p> <p>The 10th instruction goes to EX stage.</p> <p>The 11th instruction nop goes to ID stage.</p> <p>The 12th instruction nop is fetched.</p>
13	<p>The 9th instruction nop goes to WB stage.</p> <p>The 10th instruction goes to MEM stage. Writes a good value of \$s2 to MEM(0xC)</p> <p>The 11th instruction nop goes to EX stage.</p> <p>The 12th instruction nop goes to ID stage.</p> <p>The 13th instruction nop is fetched.</p>
14	<p>The 10th instruction changes the value in MEM.</p> <p>The 11th instruction nop goes to MEM stage.</p> <p>The 12th instruction nop goes to EX stage.</p> <p>The 13th instruction nop goes to ID stage.</p>