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Lab1

EE126
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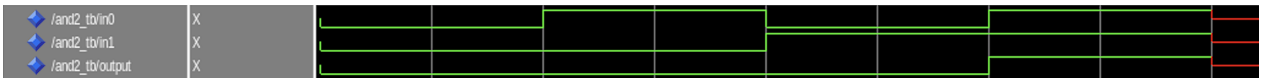
AND2

Realize logical AND of two inputs.

Data-flow: Using logical events occurring on the particular signals.

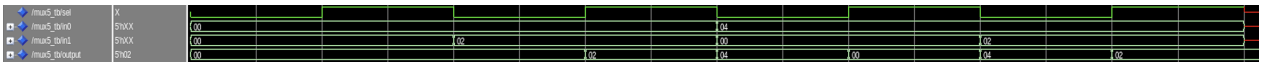


1. The logical result of 0 and 0, is 0.
2. The logical result of 1 and 0, is 0.
3. The logical result of 0 and 1, is 0.
4. The logical result of 1 and 1, is 1.

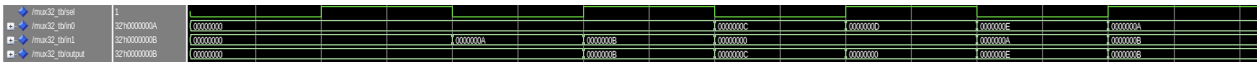
MUX5

Select one of the two input data with 5 bits.

Behavioral: Using if else clauses to executes statements sequentially.



1. The sel is 0, so the output is the data in in0 which is 00.
2. The sel is 1, so the output is the data in in1 which is 00.
3. The sel is 0, so the output is the data in in0 which is 00.
4. The sel is 1, so the output is the data in in1 which is 02.
5. The sel is 0, so the output is the data in in0 which is 04.
6. The sel is 1, so the output is the data in in1 which is 00.
7. The sel is 0, so the output is the data in in0 which is 04.
8. The sel is 1, so the output is the data in in0 which is 02.



MUX32

Select one of the two input data with 32 bits.

Behavioral: Using if else clauses to executes statements sequentially.

1. The sel is 0, so the output is the data in in0 which is 00000000.
2. The sel is 1, so the output is the data in in1 which is 00000000.
3. The sel is 0, so the output is the data in in0 which is 00000000.
4. The sel is 1, so the output is the data in in1 which is 0000000B.
5. The sel is 0, so the output is the data in in0 which is 0000000C.
6. The sel is 1, so the output is the data in in1 which is 00000000.
7. The sel is 0, so the output is the data in in0 which is 0000000E.
8. The sel is 1, so the output is the data in in0 which is 0000000B.

PC

Deliver the data under the control of two other signals.

Behavioral: Using if else clauses to executes statements sequentially.

1. The writeenable is 0 for the first 4 periods. The rst is 0, so the AddressOut remains no signal.
2. The writeenable is 0 for the next 4 periods. The rst is 1, so the AddressOut remains 00000000.
3. The writeenable is 1 for the next 4 periods. The rst is 0, so the AddressOut should be the same as the AddressIn.
4. The writeenable is 1 for the final 4 periods. The rst is 1, so the AddressOut should be 00000000.

SignExtend

Extend the signal from 16 bits to 32 bits.

Data-flow: Using logical events occurring on the particular signals.

1. It extends the 16bits signal to 32bits, when the original data is hex data ABCD, the final data should be 0000ABCD.

ShiftLeft

Logical shift left by 2 bits of the origianl data.

Data-flow: Using logical events occurring on the particular signals.

1. It shifts the data toward left in binary data format. When the hex number is 0000000F, the binary number should be 00000000000000000000000000001111, and the result should be 00000000000000000000000000111100, which is 0000003C in hex.