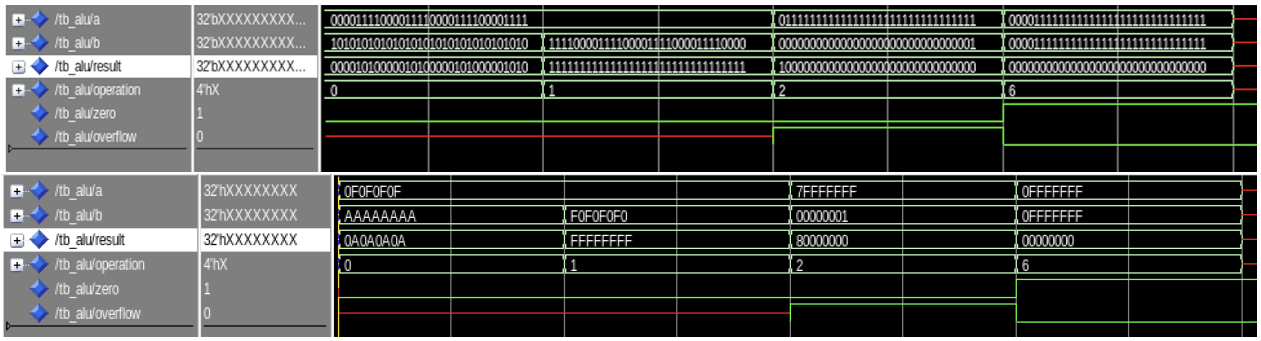
Qinlong Cui
1290554

Lab2

EE126
October 1, 2019

ADD



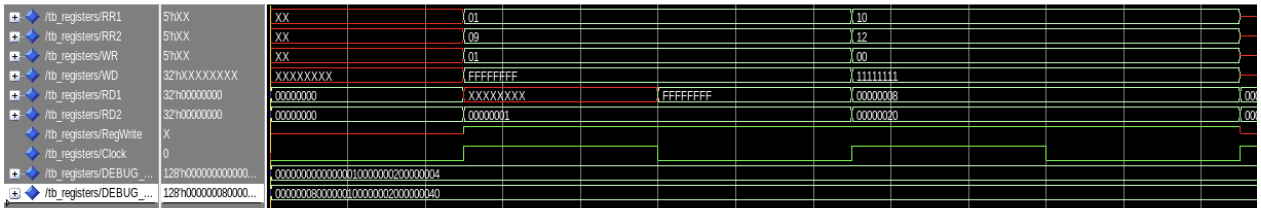
1. AND: two inputs are 0F0F0F0F and AAAAAAAA, the result should be 0A0A0A0A, without any overflow or zero.

2. OR: two inputs are 0F0F0F0F and F0F0F0F0, the result should be FFFFFFFF, without any overflow or zero.

3. ADD: two inputs are 7FFFFFFF and 00000001, the result should be 8000000. It ouverflows, but the result is not zero.

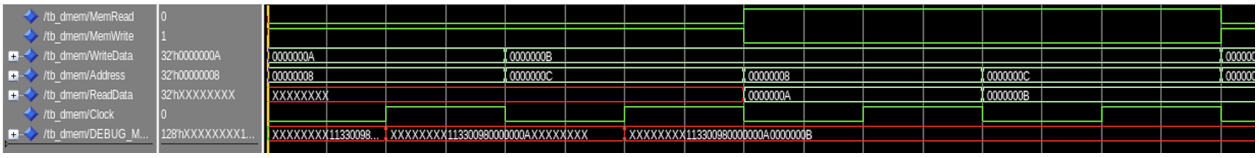
4. Subtract: two inputs are 0FFFFFFF and 0FFFFFFF, the result should be 00000000. The result is zero without overflow.

REGISTERS



1. During the first clock period, we try to write FFFFFFFF to address 00000001, at the beginning of the second period, it succeed.

2. Then we try to write 11111111 to 00000000 at the next period, nothing changes because it is prohibited.



DMEM

1. In the first period, the MemWrite is 1 and MemRead is 0, so it just writes the data to address, 0000000A -¿ 0000008,
2. In the second period, the MemWrite is 1 and MemRead is 0, so it just writes the data to address, 0000000B -¿ 000000C.
3. The next period, it reads out data from 00000008. The result is 0000000A;
4. The next period, it reads out data from 0000000C. The result is 0000000B.

Some of my work were inspired by Ruoxi.