LAB 3

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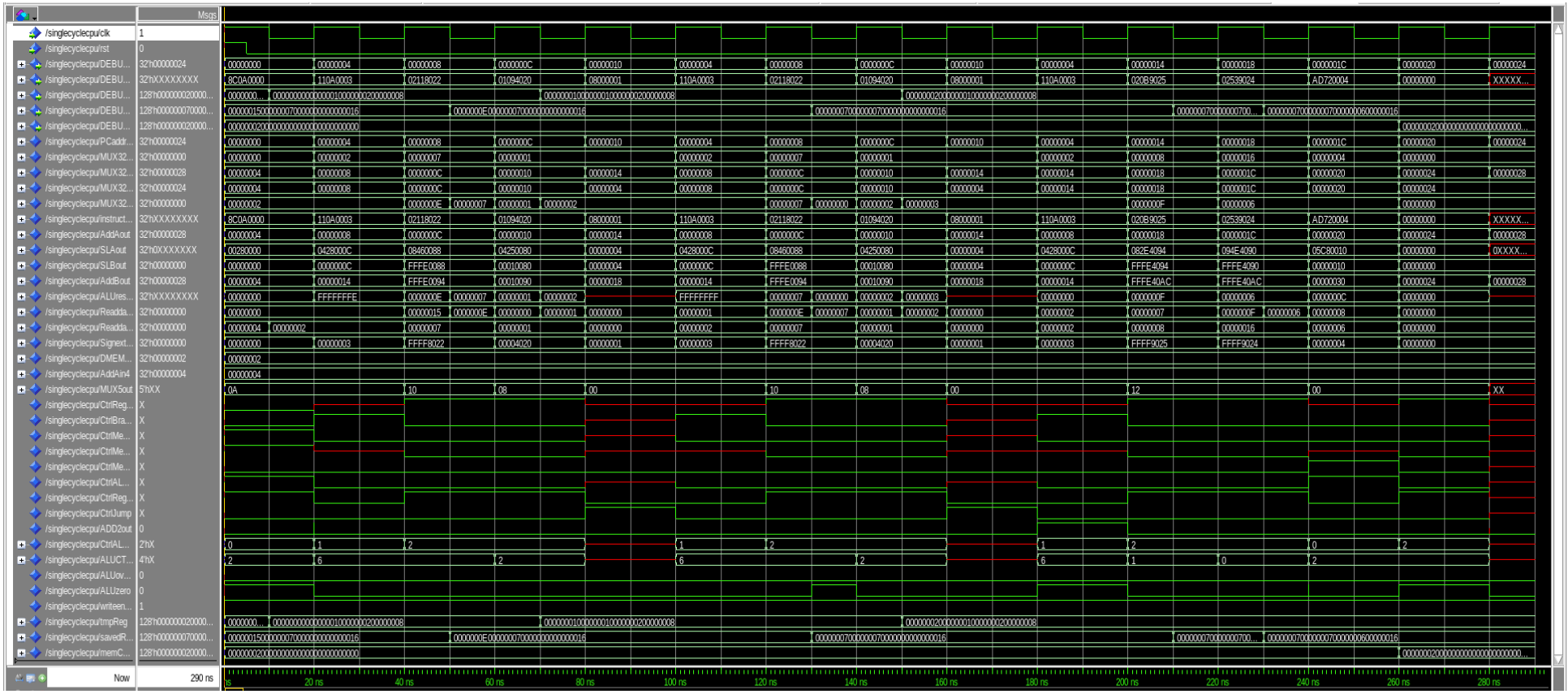

0-10ns: Rest everything. Fetch the first LW instruction, read the 0x0 of DMEM and delivery 0x00000002 to reg, $t2.
10-20ns: Fetch second BEQ instruction, $t0 is now 0x00000000, and $t2 is 0x00000002, thus will not branch.
10-30ns: Fetch the third SUB instruction. $s0 = 0x15 $s1 = 7, thus $s0 = 0xE.
40-50ns: Fetch the fourth ADD instruction. $t0 = 0 $t1 = 1, thus $t0 = 1.
50-60ns: Fetch the fifth J instruction. Jump to L1.
…
180-200ns: Fetch the second BEQ instruction. This time they are equal, branch to L2.
200-220ns: Fetch the sixth OR instruction. $S0 = 7, $t3 = 8. $s2 = 0xF.
220-240ns: Fetch the seventh AND instruction. $s2 = 0xF, $s3 = 22. Thus, $s2 = 6.
240-260ns: Fetch the eighth SW instruction. $s3 = 8,$s2 = 6.Thus, we store 6 to DMEM(0xC).

The result if we change DMEM(0x0) to 15 is 0x4.
(I was greatly inspired and taught by Ruoxi on this Lab)