EE126Lab 3

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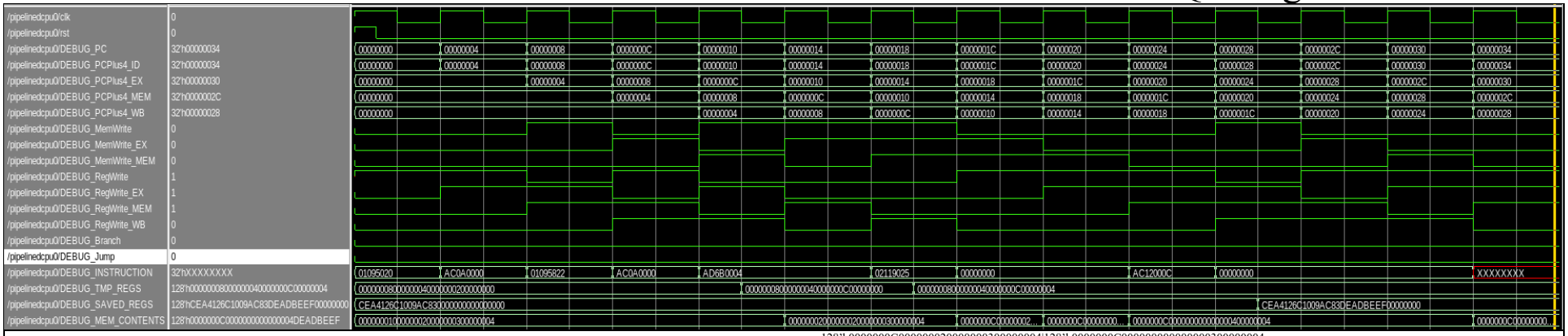

		1	2	3	4	5	6	7	8	9	10	11	12	13	14

1	The pipeline is reset, all units are set to initial value. It fetches the 1st instruction. ID of nop makes RegWrite become 1.
2	The 1st instruction goes to the ID stage. It is an ADD instruction so the RegWrite goes to 1. It fetches the 2nd instruction at the meantime.
3	The 1st instruction goes to the EX stage. The 2nd instruction goes to the ID stage. It is a SW instruction so MemWrite goes to 1. It fetches the 3rd instruction.
4	The 1st instruction goes to the MEM stage. The 2nd instruction goes to the EX. The 3rd instruction goes to ID stage. It is a SUB instruction so RegWrite goes to 1. It fetches the 4th instruction at the meantime.
5	The 1st instruction goes to the WB stage (finally with its RegWrite_WB is 1). So $t2 changes to 0xC. The 2nd instruction goes to MEM stage. But it stores a wrong value due to $t2 has been updated. The 3rd instruction goes to the EX stage. The 4th instruction gets the right value of $t2. The 5th instruction is fetched.
6	The 2nd instruction changes the value of MEM(0). The 3rd instruction goes to MEM stage. The 4th instruction goes to EX stage. The 5th instruction goes to the ID stage. Got the wrong value cause right value of $t3 is still in MEM stage. It fetches the 6th instruction.
7	The 3rd instruction goes to WB stage. Write the value of $t3. The 4th instruction write good value to DMEM. The 5th instruction goes the EX stage. The 6th instruction goes the ID stage. Read a good value from $t3. It fetches the 7th instruction.
8	The 4th instruction make the right value of $t2 write to MEM(0). The 5th instruction with wrong value goes to MEM stage. The 6th instruction goes the EX stage. The 7th instruction goes the ID stage. It fetches 8th nop instruction.
9	The 5th instruction writes the wrong value to MEM. The 6th instruction goes to MEM stage. Will write a good value. The 7th instruction goes to EX stage. The 8th instruction goes to ID stage. It fetches the 9th nop instruction.
10	The 6th instruction writes good value to MEM.

	The 7th instruction goes MEM stage. The 8th instruction nop goes to EX stage. The 9th instruction nop goes to ID stage. The 10th instruction is fetched.
11	The 7th instruction writes good value to $t2. The 8th instruction nop goes to MEM stage. The 9th instruction nop goes to EX stage. The 10th instruction goes to ID stage. Reads a good value due to 7th instruction has written back. The 11th instruction nop is fetched.
12	The 8th instruction nop goes to WB stage. The 9th instruction nop goes to MEM stage. The 10th instruction goes to EX stage. The 11th instruction nop goes to ID stage. The 12th instruction nop is fetched.
13	The 9th instruction nop goes to WB stage. The 10th instruction goes to MEM stage. Writes a good value of $s2 to MEM(0xC) The 11th instruction nop goes to EX stage. The 12th instruction nop goes to ID stage. The 13th instruction nop is fetched.
14	The 10th instruction changes the value in MEM. The 11th instruction nop goes to MEM stage. The 12th instruction nop goes to EX stage. The 13th instruction nop goes to ID stage.