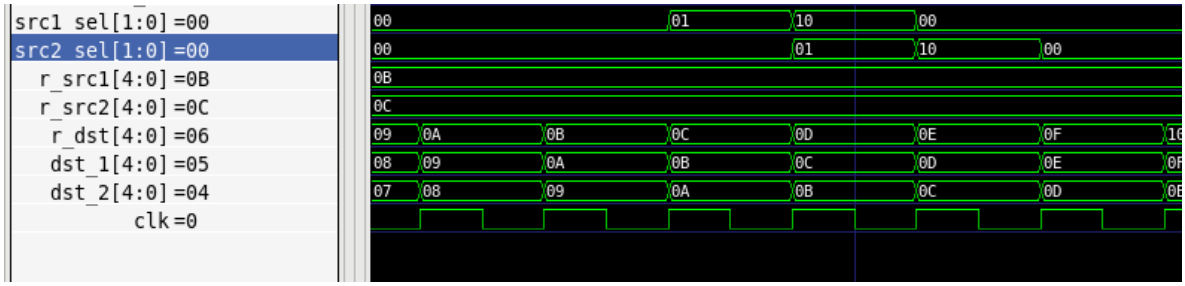
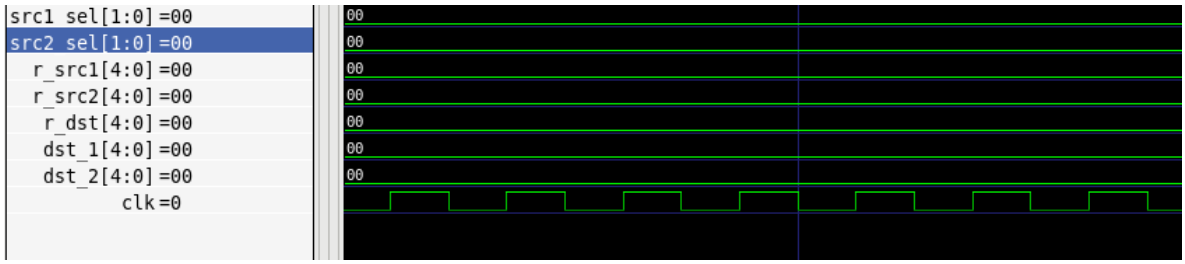
Harzard Test

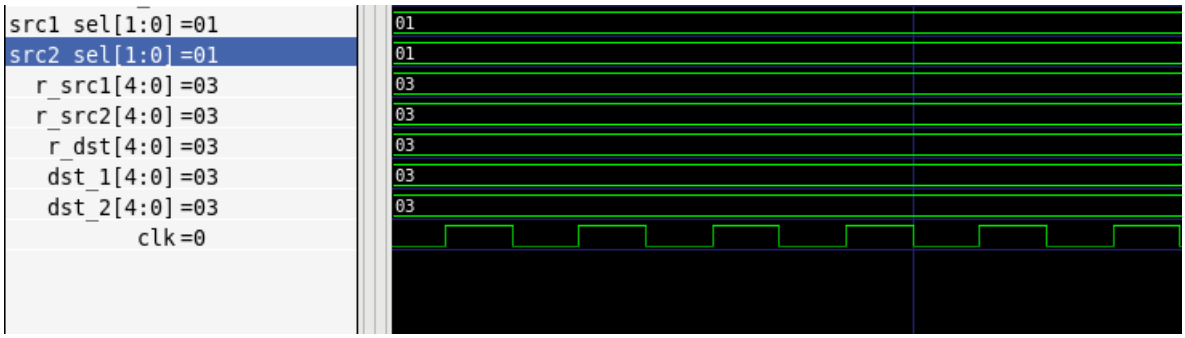
Bypass

1. 

In this situation, basic bypass signal is tested. The figure above shows that when source register is the same with the destination register of previous one or two instruction, correct data will be bypassed with the src1_sel or src2_sel signal.

2. 

In this situation,

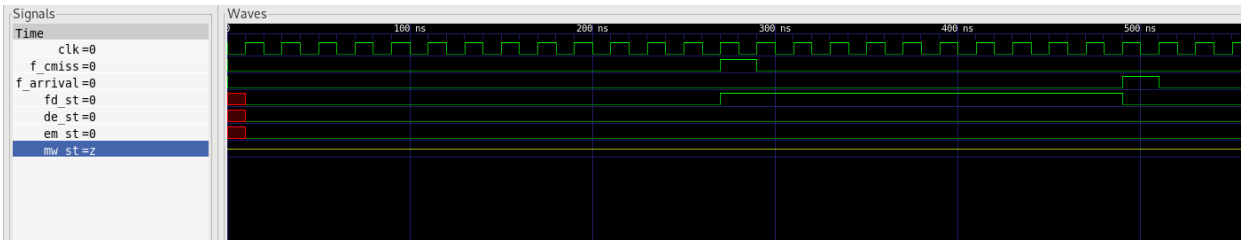
3. 

As shown as the figure above, when the destination register of the first instrction is a resource of the third instruction and the first instruction is a load instruction, the loaded data will be given directly from MEM/WB register.

Stall

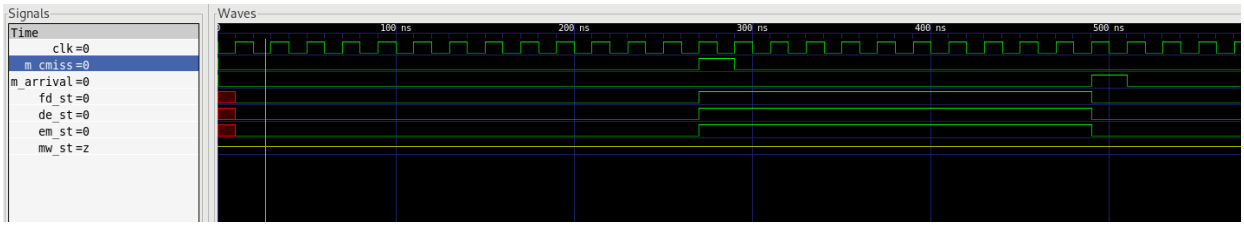
1. Cache miss

(1) IF cache miss



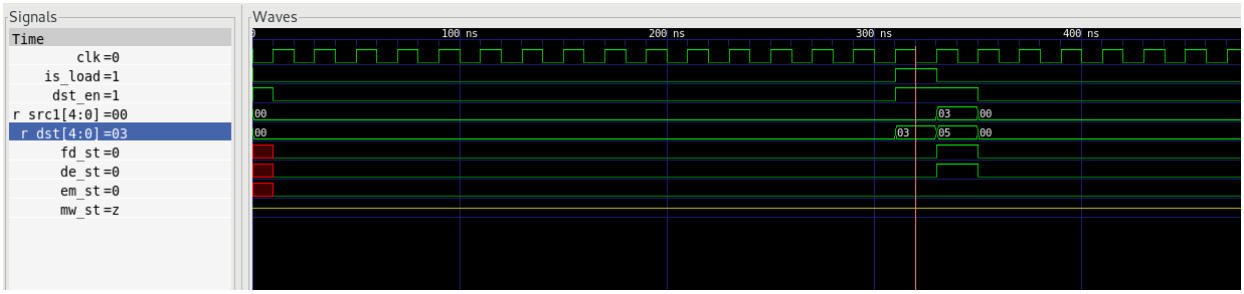
As shown in the figure, IF cache miss will cause stall of IF/ID register. The stall will last until instruction's arrival. Instructions before then will keep going in pipeline.

(2) load/store cache miss



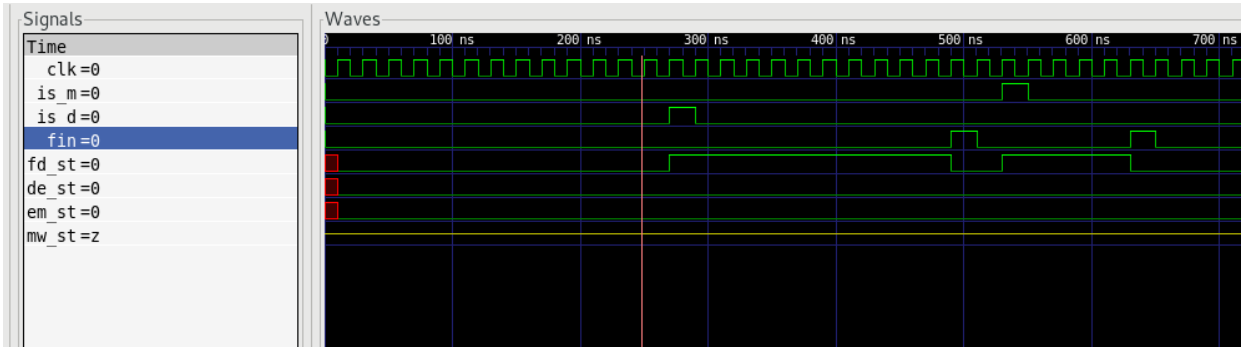
As shown in the figure, load/store cache miss will cause stall of IF/ID, ID/EX and EX/MEM register. The stall will last until instruction's arrival. Instructions before then will keep going in pipeline.

2. Data correlation



As shown in the figure, load date correlation will cause 1 cycle of stall when loaded data is used in the next instruction. IF/ID register and ID/EX register will stall. Instructions before the correlation will keep going in pipeline.

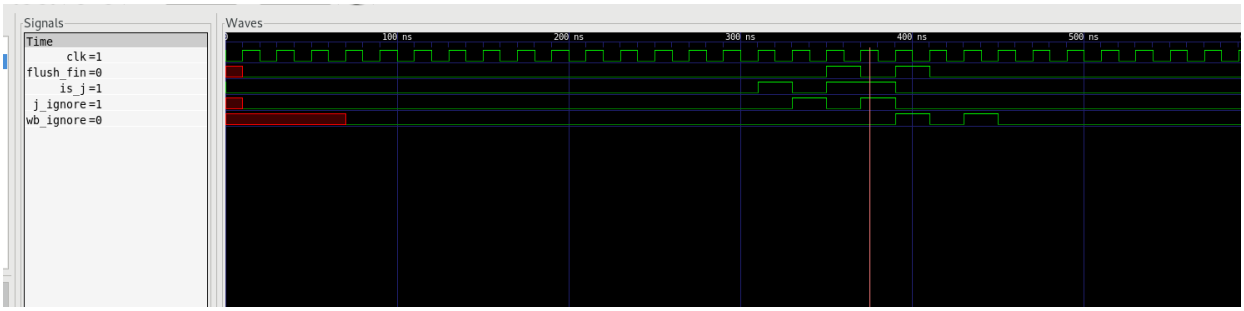
3. Multi-cycle instructions



As shown in the figure, multi-cycle instructions will cause several cycles of stall depending on the type of instruction. Because control signals of multi-cycle instruction are generated in ID stage, only IF/ID register will stall. Instructions before the correlation will keep going in pipeline.

Pipeline flush

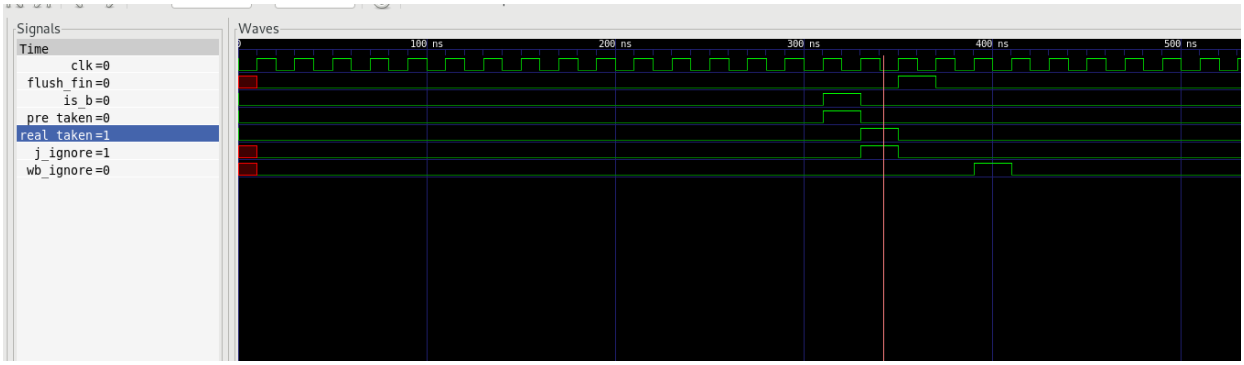
1. Jump



When jump signal is decoded, a signal of instruction type will be sent to hazard unit. As shown in the figure above, the next instruction in the figure will be flushed. If it is a single cycle instruction, its result will not be written back. Its data will not be bypassed either. If it is a multi-cycle instruction, finish signal will be sent immidiately. Same as single cycle instruction, its answer will not be bypassed or written back either.

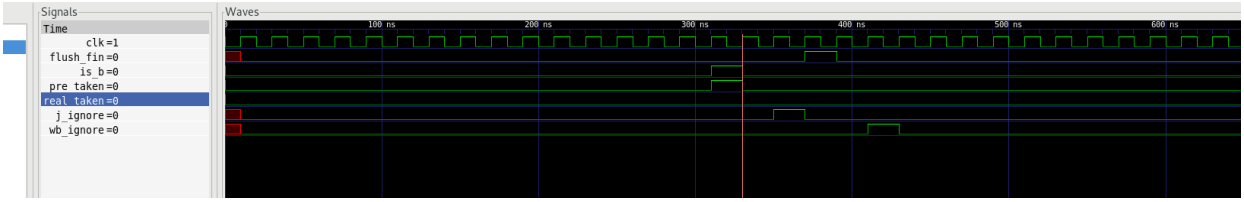
2. Branch

(1) Pridicted taken



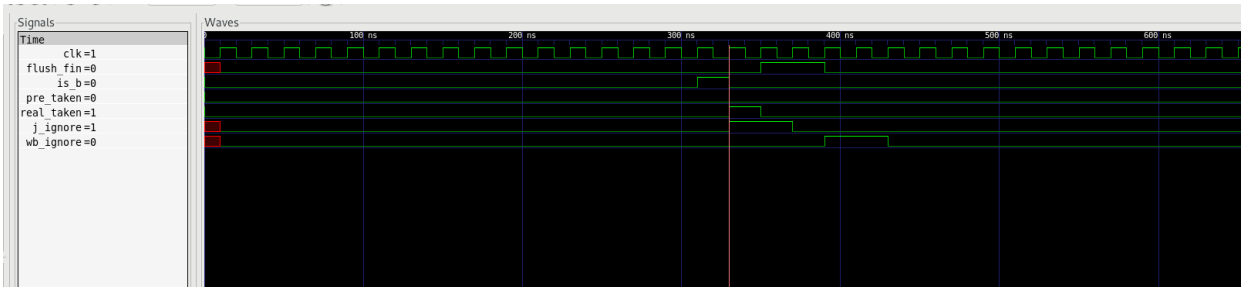
When branch signal is decoded, signal of instruction type and prediction result will be sent to hazard unit. As shown in the figure above, when the EX stage of branch signal finished, whether the branch taken will be sent to hazard unit. If prediction is correct, the next instruction in the figure will be flushed. If pridiction is wrong, the target instruction in the figure will be flushed. The operation of flush is the same as that in the Jump section.

(2) Pridicted not taken but wrong



When branch signal is decoded, signal of instruction type and prediction result will be sent to hazard unit. As shown in the figure above, when the EX stage of branch signal finished, the branch taken signal will be sent to hazard unit. The target instruction in the figure will be fetched in the next cycle. The next instruction and next+1 instruction in the figure will be flushed. When target instruction is next+1 instruction, next+1 instruction will still be flushed to simplify the control of pipeline flush. The operation of flush is the same as that in the Jump section.

(2) Pridicted not taken but wrong



As shown in the figure above, no instruction will be flushed.