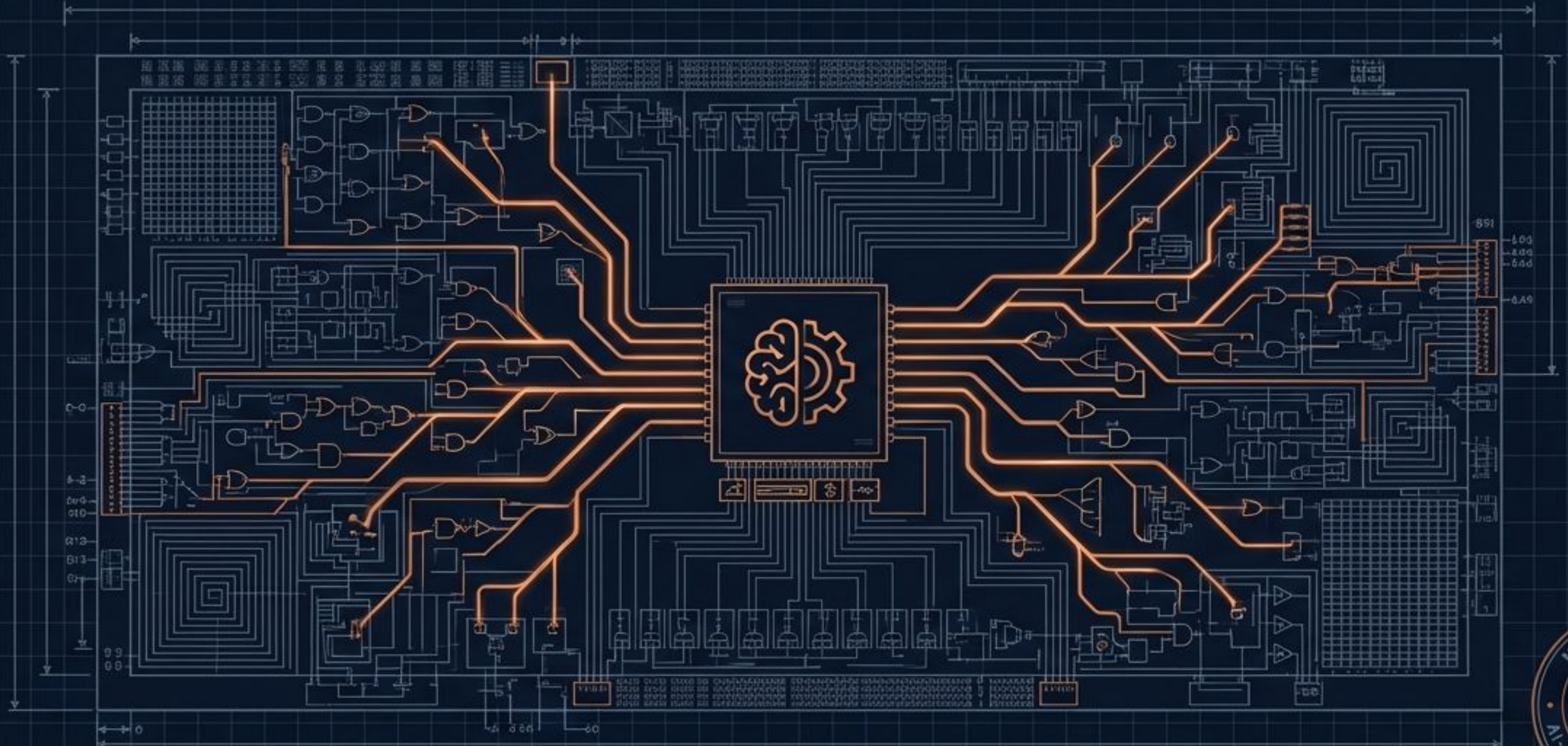
INTELLIGENT EFFICIENCY

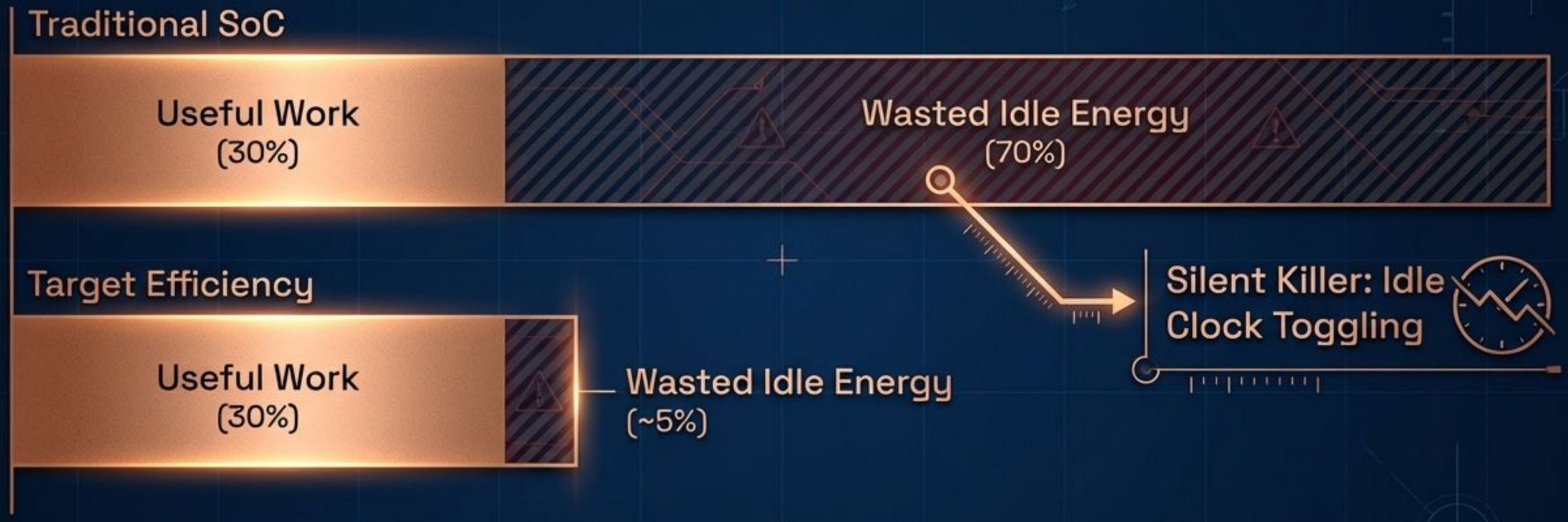
The CogniChip AI-Assisted Power Management System



Adaptive Clock Gating through Predictive Logic

GitHub Link

THE INVISIBLE BATTERY DRAIN



Problem: Unnecessary switching activity.

Consequence: Reduced battery life & thermal overhead.

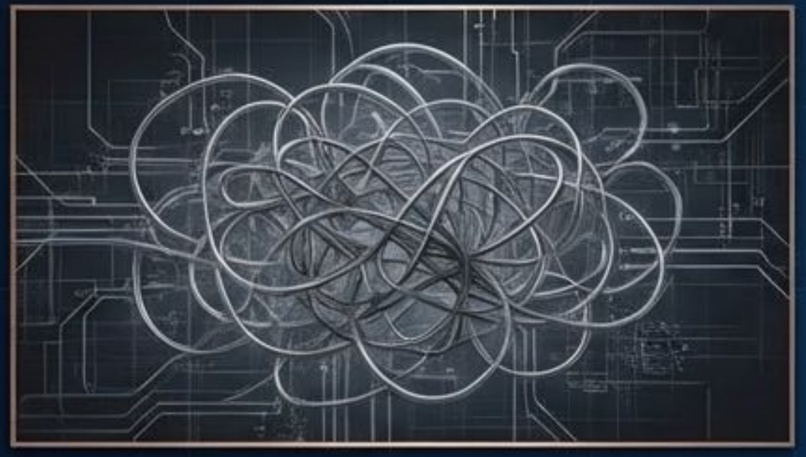
OBJECTIVE: ADAPTIVE INTELLIGENCE

Core Goals

1. **Scalability:** Modular design for N peripherals.
2. **Adaptability:** Runtime config (Performance vs. Power).
3. **Intelligence:** Prediction-based transitions.

THE ENABLER: AI-ASSISTED RTL

Traditional Flow



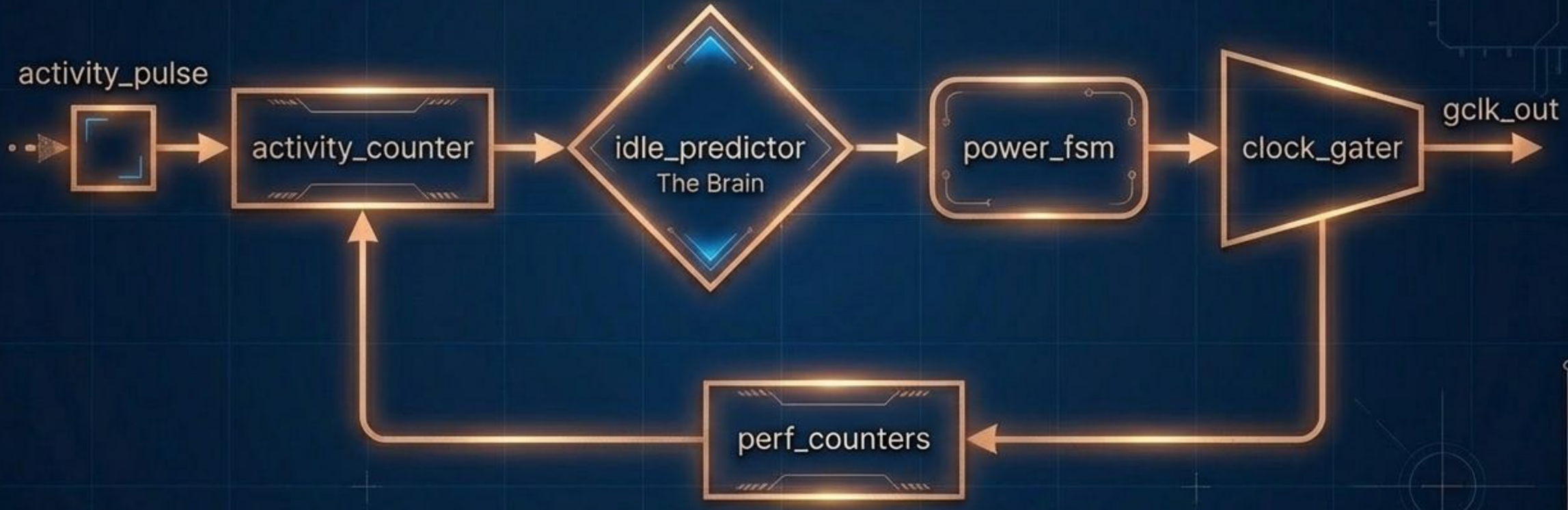
Manual Verilog, Slow Debug, Human Error.

CogniChip Flow

AI-Generated RTL, Auto-Testbenches, Rapid Bring-up.

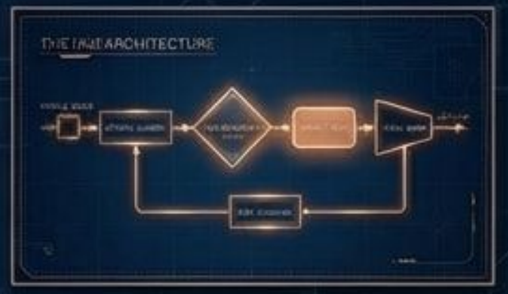
Generation (SystemVerilog) → **Dependencies** (DEPS.yml) → **Simulation** (Verilator) → **Synthesis** (Yosys)

SYSTEM ARCHITECTURE



Closed Loop System: Monitor → Predict → Decide → Act

THE HUB: CONTROL & CONFIG




```
Reg 0x00: PERIPH_EN
01000100: 010001011 ....
Reg 0x04: IDLE_THRESHOLD
01000010: 010000010 ....
Reg 0x08: ALPHA_SCALING
010100101 010111010 ....
```

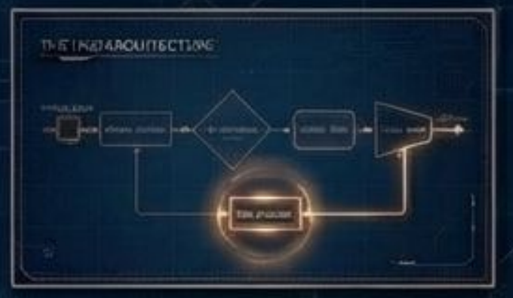
Software defines the “aggression” of the power saving policy.

QUANTIFYING SILENCE

IF pulse_detected THEN count = 0
ELSE increment count

Converts sporadic behavior into quantifiable data.

THE ORACLE: IDLE PREDICTOR



Current Silence
(idle_count)

Threshold
(idle_base_th)

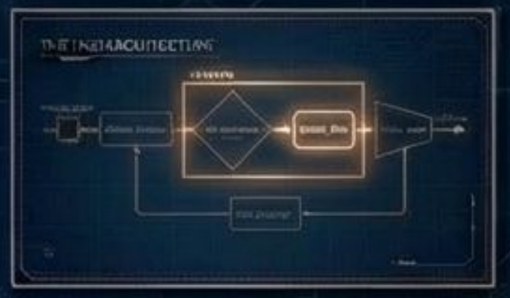
Sensitivity
(alpha)

History
(recent_activity)

`sleep_eligible”

Adaptive Logic: Prevents ‘thrashing’ by ensuring stability before gating.

THE DECISION ENGINE: FSM



ACTIVE
Clock Enabled.

No Activity

IDLE
Monitoring.

`sleep_eligible` == 1

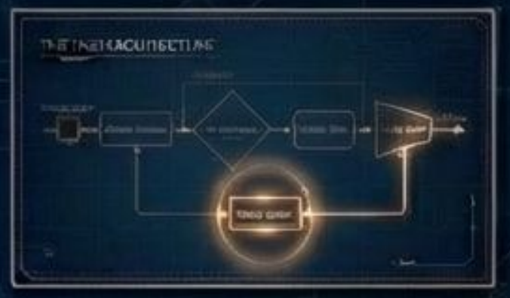
SLEEP
Clock Gated.

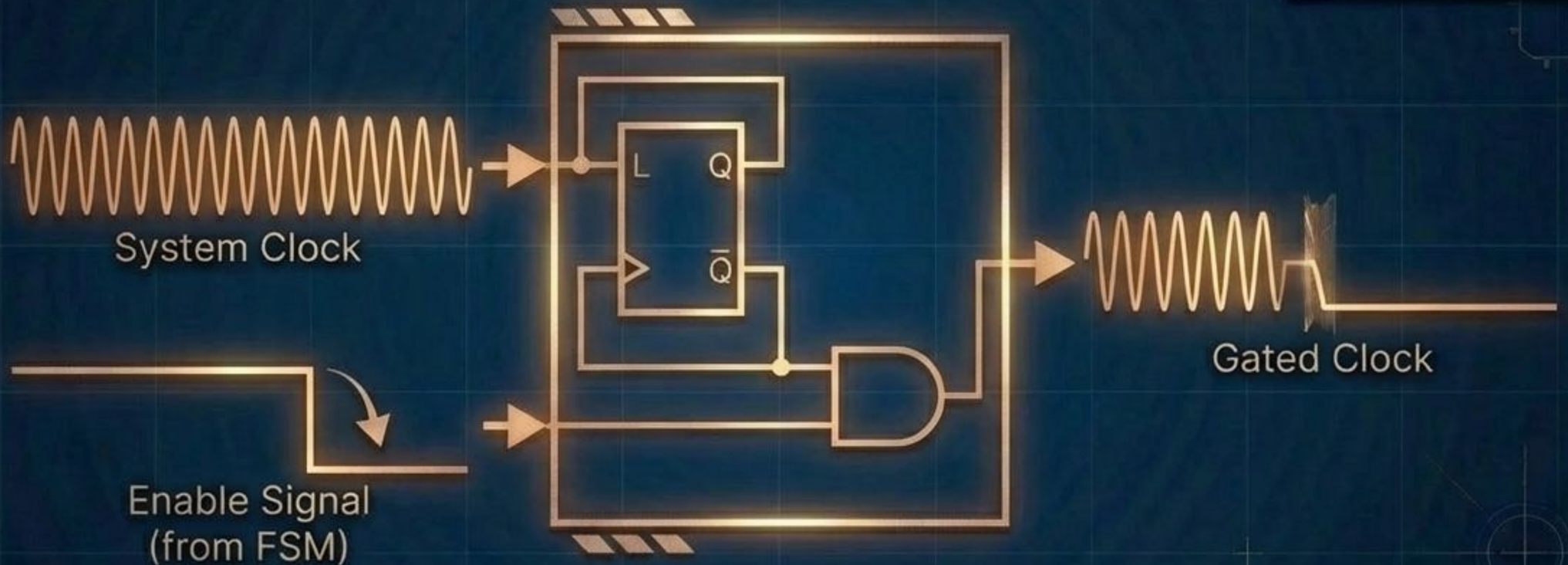
`activity_pulse`

`wake_evt`

Side note: Safeguards transitions to prevent data loss.

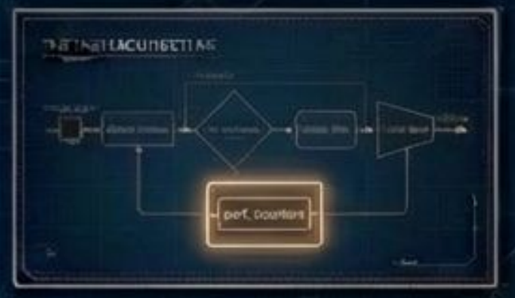
THE GATEKEEPER: PHYSICAL GATING





Zero Switching Activity = Zero Dynamic Power.

TRUST BUT VERIFY: TELEMETRY



ACTIVE_CYCLES

1,045,200

IDLE_CYCLES

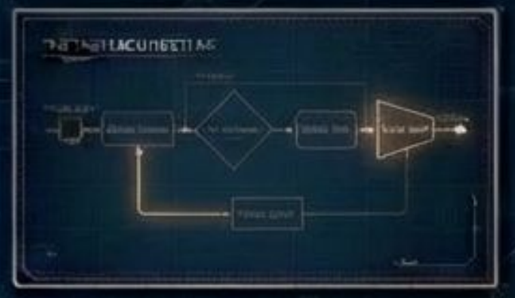
430, 100

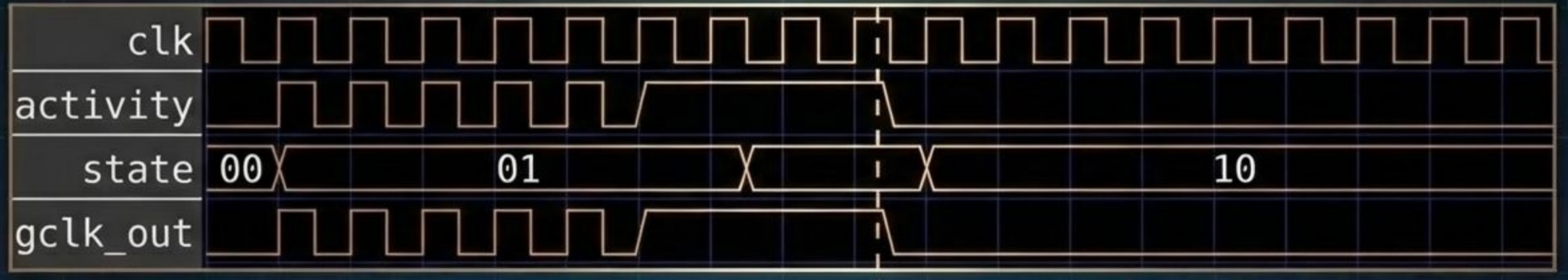
SLEEP_COUNT

850

- Real-time logging of power states.
- Enables “Performance vs. Power” analysis.

VERIFICATION & SIMULATION

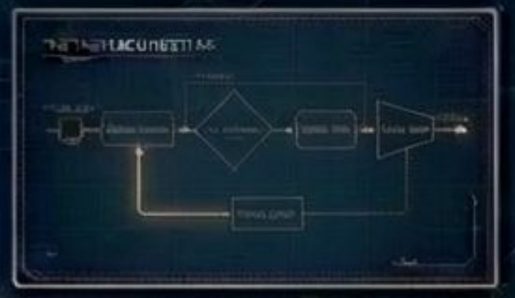




Successful Gate Event.

Environment: Verilator + CogniChip Testbenches.

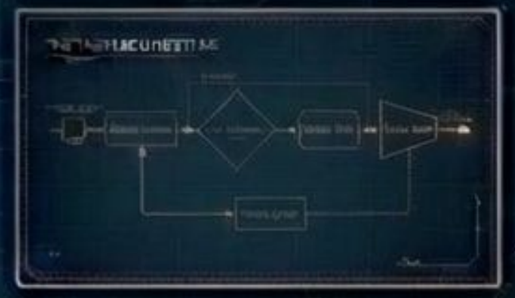
THE COGNICHIP ADVANTAGE



Feature	Traditional RTL	**CogniChip Flow**
RTL Generation	Manual	**AI-Assisted**
Testbenches	High Effort	**Auto-Generated**
Debug Loop	Slow / Complex	**Fast / Iterative**
Error Rate	Human Fatigue	**Machine Consistency**

Focus shifts from syntax to architecture.

CHALLENGES & LESSONS



Edge Cases

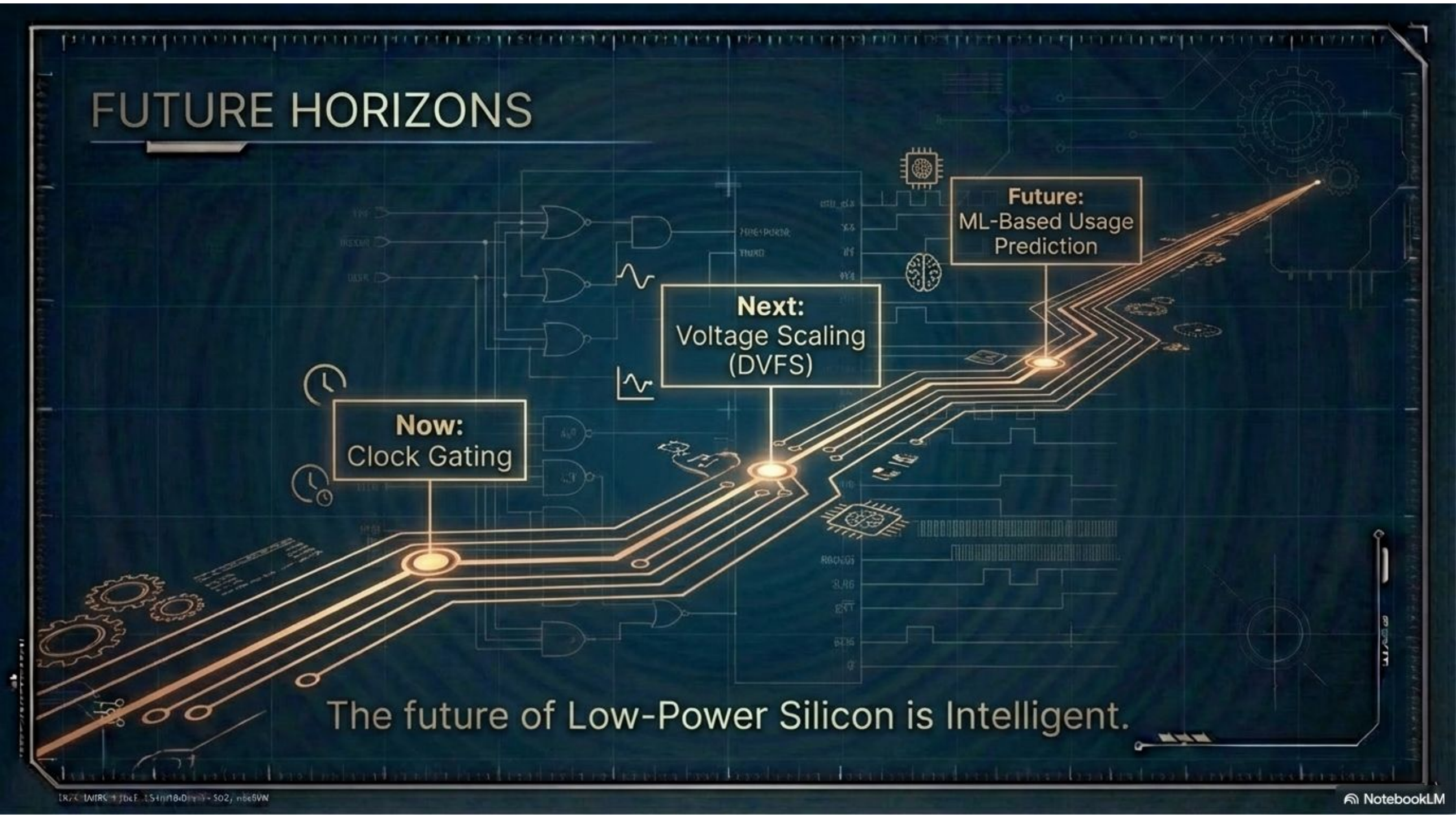
Handling wake-up events during sleep entry transitions.

Synchronization

Solving off-by-one errors in cycle counting.

Key Lesson

AI accelerates the *doing*, Engineers provide the *understanding*.


FUTURE HORIZONS
Now:
Clock Gating
Next:
Voltage Scaling
(DVFS)
Future:
ML-Based Usage
Prediction
The future of Low-Power Silicon is Intelligent.