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Transimpedance Amplifier

Welcome to the 24th article in the "Circuit Intuitions" column series. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. If you read this article, I would appreciate your comments and feedback as well as your requests and suggestions for future articles in this series. Please email me your comments: ali@ece.utoronto.ca.

In a previous article [1] of this series, we introduced the transistor as a two-port device that displays different port resistances depending on how we bias the transistor. In particular, we showed how a transistor in a common-gate configuration, where the gate terminal is common between the input and output ports, exhibits a relatively low resistance at its input port and a relatively high resistance at its output port (Figure 1). In this article, we use this configuration toward building a basic transimpedance amplifier (TIA). However, let us first distinguish an impedance from a transimpedance.

An impedance is a one-port device or a property of a one-port device that produces a voltage across its terminals if we feed a current signal through it. If the impedance is simply a resistance (i.e., it does not have any capacitance or inductance), then the voltage across the device is proportional to the current through the device, with the proportionality constant being the resistance. For example, if we feed a 200-μA (peak-to-peak) current to a 1-kΩ resistor, we produce a 200-mV (peak-to-peak) voltage signal across the resistor. In contrast, a transimpedance is a two-port device or a property of a two-port device that transforms a current signal applied to its input port to a voltage signal at its output port. For example, we may feed the same 200-μA current to the input port of a TIA and observe a 200-mV signal at the output port of the amplifier. In this case, the TIA gain is 1 kΩ simply because the amplifier multiplies the input current by a 1-kΩ equivalent resistance to produce its output voltage. In other words, in a TIA, the voltage is observed at a different port than the port receiving the current.

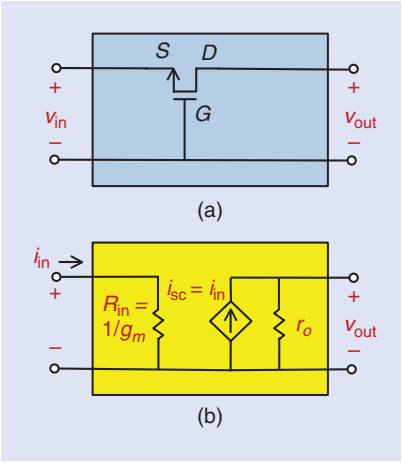

FIGURE 1: (a) The NMOS transistor in a common-gate configuration and (b) its equivalent circuit model assuming $g_m r_o \gg 1$ and neglecting the body effect [1].

One application of the TIA is in the area of optical communication receivers, shown pictorially in Figure 2. Here, the transmit data {0, 1} modulates the optical power $\{P_0, P_1\}$ sent through a fiber to the receiver. A photodiode (PD) at the receiver converts the received optical power to a small current signal (usually on the order of hundreds of μA peak-to-peak). This current is then fed to a TIA to produce an output voltage. In other words, the TIA receives an input current (from the PD) and converts it to an output voltage, exactly as we defined the transimpedance operation.

A TIA is a two-port network characterized by its transimpedance gain (as we described previously), its input and output impedances, its bandwidth, and its input referred noise. Let us now review these characteristics

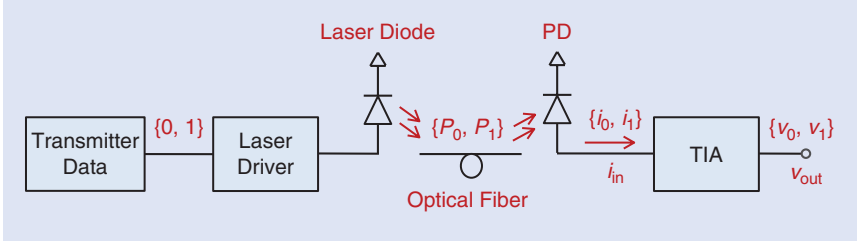

FIGURE 2: A simplified optical link: the optical signal is transferred through fiber to a photodetector, generating a current for a TIA.

Digital Object Identifier 10.1109/MSSC.2020.2987522
Date of current version: 24 June 2020

and determine their desirable values. It is desirable for a TIA to have a very low input impedance (R_{in}) compared with the PD's output impedance (R_{PD}) as shown in Figure 3. This will cause a large portion of the PD current to flow into the TIA rather than being wasted in the PD's output resistance. A typical output resistance of a PD is well in excess of 1 MΩ. As a result, if the TIA input resistance is in the order of 100 Ω, it can absorb almost all the current produced by the PD.

The use of a TIA at high frequencies is often limited by the combined bandwidth of the PD and the TIA. This is especially true if we use a discrete PD and solder it to the TIA input (Figure 3). In this case, the combined capacitance of the PD, the connection pad, and the TIA input could be on the order of 100 fF. This, combined with, say, a 100-Ω input resistance of the TIA, forms a low pass filter with a bandwidth of 16 GHz, diverting part of the higher-frequency content of the signal current to ground but not letting it flow to the TIA, where it can experience the gain. In general, the 3-dB bandwidth of this amplifier can be written as

$$f_{3dB} = \frac{1}{2\pi(R_{PD} \| R_{in})(C_{PD} + C_{in})}.$$

Naturally, if we wish to push this bandwidth higher, we can reduce either the total capacitance or the input resistance of the TIA. Because the capacitance is harder to reduce, especially if it is dominated by PD, we look at the possibilities of reducing the input resistance.

How about the desired output impedance of the TIA? As we will see next, we need to maximize the output impedance to maximize the transimpedance gain.

Figure 4 shows a simple TIA that consists of a common-gate transistor (M_1) and a current source (M_2). This circuit has a low input resistance ($\sim 1/g_m$) and a TIA gain of R_D (assuming $r_o \gg R_D$). To see why the TIA gain is R_D, we simply short the output node to ground to measure the short circuit current (i_{sc}), as

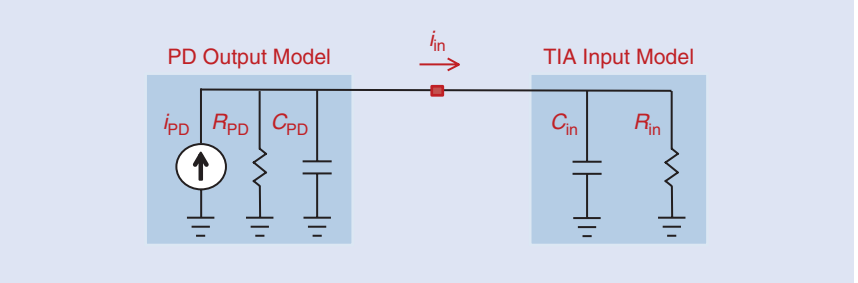

FIGURE 3: A model of a PD connected to a TIA.

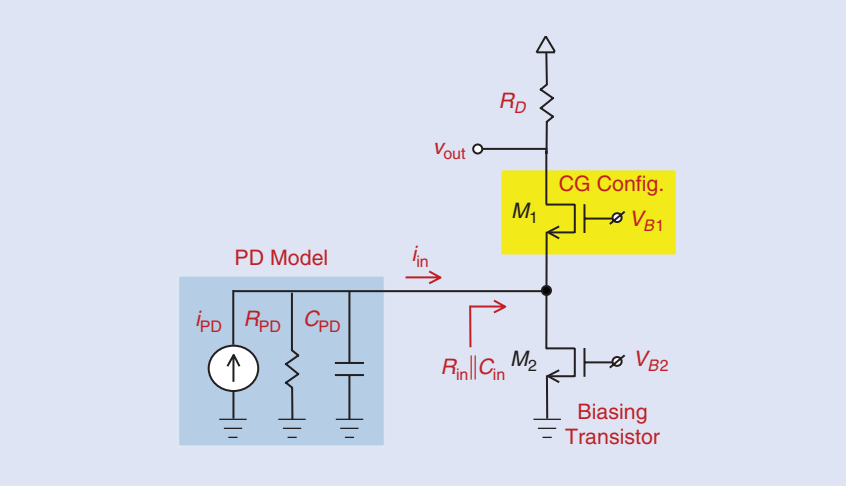

FIGURE 4: A schematic of common-gate TIA. M_1 is the common-gate transistor, and M_2 acts as a current source to bias M_1.

described in [2], and multiply it by the total resistance seen at the output node, which is approximately R_D. Because the short circuit current is equal to the input current (almost all the low-frequency input current will flow through M_1 rather than M_2), the low-frequency gain of the TIA will be R_D.

What if we need to design a TIA with a smaller input resistance? Remember that a smaller input resistance provides a larger bandwidth, as described earlier. One simple circuit for this purpose is the regulated-cascode TIA, shown in Figure 5(a). To intuitively see if the input resistance of this circuit is indeed lower, we can apply a small Δv to the input and measure the Δi that flows inside the TIA. By calculating $\Delta v/\Delta i$, we can find R_{in}. In this case, when we apply Δv to the source of M_1, the amplifier produces and applies $-A\Delta v$ to the gate of M_1, effectively increasing the v_{sg} of M_1 by a factor of $(1+A)$. This increase in v_{sg} will be multiplied by g_m of the transistor to effectively increase its input current to $(1+A)g_m\Delta v$. As a result, the input resistance will be $1/(1+A)g_m$, which is clearly a factor of $(1+A)$ smaller than the original circuit. Note that the output resistance of this TIA is about the same as the previous one; hence, the TIA gain is unaffected. The price we have paid to reduce the input resistance in this design is the addition of the amplifier, which takes silicon area and power and causes a slight increase in the input capacitance of the TIA. A simple implementation of the regulated-cascode TIA is shown in Figure 5(b) where $A = g_{m3}(R_1 \| r_{o3})$.

Given that the TIA is built with transistors and resistors, it generates some noise that appears at both the input and the output of the TIA. Generally, we wish the equivalent noise current at the input of the TIA to be much smaller than the signal

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will impact the industry and how ARM will respond.

—Denis Daly

The Smartest Designer in the Universe

- *Organizers*: Massimo Alioto, National University of Singapore; Denis Daly, Omni Design Technologies, Massachusetts; Tinoosh Mohsenin, University of Maryland; Alex Moreno, University of California, Berkeley; Mandy Pantel, Intel; Tim Piessens, ICsense, Belgium; Mahmoud Sawaby, Stanford University; Farhana Sheikh, Intel; and Tom Van Breussegem, ICsense, Belgium
- *Moderator*: Chris Mangelsdorf, Analog Devices, California
- *Panelists*: Marco Berkhout, NXP Semiconductors, The Netherlands; Alison Burdett, Sensium Healthcare, United Kingdom; Alvin Loke, Taiwan Semiconductor Manufacturing Company, California; Kenichi Okada, Tokyo Institute of Technology, Japan; Drew Hall, University of California, San Diego; and Filip Tavernier, KU Leuven, Belgium.

The Smartest Designer in the Universe quiz show participants on stage.

Good silicon engineering is like practicing sports on an Olympic scale. Be the best and be known being the best. But who is actually the smartest designer in the universe? Who is capable of combining endless creativity with superb knowledge and insight? And where will we find this person: in industry or in academia? Or will the students rise up and show the former generation their tail?

In this interactive quiz show hosted by the always entertaining Chris Mangelsdorf, three teams representing industry, academia, and students competed for the honor and the prestigious title: "Smartest Designer in the Universe." In several rounds, the contestants solved questions and puzzles covering all parts of electrical engineering. The audience was also able to participate and try to answer questions correctly using a mobile app. In the end, industry won the event, but students and academia vowed to come back in the future to get revenge!

—Denis Daly

CIRCUIT INTUITIONS

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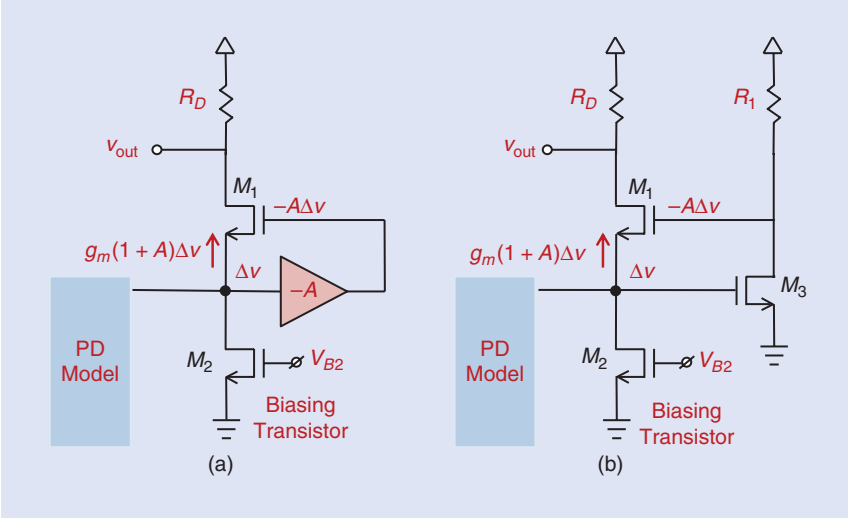

FIGURE 5: (a) A schematic of a regulated-cascode TIA using a voltage amplifier with negative gain. (b) A common-source amplifier is used to implement the voltage amplifier.

current being received from the PD. As an example, the root-mean-square noise current created by the TIA at its input can be on the order of 4 nA. To have a low bit error rate, we must ensure that the input signal to the TIA is much higher than this value for the receiver. We will discuss the noise considerations in more detail in a future article of this series.

In summary, a TIA is a two-port device that converts an input current in one port to an output voltage in another port. A TIA is expected to have a low input impedance, so as to absorb all the current produced by the PD, and a high output impedance, so as to have a high gain. We reviewed two TIA designs in this article, one using a simple common-gate amplifier and one using a regulated-cascode amplifier.

References

[1] A. Sheikholeslami, "Transfer resistor," *IEEE Solid State Circuits Mag.*, vol. 11, no. 1, pp. 7–9, Winter 2019. doi: 10.1109/MSSC.2018.2881859.

[2] A. Sheikholeslami, "Looking into a node," *IEEE Solid State Circuits Mag.*, vol. 6, no. 2, pp. 8–10, Spring 2014. doi: 10.1109/MSSC.2014.2315062.