High Performance Low Voltage Low Power Voltage Mode Analog Multiplier Circuit

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***Abstract*—This paper presents a low voltage low power analogue voltage mode four quadrant multiplier circuit using only two second generation current conveyor circuits (CCII) and two NMOS transistors operating in ohmic region. This circuit is characterized by ± 0.25 V dynamic ranges with a low total harmonic distortion (THD) around to 0.021 %, wide bandwidth (2.67 GHz) and low power consumption of about 0.43 mW. Tspice simulations using 0.18 µm CMOS TSMC parameters are performed to confirm the workability of CCII circuit and voltage mode multiplier structure.**

Keywords—active multiplier; voltage mode; second generation current conveyor CCII

I. INTRODUCTION

Analog multiplier is one of the most important electronic device widely using in many systems and applications electronic such as adaptive filters, fuzzy control, modulators, demodulators, analog signal processing and instrumentations. This device has generally two input ports (X, Y) and an output port (Z). The relationship between input-output terminals is given as Z=K.X.Y, where K is a constant with suitable dimension. This kind of device is classified into three groups depending on the operating mode. It can be configured either voltage mode or current mode or mixed mode and it can be functioned in one-quadrant or two-quadrant [1, 2] or four-quadrant [3-6].

A variety of multiplier circuits using active elements such that current conveyor (CC) [7-9], operational trans-conductance amplifier (OTA) [10, 11], operational amplifier (Op-amp) [12, 13] have received a considerable attention. For this reason, several research works are carried to improve their performances in the order to have a high accuracy, a wide dynamic range, a wide bandwidth, small active chip area and low power consumption.

In this paper, a voltage mode analogue multiplier circuit is proposed. The circuit structure is composed by two second generation current conveyor circuits and two NMOS transistors operation in linear region. The simulation results of proposed circuits have been verified by TSPICE simulator based on BSIM3v3 transistor model (level 49) for TSMC 0.18µm CMOS process available from MOSIS at 25°C.

The second generation current conveyor is characterized by a rail to rail dynamic range, low power consumption to about 290 µW, wide current (3.95 GHz) and voltage (4.25 GHz) bandwidth. The voltage mode multiplier circuit has a dynamic range extended from -0.25 V to 0.25 V with THD less than 0.021 %, wide bandwidth (2.67 GHz) and low power consumption (0.43 mW).

II. PROPOSED SECOND GENERATION CURRENT CONVEYOR CIRCUIT

The second generation current conveyor circuit CCII has three ports X, Y and Z. In perfect case, this circuit has a unity voltage gain between X and Y terminals, a unity current gain between X and Z terminals, low parasitic elements and wide bandwidth.

The proposed CMOS second generation current conveyor circuit is presented in Fig. 1. The input stage is composed by a PMOS differential pair (M1, M2) biased by M19 and three current mirrors (M3, M4), (M5, M6) as well as (M7, M8), where the drain of transistors M7 and M8 are respectively connected to the drain for transistors M4 and M6. The output stage is included two current mirrors (M11, M12, M14, M15) and (M16, M17, M18) and offset adjustment (M10, M13).

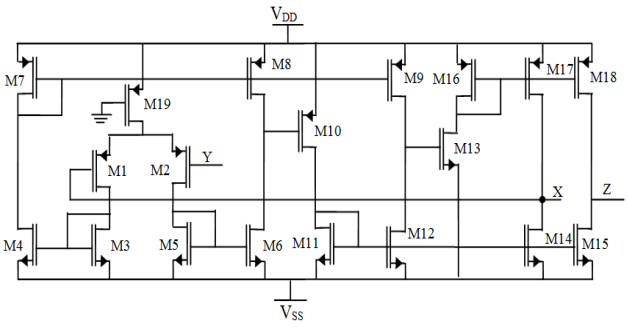

Fig. 1. Proposed second generation current conveyor CCII circuit

Using a small signal schema, the voltage mode relationship between X and Y terminals can be given by the following expression:

$$H_0 = \frac{g_{m2} r_2 A_1 r_N r_P \left(A_1 M_2 + A_2 M_1\right)}{g_{m1} r_1 r_N r_P A_4 \left(A_1 M_2 + A_2 M_1\right) + \left(r_N + r_P\right)\left(A_1 A_3 - A_2 A_4\right)\left(A_1 + g_{m1} r_1 M_1 \frac{r_N r_P}{r_N + r_P}\right)} \quad (1)$$

Where: A_1, A_2, A_3, A_4, M_1 and M_2 are given by the following expressions:

$$A_1 = \left(r_{o19} + r_{o1} + r_{o19} r_{o1} g_{m1}\right)\frac{1 + r_N g_{mN}}{r_N} + 1 \qquad A_2 = \left(r_{o19} + r_{o19} r_{o1} g_{m1}\right)\frac{1 + r_N g_{mN}}{r_N}$$

$$A_3 = \left(r_{o19} + r_{o2} + r_{o19} r_{o2} g_{m2}\right)\frac{1 + r_N g_{mN}}{r_N} + 1 \qquad A_4 = \left(r_{o19} + r_{o19} r_{o2} g_{m2}\right)\frac{1 + r_N g_{mN}}{r_N}$$

$$M_1 = \left(g_{mP}^2 + \frac{g_{mP}^2 g_{mN}^2 r_N^2 r_P^2}{\left(r_N + r_P\right)\left(r_N + r_P + r_N r_P g_{mN}\right)}\right)\frac{r_N^3 r_P^3 g_{mN} g_{mN}}{\left(r_N + r_P\right)\left(r_N + r_P + r_N r_P g_{mP}\right)^2} + \frac{g_{mN}^2 g_{mP}^2 r_N^3 r_P^3}{\left(r_N + r_P\right)\left(r_N + r_P + r_N r_P g_{mN}\right)\left(r_N + r_P + r_N r_P g_{mP}\right)}$$

$$M_2 = \left(\frac{g_{mP} g_{mN}^3 r_N^2 r_P^2}{\left(r_N + r_P\right)\left(r_N + r_P + r_N r_P g_{mP}\right)} + g_{mN} g_{mN}\right)\frac{r_N^2 r_P^2 g_{mP}}{\left(r_N + r_P\right)\left(r_N + r_P + r_N r_P g_{mN}\right)}$$

The dimensions of differential pair transistors (M_1, M_2) are equal. By considering the approximation ri gmi >> 1, the voltage gain (H_0) transfer function has become very close to unity.

$$H_0 = \frac{V_X}{V_Y} = \frac{g_{m2} r_2 A_1 \left(A_1 M_2 + A_2 M_1\right)}{g_{m1} r_1 A_4 \left(A_1 M_2 + A_2 M_1\right)} \approx \frac{g_{m2} r_2}{g_{m1} r_1} \approx 1 \quad (2)$$

The CCII circuit has some parasitic elements. To get the value of the parasitic resistance R_X, simply connect the terminal Y to the grounded (V_Y = 0). The resistance R_X is given by the following expression (3). By using the same approximation, the parasitic resistor is very close to zero.

$$R_X = \frac{R_1 \left(A_1 A_3 - A_2 A_4\right)}{A_1 A_3 - A_2 A_4 + g_{m1} r_1 R_1 \left(A_3 M_1 + A_4 M_2\right)} \quad (3)$$

III. PROPOSED VOLTAGE MODE MULTIPLIER

The proposed voltage mode multiplier circuit using two second generation current conveyor circuits and two N-Channel MOSFETs is shown in Fig. 2.

The transistors M1 and M2 have the same drain and the same source terminals. Assuming that the two NMOS transistors are operated in linear region, the current drains are given in (4) and (5).

$$I_1 = K_1\left(V_{IN2} - V_{IN4} - V_{TH1} - \frac{V_{IN1} - V_{IN4}}{2}\right)\left(V_{IN1} - V_{IN4}\right) \quad (4)$$

$$I_2 = K_2\left(V_{IN3} - V_{IN4} - V_{TH2} - \frac{V_{IN1} - V_{IN4}}{2}\right)\left(V_{IN1} - V_{IN4}\right) \quad (5)$$

Where,

- $K_{1,2} = \mu_n C_{ox} (W/L)_{1,2}$ is trans-conductance parameter,
- μ_n is the effective surface mobility,
- C_{ox} is the gate oxide capacitance per unit area,
- V_{TH} is the threshold voltage of MOS transistor and W/L is the transistor aspect ratio.

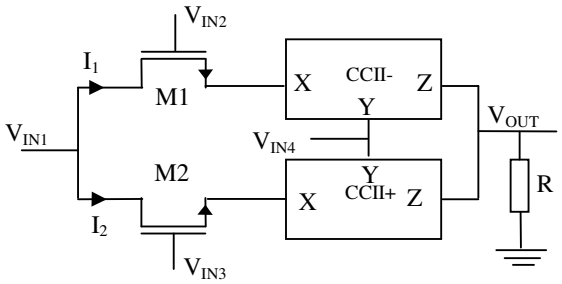

Fig. 2. Proposed voltage mode analogue multiplier

Supposing that M1 and M2 are homogenous (K_1=K_2=K and V_{TH1}=V_{TH2}= V_{TH}), the output voltage of multiplier circuit can be expressed as:

$$V_{out} = R\left(I_1 - I_2\right) = K\, R\left(V_{IN1} - V_{IN4}\right)\left(V_{IN2} - V_{IN3}\right) \quad (6)$$

IV. SIMULATION RESULTS

The performance of second generation current conveyor CCII circuit and analog voltage mode multiplier circuit are simulated using TSPICE based on BSIM3v3 transistor model

(level 49) for the TSMC 0.18µm CMOS process available from MOSIS at 25ºC.

The CCII circuit is powered by ±0.8V. The aspect ratios (W/L) of the MOS transistors were taken as (5µm/0.18µm) for M1, M2 and M19, (1µm/0.18µm) for all the other NMOS transistors and (2µm/0.18µm) for all PMOS transistors.

The DC characteristics voltage and current mode of CCII are shown in Fig. 3 and Fig. 4 respectively. In voltage mode, the current conveyor circuit has good linearity over the rail to rail dynamic range (-0.8V to 0.8V) with 0.06% error at the end of the transfer curve. The output current characteristic curve vs. input current shows a maximum error of 0.012% for an input dynamic varied from -280µA to 280µA.

The main AC characteristics of the CCII, such as plots of V_X against V_Y and I_X against I_Z, are presented respectively in Fig. 5. However, the voltage mode and current mode cut off frequency at -3 dB are equal to 4.23 GHz and 3.9 GHz respectively. From the results of simulations, it can be seen that the voltage and current gains of proposed CCII are closer to unity.

The parasitic elements on the tracks Y and Z are a resistor in parallel with a capacitor. They are given respectively (R_Y//C_Y) ∞, 75 fF and (R_Z//C_Z) 48.5 kΩ, 16.59 fF. On the other side, the parasitic resistor R_X keeps the same value of 14.79 Ω up to 100 MHz.

The frequency deviations in term of temperature variation for CCII circuit have shown in Fig. 6. The increasing of temperature causes the reduction of the cut down bandwidth and increasing the parasitic resistance R_X. With a temperature variation between -50°C to 100°C, the current mode and voltage mode cut-off frequency vary respectively from 5.47 GHz to 2.87 GHz and from 5.86 GHz to 3.07 GHz. In the same temperature interval, the parasite resistance Rx vary from 9.74Ω to 20.45Ω.

The main characteristics of proposed second generation current conveyor circuit and other circuits existence in literature are grouped in Table I.

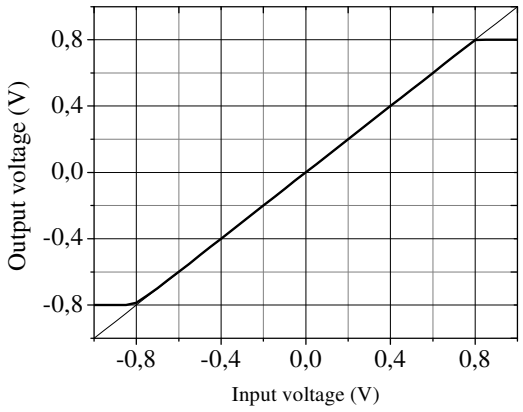

Fig. 3. Variation of output voltage as function of input voltage

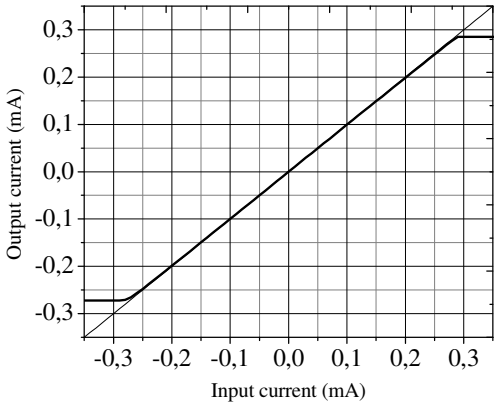

Fig. 4. Variation of output current as function of input current

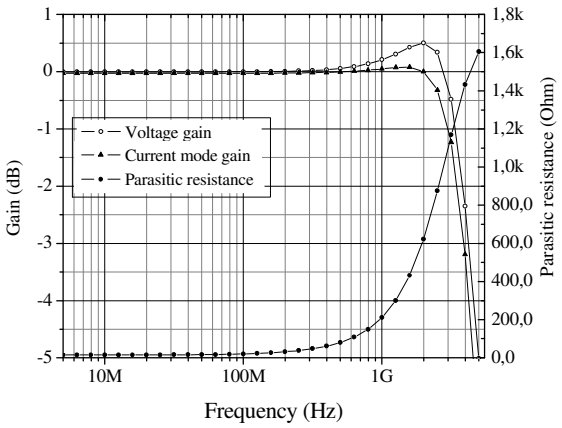

Fig. 5. Variation of voltage gain, current gain and parasitic resistance according to the frequency

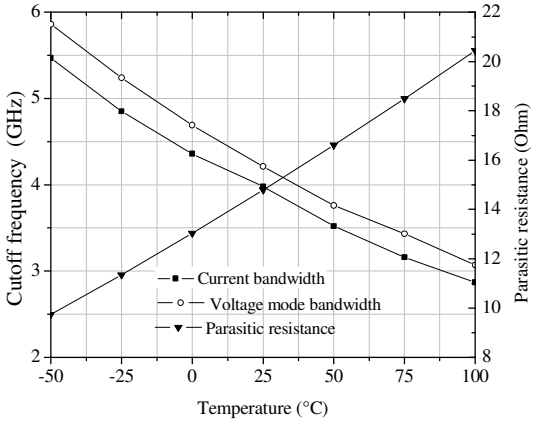

Fig. 6. Variation of the cutoff frequency voltage and current mode and parasitic resistance depending on the temperature

TABLE I. THE COMPARISON TABLE

Characteristics	Unit	Our circuit	[14]	[15]
Technology	CMOS	0.18µm TSMC	0.18µm TSMC	0.18µm TSMC
Bias voltage	V	±0.8	±0.75	±0.75
Power consumption	mW	0.291	0.6	0.268
Voltage gain	----	1	1	1
Current gain	----	1	1	1
DC voltage range	V	-0.8 to 0.8	-0.75 to 0.75	-0.75 to 0.75
DC current range	mA	-0.28 to 0.28	-150 to 150	-0.125 to 0.125
Bandwidth FCi	GHz	3.9	2.52	1.24
Bandwidth FCv	GHz	4.23	2.88	1.22
THD at 10kHz @0.3V	%	0.023		----
THD at 10kHz @10µA	%	0.025		----
Node X parasitic impedance R_X	Ω	14.79	1.01	1.8
Node Y parasitic impedance R_Y, C_Y	kΩ//fF	∞ // 75	∞//30.30	---∞//4.29-
Node Z parasitic impedance R_Z, C_z	kΩ//fF	48.5// 16.59	11.31//11.47	----

The performances of voltage mode multiplier circuit is verified by taking the size of transistors M1 and M2 equal to W= 0.5 µm and L= 0.7 µm. The values of passive resistor are equal to 10 Ω. Fig. 7 shows the DC transfer characteristics of the proposed analog multiplier. The output voltage swings between -0.25 V to + 0.25 V for the input voltage range of ± 0.5 V. Fig. 8 shows the frequency response of the proposed multiplier for various gains ranging from 0.13 V to 1.11 V. The bandwidth of the proposed analog multiplier is equal than 2.67 GHz for all gain values.

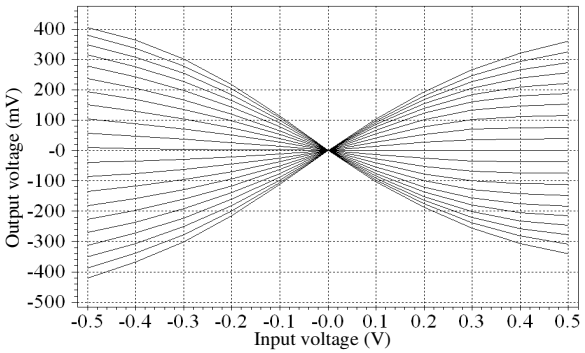

Fig. 7. DC voltage mode transfer characteristics of multiplier circuit

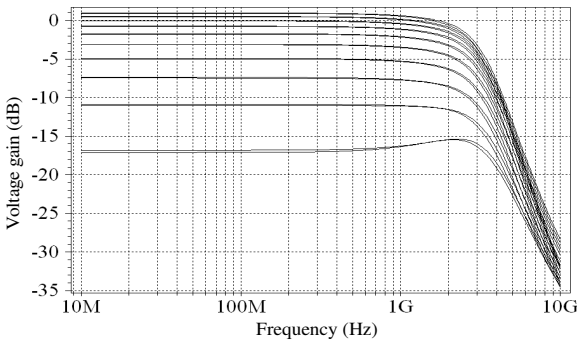

Fig. 8. Frequency response of the proposed multiplier

The normalized transient characteristic of the multiplier circuit is shown in Fig. 9 where V_{IN1} has 0.5 V amplitude and 4 MHz frequency, V_{IN2} and V_{IN3} have respectively 0.4 V and 0.1 V amplitude with the same value frequency of 1 MHz and V_{IN4} is connected to the ground.

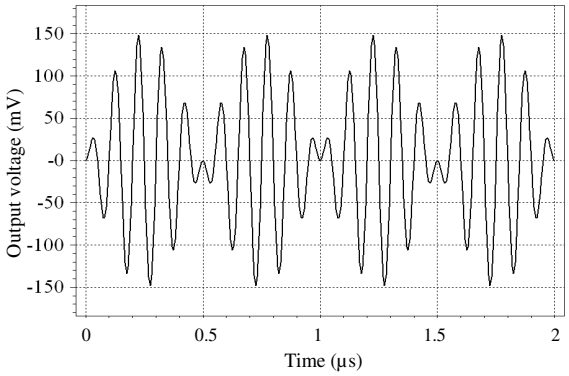

Fig. 9. Voltage mode transient response of multiplier circuit

V. CONCLUSION

This work presents a current mode four-quadrant multiplier circuit composed by two second generation current conveyor circuits and two NMOS transistors operating in linear region. The performance of proposed circuits have been verified by using TSPICE simulator based on BSIM3v3 transistor model (level 49) for the TSMC 0.18µm CMOS process available from MOSIS at 25°C. The CCII circuit shows a wide dynamic range, a high output impedance at Z and Y terminals, an excellent input impedance at X terminal (R_X = 14.79Ω) and a unity voltage and current gain with 290µW power consumption. The proposed multiplier has good voltage mode responses, where the dynamic range is ± 0.25 V with THD less than 0.021 %, wide bandwidth values equal to 2.67 GHz for different gain and low power consumption (0.43 mW).

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