An 85dB Dynamic Range Transimpedance Amplifier in 40nm CMOS Technology

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***Abstract*— A transimpedance amplifier (TIA with a nominal bandwidth of 280MHz, maximum gain of 2.5kΩ, 85dB dynamic range, 220nA rms equivalent input noise current and a high maximum input current (4mA) overdrive capability) for use with a monitor photodiode inside a packaged communication laser diode is proposed in this work. To enhance the overdrive capabilities of the TIA, a compression technique of the high input current is implemented. The proposed TIA has two regions of operation: a linear region, when the input current is small and a compression region, when the input current is high to prevent the TIA from entering saturation. The TIA is optimized for an external highly capacitive photodiode (≈15pF). The TIA is designed in 40nm CMOS.**

***Index Terms*—CMOS integrated circuits, optical receivers, feedback amplifiers, nanometer CMOS.**

I. INTRODUCTION

In optical sensing applications, an essential requirement is a high dynamic range (DR). DR is defined by the ratio of maximum and minimum detectable input current. The upper limit is defined by the maximum detectable current, whereas the minimum current is equivalent to the input referred noise current. In shunt-shunt feedback transimpedance amplifiers (TIAs), the feedback resistor influences the DR. This feedback resistor also has a strong impact on the bandwidth (BW) and hence controls the trade-off between DR and BW [1].

DR extension can be achieved by varying the TIA's transimpedance in response to the input signal strength. Various techniques have been employed to achieve this target, including switching several feedback resistors [1], placing an automatic gain control [2] or a limiting amplifier stage [3] after the TIA. However, this 3rd approach does not avoid that the TIA goes into saturation at high input levels. An alternative technique to extend the DR is the use of a TIA with nonlinear transimpedance characteristics, such as logarithmic compression [4].

One of the main challenges associated with handling high input signal levels in TIAs is to maintain stability over the full input signal range.

Stability has been guaranteed by different methods, including variable attention of the diode current before amplification [5] [6], usage of programmable gain levels by a current amplifier [7] and switched discrete gain levels [8][9].

This paper presents a high dynamic range shunt-shunt feedback TIA with monotonic transimpedance compression with high overdrive capabilities designed in 40nm CMOS technology. The proposed TIA is well suited for numerous optical sensing applications [7]. This paper is organized as follows, in section 2 and 3, the proposed TIA topology is described. In section 4, the simulation results will be presented. Finally, a conclusion is given in Section 5.

II. CIRCUIT TOPOLOGY

The basic circuit topology of the proposed high dynamic range is shown in Figure 1. To achieve a high dynamic range, the full input current range is divided into two regions: linear and compression. In the linear region, the TIA responds linearly to the input current, while in the compression region the transimpedance gain is reduced in a square-root law manner in response to high input currents.

The proposed TIA uses shunt-shunt feedback across an inverting voltage amplifier. The TIA consists of a fixed feedback shunt-shunt resistor R_F across a three-stage voltage amplifier: cascode inverter ($M_{1n,1p}$ and M_2) at the input and two common-source stages (M_5, M_7, R_1 and R_2).

In shunt-shunt feedback TIA, the bandwidth (BW) is proportional to the open-loop inverting voltage gain A as shown in equation 1. Therefore, a high open-loop gain is required to achieve the desired BW.

$$BW \propto \frac{A}{R_F \cdot C_P} \tag{1}$$

This equation is an approximation for A much greater than 1. C_P is the photodiode capacitance.

As a result of channel length modulation in nanometer CMOS technologies, the output resistance of these transistors is insufficient to achieve high gain with the classical hig

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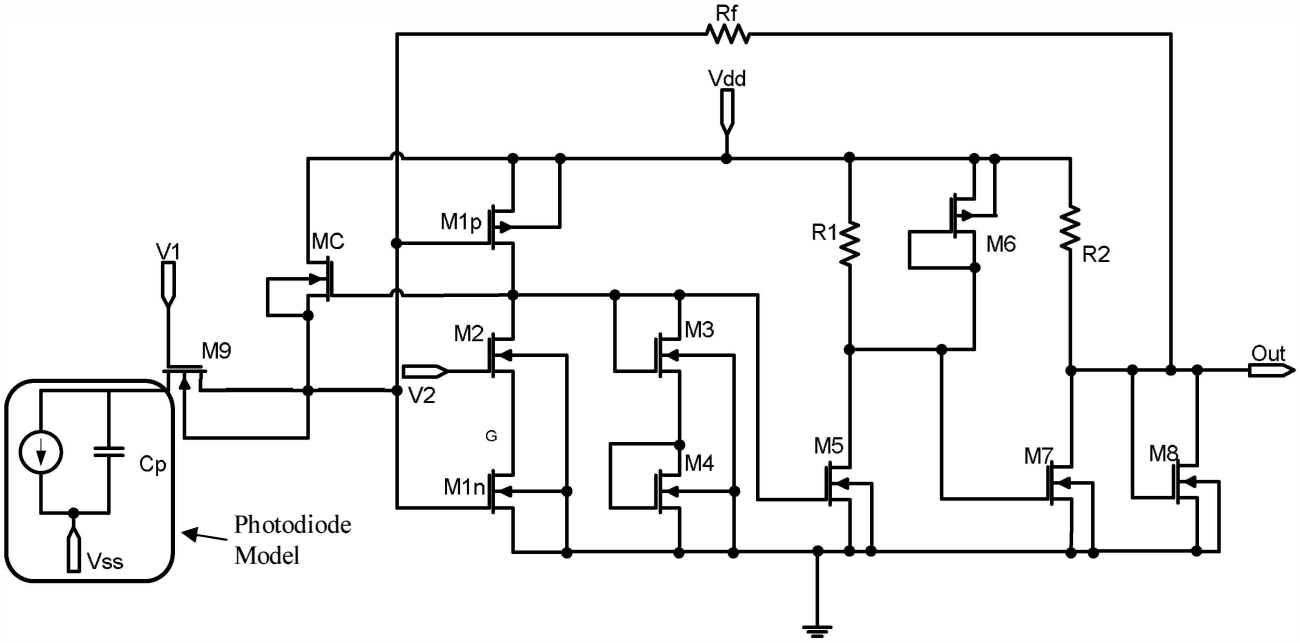

Figure 1: Proposed Transimpedance Amplifier

gain topologies such as cascode or inverter amplifier.

Thus, three stages are needed for the inverting amplifier to achieve enough gain. In this design, a cascode inverter is proposed as the first stage. This amplifier benefits from the high output resistance of the cascode and the sum of the transconductance of M_{1n} and M_{1p}, resulting in a high gain as stated in equation 2.

$$A_1 = -\left(g_{m1n} + g_{m1p}\right)\cdot\left(\frac{g_{m2}r_{ds1n}r_{ds1p}r_{ds2}}{g_{m2}r_{ds1n}r_{ds2} + r_{ds1p}}\right) \qquad (2)$$

A voltage gain of 35 dB is obtained for the gain of the first stage A1. The voltage gain A as shown in equation 3, is further increased by two resistive load common-source amplifiers (M5, R1, M7, and R2).

$$A = -A_1 \cdot \left(g_{m5} \cdot R_1\right)\cdot\left(g_{m7} \cdot R_2\right) \qquad (3)$$

Minimal length is used in transistors (M_{1n}, M_{1p}) to optimize frequency and noise response. Three times the minimal length is used for (M_5, M_7) to achieve a good g_m and r_{ds} trade-off. The widths of the NMOS transistors are chosen for a good noise performance and the widths of the PMOS transistors and the value of the resistors are chosen to achieve a DC output level of 0.55V.

Electrostatic (ESD) protection is a crucial issue in nanometer CMOS technologies. Therefore, transistor M_9 is inserted to prevent direct connection between the input pad and the TIA. M_9 acts as a switch, it turns off in ESD events to prevent the TIA from malfunction. V_1 is generated by an ESD detection circuitry. For further protection, M_{1n}, M_{1p} and M_9 are thick-oxide transistors.

III. Design Analysis

To improve the DR at the input of the TIA a compression technique of the input current signal is implemented. The basic principle is shown in Figure 2. The full input current range is divided into two regions: linear and compression.

When the TIA is operating in the linear region ($I_{IN}<I^c_{IN}$), the output voltage V_{OUT} is linearly proportional to the input current through the fixed feedback resistor R_F

$$V_{OUT} \approx I_{IN}R_F + V_{GS1n} \qquad (4)$$

The TIA operates in the linear region as long as the transistor MC is off. As the input current increases the drain voltage of M_2, increases switching on transistor M_c, thus create a parallel current path to the feedback resistor R_F.

This parallel path lowers the overall transimpedance gain of the TIA significantly in response to the increasing input current signal, increases the bandwidth and prevents the TIA from entering saturation.

The output voltage in the compression region ($I_{IN}<I^m_{IN}$), is given by:

$$V_{OUT} \approx \sqrt{\frac{2\cdot I_{IN}}{K}\cdot\frac{L}{W}} + V_{GS1n} \qquad (5)$$

Where K is the transconductance parameter of M_c, W is the width of M_c and L is the length of M_c

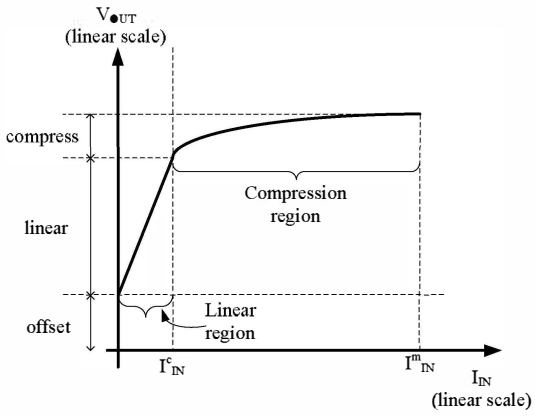

Figure 2: Principle of operation

Diode connected transistors M3, M4, M6 and M8 create a compensation circuit, which is necessary for small-signal stability over the full range of the input current. The compensation circuit lowers the output resistance of each stage, resulting in a lower overall open-loop gain and hence maintains the stability of the TIA at high input currents. The compensation circuit works only in the compression region.

IV. Simulation Results

The proposed TIA has been integrated in a standard 40nm CMOS technology with one supply voltage of 1.1 V. The characterization of the off-chip photodiode used in this application showed that the monitor photodiode's capacitance C_p is 15pF for a reverse bias of V_{ss} = 3.3V.

A. AC analysis

The power consumption of the TIA is 8.7mW. The frequency response of the TIA's state in the linear region is shown in Figure 3. The DC transimpedance gain is 68dB and the bandwidth is about 280 MHz Figure 4 shows the input spectral noise current versus the frequency. The integrated input referred noise current from DC frequencies to 280 MHz is about 220nA.

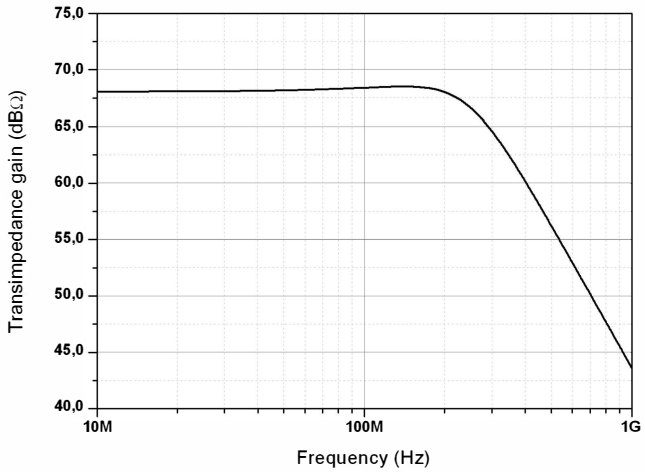

Figure 3: Frequency response

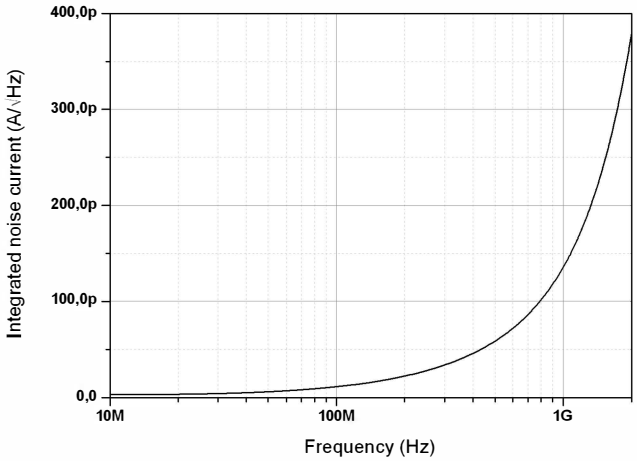

Figure 4: Noise response

B. Transient Response

Figure 5 shows the transient response of the output voltage in response to an increasing input current signal from 2µA to 4mA. The input current pulses were linearly swept from 2µA to 100µA with a step of 10µA and logarithmically from 150µA to 4mA with 5 points. The rise/fall time of the pulses was 100ps.

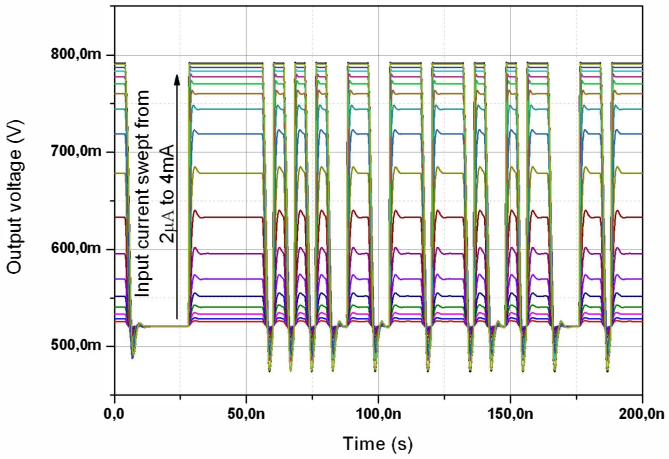

Figure 5: Output voltage transient response

Although the transient response shows some undershoots, the TIA is stable for the full input current range.

Figure 6 shows the regions of operation of the TIA clearly and the gain compression manner in decibels.

Below an input current of 100µA, the TIA is operating in the linear region. For larger inputs current up to 4mA, the TIA operates in the compression region.

Table 1 summarises the simulated results of the TIA.

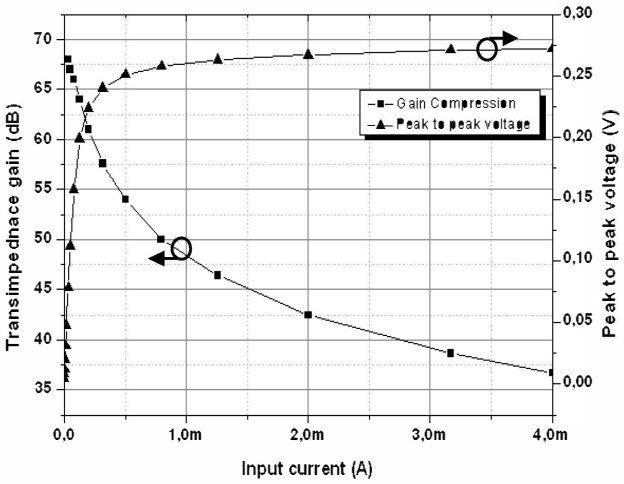

Figure 6: Peak-to-peak output voltage over input current

V. CONCLUSION

A high-dynamic range transimpedance amplifier for a monitor photodiode in 40nm CMOS technology is proposed in this work. It is designed for an external photodiode which is modelled by a capacitance of 15pF. A compression technique is implemented at the input of the TIA, allowing it to sustain a maximum input current of 4mA without entering saturation. The TIA achieves a dynamic range of 85dB and a bandwidth of 280 MHz for the highly capacitive photodiode.

TABLE I: SUMMARY OF TIA'S PERFORMANCE

Parameter	Simulation Results
Technology	40nm CMOS
Photodiode capacitance	15pF
Supply Voltage	1.1 V
Transimpedance Gain	68 dB
Bandwidth	280 MHz
Input Current Range	220nA to 4mA
Input Dynamic Range	85 dB
DC power dissipation	8.7mW

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