Wide Band Transimpedance Amplifier using Class AB FVF

Nidhi Singh[1], Vandana Niranjan[2]
[1,2]Department of Electronics & Communication Engineering
[1,2]Indira Gandhi Delhi Technical University for Women, New Delhi
1nidhisingh3636@gmail.com

Abstract – CMOS technologies have swiftly ameliorated across the past few years. To meet the demand of high performance applications like compact disc players, high definition television (HDTV), radar, medical imaging etc., this employs info conversion system for processing at later stages. Accuracy is highly desirable in many functional systems like optical communication, military surveillance etc. In optical communication system, transimpedance amplifier (TIA) is the fundamental part of optical receiver which is required to convert the low level current signal from the photodiode to an operable output voltage for further processing. Here in this paper, we propose a CMOS TIA using class-AB flipped voltage follower having less output resistance. Simulation results of the proposed circuit in 0.18µm technology depicts that the bandwidth and the transimpedance gain obtained are increased by 3.3 times and 1.03 times respectively.

Keywords- Flipped voltage follower (FVF), Optical Receiver, Transimpedance amplifier (TIA), low voltage low power design.

I. INTRODUCTION

The increasing data move on the internet due to the broadcast of digitalization in the form of Smartphone's and personal computers etc has led to tremendous research activity for the realization of cost efficient optical transceivers [1],[2]. The appropriate system for governance of this boosting measure of information is optical-fiber Communication. Optical receivers in such kind of systems employs front end transimpedance amplifier

(TIA) in context of performance of the entire optical system [1].

A detector or sensor is consistently required to observe numerous kinds of signal like thermal rays, optical signals, x rays etc. which are used for communicating information. Photodiode or photo detectors are used in these optical receivers to produce an electrical current, which is created when the p-n junction in the semiconductor is exposed to light. Once the photodiode observe the optical signal it is transferred to TIA for further conversion to voltage. So, it is necessary for TIA to have high gain and bandwidth to attain high information rate communication [1].

This paper is organized as follows- Section II describes the functionality of conventional TIA in brief. The working of proposed TIA is elaborated in section III. Section IV includes all the simulation results of the proposed circuit. Section V concludes the paper.

II. TIA

Transimpedance amplifier (TIA) are primarily a current to voltage converter or I to V converter, the ratio between the output voltage and input current is transimpedance, Z_{tr} and is often referred as transimpedance gain. On the basis of literature survey there are various topologies of CMOS TIA circuit which can be widely classified into Common Gate (CG) [3],[4], Common Source (CS) [5],[6], Regulated Cascode (RGC) [2], Differential TIA [2]. Out of all the above mentioned topologies, TIA based on Common Source topology (Fig1) is most commonly used due to its better driving capability and low noise characteristics [1].

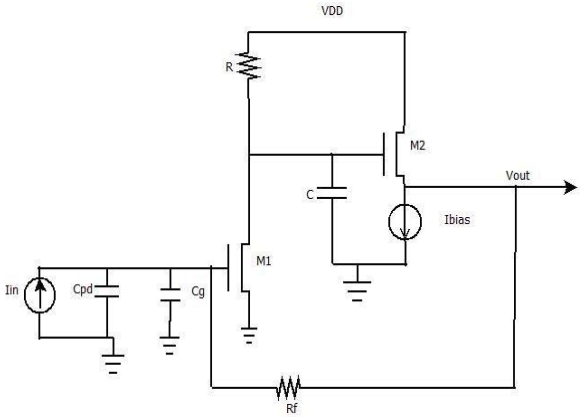

Fig 1: Conventional CS-TIA circuit [1]

It consists of CS stage as its first stage, CD as second and R_f as feedback resistor. C_g is the gate capacitance of M_1, load resistance R, photodiode capacitance C_{pd}. To conquer the problem created by increasing R to escalate the open loop gain caused the declination in the voltage headroom and also large voltage drop, a bandwidth improvement technique using the flipped voltage follower (FVF) has been proposed [1].

The Common Source TIA using FVF is shown in Fig2. It employs FVF because of its high bandwidth, low output impedance and approximately unity voltage gain. In this the transistor M_3 and FVF together makes the current mirror configuration. Overdue to this, a novel voltage gain is caused among load resistance R which is equal to 1.6KΩ [1].

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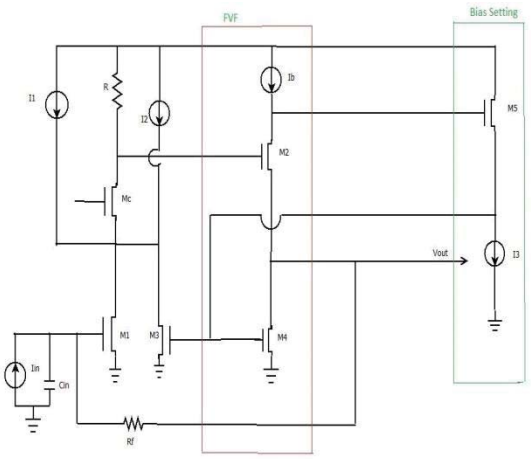

Fig 2: Schematic of CS-TIA using FVF [1]

The FVF used in Fig2 mainly offers two advantages i.e. very low output resistance and ability to sink large current. However, when M_4 turns off, the current sourcing capability of the FVF is bounded to I_b, building it a Class A circuit [7]. So, to overcome the above the above drawback, CS-TIA using Class AB FVF is proposed and described in the next section.

III. PROPOSED TIA

The class AB operation FVF used in proposed TIA shown in Fig3, offers advantage of large current sourcing capability in which transistor M_1 and M_3 gives large current sinking and sourcing respectively. M_2 stay as the voltage following device owing to constant current. To locate biasing point according to the expression given below, between gates of M_1 and M_3 a resistor R_{bat} is involved to cause battery voltage V_{bat}.

$$V_{supply} = V_{SG3} + V_{bat} + V_{GS1}$$

The battery voltage is given as $V_{bat} = I_B R_{bat}$[7].

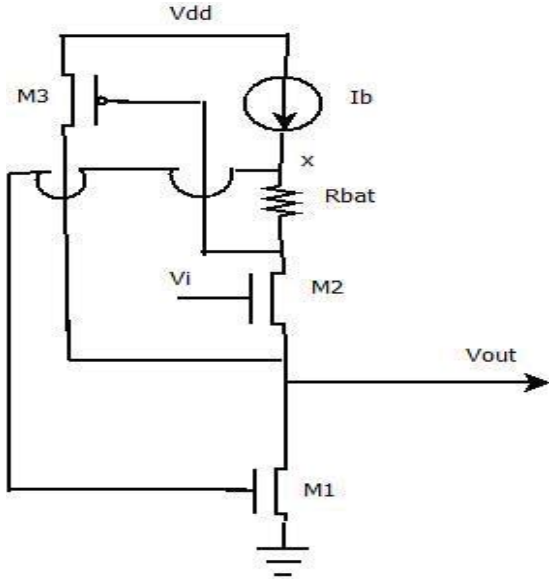

Fig 3: Class AB flipped voltage follower [7]

It does not require any additional power because of the utilization of similar biasing current from transistor M_2. In Class AB operation, V_{bat} works as the battery which provides complementary voltage variations to M_1 and M_2 transistor gates and, hence, their currents. Also constant current I_b is maintained by M_2 [7].

The Proposed TIA using Class AB flipped voltage follower is shown in Fig4.

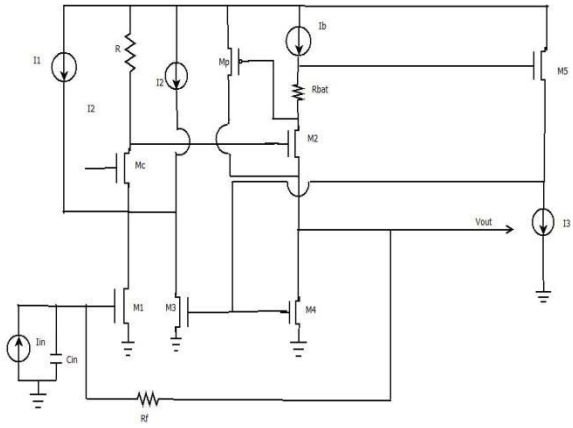

Fig 4: Proposed TIA

IV. SIMULATION RESULTS

The proposed TIA Circuit in Fig4 was simulated using Cadence Virtuoso at 0.18µm technology node. The input current and the voltage used for simulation are 60µA and 1.8V respectively.

All the simulation results of the proposed circuit are shown below.

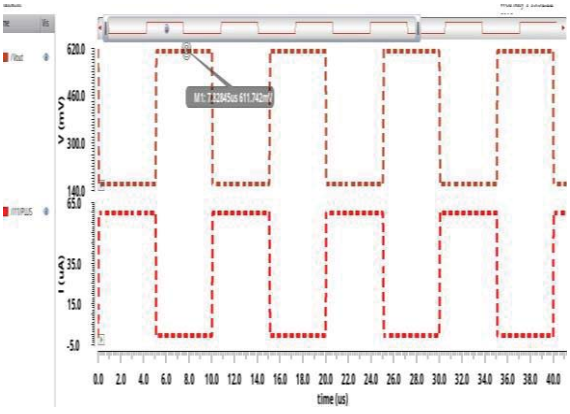

Fig 5: Transient Analysis of Proposed Circuit

The transient response in Fig5 plots the output voltage variation with input current. So, the transimpedance gain can be calculated as V_{out}/ I_{in} which gives 80.16dBΩ.

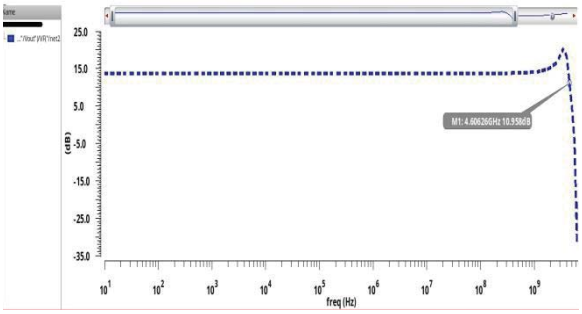

Fig 6: Bandwidth of Proposed Circuit

For the bandwidth of proposed circuit, the graph shown in Fig6 clearly depicts it as 4.606GHz.

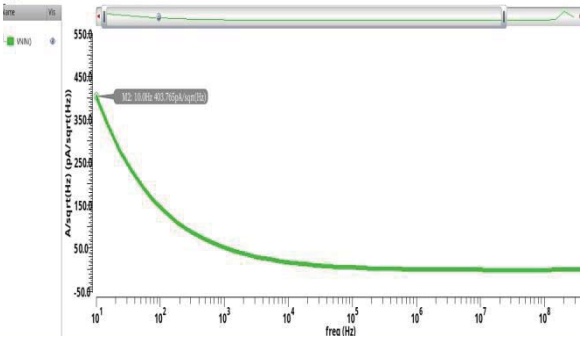

Fig 7: Input Equivalent Noise of Proposed Circuit

The equivalent input noise obtained from Fig7 is 403.76pA√Hz.

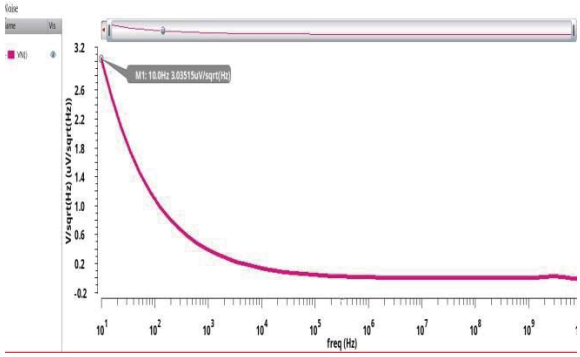

Fig 8: Output Equivalent Noise of Proposed Circuit

The equivalent output noise obtained from Fig8 is 3.035µV√Hz.

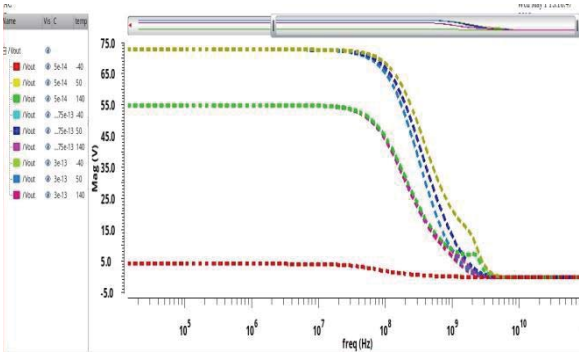

Fig 9: Output Voltage Versus Frequency plot with varying load capacitance and temperature

To illustrate the efficiency of the system with varying load capacitance C_L i.e. 50fF, 175fF and 300fF and temperature T under -40º, 50º and 140º, the AC response curve are plotted and shown in Fig9. Also, no loading effect has been observed since varying load capacitance is not affecting the output voltage. Again from Fig10, we inspected that the bandwidth of the circuit is affected at different temperature values and is obtained minimum between -1º to 1º which is undesirable.

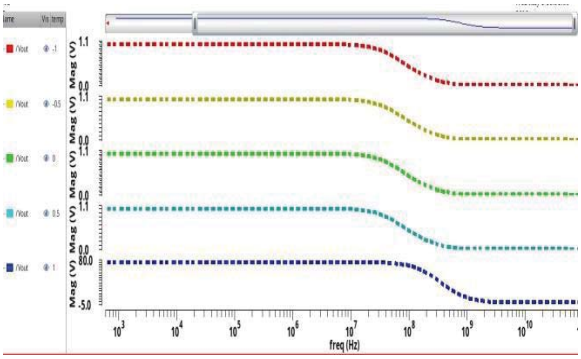

Fig 10: Output Voltage Versus Frequency plot with varying temperature between -1º to 1º

To conclude this work, the results of the conventional circuit in [1] are compared with the proposed circuit to get the perception about the refinement and the setbacks of the desirable parameters.

Circuit Parameters	**Conventional work [1]**	**Proposed work**
Technology	180nm	
Supply voltage (V)	1.8	
Photodiode Capacitance (fF)	300	
Gain (dB)	-	13.95
Transimpedance Gain (dBΩ)	77.3	80.16
Bandwidth (GHz)	1.39	4.6
Input equivalent noise (pA/√Hz)	3.59	403.7
Output equivalent noise (µV/√Hz)	-	3.03
Power Dissipation (mW)	8.75	0.3115

Table 1: Table of Comparison

From the performance summary in Table1, it is evident that transimpedance gain and the bandwidth performance are

improved by 1.03 times and 3.3 times respectively in the proposed circuit as compared to the conventional work presented in [1].

Also, we observed that the proposed TIA circuit consumes less power but the noise performance is slightly degraded.

V. CONCLUSION

In the proposed work a new CMOS TIA using class AB flipped voltage follower is present. Improvement in the transimpedance gain and bandwidth with less power consumption is achieved. This TIA can be used in applications where wider bandwidth with less power consumptions is desirable.

Further study can be done to find the stability of the circuit at various temperature values as future scope.

Also different Noise reduction techniques can be applied to the proposed work to analyze and get better insight of parameters without degrading the desirable parameters.

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