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CMOS Transimpedance Feedback Amplifier Design using Unity Gain Differential Amplifiers

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***Abstract*—Demand for mixed mode integrated circuit rapidly increases for modern high end electroinics devices. The design of linear circuit such as op-amps in CMOS technology becomes more complex and critical. Many authors and researchers devoted their time to find the optimal solution for design of analog circuits in mixed mode in an integrated circuit. This paper gives an overview on various implementation strategies for current controlled voltage source transimpedance operational amplifier (CFA) in CMOS based Integrated circuit technology.**

***Index Terms*—Analog circuits, Mixed mode, Output buffers, Differential Op-Amps, Adjoint network, CCVS, CMOS, CFA, Transimpedance Amplifiers**

I. Introduction

Transimpedance op-amp design has been the first choice among the analog designers for designing and developing the highly accurate and precise medical sensor devices. Rapid development in low power CMOS based image sensors provides integration of many functions such as analog to digital conversion, image compression, enhancement, exposure control and color processing on single semiconductor chip [1].

Researchers are trying to find the possibilities to enhance the characteristics of op-amps by incerasing input impedance, slew rate, gain, bandwidth and similarly possible reduction in noise, offset current, settling time and low output impedance [1]. These characteristics plays crucial role while designing high end devices like wideband amplifiers with high speed, DAC, Switching circuits, IF and video drivers etc.

Transimpedance op-amp is basically a resistive circuit where weak input current is converted into output voltage of larger magnitude [1][2]. The current to voltage gain is controlled by the feedback resistance. Performance of op-amp is characterised by its input impedance, its gain, bandwidth and slew rate. Ideally the values of these parameters are infinite.

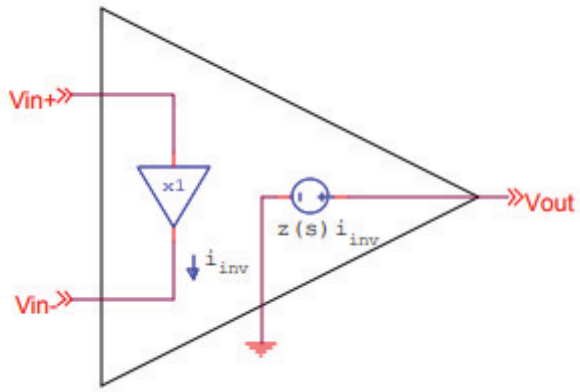

Fig. 1. Ideal Op-amp

The voltage gain in closed loop and Transimpedance equation for an inverting mode op-amp shown in fig.(2) is given as

$$A_{Vcl} = \frac{v_0}{v_i} = \frac{(1+\frac{R_f}{R_1})}{(1+\frac{R_f}{Z(s)})} \tag{1}$$

$$z(s) = \frac{Z_0}{(1+j(\frac{w}{w_0}))} \tag{2}$$

II. CMOS CFA Implementations

A. Current Conveyors Based CMOS CFA

Full dual input dual output current mode op-amp is implemented using second generation current conveyors (CCII)[3-5] system. The second generation conveyors systems works on the principle of Adjoint network theory. This system is configured to produce a constant Gain-BW product in a balanced transimpedance mode feedback amplifiers. such conveyors circuits possess both positive voltage and current follower action behaviour.

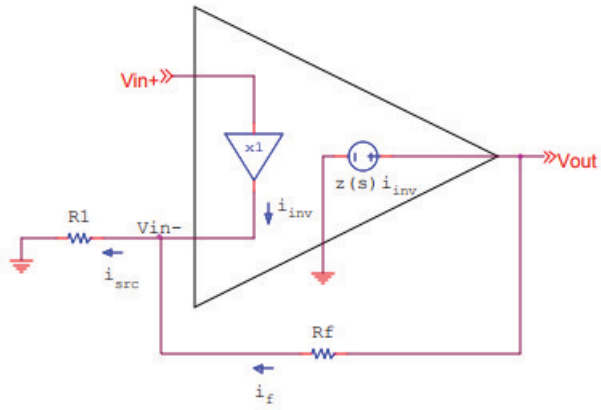

Fig. 2. Inverting Mode trans Impedance Op-amp

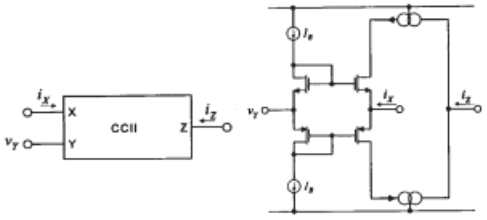

Fig. 3. Current Conveyors Circuit

The current conveyors system follows the principle of adjoint network theory which is related to conversion strategy where voltage mode circuit with transfer function is switched to current mode circuit with same transfer function as that of voltage mode. The dual working action of current conveyors circuits is reffered to as interreciprocal circuits.

The current conveyors circuits consist of interreciprocal circuits referred to as CCII- and CCI+- . The circuit with CCII+ shows a Positive voltage follower behaviour where as CCII- shows negative voltage follower action.

1) Adjoin network to replicate current mode op-amp from voltage mode mode: A voltage mode operational amplifier is represented in the form of CCII as in fig.(4). Differential input voltage is given through a transconductance denoted as g_m to a transimpedance Z_T where differential current is sourced into it. The transfer function for such circuit is produced by transimpedance Z_T connected in parallel to compensation capacitor C_c. This also gives large gain A_{dc} and constant Gain-Bandwidth (A_{dc}-BW) Product.

The current mode operational amplifiers can be obtained from fig.(4) by the application of theory of adjoint network. The current mode circuit obtained from fig. (4) is represented in fig.(5). A dual input current mode stage of an operational amplifier contains a node current of high impedance. Current from such node is transfered to the Z_T where voltage produced at resistor Z_T will be the output buffer. Feedback

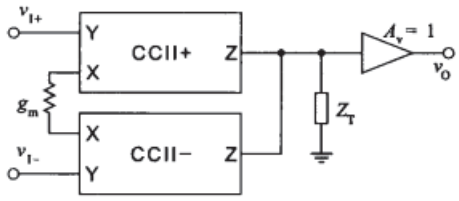

Fig. 4. Voltage Mode Op-Amp Circuit

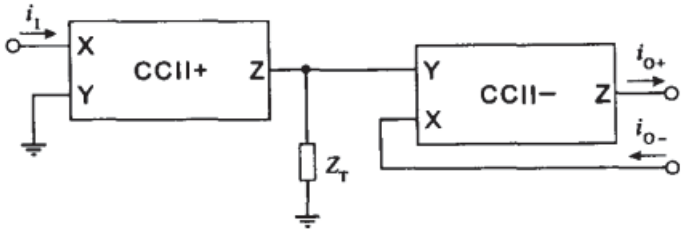

Fig. 5. Current mode Transimpedance Circuit

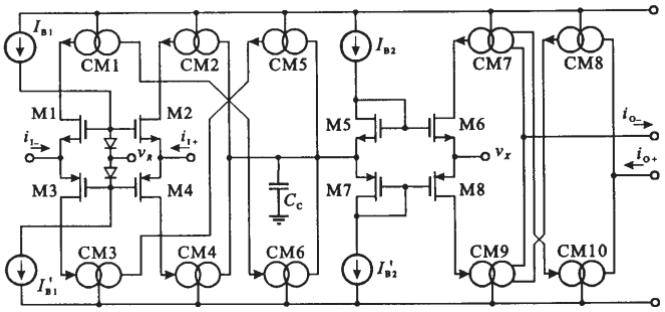

Fig. 6. Current Mode Op-Amp Circuit

configuration for this op-amp produce a same bandwidth which is independent of gain of closed loop op-amp.

While performing the conversion of the voltage controlled operational amplifier to current mode, The CCII+ is transformed to CCII- with an additional inverting buffer voltage with Y input at ground. The restructuring of this circuit is reffered to as current mode operational Amplifier. fig (6) shows the circuit.

Transfer function for current mode operational-amplifier can be obtained from fig. (4)

$$H_{COA}C(s) = \frac{I_o(S)}{I_i(S)} \tag{3}$$

The current mode op-amp circuit structure produce large value dc gain and a constant Gain-BW product. Current Gain is given as

$$A_{i(S)} = \frac{I_{o(S)}}{I_{i(S)}} = (1 + \frac{R_1}{R_2})(\frac{1}{1+R_1C_c}) \tag{4}$$

also Bandwidth is given by

$$BW = \frac{1}{R_1C_c} \tag{5}$$

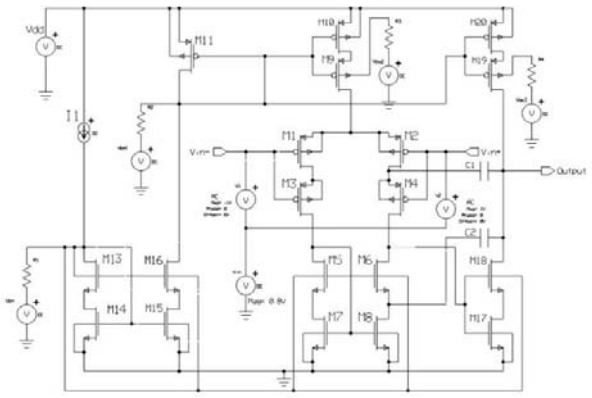

Fig. 7. Two Stage Amplifier using pseudo cascode compensation technique

The implementation of given Transimpedance operational amplifier is carried out in 2.4 μm CMOS process with dc gain of 72db with Bandwidth of 3MHz is obtained from an implementation. Above circuit structure proved that the interconnection of second generation CCII system results in efficient current mode realization from existing voltage mode amplifier circuits.

B. Pseudo Code Compensation Technique

The proposed technique [6-7] primarily focused on the designing a two stage operational amplifier using pseudo code compensation technique in 0.13 μm CMOS. The objective behind this implementation is to provide enhancement to the stability of the circuit. Presented techniques realizes an op-amp produces a DC voltage gain of 57.87 db with an unity gain frequency of value 57.390 Khz. power dissipation of 3.02 mW is calculated for a external bias current of 50 μA. The circuit provides stability with a phase margin of value 80.65° with a margin gain of 10.901db.

Implemented operational amplifier circuit consist of two interconnected stages. first stage has three sub circuits: This includes first circuit that contains M1- M4 as pMOS transistors which are having different inputs. second sub circuit has nMOS transistors M5, M6, M7 and M8 of low voltage cascode current mirror and lastly third circuit contain pMOS transistors M9, M10 which are atpower supply stage.

Second stage for the operational amplifier has M19, M20 pMOS and M17, M18 nMOS transistors which used as current source load at common source stage in op-amp. Input offset voltage of this op-amp can be minimized using proper selection of transistor size. pMos transistors M9 and M13 and nMOS transistors M5,M6 and M18 are used in sub threshold for producing large output swing. The circuit is shown in fig. (7)

C. nMOS Transistor working as an Active Feedback Resistor

The low noise, high gain operational amplifier can be realised using 0.35 μm CMOS implementation. Transimpedance gain produced through circuit is 4.43 MΩ and 4.43 MΩ for single stage and three stage design respectively. The value of power dissipation of trans impedance amplifier is 602.04μW and 1.781mW at gate voltage of 2.0V.

The proposed implementation[8] is carried out into single stage and three stage. The feedback resistor Rf of the traditional op-amp circuit is replaced by nMOS transistor which works as an active feedback resistor. Proposed circuit operates on of a supply3.3 V and for 0.5μA photocurrent.

Transimpedance amplifier has push pull inverter circuit as switching circuit for maximize transconductance of amplifier and it is used for increasing gain bandwidth product. Circuit is given in fig.(8). Amplifier takes current from input stage and convert into output voltage. Transistor T2 present in the circuit is used to minimize miller's effect and increase the bandwidth.

The trans impedance amplifier gain is expressed by either of two equations as

$$A_o = \frac{V_{out}}{V_{in}} = \frac{g_{m1}+g_{m2}}{g_{m2}} \tag{6}$$

$$A_o = \alpha + \sqrt{\frac{\mu_p}{\mu_n}\beta(1+\alpha)} \tag{7}$$

where

$$\alpha = \frac{W_1 L_2}{W_2 L_2} \tag{8}$$

$$\beta = \frac{W_3 L_2}{W_2 L_3} \tag{9}$$

gm1, gm2 and gm3 are transconductance of T1, T2 and T3 transistors respectively and W, L and Vgs be the width, length and gate to source voltage of transistors.

The feedback resistor in this circuit is given by

$$R_F = \frac{1}{(\frac{W}{L})\mu C_{ox}(V_{gs}-V_T)} \tag{10}$$

The bandwidth of the amplifier is expressed as

$$f_{-2db} = \frac{(1+A)}{2\Pi R_F C_T} \tag{11}$$

The paper shows two configurations for transimpedance amplifiers labeled as single stage and Three stage amplifiers. In single stage configuration shown in fig.(9), three nMOS and one pMOS transistors are used. similarly in three stage trans Impedance amplifier as shown in fig.(10), Three cascaded stages with seven nMOS transistors and three pMOS transistors are used.

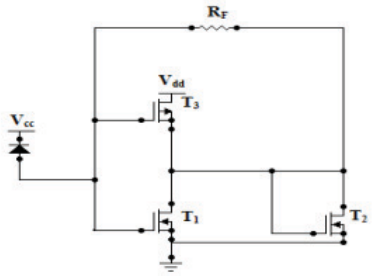

Fig. 8. Transimpedance amplifier using Push Pull Inverter

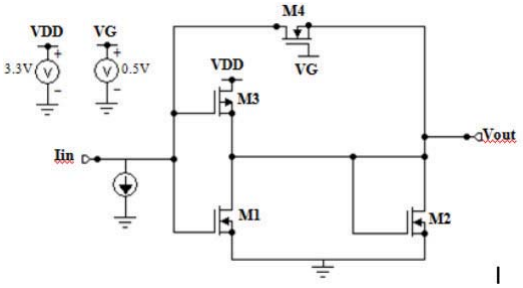

Fig. 9. Single stage Transimpedance amplifier circuit

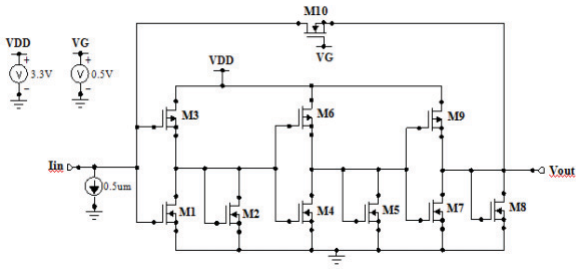

Fig. 10. Three stage Transimpedance amplifier circuit

D. Design of Transimpedance amplifier using Differential amplifiers

Differential amplifiers of class AB are configured as unity feedback to provide high value slew rate with lower input and output impedance values[9-11]. The objective of the proposed implementation is to improve bandwidth and reduce the requirement of high voltage supply. The implementation is carried out using 0.35μm CMOS technology.

The architecture shown in fig.(11) the need for high voltage supply requirement for operation has been solved by using class AB differential amplifiers. Transistors M1-M13 in the architecture forms the closed loop unity gainvoltage buffer.

Results from proposed architecture concludes that the bandwidth obtained as 63 MHzfor 3 kΩ feedback resistor and 70 MHz for 9K Ω. Slew rate obtained from this circuit produce is 8.1 v/μs. similarly settling time found to be 212 ns.

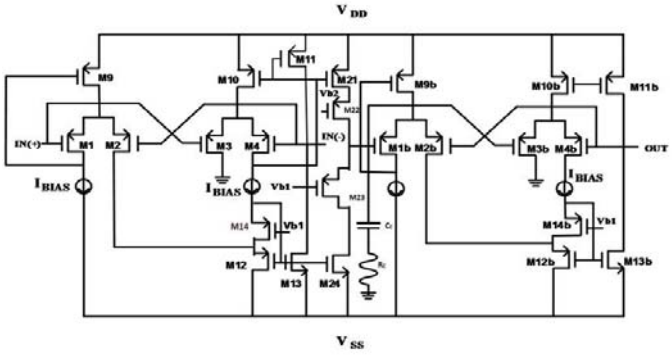

Fig. 11. Transimpedance Amplifier using class AB Differential amplifiers

III. Proposed Circuit Implementation

The Proposed circuit for CMOS feedback amplifier consist of an unity gain differential amplifier. The circuit is simulated on Tanner EDA tool. current feedback operational parameters are measured for the feedback resistor of value 12kΩ.

CMOS Transimpedance Feedback Amplifier		
Parameters	Existing Technique	Proposed Technique
Impedence	577 Ω	595 Ω
Supply Voltage	2 Volts	3 Volts
Settling Time	212 ns	137 ns
Bandwidth	2 MHz	52 MHz
Slew Rate	5.2 v/μs	7.8 v/ns

IV. Conclusion

Proposed paper presents various techniques to implement the transimpedance amplifier using CMOS integrated circuit technology. Results and performance value of each techniques has been given in respective section. The circuit of current feedback amplifier has been simulated and results are presented. As discussed throughout in this paper CMOS based transimpedance implementation has capability to design more and efficient and effective Operational Amplifiers.

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