A 1.8mW Wideband 57dBΩ Transimpedance Amplifier in 0.13μm CMOS

Firooz Aflatouni and Hossein Hashemi

Department of Electrical Engineering - Electrophysics
University of Southern California
Los Angeles, CA 90089 USA, Email: aflatoun@usc.edu, hosseinh@usc.edu

***Abstract*— In multi-hundred Gb/s parallel optical links for on-chip or chip-to-chip data transfer, system components should be very low power while occupying small chip areas. This paper presents a low power transimpedance amplifier (TIA) that is based on regulated cascode with vertically stacked inductors, and can operate up to 10Gb/s in presence of 370fF input capacitance. The 0.13μm CMOS TIA consumes 1.8mW to provide 57 dBΩ transimpedance gain, while occupying 150μm×100μm active area. The measured input referred current noise of the differential TIA is less than 30$pA/\sqrt{Hz}$ across 8 GHz.**

***Index Terms*— CMOS optoelectronic receivers, high speed integrated circuits, transimpedance amplifier.**

I. Introduction

Parallel optical links can form an area and power efficient high data-rate link. In such a system, many identical electrical and optical blocks are integrated to form a parallel data link [1][2]. Thus, low power consumption as well as small area are the key requirements for each block. Transimpedance amplifier (TIA) is one of the essential electrical blocks in such a parallel link. Low-noise wideband TIAs have been reported [3][4][5] in which the bandwidth enhancement and noise reduction design strategies have been considered. Innovative TIA circuits combined with a careful design strategy based on power optimization, while maintaining desired transimpedance gain, bandwidth, and total input referred noise can help further improve the performance of a parallel optical link.

II. TIA Topologies

In this section, a few known TIA topologies along with their design trade-offs will be reviewed briefly.

A. Passive TIA

A passive TIA is a single resistor that is placed in parallel with the photodiode capacitance, C_p. The TIA transimpedance is the value of the resistor, R, and the -3dB bandwidth is $BW_{-3dB} = 1/(RC_p)$. The integrated input referred current noise of the passive TIA (from DC to BW_{-3dB}) is $N_B = \frac{2kT}{\pi C_p R^2}$. Hence, C_p is bounded by BW_{-3dB} and N_B constraints. For instance, for a desired gain of $54dB\Omega$, bandwidth of 10 GHz, total input referred current noise of $1.4\mu A$, and $5.1fF < C_p < 31.8fF$, a passive TIA with zero power consumption can be used to directly convert the photodiode current to logic levels. Although CMOS compatible photodetectors with small capacitance have been reported, the optical power required to produce logic levels across the resistor needs to be high, especially considering typical losses in the optical domain.

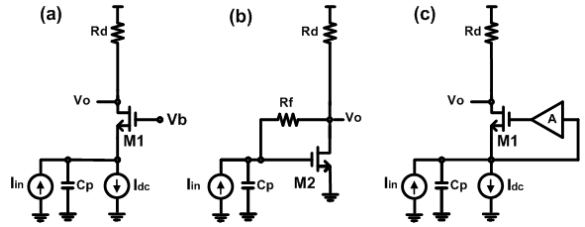

Fig. 1. Conventional TIA topologies: (a) common gate TIA, (b) common source TIA with resistive feedback, (c) common gate TIA with active feedback (CG_{AF})

B. Active TIA

A common gate (CG) TIA, a common source TIA with resistive feedback (CS_{Rf}), and a common gate TIA with active feedback (CG_{AF}) are depicted in Fig. 1. It can be shown that, for all these topologies, there is a minimum device DC current that is required to achieve the desired transimpedance gain, bandwidth, and total input referred current noise, simultaneously. Using SpectreRF simulations in a 0.13μm CMOS process and an optimization algorithm, the minimum device DC currents to achieve a desired gain of $54dB\Omega$, bandwidth of 10GHz, and total input referred current noise of $1.4\mu A$ are generated and plotted versus C_p in Fig. 2. Note that in CG_{AF} simulations, a gain of 5 and current consumption of $100\mu A$ for the feedback amplifier have been assumed.

Figure 2 shows that for small values of C_p, the minimum current consumption of the CG_{AF} TIA is dominated by the feedback amplifier's constant DC current consumption, and thus, it is higher than that of the CG TIA. As C_p increases the CG_{AF} performs better than both CG TIA and CS_{Rf}.

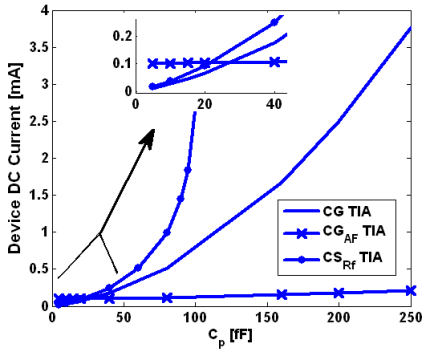

Fig. 2. Minimum device current vs. photodiode capacitance for CG TIA, CG_{AF} TIA, and CS_{Rf} TIA.

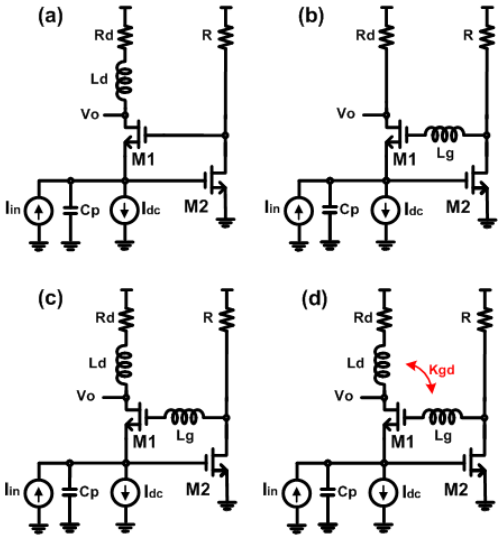

Fig. 3. Proposed TIA topology step by step formation: (a) CG_{AF} TIA with inductive drain shunt peaking, (b) CG_{AF} TIA with inductive gate peaking, (c) CG_{AF} TIA with both peaking mechanisms (d) CG_{AF} TIA with both peaking mechanisms and mutual coupling.

III. Proposed Power Optimized TIA

Assuming a total input capacitance of $370fF$, based on the graphs provided in the Fig. 2, the common gate TIA with active feedback (CG_{AF}) has been chosen as the core of the power optimized TIA. The $370fF$ input capacitance represents the photodiode capacitance of around $200fF$ and input pad and ESD protection diode parasitic capacitance of around $170fF$. The feedback amplifier can be a simple common source amplifier (M_2 in Fig. 3(a)). The second dominant pole of CG_{AF}, also known as regulated cascode, is often located at the output node. Inductive shunt peaking can be used to increase the bandwidth. Figure 3(a) illustrates a CG_{AF} TIA with inductive shunt peaking at its output. This technique improves the bandwidth by adding a zero to the transfer function. Another

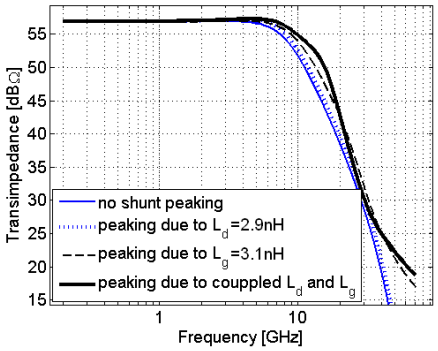

Fig. 4. Effect of various shunt peaking mechanisms on the TIA response.

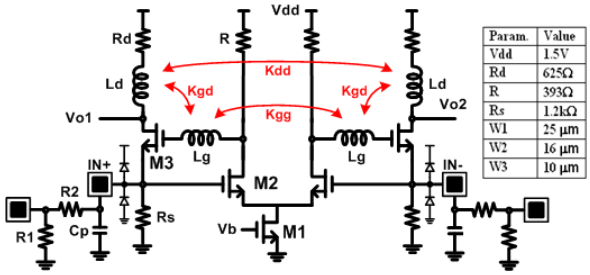

Fig. 5. The fabricated TIA core schematic (biasing and output buffer are not shown).

mechanism to create peaking in the frequency response is to add a pair of complex conjugate poles to the TIA transfer function. This can be done by adding an inductor to the gate of M_1 as depicted in Fig. 3(b). Combining both mentioned peaking techniques may further improve the bandwidth of the CG_{AF} TIA (Fig. 3(c)). The main drawback of using both L_g and L_d is the large increase in the TIA core area. One way to reduce the chip area is to vertically stack L_g and L_d. Although this reduces the chip area, it introduces a relatively large coupling between L_g and L_d that needs to be considered in the design (Fig. 3(d)). Figure 4 shows the TIA bandwidth enhancement due to addition of L_d, L_g, or both to the inductorless CG_{AF} TIA.

Considering the coupling between L_g and L_d, and ignoring all device parasitics except C_{gs1} and C_{gs2}, the transimpedance can be calculated as

$$Z_{TIA} = \frac{(R_d + sL_d)}{s^3\omega_\alpha^{-1}C_{gs1}L_g + s^2\omega_\alpha^{-1}(g_{m1}M + C_{gs1}R) + s\omega_\alpha^{-1} + 1}, \quad (1)$$

where g_ms and C_{gs}s are transistor small signal transconductances and gate-source capacitances, respectively, M is the mutual inductance between L_g and L_d, and $\omega_\alpha = g_{m1}(1 + g_{m2}R)/(C_p + C_{gs2})$.

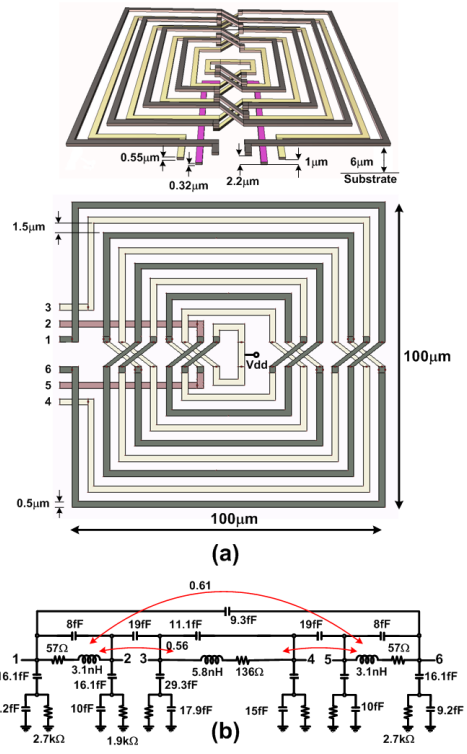

Fig. 6. Stacked L_g and L_d (only 9 turns out of 13 turns are shown). (a) Top and side views, and (b) the approximate equivalent lumped model.

From equation 1, the stability condition for the TIA in Fig. 3(d) can be found as

$$L_g \quad < \quad \frac{(g_{m1}M + C_{gs1}R)}{\omega_\alpha C_{gs1}}. \tag{2}$$

The input referred current noise due to the channel thermal noise of M_1 is

$$\overline{I^2_{in,n,M1}} =$$

$$4kT\gamma g_{d0,1}(\frac{\omega}{\omega_\alpha})^2(\frac{\omega^2 M^2 g^2_{m1}R^2_d + (R_d + L_d/\omega_\alpha)^2}{R^2_d + \omega^2 L^2_d}). \tag{3}$$

From equation 3, it can be observed that high feedback gain and low photodiode capacitance are desired to reduce the effect of the noise of M_1 on the input referred current noise of the TIA. Also, despite bandwidth improvement, large L_g increases the noise contribution of M_1 and may cause instability. The input referred current noise of M_2 can be written as

$$\overline{I^2_{in,n,M2}} \quad = \quad 4kT\gamma g_{d0,2}(\frac{\omega^2(C_p + C_{gs2})^2}{g^2_{m1}}). \tag{4}$$

Considering only the drain noise of M_1 and M_2, from equations 3 and 4, the TIA equivalent input referred current noise will be

$$\overline{I^2_{in,n,TIA}} \quad = \quad \overline{I^2_{in,n,M1}} + \overline{I^2_{in,n,M2}}. \tag{5}$$

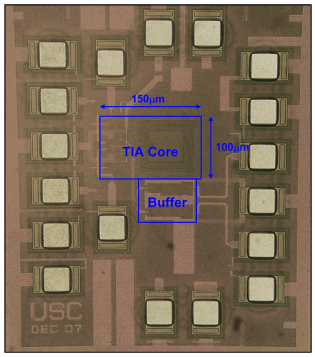

Fig. 7. Chip microphotograph

The TIA power consumption when devices are assumed to operate in the square-law region is given by

$$P \quad = \quad \frac{V_{dd}L}{2\mu C_{ox}}(\frac{g^2_{m1}}{W_1} + \frac{g^2_{m2}}{W_2}). \tag{6}$$

At this point, the TIA in Fig. 3(d) can be designed by solving the following optimization problem: Minimize the equation 6 to find W_1, W_2, L_d, L_g, M, R_d, and R subject to the following constraints:

1) V_{dd} and the photodiode parasitic capacitance C_p are known. M_1 and M_2 are operating in saturation region and have the minimum channel length L.
2) C_{gs} of a device can be approximated as $C_{gs} \approx \alpha W$ where α is technology dependent and known.
3) Gain constraint: $R_d > Z_{TIA,desired}$.
4) Bandwidth constraint: $BW > BW_{desired}$.
5) Noise constraint: total input referred current noise = $N_B = \int_{BW} \overline{I^2_{in,n,TIA}} df < N_{B,desired}$.
6) Stability constraint: equation 2 needs to be satisfied.

Optimum parameters resulting from the above optimization procedure are considered as the initial values for SpectreRF simulation and further optimization.

Figure 5 shows the differential version of the TIA in Fig. 3(d) which has been implemented in $0.13\mu m$ CMOS. An additional resistive network consisting of $R_2 = 5k\Omega$ and $R_1 = 50\Omega$ at the TIA input provides impedance matching for accurate differential measurements of the TIA without affecting its frequency response. Note that the input of the TIA is not designed to be 50Ω matched. $C_p = 200fF$ emulates the photodiode capacitance and pairs of pads $(IN+/IN-)$ are connected to the differential input of the TIA to capture the effect of the pad parasitic capacitance in the measurement. The output of the TIA is connected to a buffer stage which drives the 50Ω measurement instruments. The differential wideband TIA consumes 1.8 mW to provide 57 dBΩ transimpedance gain. The buffer consumes 9.1 mW.

As it was mentioned before, L_d and L_g were stacked to save the chip area. Figure 6 shows these two stacked

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

Ref.	BW or Data Rate	Z_T $[dB\Omega]$	Noise $[pA/\sqrt{Hz}]$	C_{in} [fF]	Chip area $[mm^2]$	Power [mW]	Technology
[5]	13.4 [GHz]	52.8	28	220	0.01	2.2	0.08 μm CMOS
[3]	10 [Gb/s]	59	25	150	0.41	18	0.18 μm CMOS
This Work	10 [Gb/s]	57	<35 up to 10GHz	370	0.015	1.8	0.13 μm CMOS

differential inductors that are implemented on the top two metal layers. A total area of $100\mu m \times 100\mu m$ was arbitrarily chosen as design constraint. The series resistance of L_d only affects the TIA DC transimpedance. Therefore knowing the series resistance of L_d, R_d can be picked such that the DC transimpedance gain requirement is satisfied. Also assuming a resistance R_g in series with L_g to model the finite quality factor for L_g, analysis shows that as long as $R \gg R_g$, the quality factor of L_g does not effect the performance of the TIA. Note that R determines the gain of the feedback amplifier and usually is set to a relatively large value. Since the TIA performance is relatively insensitive to the quality factors of L_d and L_g, very thin traces were used to produce high inductance per area to further reduce the chip area. In Fig. 6, ports 3 and 4 correspond to differential inductor L_d, and ports 1/2 and 5/6 correspond to L_g. The whole structure was simulated in Zeland's IE3D.

IV. MEASUREMENT RESULTS

The TIA is fabricated in the IBM8RF-LM $0.13um$ CMOS process (Fig. 7). Differential probed measurements are reported. The effect of input resistive divider, that is only meant to provide matching for differential measurements, is de-embedded from the measured S-parameters to derive the TIA S-parameters and transimpedance (Fig. 8).

The noise figure of the TIA was measured using a spectrum analyzer with noise figure measurement personality. The equivalent input referred current noise of the TIA was calculated by de-embedding the effect of the resistive network (Fig. 9). The performance of a few recently reported TIAs is compared with this work in Table I.

V. CONCLUSION

This paper demonstrates a low-power high-gain wideband TIA that is based on a common gate stage with active feedback. Vertically stacked coupled inductors are used to enhance the bandwidth through shunt peaking and creation of complex poles. A design optimization that minimizes the TIA power consumption given the photodiode capacitance, TIA gain, bandwidth, and total input integrated noise was employed.

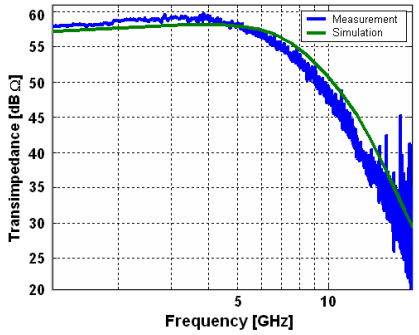

Fig. 8. Measured and simulated transimpedance of the fabricated TIA.

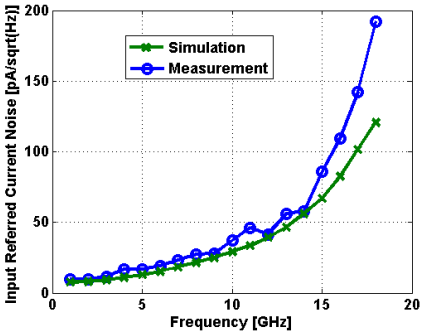

Fig. 9. Measured and simulated input referred current noise of the fabricated TIA.

ACKNOWLEDGMENT

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