10Gb/s Inverter Based Cascode Transimpedance Amplifier in 40nm CMOS Technology

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***Abstract*— This work presents the design and performance of a 10Gbit/s transimpedance amplifier (TIA) implemented in a 40nm CMOS technology. The introduced TIA uses an inverter based cascode feedback (Inv-Cascode-TIA) with shunt feedback resistor. The TIA is followed by an one-stage single-ended common-source amplifier (CS), a two-stage differential amplifier and a 50Ω differential output driver to provide an interface to the measurement setup. The optical receiver shows an optical sensitivity of –21.4dBm for a BER= 10^{-12}. The transimpedance amplifier achieves a transimpedance gain of 55.3dBΩ, 8GHz bandwidth with 0.45pF total input capacitance. The power consumption of the TIA is 3.01mW and the complete chip dissipates 19.25mW for a 1.2V single supply voltage. The complete optical receiver has a 69.2dBΩ transimpedance gain and 7GHz bandwidth.**

I. INTRODUCTION

The optical fiber links are the best candidates to deal with large data volumes because of their superior performances compared to conventional electrical links. CMOS silicon integrated circuits appear to be the best technology that can achieve the required level of integration with reasonable speed, cost, and yield. As CMOS technology is downscaled, the peak transit frequency of the transistors is increased. The design of CMOS circuits at 10GHz should be easy with the 200GHz transit frequency for 40nm CMOS technology. However, the transit frequency is usually measured at a device biased at the maximum supply voltage which is not practical for analog circuit design where the transistors are biased with around half of the maximum supply voltage. As a result, the transit frequency of a transistor at a practical bias will be lower than 100GHz. The supply voltage of nanometer CMOS chips must be decreased to prevent destructive breakdown in the MOSFETs and to save power in digital circuits. The threshold voltage is lowered by a smaller ratio than the power supply voltage which limits the circuits cascading to increase the total gain and obtaining the maximum speed. Another drawback that the transistor output resistance decreased with down scaling the transistors, as a result the intrinsic voltage gain of a transistor will be smaller [1]. Therefore, more than one stage is needed for high-gain high-speed amplifiers, which increase the overall power consumption and may affect the amplifier stability [1, 2].

The TIA is the most critical building block at the optical receiver side in an optical communication system. The TIA sensitivity essentially depends on the input-node capacitance, the feedback resistor and the transconductance of the input transistors of the amplifier. To obtain a high sensitivity despite the high input-node capacitance, the transconductance of the input transistors and therefore the current through them has to be maximized for minimum noise. TIAs which use CMOS inverters were studied extensively in the past years [3-8]. The advantage is the use of N- and P-MOSFETs at the input is to achieve higher gain due to larger effective transconductance [3]. The inverter structure shows a better noise behavior than a simple common-source amplifier (CS). The input referred noise of the amplifier, which mainly consists of the thermal drain current noise of the input transistors, is divided by the sum of the transconductances of the input transistors (of N- and P-MOSFETs) in the case of the inverter, whereas the drain current noise of the CS amplifier, consisting of the thermal noise of the transistor and the resistor noise, is only divided by the transconductance of the single transistor [4].

To achieve a high amplifier gain this requires devices that have large size to provide a sufficient transconductance. Unfortunately, large parasitic capacitance is also associated with large devices. The gate–source capacitances of the devices add directly to the input capacitance. Also the gate–drain capacitance appears directly across the feedback resistor and due to the Miller effect; this capacitance can be the limiting factor with regards to bandwidth and can dominate over the photodiode capacitance [5].

A one-stage TIA has a too low gain; also, the already noted disadvantage of the Miller capacitance occurs. Using more than one amplifier stage, the circuits become more unstable and difficult to use [1, 2]. A system with feedback is stable if the second pole's frequency is more than 2 times larger than the gain-bandwidth product which requires a large safety margin in the design. This results in circuits with either limited speed or limited transimpedance gain.

The open-loop gain is lowered by the diode-connected MOSFETs to ensure stability [6, 7]. The process dependent ratio of the mobilities appears only as a square root. The optimization of transistor sizing can limit the effect of the mobility variation [7].

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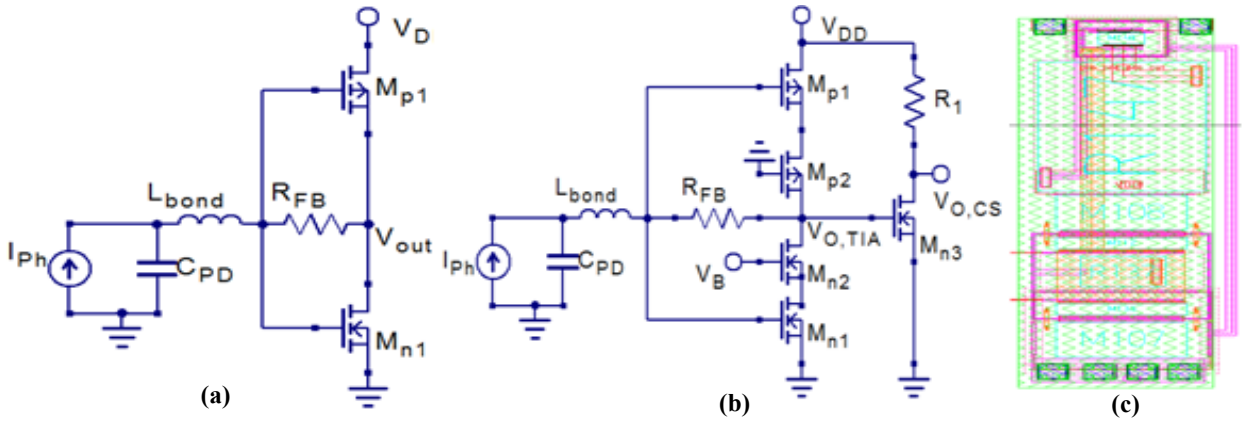

Fig,1 (a) Conventional inverter based TIA circuitry , (b) circuitry of the proposed Inv-Cascode-TIA with CS post amplifier, and (c) layout of the TIA with the single ended post amplifier

The disadvantages of this topology are that the additional diode-connected MOSFETs are always ON and always lower the gain of the amplifier. This increases the input referred noise due to lowering the gain and the additional added noise. The diode-connected MOSFETs are modified and MOSFET switches are added in [8]. At low input optical power the switches are OFF, so the diode-connected MOSFETs are disconnected from the amplifier. The amplifier gain is higher and no additional noise comes from diode-connected MOSFETs. At higher input optical power the control signal has to be increased to connect the diode-connected MOSFETs to the amplifier. This reduces the open loop gain to ensure stability.

A voltage-gain stage employing the cascode configuration can be used to boost the voltage-gain with no further degradation of bandwidth from the parasitic capacitance [3].

A folded cascode amplifier was introduced in [2]. The principle of this circuit has been known from operational amplifiers. Such a circuit has the advantage to work at low voltages and it has the advantage of a cascode stage increasing the bandwidth. Therefore, it is suitable for high-speed CMOS circuits at low supply voltages.

A three stage inverter based TIA where only one of the two transistors in the first stage was cascoded was introduced [9]. This amplifier benefits from the high output resistance of the cascode and the sum of the inverter MOSFETs transconductance, resulting in a higher gain. The TIA in [9] has a bandwidth of 280MHz, maximum transimpedance gain of 2.5kΩ, 85dB dynamic range, 220nA equivalent input noise current and a high maximum input current (4mA) overdrive capability) for use with a monitor photodiode.

A three-stage inverter-based TIA with a photodiode and pad capacitance of 60fF, and a photodiode responsivity of 0.7 A/W, is designed for a transimpedance gain of 4 kΩ, a 7 GHz bandwidth, and is sized to achieve a BER of 10^{-12} [10].

The proposed TIA employs an inverter based cascode to achieve a higher bandwidth at lower power consumption than with the normal CS-TIA and a better sensitivity than with the conventional inverter based TIA.

II. Optical Receiver Circuitry

A. *The Proposed Inverter Based Cascode TIA*

Figure 1 (a) shows the circuitry of the conventional inverter based TIA. From the small-signal model the transimpedance gain is given by:

$$Z_{T,inv}(0) \approx \frac{A_{inv} \cdot {R_{FB}}^2}{(R_{FB} + r_{ds,p1}//r_{ds,n1})(A_{in`v} + 1)} \quad (1)$$

Where $A_{inv} = (g_{m,n1} + g_{m,n2}).r_{ds,p1}//r_{ds,n1}$ (2)

$$BW_{inv} \approx \frac{1 + A_{inv}}{2\pi R_{FB}(C_{PD} + C_{PAD} + C_{gs,n1,p1} + C_{gd,n1,p1} \cdot (1 + A_{inv}))} \quad (3)$$

The main advantage of the inverter based TIA is its higher gain A_{inv} compared to the TIA with CS amplifier. Fig. 1 (b) shows the circuitry of the proposed Inv-Cascode-TIA where two transistors NMOS and PMOS (M_{n2} and M_{p2}) are added in series with the inverter transistors M_{n1} and M_{p1}, respectively where V_B is selected to be 0.9V for optimum performance. The transimpedance gain is given by:

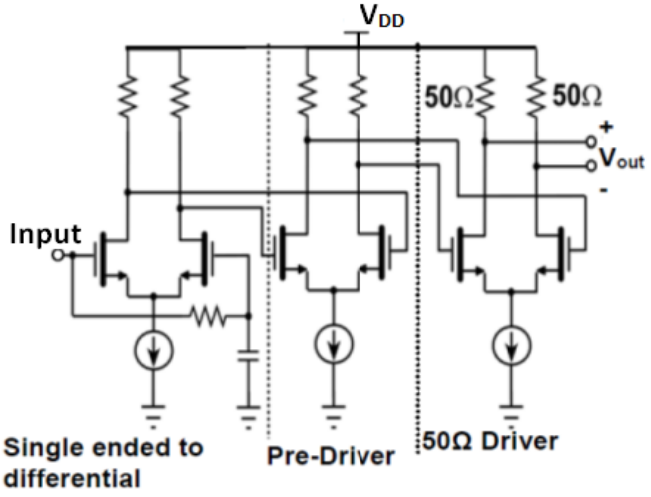

Fig.2: Single ended to differential converter, differential post amplifier and 50Ω output driver

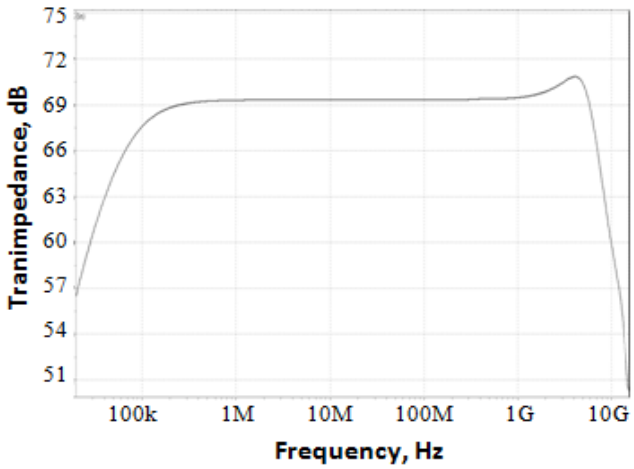

Fig.3: Post layout simulated optical receiver frequency response.

$$Z_{T,invC}(0) \approx \frac{A_{invC} \cdot R_{FB}}{(A_{invC}+1)} \quad (4)$$

The voltage gain of the cascode inverter becomes:

$$A_{invC} = (g_{m,n1} + g_{m,n2}).(r_{o1}//r_{o2}) = (g_{m,n1} + g_{m,n2}) \cdot \left[(g_{m,n2} \cdot r_{ds,n2} \cdot r_{ds,n1})//(g_{m,p2} \cdot r_{ds,p2} \cdot r_{ds,p1})\right] \quad (5)$$

$$BW_{invC} \approx \frac{1 + A_{invC}}{2\pi R_{FB}(C_{PD} + C_{PAD} + C_{gs,n1,p1} + C_{gd,n1} + C_{gd,p1})} \quad (6)$$

Due to the high output resistance of the cascode implementation the voltage gain of the cascode structure is higher than that of the regular inverter, compare equation (2) and (5). The transimpedance gain of the Inv-Cascode TIA $Z_{T,invC}$, equation (4) is a little bit higher than the transimpedance gain $Z_{T,inv}$ of in equation (1) because of its higher voltage gain.

The bandwidth of the inverter based cacode TIA BW_{invC} `in equation (6) is much higher than the BW_{inv} introduced in equation (3) because of two reasons, first, the higher cascode voltage gain. The second is the Miller capacitance effect for Cgd which is amplified by A_{inv} at the input node, see equation (3).

A comparison by simulation is performed to confirm the better performance of the presented Inv-Cascode-TIA compared to the inverter based TIA. Both inverter based TIA and Inv-Cascode-TIA were implemented in the 40nm CMOS technology and the transistor sizing was optimized to reach the maximum achievable bandwidth at using the same feedback resistor $R_{FB} = 635\ \Omega$. The maximum achievable bandwidth for the inverter based TIA is 4.2GHz and transimpedance gain is 510Ω at 2.1mA biasing current. Whereas the Inv-Cascode-TIA achieves 8GHz bandwidth and 585Ω transimpedance gain at 2.51mA biasing current.

B. Post Amplifier and Output Driver

There is a need for a post amplifier and for a 50Ω driver to have enough gain and to interface to the measurement setup. The output buffer provides enough driving capability for the 50Ω input measurement units. Fig. 2 shows the circuit diagram for the post amplifiers and the 50Ω driver. The differential output stage is better than a single-ended one with respect to common mode rejection and power supply noise. The Inv-Cascode-TIA's single-ended output is fed to a CS amplifier which makes amplification and level shifting to the input of the converter (Fig. 2) in front of the differential post amplifier (from 0.6V to 0.9V). The second input of the single-ended to differential converter is biased through a low-pass filter coming from the TIA output.

The next stage after the first differential post amplifier is a pre-driver stage to increase the gain and make the interface to the 50Ω driver. The last stage in the optical receiver is a 50Ω differential output driver to make the interface between chip and the measurement setup.

III. POST LAYOUT SIMULATION RESULTS AND DISCUSSION

The proposed optical receiver has been integrated in a 40nm CMOS technology with one single supply voltage 1.2V. The optical receiver is optimized for an off-chip InGaAs photodiode with 250fF capacitance and a responsivity of 1A/W for 1.55µm light. The ESD protection and input pad have together a 200fF capacitance. The bonding wires are modeled by 0.7nH inductors.

The Inv-Cascode-TIA alone consumes 3.01mW, and the total chip power dissipation is 19.25mW.

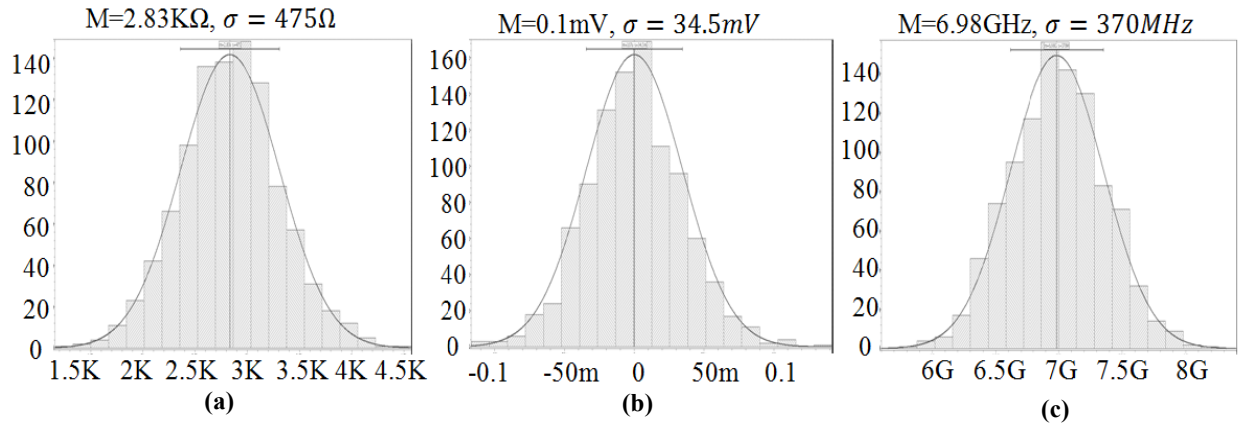

Fig.4: Monte-Carlo simulation for the optical receiver (a) transimpedance gain, (b) output voltage offset and (c) bandwidth are calculated for 1000 Monte-Carlo runs.

The active chip area of the complete optical receiver is 0.09mm^2.

The frequency response of the optical receiver obtained with post layout simulation is shown in Fig. 3. The optical receiver has a lower cut-off frequency of 70 kHz, while the optical receiver bandwidth is equal to 7GHz. The overall transimpedance is 69.2dBΩ. The Inv-Cascode-TIA itself has a bandwidth of 8GHz and a transimpedance value of 55.3dBΩ.

The effect of the process variation on the optical receiver performance based on Inv-Cascode-TIA is studied using Monte-Carlo simulation. The optical receiver's transimpedance gain, output voltage offset and bandwidth are calculated for every Monte-Carlo run up to 1000 runs, see Fig.4. Then the mean value for these 1000 values of the transimpedance gain, offset voltage, and bandwidth are calculated to be 2.83kΩ with 475Ω standard deviation, 0.1mV with 34.5mV standard deviation, and 6.98GHz with 370 MHz standard deviation, respectively.

The average input referred noise current density is 12.3pA/√Hz and the integrated input referred noise current is 1.01μA. A sensitivity of -21.4dBm is obtained for the presented optical receiver for BER=10^{-12} at a data rate of 10Gbit/s. Figure 5 shows the eye diagram at 10Gbit/s with PRBS=2^{15}-1 and an input photodiode current of 10μA.

Table I compares the post-layout simulated performance of the presented Inv-Cascode-TIA along with other recently published 10Gb/s TIAs in CMOS technology. The presented TIA shows superiority in terms of Figure of Merit (FoM) which is defined by [11]:

$$FoM = \frac{Gain(\Omega).BW(GHz).C(pF)}{Power\ Dissipation(mW).Input\ Noise(\mu A)} \quad (7)$$

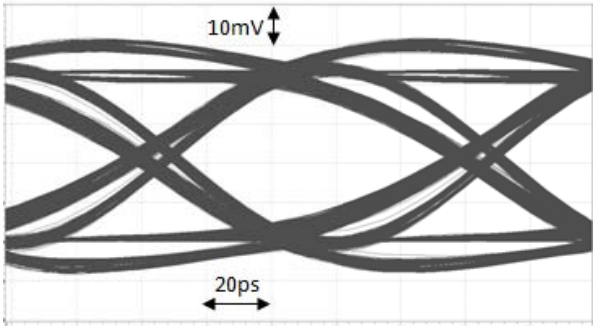

Fig.5: Eye diagram of the optical receiver at a data rate of 10Gbit/s, PRBS 2^{15}-1 and an input current of 10μA

Table I. Comparison with recently published 10Gb/s TIAs

Design	[13]	[12]	[11]	This Work
CMOS Technology	130nm	40nm	40nm	40nm
Supply Voltage	2V	0.95V	1.1V	1.2V
TIA Gain	62dBΩ	71.8dBΩ	47dBΩ	55.3dBΩ
Bandwidth	6GHz	7GHz	8GHz	8GHz
Sensitivity@ BER=10^{-12}	-15dBm	-15dBm	-19dBm	-21.4dBm
Input Capacitance	0.25pF	40fF	0.45pF	0.45pF
Power Consumption	98mW	3.95mW	2mW	3.01mW
F.O.M	12.52	161.26	213.16	692.1

CONCLUSION

A 10Gb/s high sensitivity transimpedance amplifier in 40nm CMOS is presented. The presented Inv-Cascode-TIA shows a 12.3pA/√Hz average input noise current density and 3.01mW power consumption. The introduced Inv-Cascode-TIA shows a high performance compared to the conventional inverter based TIAs due to the higher output resistance and reduction of the Miller capacitance at the input node. By using the Inv-Cascode-TIA an optical receiver with higher bandwidth and sensitivity can be designed at low power consumption.

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