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Low Noise And Low Power Transimpedance Amplifier using Inverter Based Local Feedback

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***Abstract*- The large data that needs to be transferred has led to an high usage of optical communication systems. In optical communication system Transimpedance amplifiers (TIA) plays a very important role. TIA are used at thr receiver side of optical communication system to convert the current obtained from photodiode to amplified voltage . Thus obtained appropriate voltage signal is processed in further stages of communication system. A TIA should have high bandwidth and low power consumption but due to large photodiode capacitance it is difficukt to achieve. This paper presents a transimpedance amplifier (TIA) circuit with high gain and wide bandwidth with vey low noise effect.Author has used inverter based feedback system with always on PMOS and NMOS to reduce the leakage current for nanoelectronics application and increase the bandwidth for wide band and highspeed application.With this topology achieved -3db bandwidth is 8.2 GHz with high gain of 53.2dBohms. The noise effect is 23.36pA/sqHz i.e very low compared to other topologies in 180nm design. The author had used current mirror instead of constant current source thus power dissipation is also very low i.e 3.6mW. Thus this TIA can be used efficiently in low power high band 10Gb/s applications**

Keywords : Transimpedance Amplifier (TIA), Differential Input, Regulated Gain Cascode(RGC), Small Signal Model, Bandwidth, CMOS

I. INTRODUCTION

The high amount of data transfer needs high speed communication system. Optical communication system mainly have three parts: (i) transducer-a signal converter fromelectronic signal to optical signal-(ii) transmission channel using optical fibre (iii) a sensor to detect optical signal and convert in current signal i.e a photodiode.[1-5] When long distance communication is to be performed mostly light signal degrades, thus quality attenuates. To compensate for it a solution is to be designed. A high intensity photodiode with high sensitivity to light should be used for proper transfer in long distance. The electric current generated from these light signal must be amplified properly and converted to voltage signal with low noise for further processing blocks. This amplification and conversion of current signal in to voltage signal is done by transimpedance amplifier (TIA)[6-8] Thus a low noise high tolerance TIA is needed for the system .[10-12] In this paper author has designed a low noise, low power and high gain, large bandwidth TIA for 10Gb/s applications.

Further section II of the paper includes literature survey followed by proposed methodoly in sectionIII. Section IV presents results and analysis and finally the conclusion of the paper.

II. LITERATURE REVIEW

The most important building block in optical communication is TIA at receiver end because it directly effects the systems speed and noise performance. [21, 22].Now a days silicon deep-submicron CMOS based technologies are becoming more efficient because of their less chip cost and high integration density .The main limitation imposed on TIA is due to large photodiode capacitance effect which leads to reduction in bandwidth. Various work has been done in these area to help to reduce the effect of photo diode capacitance.

Inductive peaking had played great role in increasing bandwidth as well as reducing noise. [23–25]. However; the large chip area consumption due to inductor makes the overall circuitry very expensive. Moreover these inductors also induce inductor coupling thus high chance of crosstalk .Apart from that high group delay fluctuation can cause a problem .Capacitive degeneration is also a method to increase the bandwidth by adding a zero but this leads to lower DC gain in circuit [26]. The Common Gate (CG) topology reduces the effect of high input parasitic capacitance on the bandwidth [27]. But, while using the nano scale devices the complete isolation is not possible due to poor device characteristics . Modification of the conventional CG-TIA to a regulated cascode (RGC) [28] can reduce the input impedance or by adding an active local feedback can also reduce the input impedance to increase the bandwidth. [29]. Main drawback of RGC is the noise performance which is reported as worse then Common Source (CS) topology. [30].

The proposed TIA have used an inverter based local feedback to reduce the input impedance with an NMOS as main amplifier to achieve a high bandwidth like the conventional RGC-TIA with improved noise performance and better power consumption.

III. METHODOLOGY

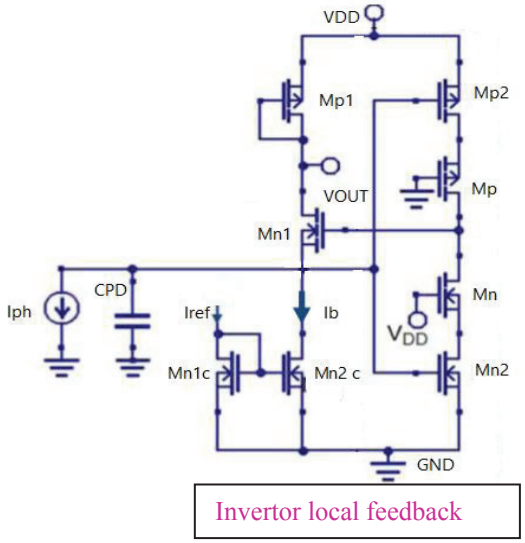

Fig. 1. The Proposed Transimpedance amplifier

Figure 1 displays a schematic of the proposed method. Here Mn1 act as main amplifier. The input given to Mn1 and inverter both. Here inverter act as local feedback. Output from inverter is given to gate of Mn1. And final output is taken from drain of Mn1.The inverter-based local feedback increases the gain and bandwidth by reducing the input impedance. In inverter always on PMOS Mp and always on NMOS Mn is added to increase the tolerance of inverter thus reducing the overall leakage current for nono-technology applications of the circuit.

Here Cpd is the photodiode capacitance and Iph is the photodiode current which is fed as input to TIA. Mn1c and Mn2c act as current mirror and is used instead of current source so that total power dissipation and area will reduce.

Mp1 act as load resistor and resistance is equal to:

$$\frac{1}{\text{gm,p1}} \;//\; rds,p1 \qquad (1)$$

Here

gm: transconductance

rds : resistance acting between drain to source.

equation of the Zin is simplified to :

$$Zin \approx \frac{1}{\text{gmn1}(1+AC1)} \qquad (2)$$

Where Ac1 is the voltage gain from the inverter-based local feedback:

$$AC1 = (gm,n2 + gm,p2).ro2 \qquad (3)$$

As Ac1 increaes input impedance reduces thus gain will increase. The impedance in input and the total capacitance of the Mn1 source is related to the bandwidth of the TIA:

$$Cin\_ \text{ proposed ckrt} = CPD + CESD + CPAD + Cgs,p2, n2 +(cgsn1 + cgd,p2,n2) \qquad (4)$$

Bandwidth of the system is derived as

$$BW = \frac{1+\text{gmn1 (ACS+1)}}{2\pi\, Cin_{proposed}ckrt} \qquad (5)$$

Noise Analysis

The input current coming from the photodiode is very small. Noise is a critical parameter of the TIA. The total input-referred input noise can be determined by determining the individual sum of noises[1]. The Mp2 and Mn2 are the transistors of the inverter circuit. The noise from the inverter feedback circuit can be calculated as:

$$I^{2,}_{inv} = \frac{1}{(gMp2+g\,Mn2)^2} \quad (4KT_{\omega}{}^2Cin^2(rg_{Mp2}+ rg_{Mn2}) + \frac{Kf}{LCox}(g_{Mp2}/W2) + (g_{Mn2}/W_2)) \qquad (6)$$

Here

k : process dependent constant

r: noise excess factor.

Cox: oxide capacitance

W, L : effective width and length.

T :temperature

g0: channel conductance when the drain-source voltage is zero

The noise generated by the Mn1 transistor is as follows:

$$I^2_{n,Mn1} = (1/(g_m{}^2_{n1}))(4KT\omega^2Cin^2(rg_{0n1}) + \frac{Kf}{Wn1LCox}(g^2_{n1}) \qquad (7)$$

The noise generated by the Mn1c transistor is as follows:

$$I^2_{n,Mn1c} = (1/(g_m{}^2_{n1c}))(4KT\omega^2Cin^2(rg_{0n1c}) + \frac{Kf}{Wn1cLCox}(g^2_{n1c}) \qquad (8)$$

The noise generated by the Mn2c transistor is as follows:

$$I^2_{n,Mn2c} = (1/(g_m{}^2_{n2c}))(4KT\omega^2Cin^2(rg_{0n2c}) + \frac{Kf}{Wn2cLCox}(g^2_{n2c}) \qquad (9)$$

Each part of the input noise of the proposed TIA is calculable by the individual amount of the noise. The total noise can be calculated as follows

$$I^2_{n,total} = I^2_{n,inv} + I^2_{n,Mn1+} I^2_{n,Mn1c} + I^2_{n,Mn2c} \qquad (10)$$

Consider $4KT_{\omega}{}^2Cin^2$ term as 'A' and $\frac{Kf}{Wn1LCox}$ term as 'B'.Apply equation 7-9 in equation 10. Then the total noise obtained as equation 11.From the $I^2_{n,total}$ it can be analyzed that the noise can reduce by the aspect ratio of Mn1. Noise will increase concerning the increase in the frequency:

$$I^2_{n,total} = \frac{1}{(gMp2+g\,Mn2)^2}(A(rg_{Mp2}+ rg_{Mn2}) + \frac{Kf}{LCox}(g_{Mp2}/W2) + (g_{Mn2}/W_2)) + (1/(g_m{}^2_{n1}))(A(rg_{0n1}) + B.(g^2_{n1}) + (1/(g_m{}^2_{n1c}))(A(rg_{0n1c}) + B.(g^2_{n1c}) + (1/(g_m{}^2_{n2c}))(A(rg_{0n2c}) + \frac{Kf}{Wn2cLCox}(g^2_{n2c}) \qquad (11)$$

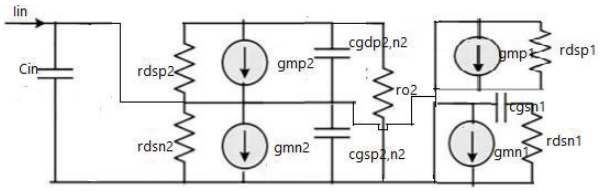

Fig. 2. The small-signal diagram

IV. Simulation Results

The proposed circuit is simulated using cadence virtuoso 180nm TSMC technology node. The parameters used are given in table 1.

The frequency response of the proposed TIA is shown in figure 3. From this obtained bandwidth is 8.2 GHz and transimpedance gain is 53.2dBohms. Figure 3 also depicts the comparison of the post layout and pre layout Ax analysis output. It can be seen that -3dB bandwidth is not much varied and gain is same for both. Thus circuit performance is good.

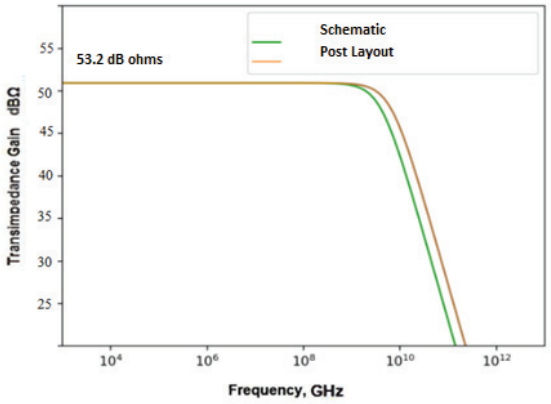

Fig. 3. The frequency response of the Proposed TIA

Fig 4 and fig 5 represents the monte-carlo simulation for gain and bandwidth of the circuit respectively.

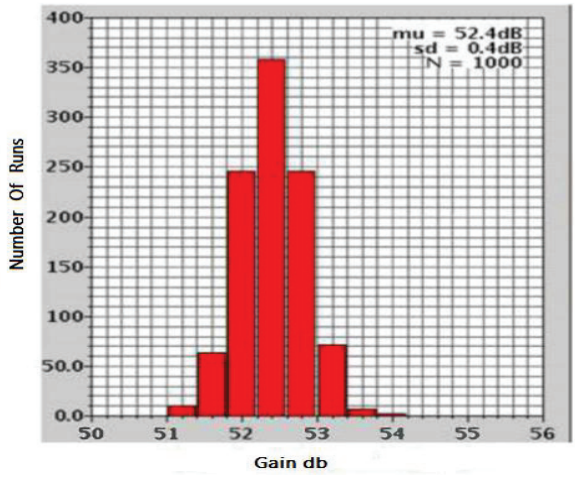

Fig. 4. The gain variation with the monte Carlo analysis

Number of samples taken were 1000 and thus it is shown that standard deviation is very low in gain of 0.4dB only and of bandwidth is also very low i.e.512.8MHz only. Thus circuit performance is stable with reference to gain and bandwidth

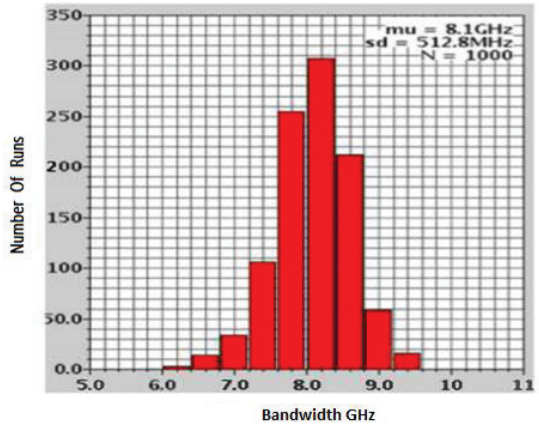

Fig. 5. The bandwidth result from the Monte Carlo analysis

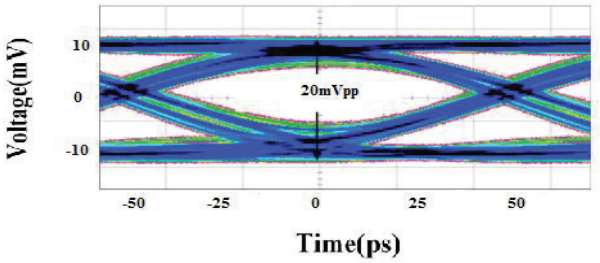

Fig. 6. The eye diagram result of the TIA

Figure 6 shows the eye diagram of proposed circuit with peak to peak voltage of 20mV this wide eye opening thus signal quality will be good, here input current was 16uA.

V. Comparison

The comparisons of the proposed system concerning the previous systems are shown below in table 2.

Author had defined the figure of merit of the circuit, it can be calculated from the equation 12:

$$FOM=(\text{Gain dB}\Omega \times \text{Bandwidth GHz})/(\text{power mW}) \quad (12)$$

It is clear from the comparison table that FOM of proposed circuit is very high as compared to other circuits. Thus proposed circuit had achieved proper trade off between gain bandwidth and power consumption.

VI. Conclusion

The proposed TIA performs very good with low power consumption and high bandwidth. When compared with conventional RGC topology its performance is very high. This topology helps in achieving low input impedance with the help of local inverter based feedback, high tolerance for leakage current due to always on PMOS and NMOS. Furthermore current mirror as current source is improving the power consumption and reducing the chip are as well. This circuit can be used efficiently for low power IOTs applications. The increasing need of high speed optical communication system can be achieved using this topology

TABLE I. PARAMETERS USED

Technology	180nm
Aspect Ratio	Mp1=10um Mn1 = 30um Mp2=Mn2 = 80um
Capacitance	450pF
Supply Voltage	1.8v

TABLE II. COMPARISON OF THE OUTPUT BETWEEN SUGGESTED TIA AND OTHER TECHNOLOGIES.

	[1]	[3]	[9]	[20]	[22]	Proposed TIA
Technology nm	180	130	180	180	180	180
Voltage supply V	1.8	1.5	1.8	1.8	1.8	1.8
Gain dBΩ	51.4	50	46	54.3	50	53.2
Bandwidth GHz	7.3	2.9	4	7	6.5	8.2
Power mW	4.3	45.6	31.5	29	14	3.6
Noise(pA/√Hz)	27	51.8	18	5.9	-	23.36
FOM	87.20	3.17	5.84	13.10	23.21	121.17

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