A High Performance TIA Design in 40 nm CMOS

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***Abstract*—In optical communication systems, transimpedance amplifiers (TIAs) play a critical role as they are used in the front end of receivers to sense the optical inputs thereby converting them into electrical signals. In this paper, a low noise, high gain, and low power TIA is presented in 40 nm CMOS technology. To compensate for the low intrinsic gain of the technology, a structure, which comprises a shunt-shunt feedback amplifier for the first stage and two post-amplifiers for the following stages are designed. Active inductive loads are employed to extend the bandwidth. Post-layout simulation results show that the designed TIA has a bandwidth over 5 GHz, a transimpedance gain 75 $dB\Omega$, and an input-referred noise current in bandwidth less than 8 $pA/\sqrt{Hz}$. The total layout occupies a chip estate of 0.0052 mm^2 while the DC power consumption is found to be 7.15 mW without the output buffer, using a single 1.1 V power supply.**

I. Introduction

In the last two decades, wireless data throughput has strongly increased with multimedia applications and video streaming as mobile devices spread all around the world [1]. Consequently, the electromagnetic spectrum below 10 GHz may not be sufficient to mitigate the necessary demand for the mobile data traffic [2]. Wireless Optical Communication (WOC) is considered as an alternative since it has important features such as high bandwidth, low power, small sizes, and better channel security [3].

WOC receivers include transimpedance amplifiers (TIAs), which amplify the photo-detector current and convert it into a voltage at the front end. The TIA design is critical as it dominates the overall noise of the receiver. Shunt-shunt feedback structure is commonly used since it provides a low impedance at both the input and the output, which is a desirable feature for a current in-voltage out amplifier [4], [5]. Photodetector capacitance dictates the bandwidth and the stability in shunt-shunt feedback amplifiers. However, especially in short channel CMOS technologies, feedback amplifiers suffer from low loop gain. An alternative solution is to use a common base or common gate (CB-CG) open loop structure since they inherently have a small input resistance [6]. On the contrary, their drawback is the poor noise performance. Also, it is not possible to make the transimpedance gain high due to the voltage drop across the resistance at the drain terminal. Regulated-cascode structures may present a better performance, but their noise characteristics are not superior to that of the CB-CG TIA [4].

The main contribution of this study is to show that it is possible to design a low noise, high gain shunt-shunt feedback-based TIA while keeping the power consumption low by utilizing the benefits of the 40 nm CMOS technology. To boost the open-loop gain, two post amplifiers have been used after optimizing the transimpedance gain of the first stage such that the input-referred current noise is minimized. Shunt peaking is utilized to extend the bandwidth by using an active inductor. In the last stage, a buffer with 50 Ω output impedance is designed to drive the output pad capacitance and to provide the impedance matching necessary for testing purposes.

The paper is organized as follows: In Section II, the proposed TIA is explained with a description of subblocks and performance metrics. In Section III, the design flow is discussed. Section IV shows the post-layout simulation results. Finally, Section IV draws the conclusions and shows the comparison with other TIAs in CMOS technology at similar speeds from the literature.

II. Circuit Description

As seen in Fig. 1, the circuit is composed of a shunt-shunt feedback cascode stage as the main transimpedance amplifier, and two conventional cascode stages as the post amplifiers with a basic common source stage as the output buffer. All stages except the buffer have shunt-peaking loads to extend the bandwidth, which is provided by $M_{3\text{-}4,7\text{-}8,11\text{-}12}$. Gate resistors $R_{G1\text{-}4}$ are used to increase the electrostatic discharge protection on gate terminals as they are directly connected to power pads.

A. Discussion of Performance Metrics

In a shunt-shunt feedback amplifier, when the open loop voltage gain of the forward path amplifier is large enough, the transimpedance gain is determined by the feedback resistance, whereas the bandwidth is determined by the total capacitance at the input C_T (the sum of the detector capacitance, C_D, and the input capacitance of the amplifier, C_{amp}), as well as the feedback resistor. The open loop voltage gain of the amplifier plays a significant role as it boosts the overall bandwidth because of the increasing loop gain. Expressions for the transimpedance gain and the overall bandwidth are given in (1) and (2) [5], where R_F is the feedback resistor, A_o is the open loop voltage gain, R_T is the DC transimpedance gain, BW is the 3-dB bandwidth, C_T is the total capacitance at the input.

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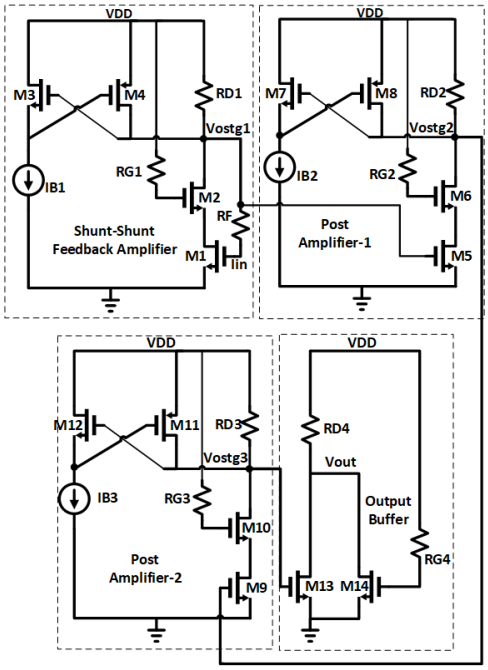

Fig. 1. The proposed circuit schematic.

$$R_T = \frac{A_o}{A_o + 1} R_F \tag{1}$$

$$BW = \frac{\sqrt{2A_o(A_o+1)}}{2\pi R_F C_T} \tag{2}$$

Another critical performance metric is the noise as TIAs are used at the front end of receivers. Minimum input-referred current noise can be acquired when the input transistor is sized such that its input capacitance matches the photodetector capacitance [7]. This condition suggests that $C_T = 2C_D$ should be satisfied for noise optimization.

Phase linearity, group-delay variation, and jitter are also important performance metrics. The pole quality factor (Q) affects the frequency and the transient response. There are two popular approaches involving Bessel and Butterworth-type responses, respectively. To achieve a small group-delay variation with no peaking in the amplitude response and a negligible amount of jitter, the Bessel-type response should be preferred since the Butterworth-type response has more group delay variation and produces more jitter [8]. In addition, the amplitude response is determined by the pole locations of the open-loop amplifier. Butterworth-type response can be achieved via pole splitting by a factor of $2A_o$, whereas the Bessel-type response requires the poles to be apart by approximately $3A_o$, which is hard to achieve in high-speed applications. Thus, in this design, the Butterworth-type approach has been preferred, which results in $Q = 1/\sqrt{2}$ and the corresponding non-dominant pole (the pole at the output of the first stage) of the open loop amplifier is given in (3) [5].

$$f_{nd} = \frac{2A_o}{2\pi R_F C_T} \tag{3}$$

B. Transimpedance Limit and Post Amplifiers

The transimpedance gain has a limit that is roughly proportional to the technology parameter f_t as seen in (4) [9]. Post-amplifiers are required to increase the gain with the cost of reduction in the total bandwidth. Therefore, the approach here is to have a dominant bandwidth in the shunt feedback stage and to keep the bandwidth of the post amplifiers as high as possible so that the total bandwidth would not be less than the design specification [5].

$$R_T \leq \frac{A_o f_{nd}}{2\pi C_T BW^2} \tag{4}$$

C. Bandwidth Extension Using Active Inductors

Inductors are generally used in narrow-band systems, but there are some applications, where they can be used for the purpose of bandwidth extension [10]. Unlike ideal passive inductors, active inductors consume real power, generate thermal noise and disturb the linearity. Thus, it is hard to design high performance oscillators and filters with them. Nevertheless, a simpler task like bandwidth extension can be carried out with active inductors, provided that their disadvantages are minimized and their structure is kept simple. Such an active inductor structure can be established through a cross-coupled transistor pair (such as the one in Fig. 1, formed by M_3 and M_4) [11], with its input impedance being given in (5). The bandwidth of the amplifier can be extended based on the location of the zero in the transfer function of this circuit.

$$Z_o = \frac{1}{g_{m2}}(1 + \frac{sC}{g_{m1}}) \tag{5}$$

D. Output Buffer

To drive the output pad capacitance and provide an output impedance of 50 Ω for the test environment, a simple common source stage with a gain around unity is designed. The overall bandwidth of the TIA is preserved based on this output buffer.

III. Design Flow

The design flow starts with the bandwidth requirement for a pre-specified detector capacitance. In this design, the bandwidth is aimed to be 5 GHz for a detector with 75 fF capacitance, which makes the total capacitance at the input 150 fF due to the capacitive noise matching requirement. The open loop voltage gain is assumed to be $A_0 = 3$ when the bandwidth is larger than 5 GHz. From (2), for $BW = 5GHz$, the transimpedance value is around 60 $dB\Omega$, which is not enough for the 70 $dB\Omega$ transimpedance requirement. Thus, two post-amplifiers have been employed, and to keep the bandwidth larger than 5 GHz, a 7 GHz bandwidth is allocated to the first stage, which enforces R_F to be equal to 750 Ω. In order to get a Butterworth-type response, the non-dominant pole f_{nd} must be around 8.5 GHz from (3). However, the realizable transimpedance according to (4) is then around 550

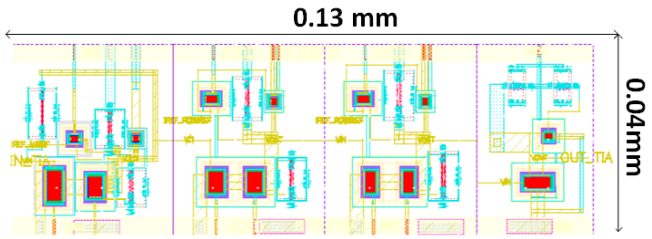

Fig. 2. The layout of the proposed circuit

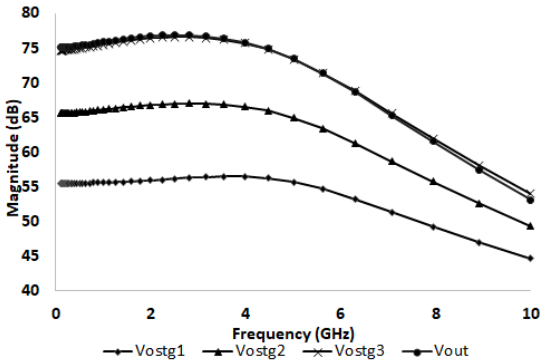

Fig. 3. The frequency response at the output of each stage.

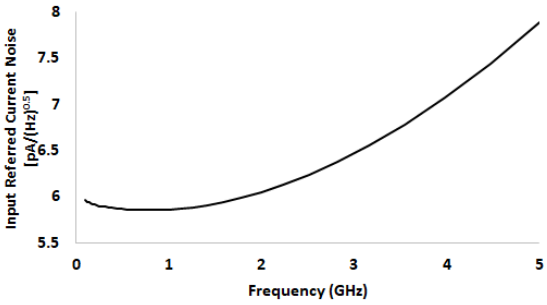

Fig. 4. The input referred noise current density.

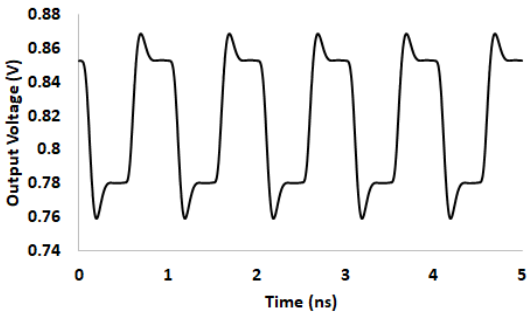

Fig. 5. The transient response for $I_{in} = 10\mu A$ @ $1GHz$.

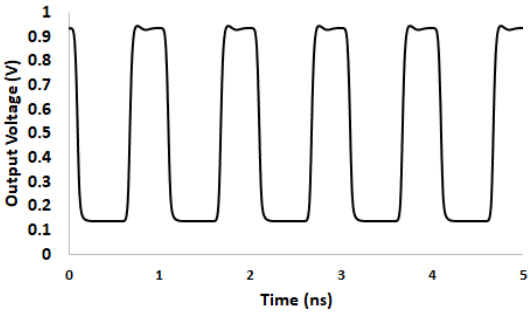

Fig. 6. The transient response for $I_{in} = 150\mu A$ @ $1GHz$.

Ω. To achieve the target gain, the necessary BW must be around 6 GHz for the first stage. The bandwidth extension load increases the transimpedance limit in (4), so the bandwidth requirement of 7 GHz for the first stage can still be met. Next, the channel length of M_1 is chosen as $2L_{min}$ (80 nm), and $W = 89$ μm for noise matching. Since the first stage is self-biased by the feedback resistor, the size of the input transistor and the drain resistance directly determine the DC current. The voltage gains of the post amplifiers are aimed to be around 10 dB so that the transimpedance gain target of 75 $dB\Omega$ can be accomplished. Finally, the buffer is designed such that it has a 50 Ω output impedance for the compliance with the test environment.

IV. Post-Layout Simulation Results

In this section, the post-layout simulation results are given. The simulations are performed using the TSMC 40 nm low-power (LP) process. The total DC current consumption is equal to 6.5 mA (excluding the buffer), which corresponds to 7.15 mW under a 1.1 V power supply. The total layout area is equal to 0.0052 mm^2, as shown in Fig. 2.

In Fig. 3, frequency response graphs have been provided for each stage. The transimpedance gain of the first stage is approximately 55 $dB\Omega$ (approximately 750 Ω) and the total transimpedance gain becomes 75 $dB\Omega$, after adding the post-amplifiers. The bandwidth equals to 6.5 GHz for the first stage and 5.2 GHz for the overall circuit. In Fig. 4, the input equivalent noise current density is given, which is between 5.85 $pA/\sqrt{Hz}$ @ 1 GHz and 7.9 $pA/\sqrt{Hz}$ @ 5 GHz. The integrated noise current equals to 0.5 μA.

In Fig. 5, the transient response corresponding to a square wave input with 10 μA amplitude at 1 GHz is shown. The output voltage is between 780 mV and 850 mV. It corresponds to a 76 $dB\Omega$ transimpedance gain, which is compatible with the AC gain. The circuit transient response for a saturating input of 150 μA amplitude at 1 GHz is demonstrated in Fig. 6.

In Fig. 7, the total frequency response is provided with and without the bandwidth extension load to prove its effectiveness. When the bandwidth extension load is not used, the bandwidth decreases by 30%, which is approximately equal to 3.6 GHz. In Fig. 8, the group delay performance is shown. It varies between 75 ps and 137 ps within the interval of 100 MHz to 5 GHz, thereby yielding a total of 62 ps long total group delay variation. Finally, Fig. 9 depicts the S_{22} graph, which indicates that the circuit matches to 50 Ω internal

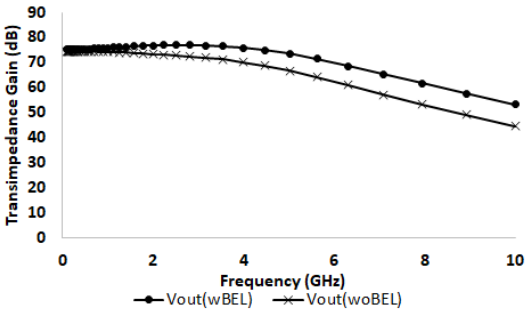

Fig. 7. The effect of the bandwidth extension load.

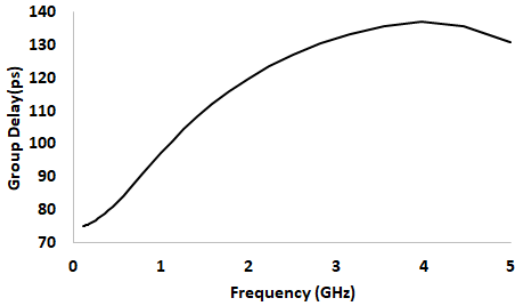

Fig. 8. The group delay vs frequency for the designed TIA.

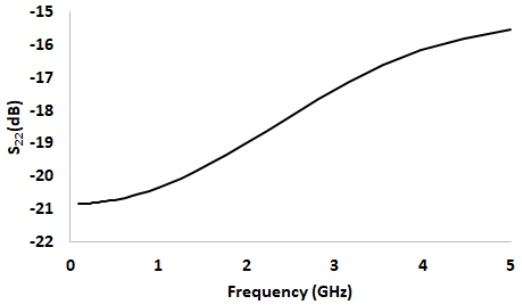

Fig. 9. S_{22} performance of the designed TIA for 50 Ω.

resistance of measurement instruments.

In Fig. 10, Monte Carlo simulation results on 1000 samples are shown for the bandwidth, transimpedance gain and the input referred noise along with their mean values and standard deviations. The worst case values of the bandwidth, gain and the noise are equal to $4.97\ GHz$, $69\ dB\Omega$ and $8\ pA/\sqrt{Hz}$, respectively. Additionally, corner analysis has been performed at $-40\ ^{\circ}C$ and $85\ ^{\circ}C$ assuming a 10% supply variation at the process corners. The worst-cases for the bandwidth, gain and the noise are observed as $4\ GHz$ at $85\ C^{\circ}$ and $1.2\ V$, with the slow-slow corner, $70\ dB\Omega$ at $85\ ^{\circ}C$ and $1.2\ V$, with the fast-fast corner and $8.3\ pA/\sqrt{Hz}$ at $85\ ^{\circ}C$ and $1\ V$, with the fast-fast corner, respectively.

To demonstrate the overall performance of the circuit figure of merit (FOM) in (6) is used, where the noise is represented by the input referred integrated noise current [12]. Table I

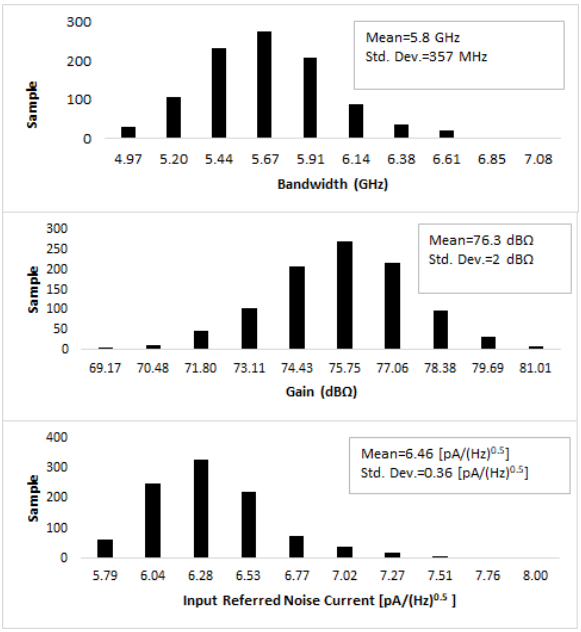

Fig. 10. Monte-Carlo simulation for bandwidth, gain and noise.

shows that the proposed circuit realizes a better FOM over the important TIAs in the literature. Moreover, the worst-case FOM based on corner simulations is found to be 319.45, which is still better than the results of the studies in Table I.

$$FOM = \frac{Gain(\Omega) \times BW(GHz) \times C_D(pF)}{Power(mW) \times Noise(\mu A)} \tag{6}$$

V. Conclusion

In this study, a high-speed transimpedance amplifier in 40 nm CMOS technology is presented. The aim of the design to concurrently achieve low noise operation and high transimpedance gain. The bandwidth extension load increases the bandwidth by 44% without damaging the noise performance and the power consumption. The design accomplishes its goals in a small chip area while consuming a relatively low amount of DC power.

TABLE I
Comparison with other TIAs from the literature

Design	[12]	[13]	[14]	[15]	This study
CMOS Technology (nm)	40	40	65	180	40
Transimpedance Gain ($dB\Omega$)	47	71.8	54	60.5	75
Bandwidth (GHz)	8	7	40	6.6	5.2
Noise ($pA/\sqrt{Hz}$)	22	27.5	19.8	10.4	6.9
Power (mW)	2.03	3.95	55.2	33.9	7.15
Detector Capacitance (pF)	0.45	0.04	0.05	0.25	0.075
F.O.M	281.92	161.262	4.55	103.1	613.63

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