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A Design of Analog C-Matrix Circuits used for Signal/Data Processing

Takayuki SUGAWARA, Yoshikazu MIYANAGA, Norinobu YOSHIDA
Graduate School of Engineering, Hokkaido University
Sapporo 060-8628, Japan
taka@ice.eng.hokudai.ac.jp

Abstract

Various calculation of matrices and vectors has been used in many digital signal processing systems. Although the calculation simply repeats multiplication and addition, the reiteration processing are usually heavy. Therefore, in order to calculate them with high speed, it is necessary to apply parallel procecccing. Although there is another issue that a circuit area becomes large in the case of digital LSI, a proposal analog circuit can realize multiplication and addition simultaneously with the simple structure which arranges capacitors in a matrix form. Furthermore, the vowel speech recognition system is designed using this circuit.

1 Introduction

Various calculation of matrices and vectors has been applied to many digital signal processing. When the matrix calculation is designed with digital LSI, the reiteration processing of addition and multiplication are usually employed. It is also possible to arrange these modules in a parallel/pipeline structure. However, the parallel/pipeline architecture requires many resources instead of high calculation speed. Accordingly the balance between speed and total design area should be considered[1],[4].

On the other hand, an analog circuit module has been used in mixed analog and digital circuits. The merit of analog circuits in LSI are mainly considered as the quite small size of a module and high speed processing. However, the analog module in LSI can not guaranteed high processing accuracy in all time. If such high processing accuracy should be required, it is necessary to consider a new sophosticated structure on analog circuits[2].

The proposed circuits are quite simple and designed with only capacitors in the main part. All capacitors are arranged in a matrix form. Accordingly its circuit structure is called a C-matrix in this report. By using C-matrix, a simple matrix calculation can be realized with analog circuits. In case of a new LSI design with C-matrix analog circuits, the small number of circuit elements, the high speed calculation and the low power consumption can be realized since the matrix calculation is designed with a quite simple structure.

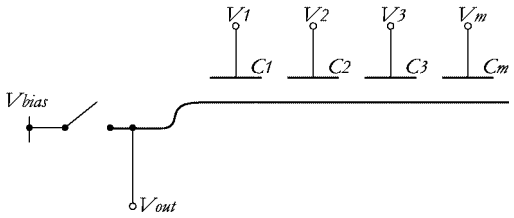

Figure 1. Capacitor Row

In this report, a part of an information media processing system, i.e., a speech recognition system, is designed with a C-matrix. As to a speech recognition system, its development is usually based on general purpose PC or DSP chip[3]. In other words, the system architecture suitable for hardware and the optimum design have been not discussed. In this report, a new data clustering/labeling method and a simple speech analysis method are designed with C-matrix and analog circuits in order to realize a small and high speed speech recognition chip.

2 An Architecture of C-matrix

In Fig.1, the capacitor row is considered. During the switch closing, the negative node is supplied V_{bias}. When the voltages $V_1, V_2, \ldots, V_m$ are given to all positive nodes, the preserved voltage diCerences at all gates

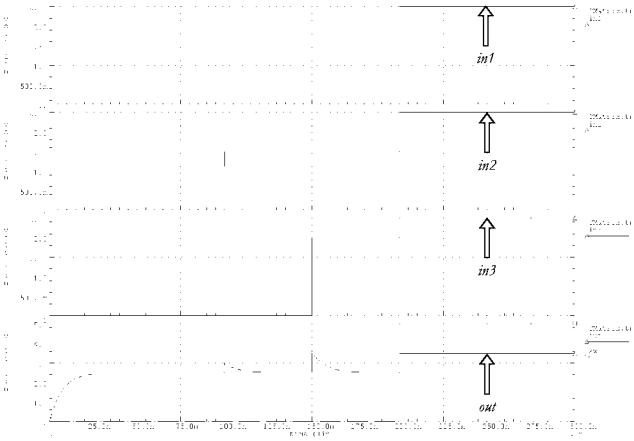

Figure 2. Simulation of the capacitor row

become V_1 . V_{bias}, V_2 . $V_{bias}, \ldots, V_m$. V_{bias}. In the next step when a switch opens, the negative node V_{bias} is cut oC and the inputs of all positive nodes change to $V_1', V_2', \ldots, V_m'$. The output voltage V_{out} is given as

$$V_{out} = \frac{\sum_{l=1}^{m} C_l(V_l' \ . \ V_l)}{\sum_{l=1}^{m} C_l} + V_{bias} \qquad (1)$$

In Fig.2, the result of SPICE simulation is depicted. The circuit module in Fig.2 is 3 gates C-matrix whose capacitors are 1pF, 2pF and 3pF. The input voltages change from 0V, 1.5V and 2V to 2.5V. The bias voltage is set to 2.5V. The output voltage is correctly given to 3.5V.

The C-matrix consists of several capacitor rows. The matrix calculation of (2) can be realized in the $k \times n$ C-matrix of Fig.3.

$$\begin{pmatrix} y_1 \\ y_2 \\ \vdots \\ y_k \end{pmatrix} = \begin{pmatrix} a_{1,1} & a_{1,2} & \ldots & a_{1,n} \\ a_{2,1} & a_{2,2} & \ldots & a_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ a_{k,1} & a_{k,2} & \ldots & a_{k,n} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{pmatrix} \qquad (2)$$

In the case of actual design, it may be necessary to consider any fringe eCect. A capacitor consists of certain minimum unit capacitors which are determined by a chip design rule. Each capacitor in a gate can be determined by setting the wiring among unit capacitors. Therefore the values of $a_{k,n}$ are positive numbers.

When the minimum value of capacitor is considered as C_0, each value of a capacitor is given by

$$C_{k,n} = a_{k,n} C_0 \qquad (3)$$

In addition, if the changing value of an input voltage

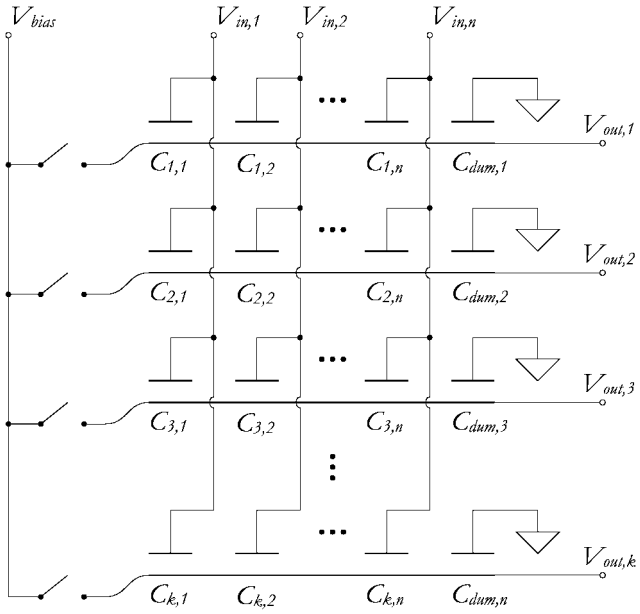

Figure 3. C-matrix

is assumed to be $V_{in,n} = x_n$, each output is given by

$$V_{out,k} = \frac{\sum_{j=1}^{n} a_{k,j} C_0 x_j}{C_{all}} + V_{bias} \qquad (4)$$

Therefore, the ratios of $V_{out,k}$ on the basis of V_{bias} is the ratios of y_k in (2). In order to keep the total capacitor value be the constant value, i.e., C_{all}, the dummy capacitor, i.e., $C_{dum,n}$, is used. The bias voltage, i.e., V_{bias}, is used for an output voltage to become positive in every time.

3 Speech Recognition System

In our speech recognition system, the block diagram of Fig.4 has been proposed. Among them, the modules of speech analysis, data clustering and labeling are designed with analog LSIs, i.e., C-matrixs and so on[6].

3.1 Speech Analysis Module

As a conventional method, the method of minimum mean square error have been widely used in a speech analysis algorithm. In this report, a basic discrete Fourier transform(DFT) which is quite suitable for the design with C-matrix is employed. When a speech signal $s(n)$ and a window function $w(n)$ are given, the log

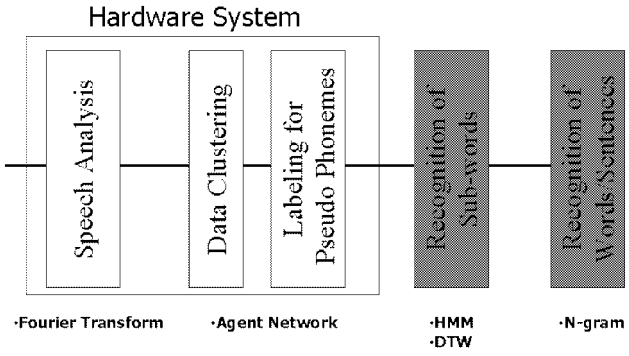

Figure 4. Outline of Speech Recognition System

power speech spectrum $S_r(k)$ is given as

$$S(k) = \sum_{n=1}^{N} s(n)w(n)e^{\cdot j\frac{2\mathrm{A}k}{N}n} \quad (5)$$

$$S_r(k) = \log|S(k)| \quad (6)$$

$$1 + k + \frac{N}{2}$$

3.2 Clustering and Labeling System

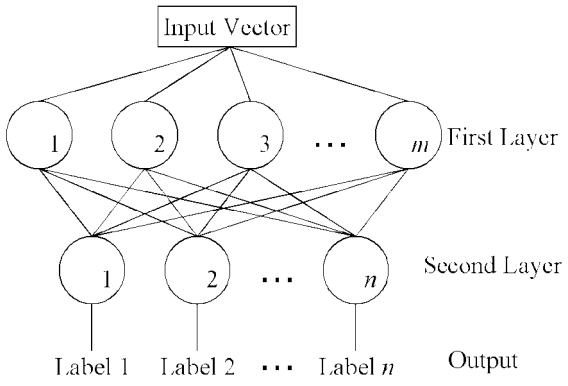

Figure 5. Clustering and Labeling System

The proposed clustering and labeling system consists of two layers shown in Fig.5. In this figure, the first layer provides a self-organized clustering mechanism in which the total number of clusters can be automatically determined with input data. In addition, the second layer realizes the labeling mechanism in which the output of the first layer can be examined according to the already trained network. The training mechanism can be easily realized in a software system and the results are used for the implementation of the clustering and labeling system. In other words, the training mechanism is not implemented in the circuit design.

The algorithm in a recognition system is given as follows: Assume the m number of clustering nodes are given in the clustering layer. Each node consists of a pattern vector $\boldsymbol{x}_i$ $(i = 1, 2, \cdots, m)$. In each node, the similarity based on Euclid distance between a pattern vector and an input vector $\boldsymbol{y}$= $(y_1, y_2, \cdots, y_p)$ is calculated:

$$D_i = \sqrt{\sum_{j=1}^{p}(y_j \ . \ x_{i,j})^2} \quad (7)$$

$$S_i = \begin{cases} 1 \ . \ (D_i/D_{\mathrm{s}})^2 & D_i < D_{\mathrm{s}} \\ 0 & D_i \ : \ D_{\mathrm{s}} \end{cases} \quad (8)$$

where the value D_s is a threshold used for the actual circuit design. In the labeling layer, the n number of nodes are used. Each node uses the m dimensional weighted vector $\boldsymbol{w}_t = (w_{t,1}, w_{t,2}, \cdots, w_{t,m})$ $(t = 1, 2, \cdots, n)$ for the output S_i from the clustering layer:

$$R_t = \sum_{i=1}^{m} w_{t,i}S_i \quad (9)$$

$$z_t = \begin{cases} 0 & R_t < 0 \\ 1 & R_t \ : \ 0 \end{cases} \quad (10)$$

4 Architecture

The processing flow chart of the proposed system is shown in Fig.6. Since the input speech signal is continuous, it is sampled with a ring counter and MOS switches. In the next stage, the sampled data are fed into the DFT block. The output data is given as a log power spectrum. By using the calculated log power spectrum, the data clustering and labeling block can recognize the input speech.

4.1 DFT Block

Since real and imaginary parts are separately calculated, two $(\frac{N}{2}+1)\times(N+1)$ C-matrices are prepared where the value N is the frame width of DFT. Since each weight of a matrix should be positive number, i.e., $a_{k,n} = w(n)\cos\frac{2\mathrm{A}k}{N}n$ and $b_{k,n} = \ .\, w(n)\sin\frac{2\mathrm{A}k}{N}n$ are weights of DFT, the ratios of these weights are changed to integers within required accuracy. Supposing it be calculated with 8bit accuracy:

$$c_{max} = \max\{a_{k,n}, b_{k,n}\} \quad (11)$$

$$c_{min} = \min\{a_{k,n}, b_{k,n}\} \quad (12)$$

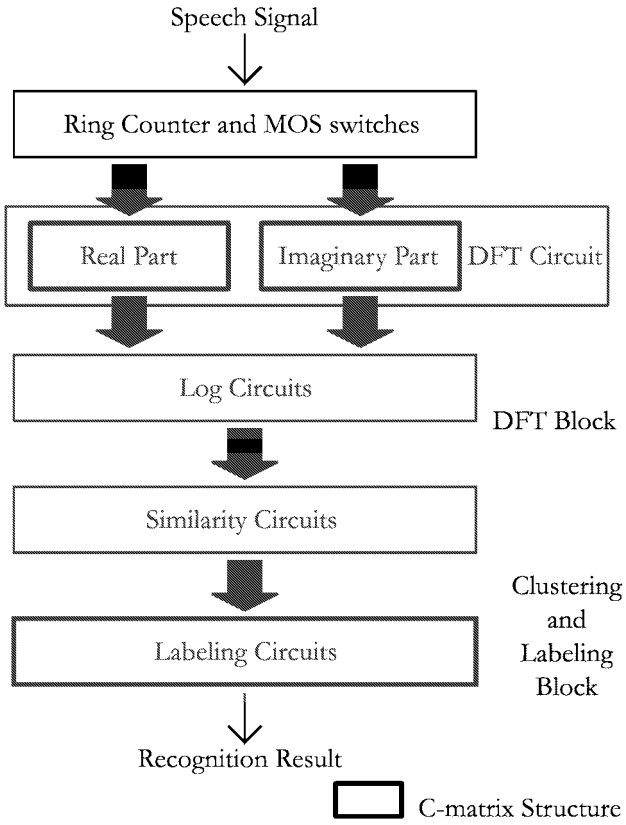

Figure 6. Processing of Speech Recognition System

Real part of C-matrix calculating is given by

$$c_{k,n} = round\left\{\frac{255a_{k,n}}{c_{max} \cdot c_{min}}\right\} \quad (13)$$

The last line of C-matrix is a compare capacitor row, and each value of capacitor is given by

$$C_{cmp,n} = |c_{min,n}| \quad (14)$$

$$c_{min,n} = \min\{c_{1,n}, c_{2,n}, \cdots, c_{k,n}\} \quad (15)$$

The other values of capacitors are given by

$$C_{k,n} = c_{k,n} + C_{cmp,n} \quad (16)$$

Therefore all values of capasitors become positve number. If the changing value of an input voltage is V_{inn}, an output of a compare capacitor row, i.e., V_{cmp}, and the other outputs V_{outk} are given as

$$V_{cmp}=\frac{\sum_{n=1}^{N} C_{cmp,n}V_{in,n}}{C_{all}} + V_{bias} \quad (17)$$

$$V_{out,k}=\frac{\sum_{n=1}^{N} c_{k,n}V_{in,n} + \sum_{n=1}^{N} C_{cmp,n}V_{in,n}}{C_{all}} + V_{bias} \quad (18)$$

$$V_{out,k} \cdot V_{cmp} = \frac{\sum_{n=1}^{N} c_{k,n}V_{in,n}}{C_{all}} \quad (19)$$

The imaginary part is the same.

As shown in (19), $V_{out,k}$ and V_{cmp} are fed into the log circuit as a diCerential input. The log circuit consists of a pair of diCerential transconductance amplifiers and current mirrors. If the changing value of an input voltage is assumed to be V, an output current , i.e., I_{out}, is given by

$$I_{out} = I_0 \tanh\left\{\frac{;|V|}{2}\right\} \quad (20)$$

This system uses the curve swept by (20) as log curve. Both outputs from a real part and an imaginary part become the current sum and they are fed into the diode-connected nMOS which changes current to a voltage.

4.2 Clustering and Labeling Block

The similarity circuit consists of m distance circuits which input vector is p dimensions[5]. The outputs of the similarity circuit corresponds to (7),(8), and are fed into the labeling circuit. Although the labeling circuit uses C-matrix which has a compare capacitor row the same as DFT circuit, $V_{out,n}$ and V_{cmp} are fed into the comparator. In labeling circuit, each value of capasitors is given by the same modification as (11)-(16). Since it is $V_{out,n} > V_{cmp}$ in order to set the output from the comparator to V_{dd}:

$$\frac{\sum_{n=1}^{N} c_{k,n}V_{in,n}}{C_{all}} > 0 \quad (21)$$

Therefore it is the same calculation as (9),(10).

5 Simulation

We design the DFT block and excute the SPICE simulation. The frame width is 64, the accuracy of the operation is 8bit, V_{dd} is 5V and V_{bias} is 2.5V. The Hamming window is used for window function. Input signal is 64 points of the synthetic voice signal sampled by 11.25kHz. They are rounded oC from 0V to 5V on the basis of 2.5V. The first, second, and third formant are 1.0kHz, 1.7kHz, and 3.0kHz. The output of the circuit and true spectrum are shown in Fig.7.

At high energy, the output of the DFT block changes almost on a par with the output by computer simulation. But there is alomost no change of each output at low energy. Therefore the first and second formant are emphasized, but third formant is hardly understood.

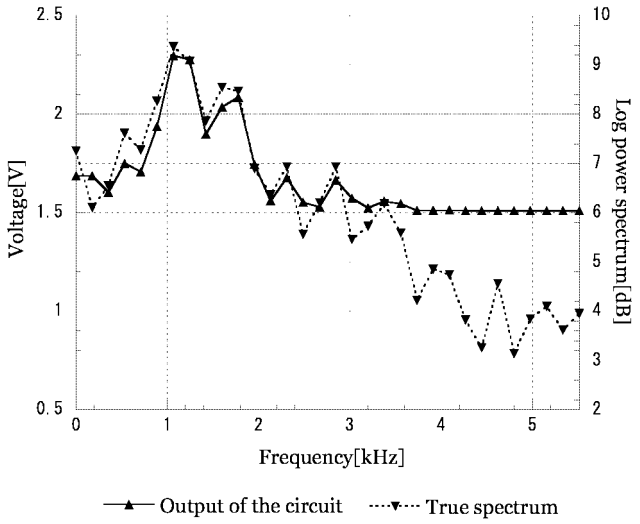

Figure 7. Simulation of DFT Block

Two reasons are considered. In the first place, output voltage of the C-matrix decreases according to the increase in the total capacitor value C_{all}. The second reason is for the characteristic to get worse when the diCerence input fed into the log circuit is very small. As to an accurate log circuit, we consider it should be the next issue.

6 Conclusions

This report has introduced the structure of C-matrix. Although the C-matrix is quite simple and designed with only capasitors, it can realize a simple matrix calculation with analog circuit. Then this report has proposed the analog architecture of speech recognition system. In this system, the DFT circuit and the labeling circuit are constituted of C-matrix.

In a digital circuit, a matrix calculation employs many resources. If C-matrix is used, high speed parallel operation can be performed. It is eCective to use for the signal processing systems by which a real time response is demanded.

Acknowledgements

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