A Low-Power Low-Noise Transimpedance Amplifier for an Integrated Biosensing Platform

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***Abstract*— In this paper, we design a low power, low noise transimpedance amplifier for ultra-low biosignal amplification. The proposed transimpedance amplifier is implemented in a standard 6 metal, 1 poly 0.18μm CMOS process. The amplifier is capable of producing 215MΩ transimpedance gain, 0.615MHz bandwidth; 910fA/√Hz input referred noise at 100Hz while consuming only 139μW DC power.**

I. INTRODUCTION

Low cost, low power and ease of miniaturization make electrical biosensors promising candidates for point-of-care diagnoses and biological agent detection. Due to their small size and low power requirements, biosensors require sensitive readout circuitry. In literature, biosensors have been reported for detection of proteins at the single molecule level, glucose monitoring in Diabetic patients, cholesterol tests in blood serum and readout for DNA probing and surveying systems [1-4]. Many of these sensors are realized in other technologies, such as vertically aligned carbon nanofibers and metal nanowires [2, 4]. Sensitivity and resolution of such an integrated system depends heavily on the characteristics of the readout circuitry. This paper focuses on readout circuitry for electrochemical measurements of ions using vertically aligned carbon nanofibers. Typical measurements using these fibers require bulky, expensive current measuring devices, which are not suitable for lab-on-chip and portable applications.The currents generated during these experiments may be measured using CMOS transimpedance amplifiers (TIAs). These TIAs may be integrated with the technologies using clean room microfabrication techniques [5].

Sensor output currents lie in the range of tens of pA to nA while frequencies may be as low as 0.01 Hz to 10kHz [6]. Thus, a sensitive and selective current measuring readout circuitry is necessary with the transducer. Transimpedance amplifiers are useful for such an application. The amplifier needs to have good noise performance and be capable of detecting weak low frequency signals. Poor noise performance of traditional transimpedance amplifiers have been addressed using capacitive feedback TIA topology [7]. These amplifiers have excellent noise performance but poor low frequency response. To achieve a satisfactory low cutoff frequency with this topology, a very high feedback capacitor is required. In terms of CMOS implementation, this requires large chip area and thus may not be an optimum choice for many applications. Therefore, for an integrated biosensing platform, an amplifier structure is required considering the tradeoffs between noise, power, gain, cutoff frequency and compact layout area.

Common gate amplifiers have good low frequency response but suffer from poor noise performance due to low input impedance and direct coupling of the load noise to the input. Noise and voltage headroom constraints in common gate transimpedance amplifiers present a challenge to TIA design for low noise application. In this work we propose that the low noise requirement could be addressed by biasing the amplifier with a sufficiently low bias current. With reduced flicker and shot noise at low bias currents, a common gate input stage is chosen as an alternative choice for TIA for the target application. A difference common gate input pair followed by source follower and common source differential pair is adopted for the design. This approach improves the amplifier noise performance by suppressing supply and substrate noise. Low bias current ensures minimum power consumption and the proposed topology also realizes a smaller footprint on chip.

The paper is outlined as follows: Section II introduces the topology adopted for the design. Section III covers the mathematical analysis including noise analysis of the proposed TIA design. Simulated results, Monte Carlo simulations and experimental results are discussed in section IV, and conclusion is given in section V.

II. CIRCUIT DESCRIPTION

The topology adopted for the transimpedance amplifier is shown in Figure 1. The proposed transimpedance amplifier consists of a common gate difference input pair followed by

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level shifting source follower and a common source differential stage. The input current converts to voltage through load transistors M3 & M4, which is then further amplified at the common source stage. The load at the common gate stage is realized by transistors biased in the linear region. The transistors size is chosen from constraints such as load resistance, bias current, and voltage headroom. The source follower stage acts as a level shifter and provides low output impedance to improve amplifier frequency response by pushing the dominant pole to higher frequencies. Open loop amplifier architecture with a low bias current 50nA at the initial stage is chosen to ensure better noise performance. At the same time, the bias current allows sufficient current headroom for the input signal to ensure the DC quiescent point remains unaffected by the input signal swing. The operating region of the common gate amplifier is in subthreshold, and the level shifter and the common source differential stage transistors are biased in the above threshold saturation region. The aspect ratio of the load transistor and the common gate amplifier transistors are chosen based on the input bias current and the tradeoffs between gain, noise, power and practical transistor size for a compact layout.

III. Circuit Analysis

A. AC Small signal Analysis

The small signal equivalent circuit of the common gate based transimpedance amplifier is shown in Figure 2. In the circuit, the transconductance of corresponding transistors are denoted as g_m, the transistor output resistance as r_o, input capacitances as Ci1 & Ci2, the total capacitance at the output of common gate and input of the source follower stage as C_1& C_2, the total capacitance at the output of source follower and input of the common source stage as C_3& C_4, the load capacitance as C_L and the common gate active loads as R_3 & R_4. The transimpedance gain of the amplifier at low frequency may be written as:

$$Avi = g_{ml6}r_{O16}\left[\frac{g_{ml3}\,/\,g_{ml4}}{1+g_{ml3}r_{O8}}.R_3.\frac{g_{ml0}r_{O9}}{1+g_{ml0}r_{O9}}\right]+r_{16}\left[\frac{g_{ml5}}{1+g_{ml5}r_8}.R_4.\frac{g_{ml2}r_{O11}}{1+g_{ml2}r_{O11}}\right] \quad [1]$$

From equation [1] it is evident that transimpedance gain is proportional to the transconductance of the common source

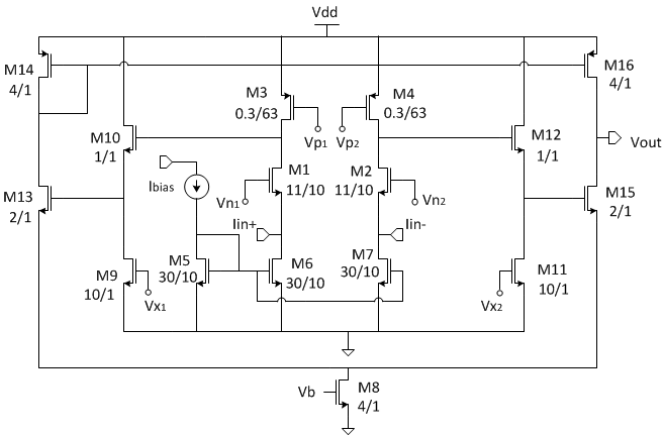

Figure 1. Schematic of proposed Transimpedance amplifier. Units of widths and lengths are in µm.

stage, active loads of common gate stage and active loads of the common source stage. To achieve a high gain, aspect ratios of the common source and source follower transistors are chosen to keep transistors in saturation for a relatively large bias current of the stage (µA) compare to the input stage which increases transconductances. The size of the common gate load is chosen from the bias current such that the load transistor stays in the linear region. The dominant pole of the amplifier is located at the high impedance node of the common source stage. Load capacitance of several tens of pF hence affects the net frequency response of the amplifier. Inclusion of a buffer at the common source amplifier output will further improve the frequency response of the amplifier and enhance amplifier load driving capacity.

B. Noise Analysis

Generally two sources of noise are considered in CMOS circuits: flicker noise and thermal noise. For short channel MOSFET shot noise also generates due to the gate tunneling currents. Shot noise is proportional to the bias current. Due to the low bias current at the input stage shot noise contribution is small compared to flicker and thermal noise and ignored in following analysis. Flicker noise dominates at the low frequency. The input referred current noise for the proposed transimpedance structure may be written as:

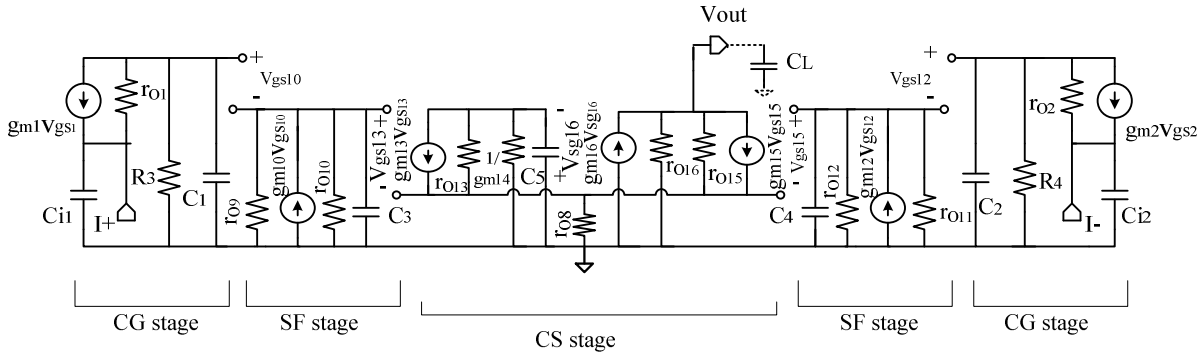

Figure 2. Schematic of proposed Transimpedance amplifier

$$i_N^2 = 8kT\left[\frac{2}{3}g_{m6,7} + \frac{1}{r_1}\right] + \frac{2K_f}{Cox.f}\left[\frac{g_{m6,7}^2}{(WL)_{6,7}} + \frac{g_{m3,4}^2}{(WL)_{3,4}}\right] \quad [2]$$

Where, W is the width, L is length of the transistor , C_{ox} is the oxide capacitance, f is the frequency, K_f is the flicker noise constant, T is temperature, k is Boltzmann's constant and g_m is the device transconductance and common gate load resistance $r_1 = R_3 = R_4$.

Due to the high transimpedance gain at the first stage, noise contributions of the later stages are less prominent at the input and hence can be ignored. Equation [2] shows that the total input noise is proportional to the transconductance of the input stage current source and reduces with the increase of total transistor areas. As transconductance of the input common gate stage dominates the amplifier noise, lowering the transconductance of the input stage reduces the noise of the amplifier. Hence a low bias current is chosen for the input stage. The flicker noise in the noise equation is inversely proportional to the transistor area and proportional to the transconductance. Increasing the transistor area while keeping desired aspect ratio for the proper region of operation helps reduce this source of noise. Therefore, all key noise contributing transistors (M3, M4, M6, and M7) of the amplifier are designed to have large lengths or, widths that are allowed in the 0.18µm CMOS process while maintaining the calculated aspect ratio.

IV. Results and Discussion

The proposed transimpedance amplifier has been implemented in a standard 0.18µm 6 metal, 1 poly CMOS process. Mismatch (variation of transistor threshold, body effect, and other parameters) and process variations (chip to chip variation in mobility, velocity saturation, early voltage and temperature dependence, etc.) were analyzed by Monte Carlo simulation with 1000 random samples. The proposed topology shows better performance compared to prior arts (Figure 3(a) shows that the TIA has a DC gain of 215MΩ , -3dB bandwidth of 642KHz and phase shift less than 10 degrees up to 100KHz and 75 degrees at 1MHz. The -3dB frequency with a 10pF load capacitor is 60kHz. Figure 3(b) shows the input referred noise current (IRNC) of the TIA. The IRNC is 112fA/√Hz at 20 kHz and 910fA/√Hz at 100Hz.) Figure 4 (a) shows the DC sweep analysis of the amplifier displaying a linear region of operation from 0 to 2.25nA. The amplifier consumes only 139µW power during operation. The low frequency CMRR of the amplifier is 42dB. CMRR is calculated as a change in output voltage due to a change in common mode input current. Therefore a common mode current could change the amplifier output by 1 %. PSRR calculations demonstrate supply noise immunity of the proposed structure.

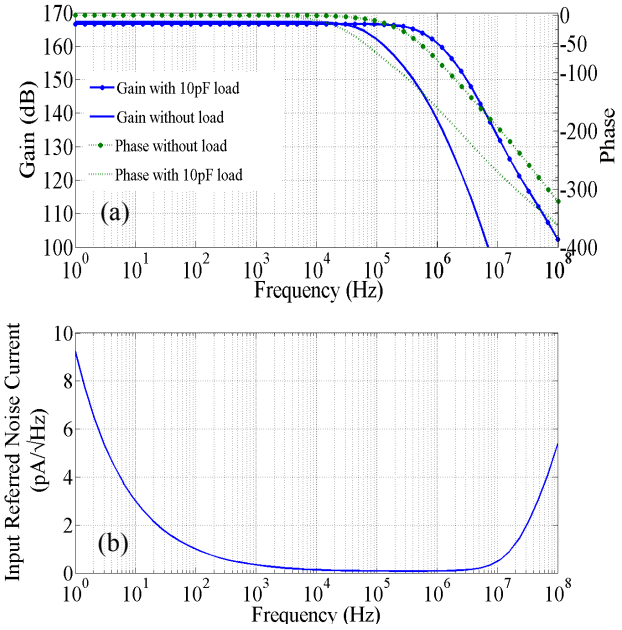

Figure 3. (a) AC gain and Phase response of TIA; (b) Input reffered noise current of the TIA.

The simulated and experimental test results of the source follower and common source differential portions are shown in Fig 4(b). The measured results show a gain of 29.20dB with a -3dB frequency of 58kHz. This agrees quite well with the simulated results of 31.49dB gain and 60 kHz -3dB frequency. The most likely cause of any differences is parasitic capacitances which introduce early roll-off and lowered bandwidth. An integrated buffer at the output would minimize the stray capacitor bandwidth limiting effects.

Monte-Carlo analysis of the complete TIA structure was performed over 1000 random samples in order to test the circuit performance susceptibility to process variations and mismatch. The analysis shows that 78% samples are within 1 standard deviation of gain ranging 151 – 279 MΩ. 99% of the

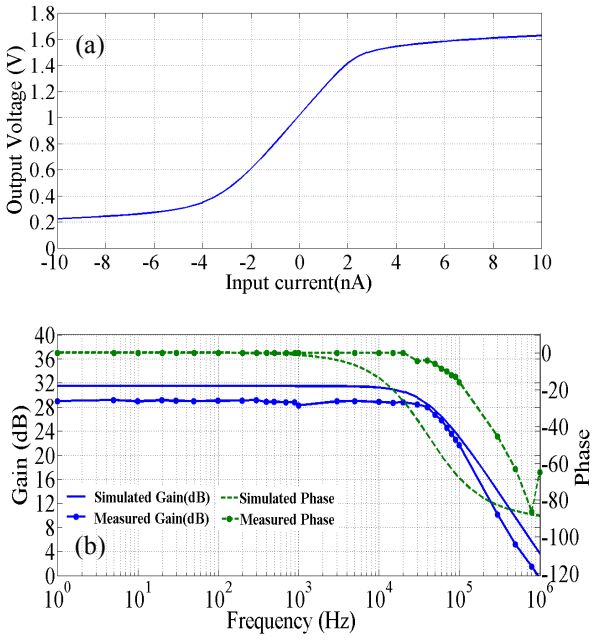

Figure 4. (a) DC transfer curve of the amplifier; (b) Experimental source follower-common source outer stage ac response.

samples show -3dB bandwidth variation 60-100 kHz with a 10pF load capacitor. From figure 5(a) and figure 5(b) it is evident that if both process variation and device mismatch are considered mean gain would be 195MΩ with σ=64 and -3dB bandwidth would be 94 kHz with σ=67. However, if only the process variation is considered mean gain is 234MΩ with σ=35 and mean -3dB bandwidth 100 kHz with σ=5. The lower tail of the Monte-Carlo gain plot and the upper tail of the Monte-Carlo -3dB plot are caused by transistor mismatch. The mismatch effects may be minimized by adopting careful layout techniques to minimize transistor mismatch such as using interleaving and common centroid techniques. Due to the amplifier open loop configuration, the amplifier may be prone to variation and each amplifier will have to be characterized before any practical use.

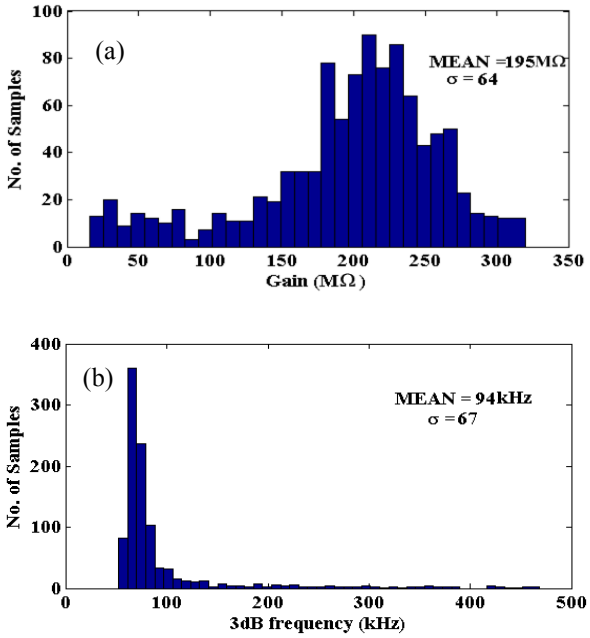

Figure 5. Monte Carlo simulation results of the TIA structure (a) histogram for gain and (b) -3dB bandwidth . Results show good agreement with design constraints.

V. CONCLUSION

A low-power, low-noise, high gain transimpedance preamplifier has been developed for use with vertically aligned carbon nanofibers for high resolution amperometric sensing. The design has been implemented in a commercially available 6 metal, 1 poly 0.18µm CMOS process. The amplifier shows a transimpedance gain of 215MΩ with 0.615MHz -3dB bandwidth, less than 10 degree phase shift up to 100 kHz, low input referred noise of 910fA/√Hz at 100Hz and consumes only 139µW for a supply of 1.8V. Experimental measurements of the voltage amplification stage show good agreement with simulation. Monte Carlo simulations of the complete TIA structure show that 78% of the fabricated structures will conform to the design constraints. This amplifier is suitable as a low power front end preamplifier stage in an integrated biosensing platform.

TABLE I: Comparison of Performance of TIA

Parameter	[8]	[9]	[10]	This Work
Application	Biosensor	MEMS	Biosensor	Biosensor
Technology	0.35um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS
Topology	Integrator differenti ator	Capacitive feedback	Capacitive feedback	Common gate
Supply	3.3	1.8V	1.8V	1.8V
Midband Gain	30M	56M	100M	215M
Bandwidth	2MHz	1.8MHz	1MHz	615kHz/ 60kHz (10pF capacitive load)
GBW	60	100.8	100	132.2
Lower cutoff frequency	100Hz	1kHz	40Hz	1Hz
Input Referred Noise Current	4fA/√Hz @100Hz	250fA/√Hz @1KHz	1100fA/ √Hz @ 100Hz	910fA/√Hz @100Hz
Integrated Input Referred Noise**	28.24pA*	99.52pA*	318.49pA*	95.08pA
Power	21mW	436µW	132µW	139µW

* Input referred noise plot is available from lower cutoff frequency

**Integrated noise is calculated over respective noise equivalent band from the Input referred noise plot. For cases (*), integration carried out from lower cutoff to noise band which might underestimate the overall integrated noise.

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