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A 40-Gb/s NRZ Inductorless Transimpedance Amplifier in a 0.18-μm SiGe BiCMOS Technology

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***Abstract*—In this study, an inductorless broadband transimpedance amplifier (TIA) is implemented using TSMC 0.18-μm SiGe BiCMOS technology. The regulated cascade circuit is used for the input stage of the TIA. The core amplifier is a fully differential amplifier paralleling with a differentiator that is capable of enhancing the bandwidth of the TIA. The TIA has a differential transimpedance gain of 39.4 dBΩ, a bandwidth of 32.9 GHz, and an average input-referred current noise density of 37 pA/√Hz. The TIA has a power consumption of 77 mW with a supply voltage of 3.3 V, and the chip area is 0.45 mm^2 including pads. In the chip testing, the 25- and 40-Gb/s non-return-to-zero eye diagrams are measured and sufficiently clear.**

Keywords—transimpedance amplifier, SiGe BiCMOS, optical receiver

I. INTRODUCTION

In recent years, with the development of high-density video, cloud computing, and high-speed mobile communication technologies, there has been an increasing demand for high-speed optical fiber transmissions. Because the transmission speed of data input and output (I/O) interfaces is also continuously increasing in the computer data storage, storage area network, and data center, I/O interfaces that use optical fiber transmissions are also required [1],[2]. The Ethernet 40 Gb/s and 100 Gb/s standard was published in 2010 [3]. Eight-channel 25-Gb/s or 50-Gb/s optical links can be used to realize the 200 or 400 Gigabit Ethernet [4].

A non-return-to-zero (NRZ) signal is usually utilized in high-speed optical fiber transmissions. Generally, the required transmission bandwidth of the NRZ signal is approximately equal to 70%–80% of the transmission data bit rate. The integrated circuits for high-speed operations are usually implemented in a smaller size or by using a more advanced complementary metal-oxide-semiconductor (CMOS), SiGe, GaAs, or InP process technologies. The addition of inductors to high-speed circuits is a common technique of bandwidth enhancement; however, the inductor is often a large-area component in integrated circuits, and its performance is also not easy to control.

In this study, we design a wide-bandwidth, fully differential TIA with a 0.18-μm SiGe BiCMOS process technology. The TIA does not use any inductors. A technique of bandwidth enhancement is proposed, which involves the core amplification of the TIA parallels with a differentiator.

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II. CIRCUIT ARCHITECTURE AND ANALYSIS

The schematic of our TIA circuit is presented in Fig. 1. The TIA circuit contains an input stage and a core amplifier. As the input signal for the TIA is a current signal from the input port, the regulated cascode (RGC) circuit with low input impedance is suitable for use as the input stage of the TIA. The RGC circuit can also transform a current signal to a voltage signal. The RGC circuit can isolate the parasitic capacitance from the input port, and the input pole frequency can become higher due to a lower input resistance.

The second stage is a fully differential amplifier. A differential pair with a degenerated source resistor acts as a core amplifier, another differential pair with a degenerated source capacitor acts as a differentiator, and the core amplifier parallels with the differentiator to implement the second stage of the differential TIA. The core amplifier parallels with a differentiator circuit, which is a technique of bandwidth enhancement. To reduce the chip area, the second stage is also the output stage of the TIA. Therefore, the output impedance of the core amplifier is set to 50 Ω to match the load impedance. The low output resistors will also cause the low voltage gain of the differential amplifier.

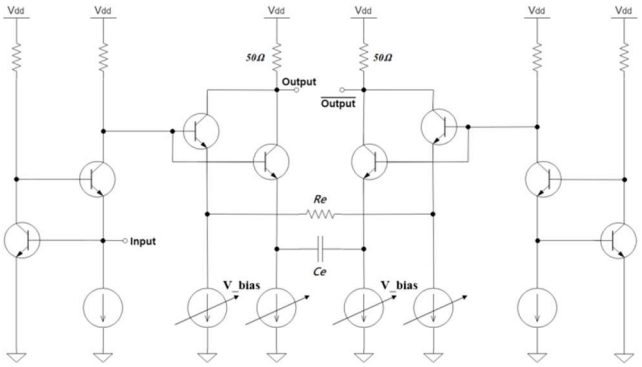

Fig. 1. Schematic of our TIA circuit.

Our TIA was designed in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm SiGe BiCMOS technology. The layout of the TIA is presented in Fig. 2, and the chip area, including pads, is 0.45 mm^2. The TIA does not use any inductors. The input pad, Input, can be connected with a photodiode or be input via a current signal, and the two output pads, Out and $\overline{\text{Out}}$, are differential outputs. The chip has two voltage source pads, VDD, and four ground pads, GND, for uniform current density and ground potential.

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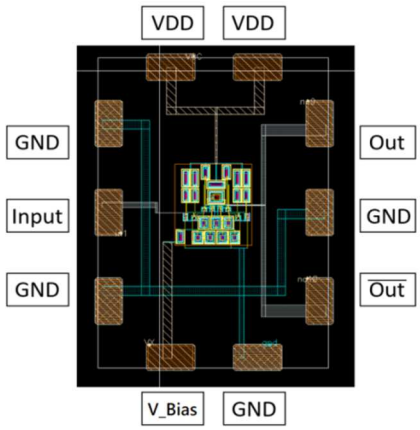


Fig. 2. Layout diagram of the TIA chip.

III. Results and Discussions

The post-layout simulated DC transfer curve of the TIA is presented in Fig. 3(a). The transimpedance gain can be estimated to be 39.4 dBΩ through the curve slope within an input current of 1.6 mA. The maximum output voltage amplitude is 150 mV. The post-layout simulated frequency response of the TIA is presented in Fig. 3(b); an output coupled capacitor and a 50-Ω road resistor were considered in this simulation; the −3 dB bandwidth is 32.9 GHz. The input-referred current noise density of the TIA is simulated, as presented in Fig. 3(c). Within the bandwidth, the input-referred current noise density is below 57 pA/√Hz, and the average is 35 pA/√Hz. An average noise current of 6.35 μArms is estimated from the current noise density; therefore, the minimum input current amplitude is 89.9 μA_{pp} under a bit error rate of 10−12. The 50-Gb/s NRZ output eye diagrams were simulated at an input current pseudo-randomness binary sequence (PRBS) signal of 400 μA, as presented in Fig. 3(d). The eye diagram is clear, and the total output voltage amplitudes are 17 mV. The single-ended transimpedance gain is estimated to be 32.6 dBΩ as the output end of the TIA was connected with a 50 Ω load resistor. The differential gain of the TIA with a 50 Ω output load resistor is 38.6 dBΩ.

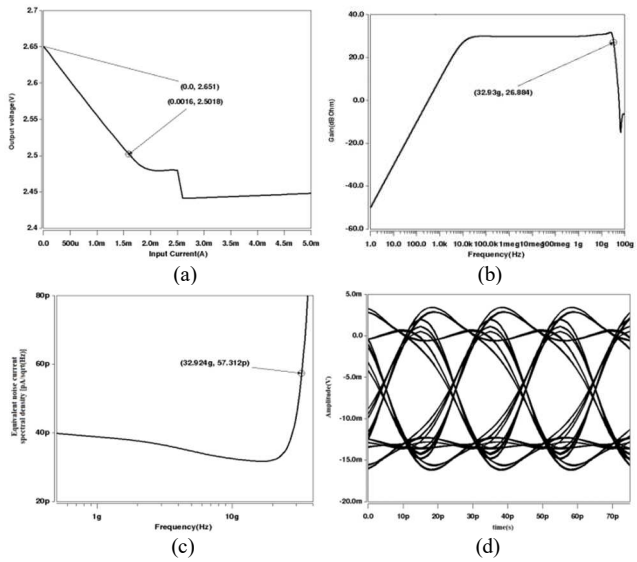


Fig. 3. Post-layout simulated (a) DC transfer curve, (b) frequency response, (c) input-referred current noise density, and (d) 50-Gb/s NRZ output eye diagrams of the TIA.

Our TIA chip was implemented in TSMC 0.18-μm SiGe BiCMOS technology, and the chip performance was also confirmed through measurements of the eye diagram. The TIA chip was die-bonded and wire-bonded on a printed circuit board (PCB), as presented in Fig. 4. The testing PCB was designed by us, the material of the high-frequency signal layer of the PCB was Rogers 4350B, and the high-speed signal traces were designed using the grounded coplanar waveguide structure. The Anritsu MP 1800A was used as a PRBS pattern generator, and a −20 dB attenuator was inserted between the output end of the pattern generator and the signal input end of the PCB to generate a low-current input signal. The eye diagrams could be observed through a high-speed digital sampling oscilloscope (Tektronix DSA8300).

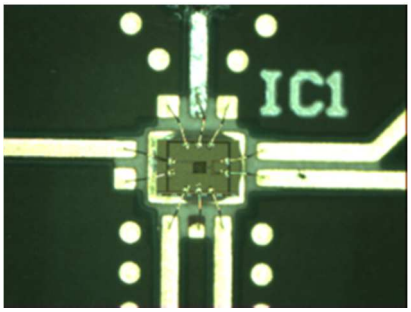
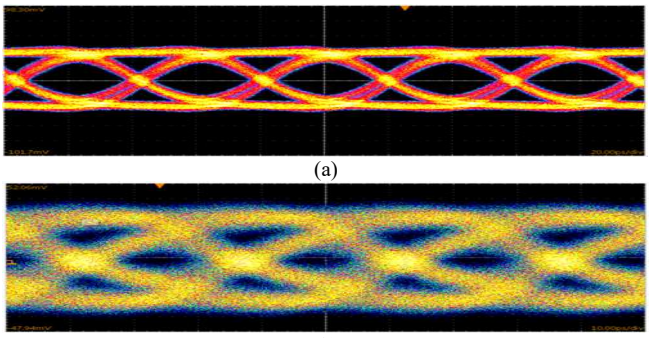


Fig. 4. TIA chip bonded on a PCB.

Using an input current signal of 1.5 mA_{pp}, the measured 25- and 40-Gb/s NRZ eye diagrams of the TIA output voltage signals are presented in Figs. 5(a)&(b). The voltage amplitude of the 25-Gb/s NRZ output eye diagram is 64 mV_{pp}. The transimpedance gain was estimated to be 32.6 dBΩ. The voltage amplitude of the 40-Gb/s NRZ output eye diagram is 40 mV_{pp}. A clear 50-Gb/s NRZ eye diagram could not be observed using our TIA.



(a)

(b)

Fig. 5. Measured (a) 25-Gb/s (b) 40-Gb/s output NRZ eye diagrams.

IV. Conclusion

We realized an inductorless wide-bandwidth TIA in TSMC 0.18-μm SiGe BiCMOS technology. The TIA circuit included two stages: the first stage was an RGC circuit, and the second stage was the core amplifier. The bandwidth of our TIA could be achieved at 32.9 GHz, and the transimpedance gain was 39.4 dBΩ. Through the eye diagram testing, our TIA chip can be applied in 40-Gb/s NRZ optical receivers.

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