Transimpedance Amplifier (TIA) Design for 400 Gb/s Optical Fiber Communications

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(ABSTRACT)

Analogcircuit/IC design for high speed optical fiber communication is a fairly new research area in Dr. Ha's group. In the first project sponsored by ETRI (Electronics and Telecommunication Research Institute) we started to design the building blocks of receiver for next generation 400 Gb/s optical fiber communication. In this thesis research a transceiver architecture based on 4x100 Gb/s parallel communication is proposed. As part of the receiver, a transimpedance amplifier for 100 Gb/s optical communication is designed, analyzed and simulated. Simulation results demonstrate the excellent feasibility of proposed architecture.

Bipolar technology based on III-V materials (e.g. - GaAs, InP based HBT, HEMT) has always dominated the high speed optical transceiver design because of their inherent properties of high mobility and low noise. But they are power hungry and bulky in size which made them less attractive for highly integrated circuit design. On the contrary, CMOS technology always drew attraction because of low cost, low power dissipation and high level of integration facility. But their notorious parasitic characteristic and inferior noise performance makes high speed transceiver design very challenging. The emergence of nano-scale CMOS offer highly scaled feature sized transistors with transition frequencies exceeding 200 GHz and can improve optical receiver performance significantly.

Increasing bandwidth to meet the target data rate is the most challenging task of TIA design especially in CMOS technology. Several CMOS TIA architectures have been published recently [6]-[11] for 40 Gb/s data rate having bandwidth no more than 40 GHz. In contrast to existing works, the goal of this research is to step further and design a single channel stand-alone

TIA compatible in serial 100 Gb/s data rate with enhanced bandwidth and optimized transimpedance gain, input referred noise and group delay variation.

A 100 Gb/s transimpedance amplifier (TIA) for optical receiver front end is designed in this work. To achieve wide bandwidth and low group delay variation a differential TIA with active feedback network is proposed. Proposed design also combines regulated cascode front end, peaking inductors and capacitive degeneration to have wide band response. Simulation results show 70 GHz bandwidth, 42 dBΩ transimpedance gain and 2.8 ps of group delay variation for proposed architecture. Input referred noise current density is 26 pA/$\sqrt{Hz}$ while the total power dissipation from 1.2V supply is 24mW. Performance of the proposed TIA is compared with other existing TIAs, and the proposed TIA shows significant improvement in bandwidth and group delay variation compared to other existing TIA architectures.

To my parents

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Chapter 1

Introduction

1.1 Motivation

The rapid growth of telecommunication networks and data communication technology have rekindled research interest in high speed optical and electronic devices and systems. Development of faster communication channels was motivated by proliferation of the Internet, high-speed microprocessors, and inexpensive memory in recent years. In addition, optical fiber communication also received immense attraction because of its advantages over electrical communication, such as transmission capacity, low power consumption, high security, low cost, less cross-talk, and lower EMI. The provisions of scalable bandwidth through dense wavelength division multiplexing (DWDM) and novel interconnect network architectures such as passive star or ring networks also have made optical communication a suitable replacement for electronic interconnect networks. Realization of cost effective optical transceivers and homogeneous integration of optoelectronic systems with highly complex digital circuitry have drawn tremendous research activity.

The goal of an optical communication (OC) network is to carry a large volume of data over a long distance. For instance, the telephone traffic in Europe is connected to the United States through a fiber system installed across the Atlantic Ocean. A simple OC network consists of three components: (1) an electro-optic transducer (e.g. a laser diode), which converts the electrical information to optical information, (2) an optical fiber, which carries the optical information over a considerable distance, and (3) a photodetector (e.g. a photodiode) which senses the light and converts the optical information back to its electrical form. With long or low quality optical fiber, the light attenuates considerably as it travels from one end to the other end. So, to ameliorate the performance of an optical network a couple of more building blocks are added to the system such as laser driver, transimpedance amplifier (TIA), phase locked loop

(PLL), and limiting amplifier. The roles of these building blocks will be discussed in details in Chapter 2.

The front-end preamplifier or transimpedance amplifier is a critical element for an optical receiver affecting the whole system performance including speed, sensitivity, and signal-to-noise ratio. Therefore, design of the transimpedance amplifier mandates careful optimization of a number of tradeoffs including bandwidth, gain, noise, and power consumption. III–V materials such as GaAs, InP-based HBT, and HEMT have been the dominant materials used to realize such amplifiers due to their inherently high-speed and low-noise characteristics. However, silicon technologies—particularly submicron CMOS technologies—have recently become very attractive due to their low cost and high integration level characteristics. Even in terms of speed, CMOS can provide comparable performance to GaAs technologies.

1.2 Review of CMOS TIAs

Many works on TIA design for high speed (such as 10 Gb/s, 16Gb/s, 25 Gb/s, 40 Gb/s) data rates have been published in recent years. For example, the gain-bandwidth limit of wide-band amplifier was addressed in [1] and a TIA was designed in 0.18 μm BiCMOS technology for 10 Gb/s data rate. In addition, a practical design methodology to absorb the parasitic capacitance of transistors is proposed in [1]. The TIA achieves 3-dB bandwidth of 9.2 GHz in the presence of a 0.5 pF photodiode capacitance, while the input sensitivity of the TIA is -18 dBm for a bit error rate of 10^{-12}.

Chan and Chen [2] proposed an inductor-less 10 Gb/s CMOS TIA using a source-follower, regulated cascode and double active feedback schemes based on the 0.18 μm CMOS technology. By using source follower regulated cascode structures, the proposed transimpedance stage not only compensates input capacitance of the photodiode and input bonding pad but also avoids the headroom effect. The TIA under the supply voltage of 1.8 V achieves a bandwidth of about 7.7 GHz with a total transimpedance gain of 1.12 KΩ and an input capacitance of 300 fF.

Lu et al. [3] proposed a novel bandwidth enhancement technique based on the combination of capacitive degeneration, broad-band matching network, and the regulated cascode (RGC) input stage which turns the TIA design into a fifth-order low pass filter with Butterworth response. The TIA achieves a 3-dB bandwidth of about 8 GHz with 0.25 pF photodiode capacitance.

Ngo et al. [4] reported implementation of a TIA, using the combination of the shunt-feedback technology with the RGC input stage and broad-band matching network, in a 0.13 μm CMOS technology. The TIA achieves a 3-dB bandwidth of 7.5 GHz, transimpedance gain of 50 dBΩ in the presence of 300 fF photodiode capacitance.

Lu et al. [5] reported a novel current-mode TIA exploiting the common gate input stage with common source active feedback that was realized in CHRT 0.18 μm-1.8 V RFCMOS technology. The proposed active feedback TIA input stage is able to achieve low input impedance similar to that of the well-known regulated cascode (RGC) topology. The TIA design also employs series inductive peaking and capacitive degeneration techniques to enhance the bandwidth and the gain. Measurements show a transimpedance gain of 54.6 dBΩ with a 3-dB bandwidth of about 7 GHz for a total input parasitic capacitance of about 0.3 pF.

A 40 Gb/s TIA was realized in 0.18 μm CMOS technology in [6]. Measurement of S-parameter shows a transimpedance gain of 51 dBΩ and 3-dB bandwidth up to 30.5 GHz. A bandwidth enhancement technique pi-type inductive series peaking (PIP) was proposed in [6] to achieve a bandwidth ratio of 3.31. Also the noise response shows that the PIP topology decreases the noise current as the frequency increases.

Liao and Liu [7] proposed a high-speed front end amplifier which incorporates a novel bandwidth enhancement technique called reverse triple resonance networks (RTRNs). Mathematical modeling of the circuit showed that the RTRN technique extends the bandwidth more than the shunt-series peaking technique, especially when the parasitic capacitance is dominated by the next stage. At 40 Gb/s data rate the amplifier provides an overall gain of 2 KΩ and a differential output swing of 520 mV_{pp} with BER < 10^{-9}.

A low power, 40 Gb/s optical transceiver front-end is demonstrated in a 45 nm silicon-on-insulator (SOI) process in [10]. The proposed transimpedance amplifier and limiting amplifier combination achieves 55 dBΩ of transimpedance gain over 30 GHz of bandwidth. The TIA consumes only 9 mW power when the supply is 1 V.

Optimization of group delay variations, while achieving high bandwidth, is extensively investigated in [8]. A 40 Gb/s TIA is proposed in this work using multistage inductive series peaking for low group delay variation. The TIA was implemented in a 0.13 μm CMOS technology and achieved a 3-dB bandwidth of 29 GHz.

Bashiri et al. [9] proposed a 40 Gb/s transimpedance amplifier in 65 nm CMOS technology adopting a modified RGC network and ultra-compact peaking inductors to provide improved frequency response and lower input referred noise. The bandwidth of their proposed TIA was 21.6 GHz with 46.7 dBΩ of gain for an input capacitance of 200 fF. Simulated input referred noise was below 30 pA/$\sqrt{Hz}$.

A 40 Gb/s optical receiver analog front end integrating a transimpedance amplifier and a limiting amplifier is presented in [11]. To achieve wide band operation, nested feedback TIA and an interleaving post-amplifier with split series peaking are proposed in this design. The receiver provides transimpedance of 92 dBΩ with 3-dB bandwidth of 35 GHz.

1.3 Research Objective

All of the aforementioned works are based on CMOS technology and achieve the rate of 10 Gb/s or 40 Gb/s. The objective of the proposed work is to design a 100 Gb/s TIA with a wide bandwidth, a sufficiently high transimpedance gain, low input referred noise, and a low group delay variation, and no existing design has achieved the objective, yet. The primary task of this work is to increase the bandwidth high enough for 100 Gb/s data rate, as it is the most challenging and critical part of the TIA design in CMOS technology. Optimization of noise and group delay performance, while sustaining the same bandwidth and transimpedance gain, is also part of the design goal.

1.4 Contributions of the Proposed Research

The major contributions of the thesis research are:

- A future 400 Gb/s transceiver architecture is proposed based on 4x100 Gb/s parallel communication.
- A CMOS TIA (transimpedance amplifier) is designed, analyzed and simulated for 100 Gb/s optical communication. Simulation results demonstrate excellent performance, especially in terms of bandwidth and group delay variation.

1.5 Organization of The Thesis

The thesis work is organized as follows. Chapter 2 discusses in details about the background of the research work. Chapter 3 reviews all the significant works of TIA with their design details and performance. Chapter 4 presents the proposed design of 100 Gb/s TIA in 65nm CMOS technology. Chapter 5 demonstrates the effectiveness of the proposed design by discussing the simulation results. Chapter 6 draws the conclusion of this work.

Chapter 2

Preliminaries

This chapter discusses the preliminaries of the research work. Section 2.1 describes the background of ethernet and IEEE 802.3 standards and how they are closely related to each other. It also mentions about latest standard of optical communication - IEEE 802.3ba and its role to govern 40 Gb/s and 100 Gb/s optical communication. Section 2.2 explains the working principle and role of the building blocks of optical receiver and transmitter in detail. Section 2.3 discusses about the basic working principle of TIA, and section 2.4 familiarizes us with the conventional topologies of TIA.

2.1 Background of Ethernet and IEEE 802.3

Xerox Corporation's Palo Alto Research Center (PARC) developed Ethernet in the 1970s. Ethernet was the technological basis for the IEEE 802.3 specification, which was initially released in 1980. Shortly thereafter, Digital Equipment Corporation, Intel Corporation, and Xerox Corporation jointly developed and released an Ethernet specification (Version 2.0) that is substantially compatible with IEEE 802.3. Together, Ethernet and IEEE 802.3 currently maintain the greatest market share of any local-area network (LAN) protocol. Today, the term Ethernet is often used to refer to all carrier sense multiple access/collision detection (CSMA/CD) LANs that generally conform to Ethernet specifications, including IEEE 802.3.

When it was developed, Ethernet was designed to fill the middle ground between long-distance, low-speed networks and specialized, computer-room networks carrying data at high speeds for very limited distances. Ethernet is well suited to applications where a local communication medium must carry sporadic, occasionally heavy traffic at high peak data rates.

Ethernet and IEEE 802.3 specify similar technologies. Both are CSMA/CD LANs. Stations on a CSMA/CD LAN can access the network at any time. Before sending data, CSMA/CD stations "listen" to the network to see if it is already in use. If it is, the station wishing to transmit waits. If the network is not in use, the station transmits. A collision occurs

when two stations listen for network traffic, "hear" none, and transmit simultaneously. In this case, both transmissions are damaged, and the stations must retransmit at some later time. *Backoff* algorithms determine when the colliding stations retransmit. CSMA/CD stations can detect collisions, so they know when they must retransmit.

Both Ethernet and IEEE 802.3 LANs are broadcast networks. In other words, all stations see all frames, regardless of whether they represent an intended destination. Each station must examine the received frames to determine if the station is a destination. If so, the frame is passed to a higher protocol layer for appropriate processing.

Differences between Ethernet and IEEE 802.3 LANs are subtle. Ethernet provides services corresponding to Layers 1 and 2 of the OSI reference model, while IEEE 802.3 specifies the physical layer (Layer 1) and the channel-access portion of the link layer (Layer 2), but does not define a logical link control protocol. Both Ethernet and IEEE 802.3 are implemented in hardware. Typically, the physical manifestation of these protocols is either an interface card in a host computer or circuitry on a primary circuit board within a host computer.

IEEE 802.3ba is the Ethernet standard governing 40 Gb/s and 100 Gb/s simultaneously, paves the way for the next generation high speed server connectivity and core switching. An amendment to the previous Ethernet standard IEEE 802.3, IEEE 802.3ba is expected to trigger further expansion of the 40 gigabit and 100 gigabit Ethernet families of technologies by driving new development efforts, as well as providing new aggregation speeds. It defines physical layer technologies for backplane, copper cable assembly, and optical fiber medium, and leverages existing 10 Gb/s technology where possible. In addition, IEEE802.3bg of March 2011 specifies a new Physical Medium Dependent (PMD) sublayer, 40GBASE-FR, for serial 40 Gb/s operation over up to 2 km of single-mode fiber.

2.2 Building blocks of optical receivers and transmitters

Building blocks of a generic optical communication network will be discussed in detail in this section. As it was mentioned in the introduction, a basic optical communication system is comprised of three components: (1) a laser diode, (2) optical fiber, and (3) a photodiode. Figure 1(a) depicts a basic optical communication network. Also, lasers are driven by electrical current while photodiodes sense the light and generate an output current.

With long or low quality fiber the transmitted data experiences substantial attenuation as it travels from the 'near end' to 'far end'. Thus (1) the laser needs to produce light with high intensity; (2) the photodiode must exhibit high sensitivity to received light; and (3) the output current of the photodiode must be amplified with low noise. These observations lead to the more complete system where "a laser driver" delivers large current to the laser and amplifies the laser output, and a "transimpedance amplifier" amplifies the photodiode output current with low noise and sufficient bandwidth and converts it to a voltage for further signal processing in the subsequent stages. Figure 1 (b) shows the inclusion of laser driver and TIA in the basic system.

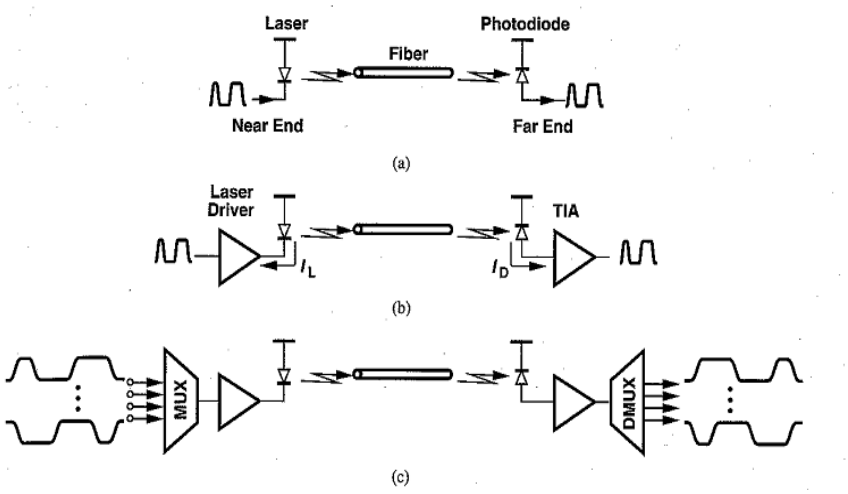


Figure 1: (a) Simple optical system, (b) addition of driver and amplifier, (c) addition of MUX and DMUX, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

The transmitted and received signal in Figure 1(b) is high speed serial data e.g. a high stream data at 10 Gb/s. However, in a more realistic system there are many low speed channels ("parallel" data) produced by multiple users. Thus to accommodate multiple users a "multiplexer" is necessary in the transmitter to convert low speed "parallel" channels to a high speed serial data stream. Similarly, receiver (RX) must incorporate a "demultiplexer" (DMUX) which regenerates received serial data stream from original parallel channels. This is shown in Figure 1(c).

The system is still incomplete because the multiplexer requires a number of clock frequencies with precise edge alignment to multiplex the parallel low speed channels. These clocks are generated by a phase locked loop (PLL). In addition, in a practical set-up the output of the multiplexer suffers from non-idealities like "jitter" and "inter symbol interference (ISI)",

mandating the use of a “clean-up” flip-flop preceding the laser driver. These modification leads to the transmitter as shown in Figure 2(a).

The receiver end needs some more functional blocks to successfully regenerate the original parallel data stream. Output voltage of a TIA might not be high enough to determine the logical level, that’s why a high gain amplifier or limiting amplifier follows the TIA. Moreover, since the received signal is corrupted by channel and circuit noise, a clean-up flip-flop is incorporated between the LA and the DMUX. The modified optical system is thus depicted in Figure 2(b).

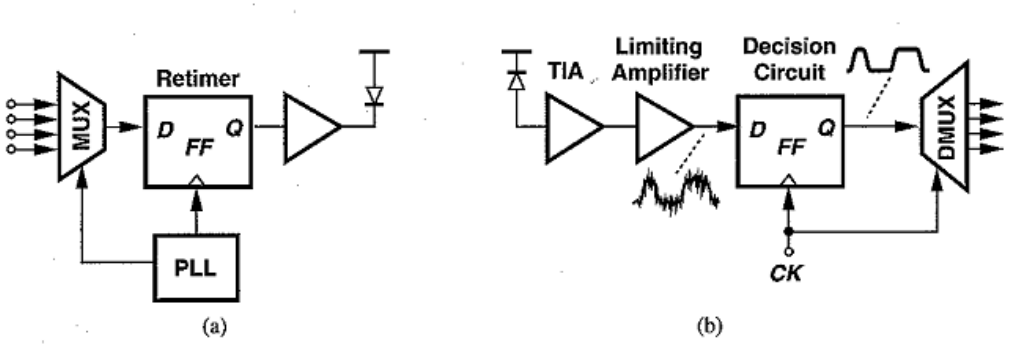


Figure 2: Modified transmitter and receiver, Behzad Razavi-“Design of Integrated Circuits for Optical Communications”. Used under fair use, 2013.

The receiver entails a well-defined clock signal which must bear a well-defined phase relationship with respect to the received data. Thus the flip-flop would be able to sample data optimally i.e., at the midpoint of each bit. The operation of generating such a clock from the incoming signal is called “clock recovery”. The overall operation of “clock recovery” and “data cleanup” is called “clock and data recovery” (CDR). Figure 3 shows the complete optical communication system. For better performance the laser driver incorporates power control and the TIA employs automatic gain control (AGC).

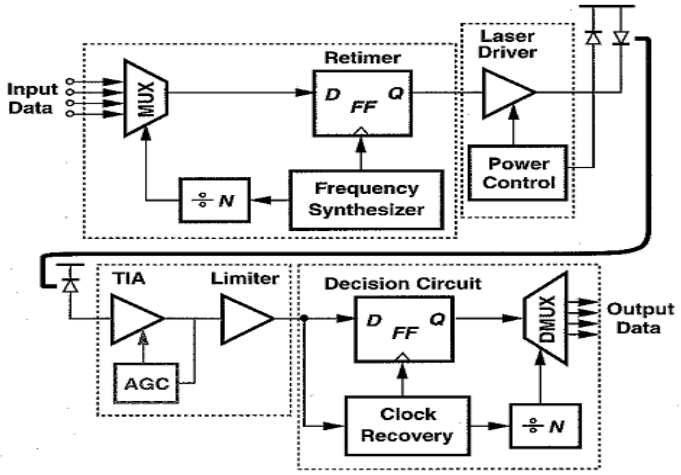


Figure 3: Complete optical communication network, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

2.3 Role and working principle of TIA

A transimpedance amplifier converts an input current, I_{in}, to an output voltage, V_{out}. The circuit is characterized by a "transimpedance gain" (R_T) where $R_T = dV_{out} / dI_{in}$. Since photodiodes generate a small current and most of the subsequent processing occurs in the voltage domain, the current must be converted to voltage. As depicted in Figure 4, a single resistor can perform this function, providing a transimpedance gain equal to R_L. However, the time constant $R_L C_D$ leads to a severe trade-off between gain, noise and bandwidth.

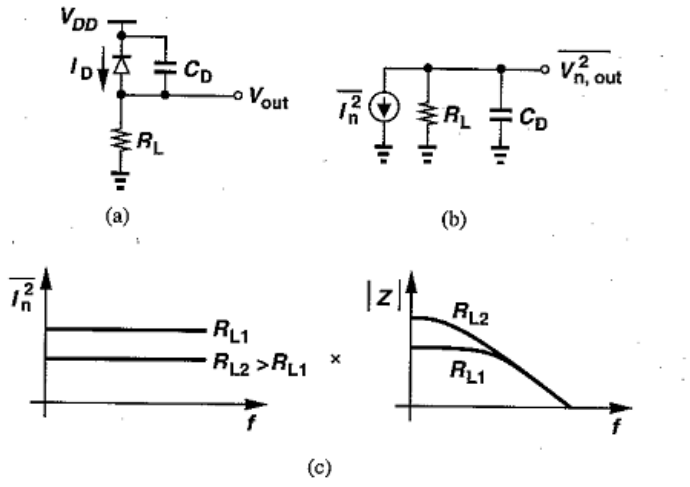


Figure 4: (a) Conversion of photodiode current to voltage by a resistor, (b) equivalent circuit for noise calculation, (c) effect of resistor value, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

The resistor thermal noise is white noise and noise current is $\overline{I_n^2} = 4kT/R_L$ (per unit bandwidth).

Noise voltage thus can be obtained from,

$$\overline{V_{n,out}^2} = \int_0^\infty \frac{4kT}{R_L} \left| R_L \parallel \frac{1}{C_D j2\pi f} \right| df$$

$$= \int_0^\infty \frac{4kT}{R_L} \frac{R_L^2}{R_L^2 C_D^2 4\pi^2 f^2 + 1} df$$

$$= \frac{kT}{C_D} \tag{1}$$

Equation (1) shows that the total integrated noise is independent of R_L. From Figure 4(c) when R_L increases, noise current density decreases, but the area under $|Z|^2 = \frac{R_L^2}{R_L^2 C_D^2 4\pi^2 f^2 + 1}$ increases so the total integrated voltage $\overline{V_{n,out}^2}$ remains the same. Though, the circuit following the diode/resistor combination limits the noise bandwidth to less than infinity, kT/C_D provides a very rough estimate in initial calculation. However, for a fair comparison we are more interested in input referred noise, which can be obtained from total integrated noise voltage by,

$$\overline{I_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{R_L^2} = \frac{kT}{R_L^2 C_D} \tag{2}$$

Equation (2) indicates that R_L must be maximized to have less input referred noise. On the other hand, 3-dB bandwidth of diode-resistor combination is $(2\pi R_L C_D)^{-1}$, which must be equal to the bit rate R_B. If we summarize the circuit's properties as ,

$$\text{Transimpedance gain} = R_L \tag{3}$$

$$\text{Bandwidth, } R_B = (2\pi R_L C_D)^{-1} \tag{4}$$

$$\text{Input referred noise, } \overline{I_{n,in}^2} = \frac{kT}{R_L^2 C_D} \tag{5}$$

Equation (4) and (5) indicates a direct trade-off between speed and noise. More specifically, eliminating C_D and R_L from these equations shows the direct-trade off as following.

$$\overline{I_{n,in}{}^2} = 2\pi kT\frac{R_B}{R_L} \tag{6}$$

$$\overline{I_{n,in}{}^2} = 4\pi^2 kTC_D R_B{}^2 \tag{7}$$

From (4), if R_L is increased to increase the transimpedance gain, bandwidth goes down proportionally. On the other hand, if R_L is decreased, bandwidth and input referred noise both go up from (4) and (6). Moreover, from (7), if bandwidth goes up, input referred noise goes up proportional to the square of the bandwidth. These relations show several trade-offs between transimpedance gain, bandwidth and input-referred noise that can't be mitigated using a simple diode/resistor combination. Rather, a more complex and sophisticated circuit design is necessary to relax these trades-offs and increase the flexibility of design.

2.4 Conventional topologies of TIA

2.4.1 Common gate TIA

The common gate TIA shown in Figure 5 is a basic implementation. Neglecting second order effects in the transistors, the input impedance is $1/g_m$, where g_m denotes the transconductance of the input transistor. Proper choice of bias current provides a low input resistance, maximizing the input bandwidth. The noise current of the load resistor and the bias current source are directly referred to the input, leading to high noise at low supply voltage. So, it's difficult with common gate TIA to achieve high bandwidth and a reasonable transimpedance gain at low noise application with low supply voltages. Some kind of feedback topology is necessary to ameliorate the trade-offs.

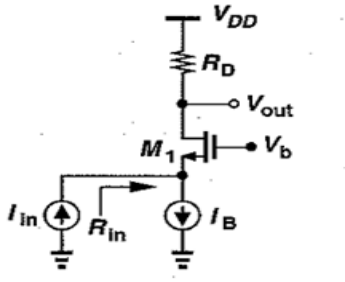


Figure 5: Common Gate TIA, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

2.4.2 Common source TIA with feedback

Most common feedback topology for TIA is “voltage-current” or “shunt-shunt” feedback topology as shown in Figure 6. This type of feedback is chosen because it lowers both the input resistance and thus increasing the bandwidth by increasing the input pole magnitude and output impedance, thereby yielding better drive capability. To achieve high sensitivity and wide bandwidth simultaneously, a common source TIA as depicted in Figure 6 is preferred. For the common source configuration of TIAs, shunt feedback resistance, R_F, is usually employed to provide low input impedance. Resistive load, R_L, is typically used to have wideband response but it suffers from direct trade-off between gain and voltage headroom. At low voltage supplies, the headroom required by load resistance reduces the achievable transimpedance gain of each stage. If the resistive load is replaced by PMOS load then the voltage headroom can be slightly relaxed from gain and gain can be increased.

Highly scaled CMOS technologies such as 65 nm or 45 nm CMOS provide NMOS and PMOS devices with high unity gain cut-off frequencies. As a result, these technologies can be advantageous for high speed data communication. However, as the device size shrinks the breakdown voltage of transistors scales down too, necessitating low supply voltage for successful operation. So, trade-off between gain and voltage headroom is more critical for common source TIA in nano-scale circuit design.

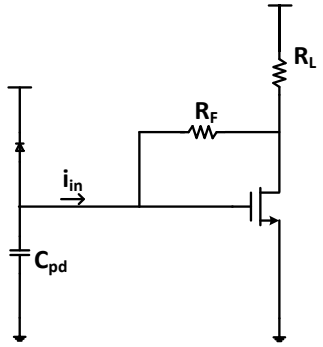


Figure 6: Common source TIA with shunt feedback

The input resistance and transimpedance gain of a common source TIA with shunt feedback (Figure 6) are (8) and (9) respectively,

$$R_T - \frac{g_m R_F - 1}{g_m R_L + 1} R_L \approx -R_F \tag{8}$$

$$R_{in} = \frac{R_F + R_L}{g_m R_L + 1} \tag{9}$$

As it can be seen from (8) and (9), trade-off exists between input resistance and transimpedance gain of common source TIA. To make transimpedance gain higher R_F needs to be increased. But increasing R_F increases the input impedance which results in reduction of the input pole frequency.

2.4.3 Regulated cascode

The regulated cascode amplifier shown in Figure 7 is widely used for broad-band TIA design in high-speed optical communication. It's a modified common gate amplifier composed of common gate architecture with a local feedback. The common gate amplifier consists of transistor M_1 and resistor R_1 while local feedback is created by transistor M_2 connected between the gate of M_1 and its source.

Transistor M_2 with resistor R_2 forms a common source configuration which gets a small portion of input signal and creates a voltage at the gate of M_1. This signal is amplified at the output of M_1 and increases the amplified output of M_1 in common gate configuration. M_2 increases the effective transconductance of whole architecture which helps to reduce the input resistance to isolate the input pole associated with large parasitic capacitance, C_{pd} from the bandwidth determination. Accordingly, unlike common gate or common source TIAs, the dominant pole of RGC is usually located within the amplifier rather than at the input node. The input resistance and transimpedance of RGC are shown in (10) and (11) respectively [9].

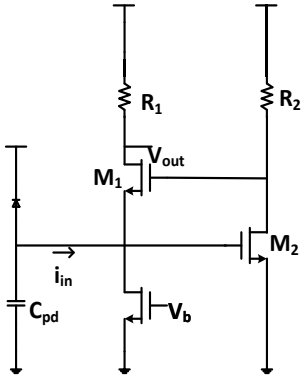


Figure 7: Conventional regulated cascode (RGC)

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2}R_2)} \tag{10}$$

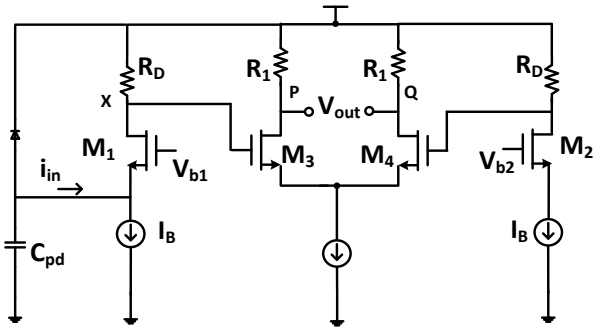
$$Z_{TIA} = \frac{v_{out}}{i_{in}} = \frac{R_1}{s^2 C_{PD} C_o R_{in} R_{out} + s(C_{PD} R_{in} + C_o R_{out}) + 1} \tag{11}$$

The typical RGC amplifier suffers from trade-off between gain, bandwidth and input referred noise. Modification of the RGC architecture can improve the performance by relaxing these trade-offs.

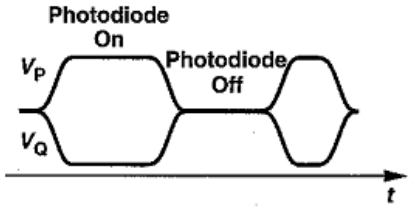
2.4.4 Differential TIA

Differential TIA as shown in Figure 8(a) is usually employed to suppress the effect of supply and substrate noise. It also improves the linear performance of the amplifier. Another advantage is that the output voltage swing of a differential TIA is two times the voltage swing of a single ended amplifier.

There are three major issues in differential TIA design [12]. Firstly, the signal generated at node X propagates to the output through two different paths with M_3 acting as a common source stage in the X-P path and M_3-M_4 as cascade of a source follower and common gate stage in the X-Q path. As a result, an asymmetric output waveform is produced because high frequency signal components experience unequal gain and phase shifts. Second, input referred noise of a differential TIA is $\sqrt{2}$ times the input referred noise of a single ended TIA. Third, if the circuit is perfectly symmetric, the output swings are not fully differential as illustrated in Fig. 8. This is a serious issue, because it causes threshold voltage modulation and makes the choice of decision threshold difficult.



(a)



(b)

Figure 8: (a) Pseudo-differential CG stage, (b) output waveforms, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

Figure 9 depicts one of the most common approaches to convert the output of a single-ended TIA to a truly differential signal. Here, the low pass filter consisting of R_1 and C_1 extracts the dc level of the TIA output, applying the result to the gate of M_3. Since both V_X and V_Y have same average voltage, output V_X-V_Y is free from dc offset and the output is truly differential.

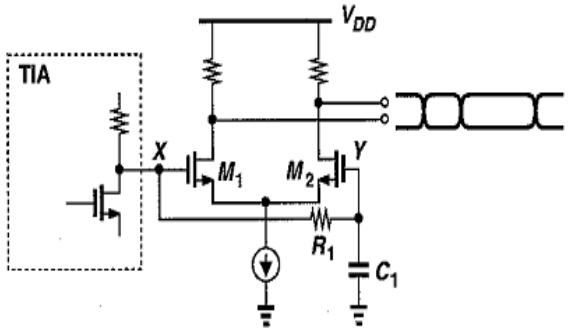


Figure 9: Single-ended to differential conversion, Behzad Razavi-"Design of Integrated Circuits for Optical Communications". Used under fair use, 2013.

Chapter 3

Review of High Speed CMOS TIAs

Until now, CMOS TIAs of maximum data rate of 40 Gb/s have been published in different IEEE conferences and journals. Before we start designing a 100 Gb/s TIA, an intensive study of all the published papers of 40 Gb/s TIAs have been made to get insight into different design ideas and to be aware of the state of the art CMOS TIAs. In this section we will discuss the underlying design concepts and performance of different 40 Gb/s TIAs studied.

3.1 Modified regulated cascode

Bashiri et al. [9] proposed a modified version of regulated cascode amplifier to achieve improved frequency response and lower input referred noise. The modified structure is depicted in Fig. 10 (a) which incorporates a local feedback network that connects the gate of M_1 to its drain. The basic idea is to implement a Cherry-Hooper configuration to increase the bandwidth. Similar to a Cherry-Hooper amplifier, local feedback reduces the resistance seen at node X and output. So, poles associated with those nodes are pushed to higher frequencies and the bandwidth of the TIA is increased. In a previous work [5] only the resistor was placed in the feedback path whereas in this work an inductor is also placed for further bandwidth enhancement.

In this design, shown in Figure 10, M_1 acts as a common source amplifier to the signal flowing from the drain of M_2 to the gate of M_1 and it experiences miller effect. The inductor in the feedback path can be chosen to resonate with miller C_{gd1} to achieve enhanced bandwidth.

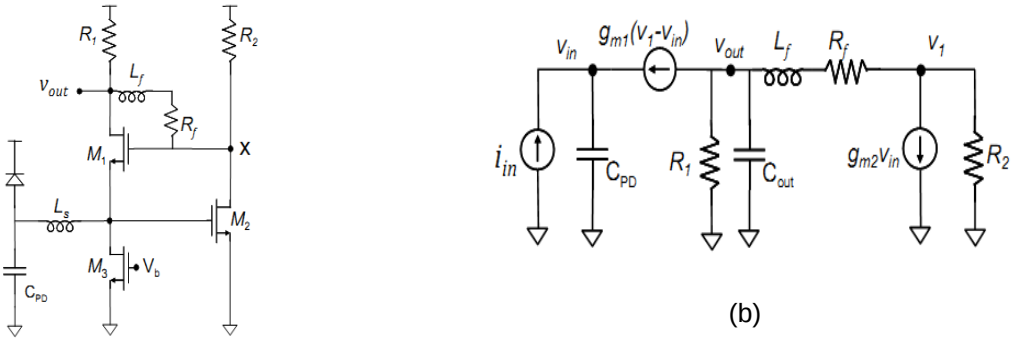


Figure 10: (a) Modified regulated cascode, (b) Small signal equivalent of modified RGC, S. Bashiri, C. Plett, J. Aguirre and P. Schvan "A 40 Gb/s Transimpedance Amplifier in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp- 757-760, May 2010. Used under fair use, 2013.

The modified regulated cascode architecture also modifies the biasing property of the circuit by creating an additional path for bias current to flow. Without a feedback path, the total bias current of M_1 flows through R_1 and voltage stress on it limits the gain and input referred noise of the circuit. The feedback path creates an additional path for bias current to flow and voltage stress on R_1 is largely reduced. So, R_1 can be increased keeping the same bias current to improve the gain and input referred noise.

Figure 10 (b) shows the simplified small signal model of modified RGC [9] excluding series inductor, L_s. The input resistance and transfer function of TIA are shown in (5) and (6) respectively [9]. The feedback path makes the two real poles as in (2) to complex conjugate poles that can be utilized for bandwidth extension. In addition, the inductor in the feedback path adds another pole to resonate with C_{gd1}. The inductor also introduces a zero, which can be placed close to the poles to exhibit more peaking. Since peaking increases overshoot and jitter of eye diagram, the optimum value of inductor needs to be chosen for flat response. Figure 11 shows the effect of L_f on the bandwidth of TIA and flat response is achieved when L_f is 500 pH.

$$R_{in} = \frac{R_f + R_1(1+g_{m1}R_2)}{g_{m1}(1+g_{m2}R_2)(R_1+R_f)} \tag{12}$$

$$Z_{TIA} = \frac{\frac{R_1}{R_1+R_f}(sL_f+R_f)}{s^3 C_{in}C_o L_f \frac{R_1}{g_{m1}(1+g_{m2}R_2)(R_1+R_f)} + s^2\left[\frac{C_{in}L_f}{g_{m1}(1+g_{m2}R_2)(R_1+R_f)} + C_o L_f \frac{R_1}{R_1+Rf} + C_{in}C_o \frac{R_1(R_f+R_2)}{g_{m1}(1+g_{m2}R_2)(R_1+R_f)}\right] + s\left[\frac{L_f}{R_1+R_f} + C_{in}\frac{R_f+R_1(1+g_{m1}R_2)}{g_{m1}(1+g_{m2}R_2)(R_1+R_f)} + C_o\frac{R_f R_1}{R_1+Rf}\right]+1}$$

(13)

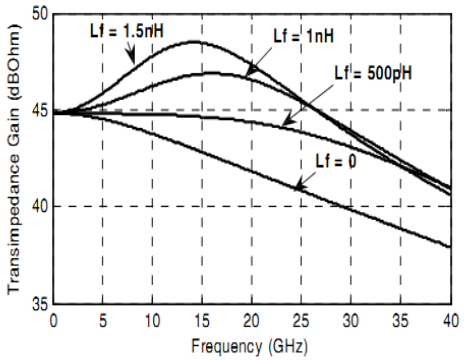


Figure 11: Effect of L_f on the bandwidth of TIA, S. Bashiri, C. Plett, J. Aguirre and P. Schvan "A 40 Gb/s Transimpedance Amplifier in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp- 757-760, May 2010. Used under fair use, 2013.

In addition to the local feedback, the input series inductor L_S, shown in Figure 12, introduces complex poles in the transfer function which can increase the bandwidth more when the resonance frequency of L_S and CPD are coincident with the dominant pole of TIA.

For noise analysis, E_n-I_n model is used as illustrated in Figure 12. This incorporates both noise current from the TIA and noise voltage from photodetector diode capacitance, C_{PD}. This assumes that I_n and E_n are uncorrelated equivalent input referred noise is as in (14). From equation (14) it is also evident that the high frequency noise up to the resonance frequency of L_s and C_{PD} is suppressed.

$$i_{n,eq}^2 = (1-\omega^2 L_s C_{PD})^2 I_n^2 + \omega^2 C_{PD}^2 E_n^2 \qquad (14)$$

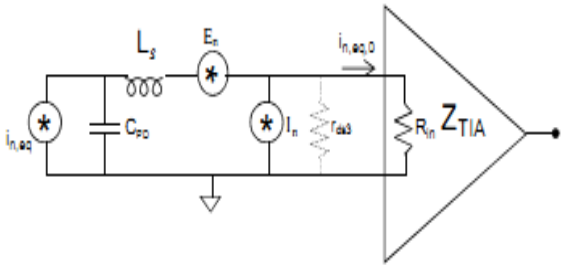


Figure 12: E_n-I_n model for noise analysis, S. Bashiri, C. Plett, J. Aguirre and P. Schvan "A 40 Gb/s Transimpedance Amplifier in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp- 757-760, May 2010. Used under fair use, 2013.

Figure 13 shows the comparison of transimpedance gain and input referred noise current density of the circuit proposed by Bashiri et al. [9], typical RGC structure and RGC with series L_s through analysis. Proposed architecture of Bashiri et al. [9] achieves higher bandwidth and lower input referred noise than other RGC architectures.

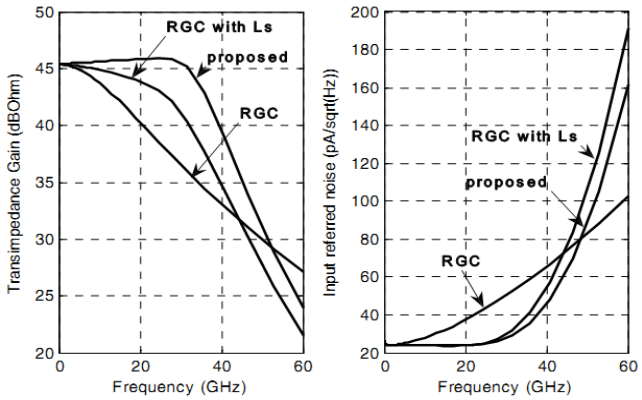


Figure 13: Gain and noise comparison of the modified RGC with typical RGC and RGC with series peaking inductor , S. Bashiri, C. Plett, J. Aguirre and P. Schvan "A 40 Gb/s Transimpedance Amplifier in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp- 757-760, May 2010. Used under fair use, 2013.

3.2 Low power push pull transimpedance amplifier

Kim and Buckwalter [10] proposed a push-pull architecture TIA as depicted in Figure 14 in 45 nm SOI CMOS technology. In this architecture, a PMOS transistor replaces the resistive load of common source TIA and the gate of NMOS and PMOS are tied to the input signal. A shunt feedback resistor RF is incorporated in the first stage to provide constant input and output biasing and to control transimpedance and input resistance. The geometry of NMOS and PMOS

are chosen to produce a symmetric voltage transfer function that achieves maximum gain when input and output are biased to $V_{DD/2}$.

This architecture has two major advantages. Firstly, the drain current is reused and intrinsic gains of both devices are utilized while increasing the effective transconductance g_m of the circuit. Secondly, the voltage headroom is largely relaxed as resistance is replaced by PMOS and power dissipation is reduced.

Figure 15 shows simulated unity gain cut-off frequency of 45 nm SOI CMOS process. For both NMOS and PMOS, cut-off frequency is greater than 250 GHz at a current density of 0.1 mA/μm. This level of high cut-off frequencies of transistors enable this technology to realize simple architecture of push-pull or "inverting" amplifier to achieve sufficiently high bandwidth for 40 Gb/s data rate.

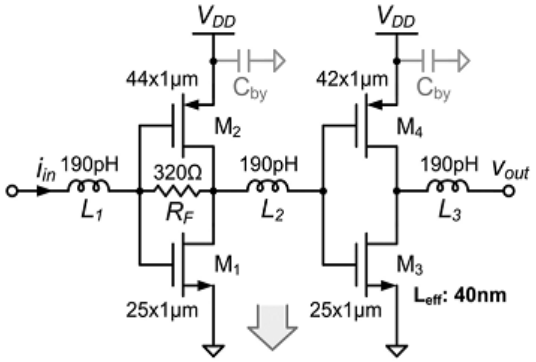


Figure 14: Push-pull TIA proposed by by J. Kim and J. F. Buckwalter "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 1-4, March 2012. Used under fair use, 2013.

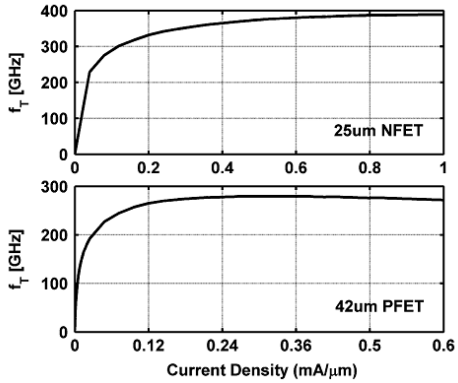


Figure 15: Simulated unity gain cut-off frequency for 45 nm SOI NMOS and PMOS devices [10], J. Kim and J. F. Buckwalter "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS", *IEEE Journal of Solid-State* vol. 47, no. 3, pp. 1-4, March 2012. Used under fair use, 2013.

The unique characteristic of a push-pull amplifier is that it places NMOS and PMOS transistors in parallel and the total transconductance becomes a combination of transconductance of both devices $g_{m,o} = g_{m,n} + g_{m,p}$. Similarly, the combined channel transconductance is $g_{ds,o} = g_{ds,n} + g_{ds,p}$ where $g_{ds,n}$ and $g_{ds,p}$ are channel conductance of NMOS and PMOS respectively. The transimpedance gain, R_T can be expressed as equation (15) [10].

$$R_T = \frac{1 - g_{m,o} R_F}{g_{m,o} + g_{ds,o}} \approx \frac{-R_F}{1 + \frac{1}{|A_o|}} \tag{15}$$

Here $A_o = -g_{m,o} / g_{ds,o}$ is the small signal intrinsic gain of the amplifier. A post amplifier stage is cascaded with the TIA to achieve increased gain. The amplifier stages are dc coupled, so they are self-biased through R_F .The input impedance can be found as equation (16) [10].

$$R_I = \frac{1 + g_{ds,o} R_F}{g_{m,o} + g_{ds,o}} \approx \frac{R_F}{|A_o|} \tag{16}$$

For measurement purposes, input impedance is typically matched to 50 Ω and R_F is chosen based on A_o. However, transimpedance gain also depends on RF and trade-off exists between transimpedance gain and input impedance.

The small signal model of the TIA proposed by Kim and Buckwalter [10] is shown in Figure 16. For achieving high bandwidth and low group delay variation, a π-network is formed by inserting inductors between amplifier stages and also between the photodiode and TIA input. The inductors present in the network cause peaking in the transimpedance response and increase the bandwidth. The optimum inductor is required to design for flat response with low group delay variation. π-network also improves the frequency response of the input impedance and inter-stage matching network.

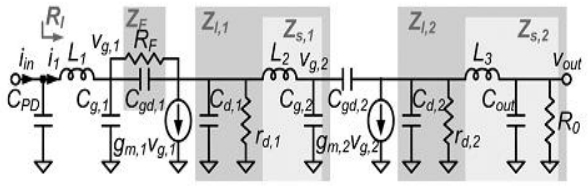


Figure 16: Small signal model of push-pull TIA , J. Kim and J. F. Buckwalter "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS", *IEEE Journal of Solid-State* vol. 47, no. 3, pp. 1-4, March 2012. Used under fair use, 2013.

The total transimpedance of the TIA can be expressed as [10],

$$Z_{T,total} = H_o(s) \cdot Z_{T,1}(s) \cdot A_2(s) \tag{17}$$

Here $H_o(s)$ is the current transfer function from the photodiode to the input of TIA. $Z_{T,1}(s)$ is the transfer function of the transimpedance amplifier with π-network for inductive series peaking. $A_2(s)$ is the voltage gain of the post amplifier. Figure 17 shows the analytical result of transimpedance and group delay based on the transfer function (17). To get the optimum value of inductors they are swept across three different values. 190 pH provides the best response.

The total input referred noise current of shunt feedback TIA is expressed as,

$$\overline{I_{n,TIA}{}^2}(f) = \overline{I_{n,RF}{}^2}(f) + \overline{I_{n,AMP}{}^2}(f) \tag{18}$$

Here, $\overline{I_{n,RF}{}^2}(f)$ is the thermal noise of the feedback resistor and $\overline{I_{n,AMP}{}^2}(f)$ is the input referred amplifier noise. Fig. 18 shows the simulated input referred noise of the TIA with noise contribution of shunt resistor RF. At low frequencies noise from RF dominates. At higher frequencies the noise contribution due to the channel f^2 noise dominates and the total spectral density increases.

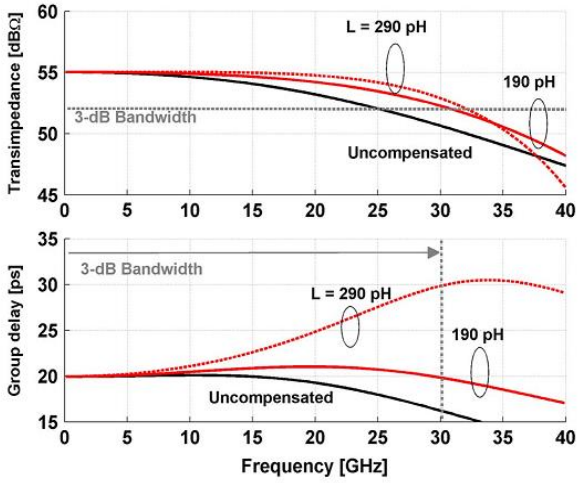


Figure 17: Analytical results of transimpedance and group delay , J. Kim and J. F. Buckwalter "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS", *IEEE Journal of Solid-State* vol. 47, no. 3, pp. 1-4, March 2012. Used under fair use, 2013.

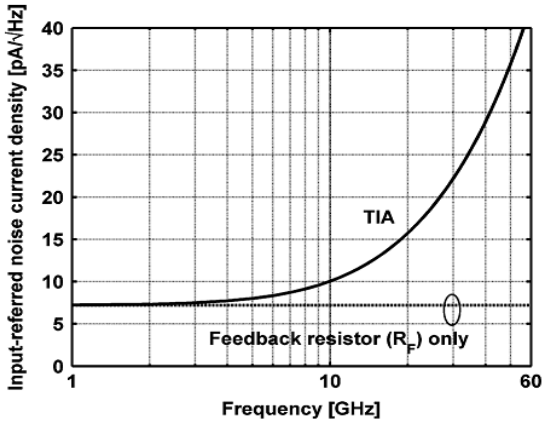


Figure 18: Simulated input referred noise current density J. Kim and J. F. Buckwalter "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS", *IEEE Journal of Solid-State* vol. 47, no. 3, pp. 1-4, March 2012. Used under fair use, 2013.

3.3 Differential TIA with nested feedback

Chou et al. [11] proposed a differential TIA in 65 nm CMOS technology as shown in Figure 21. Figure 19 illustrates only the core amplifier of TIA consisting of three cascaded transconductance stages with dual feedback paths. Feedback path I (G_{mf1}) suppresses the impedance at internal nodes by providing higher loop gain and eventually extends the bandwidth.

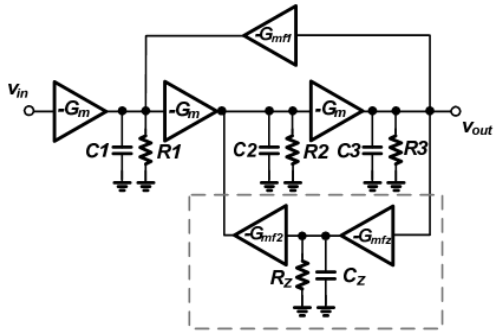


Figure 19: TIA core amplifier, S. T. Chou, S. H. Huang, Z. H. Hong, and W. Z. Chen "A 40 Gbps Optical Receiver Analog Front-End in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS),* pp.-1736-1739, May 2012. Used under fair use, 2013.

In a previous work [14] only feedback path I was incorporated. The addition of feedback path II, composed of G_{mfz}, G_{mf2}, C_z and R_z in this work, improves the bandwidth more by splitting the internal poles for stagger bandwidth turning. In addition, feedback path II introduces

a pole and a zero in the transfer function. If the pole frequency is designed to be much higher than the zero frequency, the zero can be utilized for extending the bandwidth further. From the simulated frequency response of the core amplifier as shown in Figure 20, feedback path II increases the 3-dB bandwidth from 19 GHz to 25 GHz.

In the actual circuit implementation as depicted in Figure 21, inductors are incorporated to increase the bandwidth. Shunt peaking inductor L_D introduces a zero and complex pole in the transfer function that increases the bandwidth. Input series peaking inductors L_{s1} and L_{s2} isolate the photodiode capacitance from the input node of the TIA. Similarly, output series peaking inductor L_{s3} isolates the large load capacitance of the limiting amplifier and improves the bandwidth.

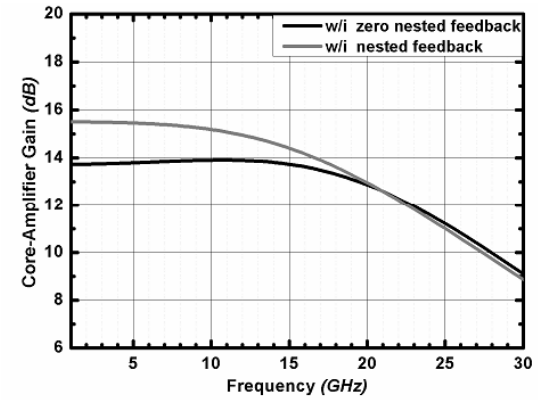


Figure 20: Simulated frequency response of core amplifier, "A 40 Gbps Optical Receiver Analog Front-End in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp.-1736-1739, May 2012. Used under fair use, 2013.

Noise analysis was not done for the TIA proposed by Kim and Buckwalter [11] and was not reported in the paper. Group delay analysis was not done and also not reported. This is a major drawback of this work, since large group delay variation can introduce significant data dependent jitter in data eye and degrade the signal integrity.

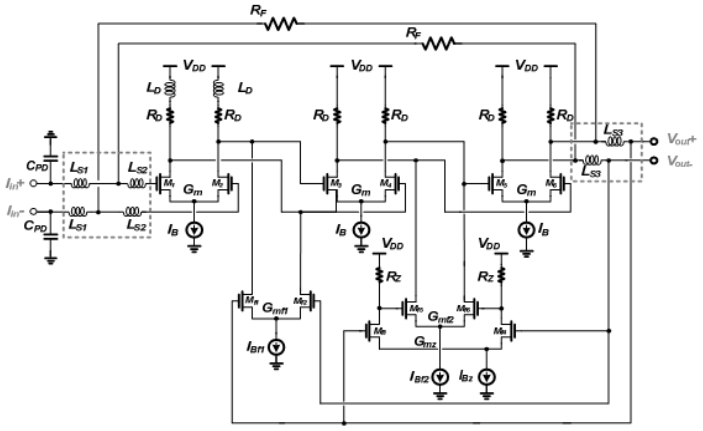


Figure 21: Circuit schematic of TIA proposed by Chou et al. "A 40 Gbps Optical Receiver Analog Front-End in 65 nm CMOS", *International Symposium on Circuits and Systems (ISCAS)*, pp.-1736-1739, May 2012. Used under fair use, 2013.

3.4 Common gate TIA with RTRN (Reverse Triple Resonance Network)

Liao and Liu [7] proposed a new bandwidth enhancement technique- RTRN (Reverse Triple Resonance Network) to enhance the bandwidth of TIA. A mathematical model of the system was derived in their work to facilitate the design and analysis of the RTRN based network, also manifesting that the network is better than the shunt-series peaking technique for improving bandwidth.

The implementation of the TIA proposed by Liao and Liu [7] is shown in Figure 22. The TIA circuit incorporates a common gate circuit with RTRN network and differential amplifier to allow easier biasing scheme and improve the immunity of the network from bond wire inductance on the supply pads. Source followers are inserted between the feedback resistors and the differential stage to mitigate the loading effect of the resistors.

To take advantage of the feedback loop, gain needs to be maintained up to high frequencies, requiring some bandwidth enhancement technique. [15] shows that shunt-series peaking or triple resonance network (TRN) as shown in Fig. 19 (b) increases the bandwidth 3.5 times if the parasitic capacitances are evenly distributed between the present and next stage, but starts to deteriorate in a more realistic scenario when the capacitance of the next stage is significantly larger than the present stage. Hence, improved bandwidth enhancement technique is

necessary. To do this, the input and output ports of the network formed by L_1-R_1-L_2 in [15] is interchanged resulting in the inductive series-shunt peaking configuration as shown in Figure 23 (a).

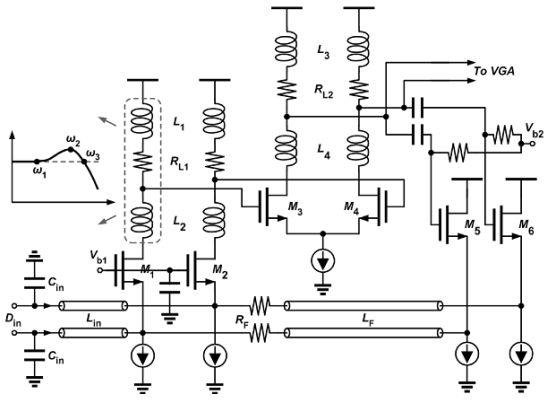


Figure 22: Circuit schematic of TIA proposed by C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 - 655 March 2008. Used under fair use, 2013.

The proposed inductive shunt-series peaking network is called RTRN (reverse triple resonance network). To facilitate the effectiveness of RTRN, the parasitic capacitance is considered distributed unevenly, with $C(1-\alpha)/2$ on the present stage and $C(1+\alpha)/2$ on the next stage. Since the sum of C_{GS} and Miller capacitance C_{GS} is usually larger than the drain-bulk junction capacitance, it's tacitly assumed greater than zero in the following analysis.

From Figure 23 (a) the network is fourth order and simply getting the transfer function of it will not give any insight of the network. So, the network is simplified by making the Norton equivalent of the circuit left to the dotted line as depicted in Figure 23(b). The overall network can be further simplified as in Figure 23(c), where the equivalent impedance Z_{tot} is expressed as,

$$Z_{tot}(j\omega) = (R_{eq} + j\omega L_{eq}) \parallel \frac{1}{j\omega C_{eq}}$$

$$= [\frac{R_1}{1-\omega^2 L_2 \frac{C}{2}(1-\alpha)} + j\omega \frac{L_1}{1-\omega^2 L_2 \frac{C}{2}(1-\alpha)}] \parallel [\frac{1}{j\omega C} \frac{L_1}{1-\omega^2 L_2 \frac{C}{4}(1-\alpha^2)}] \qquad (19)$$

From (19) the network it can be observed that there are three resonance frequencies, ω_1, ω_2 and ω_3 among them ω_1, ω_2 are in the first term and ω_3 is in the second term. Because of the three resonance frequencies and horizontally flipped configuration of shunt-series peaking network, the proposed network is called RTRN. From above analysis, it is also possible to design easily the desired frequency response.

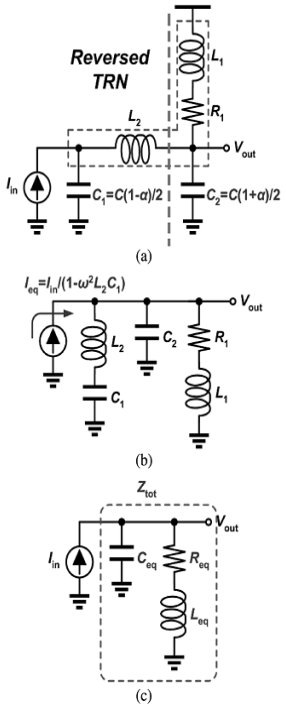


Figure 23: (a) Model of the RTRN, (b) simplified version, (c) final equivalent circuit C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 - 655 March 2008. Used under fair use, 2013.

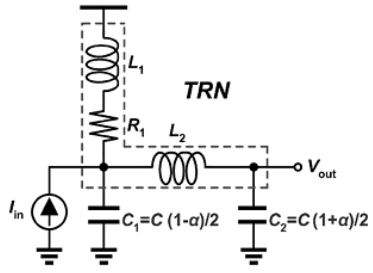


Figure 24: Model of the TRN, C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 - 655 March 2008. Used under fair use, 2013.

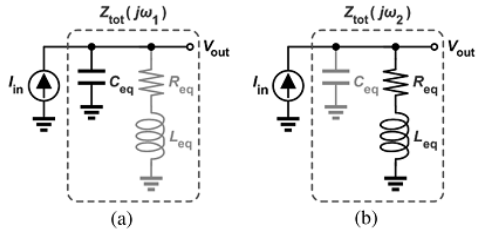


Figure 25: Equivalent Z_{tot} when resonance occurs at two different frequencies, C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 - 655 March 2008. Used under fair use, 2013.

From analysis, the three resonance frequencies can be obtained as,

$$\omega_1 = 1/\sqrt{L_1 C}\,,\ \omega_2 = \sqrt{\frac{2}{1+\alpha}}\omega_1 \text{ and } \omega_2 = \frac{f(\alpha)}{(1-\alpha)^2}\frac{2\sqrt[4]{6}}{CR_1} \text{ where,}$$

$$f(\alpha) = \sqrt[4]{1-\frac{\alpha}{3}}\,\mathrm{X}\sqrt{\frac{-\alpha\sqrt{6-2\alpha}+\sqrt{1+4\alpha^2-2\alpha^3+\alpha^4}}{1+\alpha}}$$

The above methodology can be applicable to TRN as shown in Figure 24 as well. Subsequently, the TRN can be simplified to the form as (19) except α is replaced by $-\alpha$. In addition, the resonance frequencies and the 3-dB frequency can also be found using the same analysis. Figure 26 and Figure 27 plot the locations of ω_2 and ω_3 as well as the gain at these frequencies for these two kinds of peaking networks. As α increases i.e. the capacitance in the following stage increases, the gain of RTRN network increases and shows more efficiency compared to the TRN network.

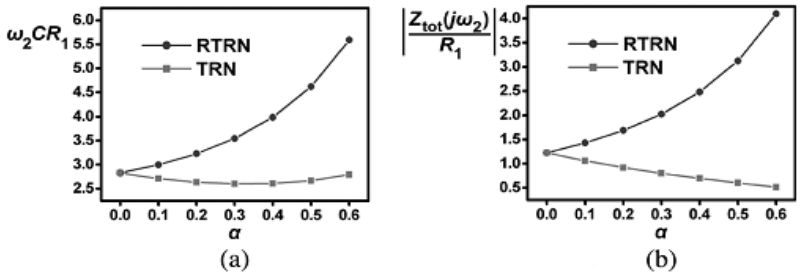


Figure 26: (a) ω_2 and (b) gain at ω_2 for different α , C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 – 655,March 2008. Used under fair use, 2013.

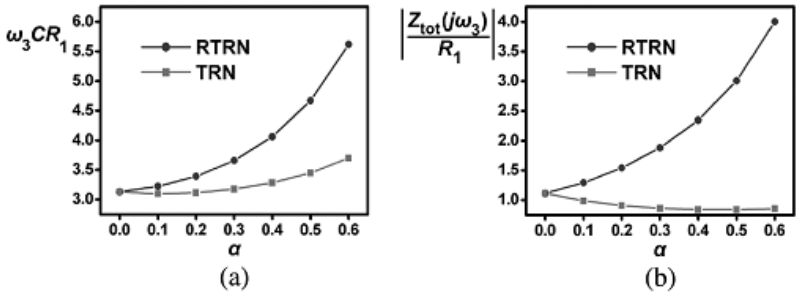


Figure 27: (a) ω_3 and (b) gain at ω_3 for different , C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 – 655, March 2008. Used under fair use, 2013.

To show more explicitly the effectiveness of RTRN network $\omega_{3,dB}$ in both cases are derived and plotted in Figure 28. Also, the simulated frequency response of RTRN, TRN and uncompensated TIA as shown in Figure 29 confirms that the RTRN network achieves higher bandwidth than the other two cases. However, the RTRN network does not require more inductors than the TRN network but achieves higher bandwidth enhancement.

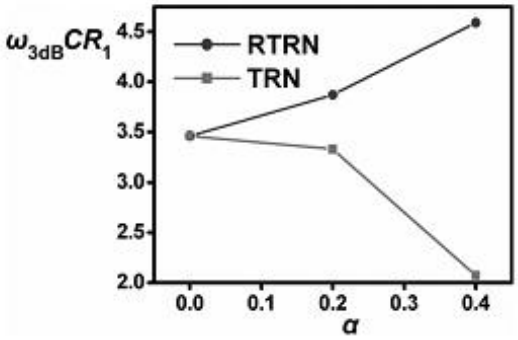


Figure 28: $\omega_{3,dB}$ for different α , C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 – 655, March 2008. Used under fair use, 2013.

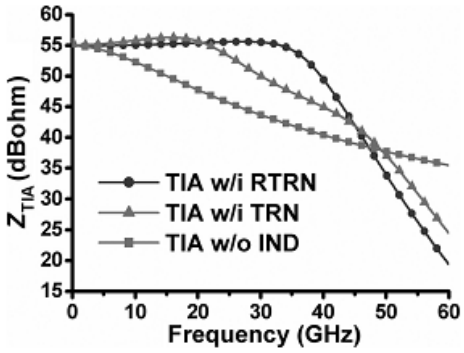


Figure 29: Comparison of simulated frequency response of RTRN, TRN and TIA without inductor C. F. Liao and S. L. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 642 – 655, March 2008. Used under fair use, 2013.

3.5 Group delay optimized TIA

A tradeoff between BWER and the phase linearity is often overlooked for bandwidth-enhancement techniques. Linear phase delay is represented by a flat group-delay response. Large group-delay variation results in DDJ (data dependent jitter) which degrades the signal integrity of the data eye. Kim and Buckwalter [8] proposed a technique to increase the bandwidth by inter-stage inductive series peaking while optimizing the group delay variation.

For analysis, a pi-network comprised of inter-stage inductor is inserted between the capacitance of the cascaded stages as shown in Fig. 30. With the absence of inter-stage inductor L, current of the first common source stage $i_{in}=g_m v_{gs}$ charges capacitance C_1+C_2 while voltage is limited by the RC time constant, where $C=C_1+C_2$. The presence of inductor L prevents the flow of current to the capacitance C_2 at the beginning so initially only the capacitance C_1 is charged. So, the rise time decreases and gain bandwidth product increases in the presence of L. However, frequency dependent network delay also increases with increased gain-bandwidth, which causes signal distortion at the output.

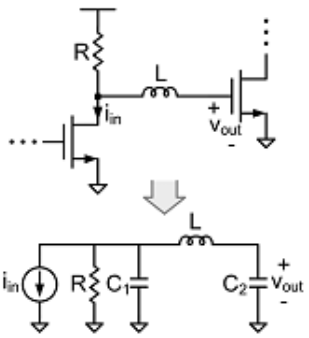


Figure 30: Series inter-stage inductor and equivalent small signal model, J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

The transimpedance of the inductive series pi-network between the drain of first stage and gate of subsequent stage acts as a third order response,

$$Z_{\pi}(s) = \frac{v_{out}(s)}{i_{in}(s)}$$

$$= \frac{R}{s^3 RLC_1C_2 + s^2 LC_2 + sR(C_1 + C_2) + 1}$$

$$= \frac{R}{(\frac{s}{\omega_u})^3 mn(1-n) + (\frac{s}{\omega_u})^2 mn + \frac{s}{\omega_u} + 1} \qquad (20)$$

where, $m = L/R^2(C_1 + C_2)$ and $n = C_2/(C_1 + C_2)$ are dimensionless parameters and their frequency responses are normalized to $\omega_u = 1/R(C_1 + C_2)$, the 3-dB bandwidth of the uncompensated transimpedance. The m parameter is characterized by the product of the, L/R and RC time constants, while the n parameter characterizes the capacitance ratio of C_1 and C_2 which are primarily determined by the relative size of active devices and associated device parasitic capacitances. Assuming that the gate capacitance is three times larger than the drain capacitances for devices of similar size n is approximately 3/4. Normalizing C_1 and C_2 to 0.25F and 75F, respectively, the 3-dB bandwidth of uncompensated case is unity, and $R_1 = 1$.

Figure 31 shows the normalized transimpedance gain response for different values of m. m=0 corresponds to the uncompensated case with unity bandwidth. As m is increased, the 3-dB bandwidth varies and maximally flat Butterworth response is achieved when m=2/3 and n=3/4.

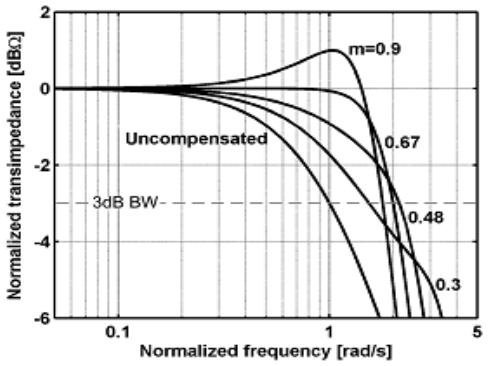


Figure 31: Normalized transimpedance response of inductive series peaking pi-network with varying m, J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

At this point, bandwidth improves by 100% from the uncompensated case. On the other hand, Bessel response corresponds to maximally flat group delay response and is only achieved when m=0.48 and n=0.83. But, the BWER (Bandwidth Enhancement Ratio) degrades to 1.8 for that case.

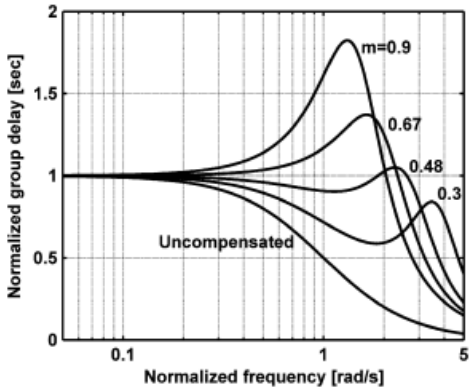


Figure 32: Normalized group delay response of inductive series peaking pi-network with varying m, J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

The denominator in (20) is a third-order polynomial with at least one real pole and two complex poles. The phase response is obtained by $\Phi_k(\omega)$ and summing the phase contribution of each pole.

$$\Phi(\omega) = \arg\{Z_\pi(\omega)\} = \sum_{k=1}^{3} \arctan \frac{\omega \pm \omega_k}{\sigma_k} \tag{21}$$

The normalized Butterworth poles are $s_1 = -2$ and $s_2, s_3 = -1 \pm j1.73$. The normalized Bessel poles are $s_1 = -2.32$ and $s_2, s_3 = -1.34 \pm j1.75$. For the maximum BWER, the normalized poles are $s_1 = -1.51$ and $s_2, s_3 = -1.24 \pm j2.41$. Since the group delay is defined by $\tau_g = -(d(\Phi)/d\omega)$, the group delay for the network is found by differentiating (21),

$$\tau_g = -\sum_{k=1}^{3} \frac{\sigma_k}{{\sigma_k}^2 + (\omega \pm \omega_k)^2} \tag{22}$$

Figure 32 shows the group delay response of the inductive series network and can be compared to the transimpedance gain response as shown in Fig. 31. From those two plots, there are several responses that offer high BWER, but not necessarily show low group delay variation. Butterworth response is achieved when m=0.48, but group delay variation is very high at this value. So, neither the Butterworth response, nor the Bessel response would be acceptable to have an optimized response between BWER and group delay variation. Accordingly, to make a compromise between these two extreme cases, m=0.67 is chosen which offers 2.13 times bandwidth enhancement with low group delay variation.

The TIA proposed by Kim and Buckwalter [8] is shown in Figure 33. The TIA structure is composed by transimpedance stage and two post-amplifier stages and realized in 0.13 μm CMOS technology with f_T=85 GHz. The TIA structure also incorporates an inter-stage inductive series network for enhanced bandwidth with low group delay variation.

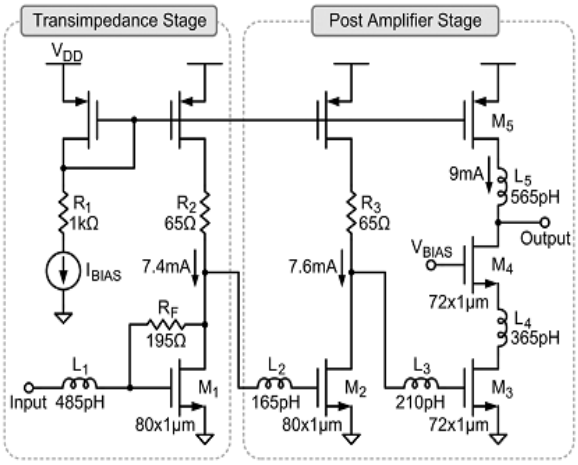


Figure 33: Circuit schematic of TIA proposed by J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

The small signal equivalent circuit of the proposed TIA is shown in Figure 34. The transimpedance and post amplifier stages are composed of a common source amplifier with PMOS load. The PMOS FETs act as a current source load and resistances R_2, R_3 and R_4 are inserted between the current source load and the drains of M_1, M_2 and M_3 to match the bias voltages and drain currents across each of the amplifier stages, but can be eliminated with reduced sizing of the PMOS load. An input series inductor L_1 is inserted between the photodiode capacitance and the input transimpedance stage to isolate the effect of photodiode capacitance from bandwidth determination.

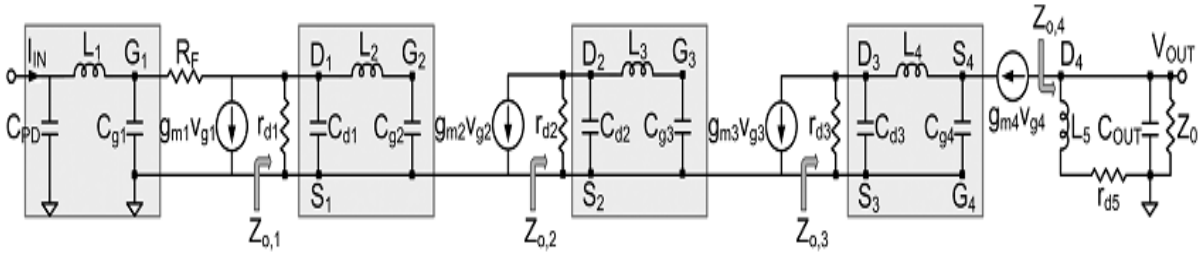


Figure 34: Small signal equivalent circuit of TIA proposed by J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

The detailed analysis of the transfer function of whole network can be found in [8]. Following the same analysis for BWER with low group delay variation, the poles are chosen for the transimpedance amplifier stage. The capacitance ratio in this case becomes $n = C_{PD}/(C_{PD}+C_I)$, where C_{PD} is photodiode plus bond capacitance and C_I is the input capacitance. This results in a capacitance ratio of 0.8. Figure 35 shows the simulated and analytical frequency response of the TIA. The predicted frequency response is accurate over the 3-dB bandwidth, but the analysis predicts a slightly higher bandwidth due to an underestimation of the poles above the simulated 3-dB bandwidth.

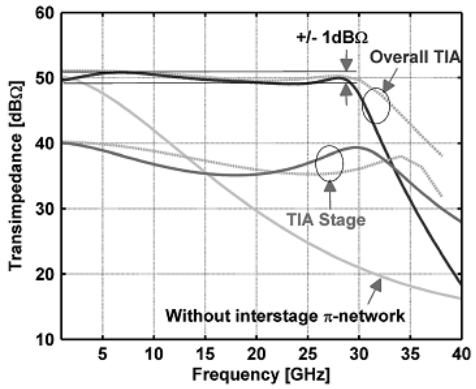


Figure 36: Simulation and analytical results of transimpedance response , J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

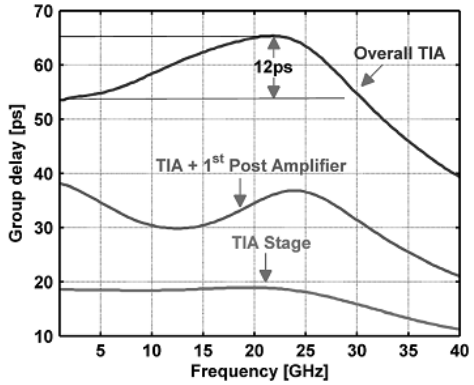


Figure 35: Group delay response of TIA, J. Kim and J. F. Buckwalter, "Bandwidth Enhancement with Low Group-Delay Variation for a 40-Gb/s Transimpedance Amplifier", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 57, no. 8, pp.- 1964 – 1972, August 2010. Used under fair use, 2013.

Group delay response of the TIA is shown in Figure 36. Based on the analysis, m is chosen as ≈0.52 to achieve low group delay variation. The low group delay of the first TIA stage causes a transimpedance ripple of 5 dBΩ at 18 GHz as shown in Figure 35. Therefore, extending the 3-dB bandwidth with low group-delay variation in the post amplifier stages requires the pi-network over the two subsequent stages to compensate the TIA transimpedance ripple.

3.6 Performance comparison of existing TIAs

In Table 1, performances of all the existing 40 Gb/s TIAs are summarized and compared to get a clear picture of different topologies. The red circles indicate the best performances for specific design parameters of the circuits.

Table 1: Comparison of existing TIAs

Paper No.	Process	Bit Rate (Gb/s)	BW (GHz)	Z_T (dB Ω)	GD (ps)	S22 (dB)	Noise ($pA/\sqrt{Hz}$)	Supply (V)	Power (mW)	Area (mm^2)	$BW\Omega/P_{DC}$ (Ω/J)
JSSC 2012 [10]	45 nm SOI	40	33	55	7.8	-10	20.47	1.0	9	0.29	1874.5
ISCAS 2010 [9]	65 nm	40	22	46.7	13 (sim)	-12	30 (sim)	1.2	39.9	0.044	----------
IEEE Tran. 2010 [8]	0.13 µm RF	40	29	50	16	-7.4	51.8 (sim)	1.5	45.7	0.4	200.7
ISCAS 2012 [11]	65 nm	40	35	52	-----	----	14	1.2	168	0.825	----------
JSSC 2008 [6]	0.18 µm	40	30.5	51	125	-10	55.7 (sim)	1.8	60.1	0.5382	180.1
JSSC 2008 [7]	90 nm	40	22	66	----	-----	22	1.2	75	0.56	585.3

Chapter 4

Proposed 100 Gb/s TIA

The increasing need of data transfer speed expects standardization of optical communication speeds greater than 100 Gb/s (~400 Gb/s) by 2014. The main goal of this project is to develop a CMOS integrated optical transceiver for 400 Gb/s optical fiber communication to meet the next generation data communication system. Designing high speed optical transceiver system is technically challenging and requires novel design approaches as well as design trade-offs involving many design parameters such as bandwidth, gain, supply voltage, noise, linearity, etc. In this section we are proposing a scheme to achieve the target data rate based on wavelength division multiplexing.

4.1 System block diagram

Figure 37 shows the block diagram of the proposed system, and it consists of four parallel channels with 100 Gb/s data rate for each channel. Clock and data recovery (CDR) blocks remove the noise from the parallel data and make the phase alignment of the data signals with well-defined clocks so that they can be reproduced precisely in the receiver side. Directly modulated lasers (DML) directly modulate the electric signal to optical signal. In May 2011, Fujitsu declared the successful operation of DML lasers of 40 Gb/s data speed without need for cooling and by 2014 it's expected that DML lasers of 100 Gb/s will come out. DML drivers increase the driving current of the DML lasers and increase the output light intensity. In the final stage, the WDM multiplexer multiplexes the four channels by wavelength division multiplexing to a single channel of 400 Gb/s speed and couples it to a single mode fiber (SMF).

On the receiver side, the 400 Gb/s stream of data is de-multiplexed by WDM DMUX and converted back to four parallel channels of 100 Gb/s. In the PD/TIA blocks photodetectors (PD) convert the optical data into electrical current and transimpedance amplifiers (TIA) amplify the current to a significantly large voltage. Then the converted voltage signals are passed through the

CDR blocks again to be cleared up from noise and converted back to the original data by analog to digital conversion.

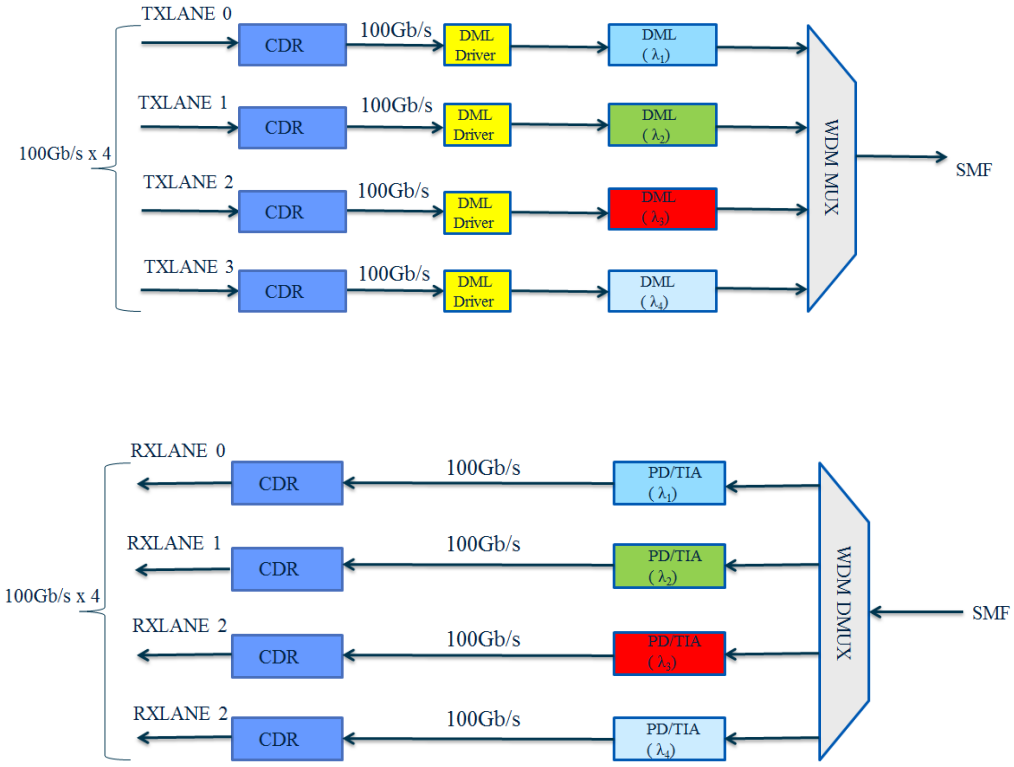


Figure 37: Proposed 400 GE Transceiver System

4.2 Proposed design of TIA

Currently available IEEE 802.3ba standard for 100 Gb/s optical communication - 4×25 Gb/s and 10×10 Gb/s wavelength division multiplexing suffer from several drawbacks such as, inter-channel crosstalk and high power consumption, mandating less no. of channels to accommodate 100 Gb/s data rate. Accordingly, the next generation 100 Gb/s optical transmission will be focused on reducing the number of channels to mitigate these issues. In the light of this circumstance, a single channel 100 Gb/s TIA in CMOS technology has been proposed in this work. The primary challenge of the proposed work is to increase the bandwidth much higher than the existing TIA architectures to minimize the inter-symbol interference (ISI) in 100 Gb/s data rate. In addition, high transimpedance gain, low input referred noise and small group delay variation are parts of design goal. Since total integrated noise of TIA trades with bandwidth, TIA

bandwidth is usually designed as 0.7 times bit rate to keep integrated noise as moderate as possible. Also, the trade-off between bandwidth and group delay variation [8] makes it extremely challenging to design a TIA in data rate as high as 100 Gb/s.

4.3 Block diagram of proposed TIA

Notorious parasitics of CMOS technology pose a severe hindrance to achieve high bandwidth which can be alleviated by judicial design architecture. A differential TIA is proposed in this work with a negative feedback network and RGC input to achieve enhanced bandwidth. The block diagram of proposed TIA is shown in Figure 38.

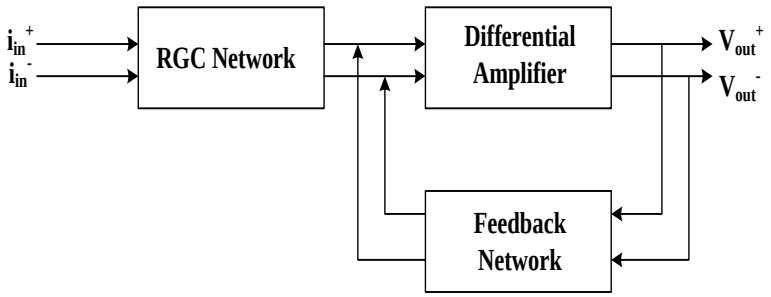


Figure 38: Block diagram of proposed TIA

4.3.1 Differential amplifier

The original circuit implementation of proposed TIA is shown in Figure 39. A differential amplifier is the core of the proposed architecture. A single-ended stand-alone TIA suffers from capacitive and inductive coupling from off-the chip bond wires to the input of the TIA, supply, and substrate. In differential architecture it is greatly reduced as the coupling is determined by the mismatches between two nominally identical paths [12]. To achieve wide-band response shunt-series peaking inductors L_{D2} and L_{S3} are incorporated in the architecture. The peaking inductors can increase the bandwidth up to 3.5 times the uncompensated bandwidth by forming a triple resonant network [15]. To improve the bandwidth more a capacitive degeneration network, R_S-C_S is employed to introduce additional peaking in the frequency response. Neither the Butterworth nor the Bessel response is ideal for a TIA to achieve high BWER (bandwidth enhancement ratio) with low group delay variation. Thus the desired response should be in

between these two extremes [8]. The values of inductors and degenerative capacitance are chosen accordingly.

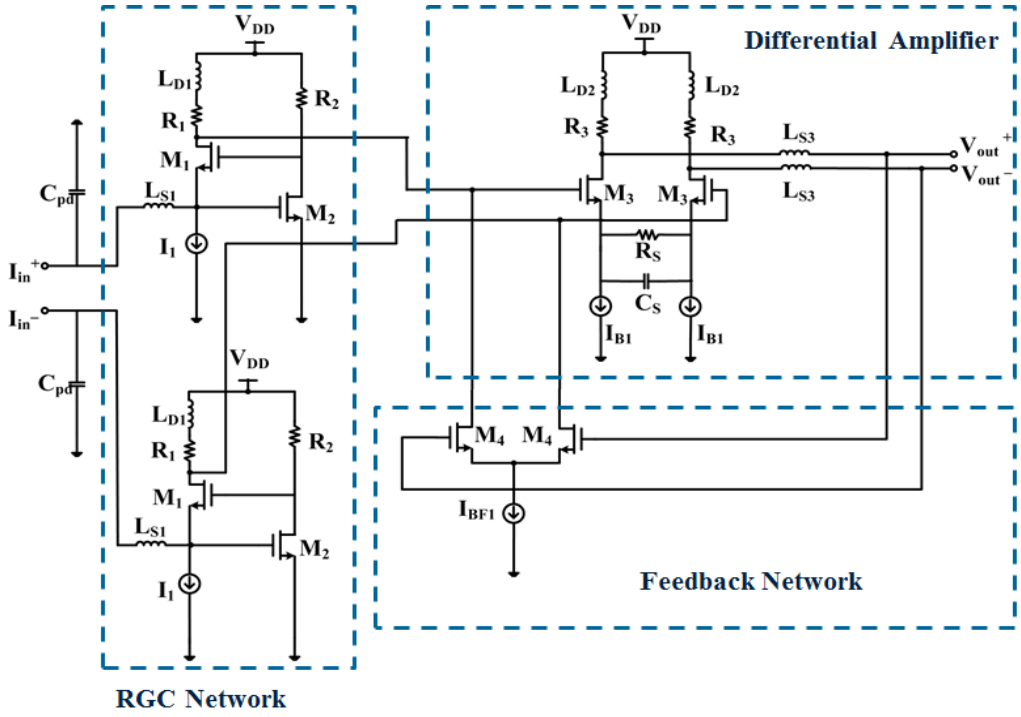


Figure 39: Circuit implementation of proposed TIA

4.3.2 RGC Network

Regulated cascode (RGC) is widely used for broad-band TIA design in high-speed optical communication. In the proposed design a RGC network is inserted between the input of differential amplifier and photodiode to attain wide band response. RGC is essentially a common gate amplifier with a local feedback. In the proposed architecture as depicted in Figure 39, transistor M_2 with resistor R_2 forms the local feedback of RGC amplifier. Local feedback herein acts as a common source amplifier which gets a small portion of input signal and creates a voltage at the gate of M_1. This signal is amplified at the output of M_1. Moreover, it increases the effective transconductance of common gate structure which reduces the input resistance [9]. Reduction in input resistance isolates the input pole associated with large parasitic capacitance, C_{pd} from the bandwidth determination. As a result, the dominant pole of TIA is located within the amplifier rather than at the input node. To increase the bandwidth more, shunt peaking

inductor L_{D1} and series peaking inductor L_{S1} are also incorporated in the RGC structure. These inductors are chosen similar to the technique described for the peaking inductors of differential amplifier.

4.3.3 Feedback network

Finally, a negative feedback network formed by transistor M_4 is implemented for further bandwidth enhancement. Feedback network increases the bandwidth by splitting the poles by stagger bandwidth tuning [1].

4.4 System analysis

In this section the circuit is analyzed to get more insight into the design. Analysis would be helpful to attain optimum performance of gain, bandwidth, input-referred noise and group delay variation. To have intuitive understanding of the circuit, simple approximation are made with proper reasoning and straight forward and complicated calculations are avoided.

4.4.1 Small signal model

Small signal model of proposed TIA architecture without the peaking inductors is shown in Figure 40. Without losing the generality and using the half circuit concept of differential architecture, small signal model of single ended version is shown in here. The other half of the circuit would be a duplication of this one with reverse polarity of input current. In Figure 40,

$$C_x = C_{gsb} + C_{sb1}$$

$$C_y = C_{gs1} + C_{gd2}$$

And, $C_z = C_s + C_{sb3}$

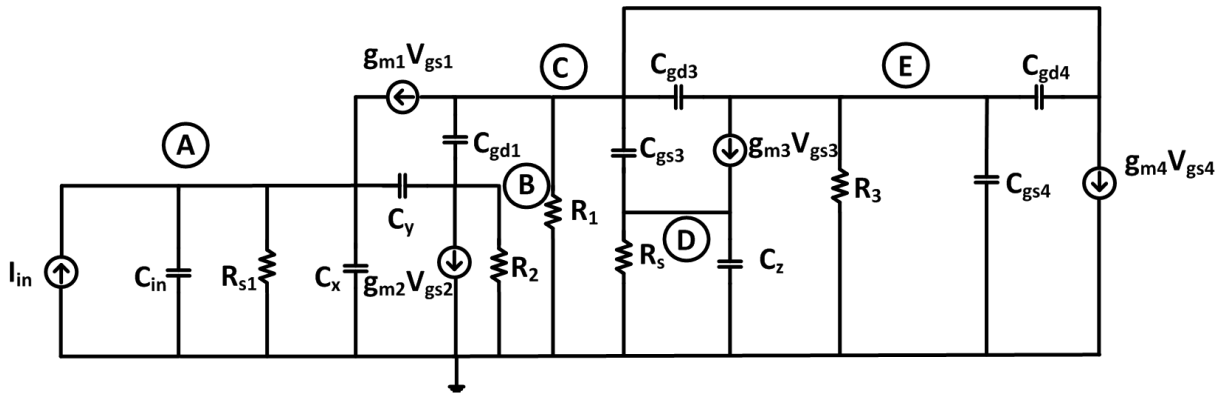


Figure 40: Small signal model of proposed circuit (without peaking inductors)

4.4.2 Transimpedance gain and location of poles

From Figure 40 transimpedance gain of the architecture and approximate location of poles are determined. To achieve the expression of transimpedance gain, Figure 40 is considered at low frequency with capacitors open circuited. Analyzing the circuit shows that the transimpedance gain is,

$$Z_T(0) = \frac{R_1 g_{m3} R_3}{1 + g_{m3}R_s + g_{m3}g_{m4}R_1R_3} \times \frac{g_{m1}R_{s1}(1 + g_{m2}R_2)}{1 + g_{m1}R_{s1}(1 + g_{m2}R_2)}$$

$$\cong \frac{R_1 g_{m3} R_3}{1 + g_{m3}R_s + g_{m3}g_{m4}R_1R_3} \tag{23}$$

Here loop gain is, $T = \frac{R_1 g_{m3} R_3 g_{m4}}{1 + g_{m3}R_s}$ .To determine the location of poles for the circuit as depicted in Figure 40, procedure described in [12] is followed. Poles are associated with each node and they can be determined by finding out the capacitance present from the nodes to ground and associated equivalent resistance parallel to the capacitors. When capacitors are connected between two nodes instead of from node to ground, they are split into two capacitors from each node to ground following Miller's theorem [12] as follows:

First pole located at node A is, $\omega_{p1} \cong \frac{1}{\frac{C_{total}}{g_{m1}(1 + g_{m2}R_2)}} \cong \frac{g_{m1}(1 + g_{m2}R_2)}{C_{total}}$ (24)

Here, $C_{total} = C_{in} + C_x + C_y(1 + g_{m2}R_2)$

Second pole located at node B is, $$\omega_{p2} \cong \frac{1}{(C_y + C_{gd1}(1 + \frac{g_{m1}R_1(1 + g_{m2}R_2)}{g_{m2}R_2}))R_2} \quad (25)$$

Third pole located at node C is,

$$\omega_{p3} \cong \frac{1}{(C_{gd1}(1 + \frac{g_{m2}R_2}{g_{m1}R_1(1 + g_{m2}R_2)}) + C_{gs3}(1 + \frac{g_{m3}R_s}{1 + (g_{m3} + g_{mb3})R_s}) + C_{gd3}(1 + g_{m3}R_3) + C_{gd4}(1 + g_{m3}R_3))(\frac{R_1}{1+T})}$$

(26)

Fourth pole located at node E is, $$\omega_{p4} \cong \frac{1}{(C_{gs4} + C_{gd3} + C_{gd4})(\frac{R_3}{1+T})} \quad (27)$$

And fifth pole located at node D is,

$$\omega_{p5} \cong \frac{1}{(C_{gs3}(1 + \frac{1 + (g_{m3} + g_{mb3})R_s}{g_{m3}R_s}) + C_z)(R_s \parallel \frac{1 + g_{m3}g_{m4}R_1R_3}{g_{m3}})} \quad (28)$$

Here, $C_z = C_{sb3} + C_s$

4.4.3 Location of zeros

One of the drawbacks of the aforementioned method is that the location of zeros cannot be determined. For instance, degenerating capacitance C_s introduces a zero in the system to cause peaking in the transfer function and enhance the bandwidth. Location of that is not achievable using above method. Using a simple common source amplifier as shown in Figure 41 with source degeneration the location of the zero can be easily found which is not affected by the feedback loop in the original circuit.

$$\omega_{z1} = \frac{1}{R_s C_s} \quad (29)$$

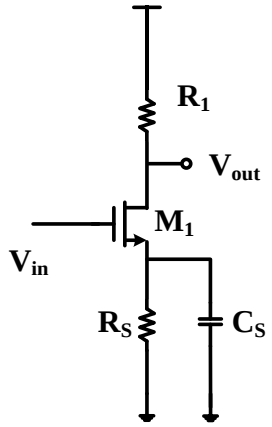


Figure 41: Common source amplifier with capacitive degeneration

Another zero can be found in the RGC network which is located at,

$$\omega_{z2} = \frac{1}{R_2 C_y}$$

Taking the zeros into account, transimpedance gain expression becomes,

$$Z_T \cong \frac{Z_T(0)(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})(1+\frac{s}{\omega_{p4}})(1+\frac{s}{\omega_{p5}})} \qquad (30)$$

From the equations (24) to (28), the dominant pole of the system is the third pole located at the node associated with R_1. The zero in (29) is placed very close to the dominant pole to mitigate the effect of the pole. The function of shunt and series peaking inductors is to improve the system transfer function by converting the real poles of the system to complex pole and introducing zeros. Their functionality is discussed in details in [12] and [15] and is not discussed here to avoid repetition.

4.4.4 Noise analysis

In this section an analysis to obtain input referred noise of the circuit at low frequency is done. Figure 42 shows the circuit with all the noise sources present. Shot noise from the photodetector, resistor thermal noise and drain thermal noise of the MOSFETs are considered as the main noise sources in the circuit.

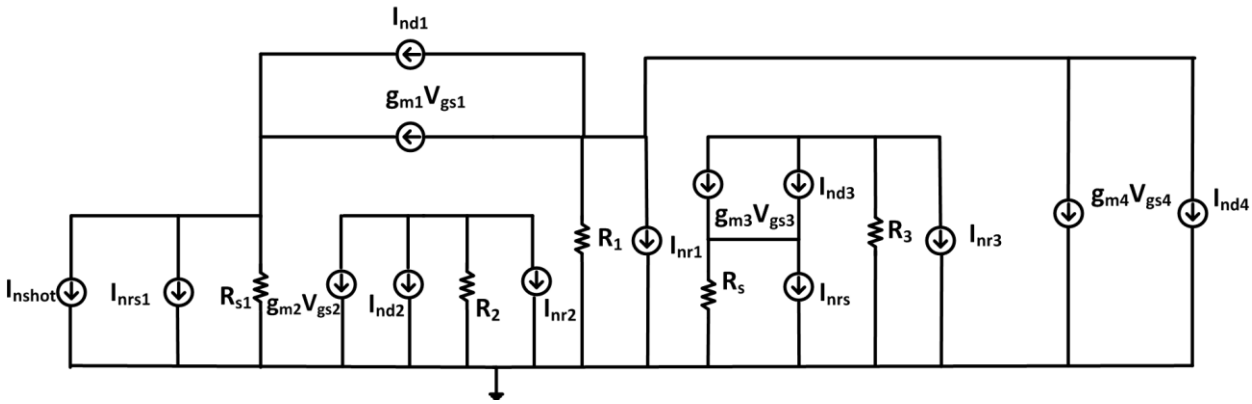


Figure 42: Circuit for low frequency noise analysis

Output noise voltage generated by the photodetector shot noise and thermal noise from R_{s1} is,

$$V_{n01} = \frac{R_1 g_{m3} R_3}{1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3} (I_{nshot} + I_{nrs1}) \tag{31}$$

Output noise voltage generated by the thermal noise from R_1 is,

$$V_{n02} = \frac{R_1 g_{m3} R_3}{1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3} I_{nr1} \tag{32}$$

Output noise voltage generated by the drain thermal noise from M_4 is,

$$V_{n03} = \frac{R_1 g_{m3} R_3}{1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3} I_{nd4} \tag{33}$$

Output noise voltage generated by the drain thermal noise from M_1 is,

$$V_{n04} = \frac{R_1 g_{m3} R_3}{(1 + g_{m1} R_{s1} (1 + g_{m2} R_2))(1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3)} I_{nd1} \tag{34}$$

Output noise voltage generated by the drain thermal noise from M_2 and thermal noise from R_2 is,

$$V_{n05} = \frac{g_{m1} R_1 g_{m3} R_3 R_2}{(1 + g_{m1} R_{s1} (1 + g_{m2} R_2))(1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3)} (I_{nd2} + I_{nr2}) \tag{35}$$

Output noise voltage generated by the drain thermal noise from M_3 is,

$$V_{n06} = \frac{R_3}{1 + g_{m3} R_s + g_{m3} g_{m4} R_1 R_3} I_{nd3} \tag{36}$$

Output noise voltage generated by the thermal noise from R_3 is,

$$V_{n07} = \frac{R_3(1+g_{m3}R_s)}{1+g_{m3}R_s+g_{m3}g_{m4}R_1R_3} I_{nr3} \tag{37}$$

Finally, output noise voltage generated by the thermal noise from R_s is,

$$V_{n08} = \frac{R_3 g_{m3} R_s}{1+g_{m3}R_s+g_{m3}g_{m4}R_1R_3} I_{nrs} \tag{38}$$

For the equivalent noise source the output noise voltage is,

$$V_{neq} = \frac{R_1 g_{m3} R_3}{1+g_{m3}R_s+g_{m3}g_{m4}R_1R_3} I_{neq} \tag{39}$$

Equating equation (39) with the summation of equation from (31)-(39) results in,

$$V_{neq} = V_{n01}+V_{n02}+V_{n03}+V_{n04}+V_{n05}+V_{n06}+V_{n07}+V_{n08}$$

$$\Rightarrow I_{neq} = I_{nshot}+I_{nrs1`}+I_{nr1`}+I_{nd4`}+\frac{1}{1+g_{m1}R_{s1}(1+g_{m2}R_2)} I_{nd1}+\frac{g_{m1}R_2}{1+g_{m1}R_{s1}(1+g_{m2}R_2)}(I_{nd2}+I_{nr2})$$

$$+\frac{1}{g_{m3}R_1} I_{nd3}+\frac{1+g_{m3}R_s}{g_{m3}R_1} I_{nr3}+\frac{R_s}{R_1} I_{nrs} \tag{40}$$

According to (40), photodetector shot noise, thermal noise generated by source resistor of M_1, resistor R_1 and drain thermal noise of M_4 directly contributes to the input equivalent noise current. Other noise sources reflect to the input with some factors. At high frequency these factorized noise sources also show frequency dependence which is not shown in here. But intuitively as the transimpedance gain response of the TIA is a low pass filter response, the frequency dependence of input equivalent noise would be a high pass response.

Chapter 5

Simulation Results

5.1 Simulation environment

The proposed TIA is designed in 65nm CMOS technology with 1.2 V supply voltage. RF NMOS and PMOS transistors are used for high frequency operation. Photodetector capacitance is emulated using 60 fF MIM capacitor, and spiral inductors are used as peaking inductors. The whole system is characterized in SPECTRE environment.

5.2 Transimpedance gain response

SPECTRE simulation of transimpedance gain response is shown in Figure 43. Transimpedance gain response is investigated in three different scenarios - when there is no compensation, compensation with degenerating capacitance and feedback network and compensation with degenerating capacitance, feedback network, and peaking inductors. It shows that without any compensation the bandwidth is 20 GHz. Incorporating degenerating capacitance and feedback network increase the bandwidth up to 33.5 GHz.

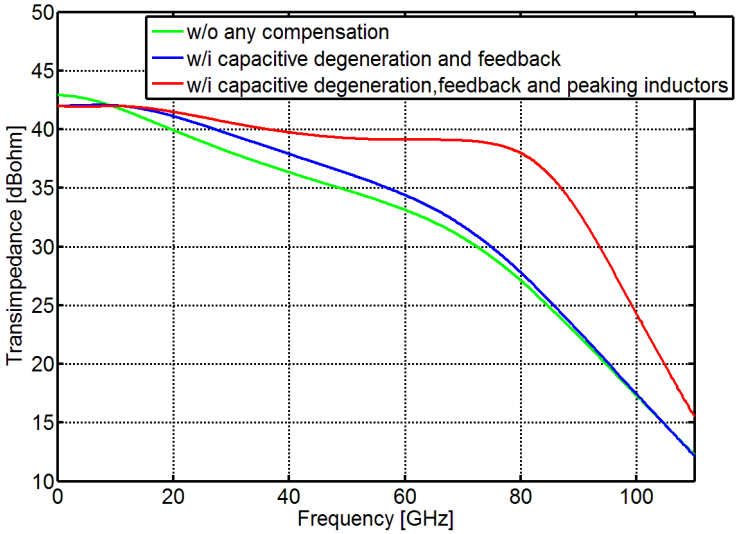


Figure 43: Transimpedance gain response of proposed TIA

Finally, with the peaking inductors bandwidth goes up to 70 GHz. So, the proposed architecture achieves 42 dBΩ of transimpedance gain with 3-dB bandwidth of 70 GHz. Compensating elements enhance the bandwidth 3.5 times the uncompensated case.

5.3 Input referred noise

Figure 44 shows the simulated input referred noise current density of the circuit without compensation and with compensation. As discussed in previous chapter, low frequency noise is white noise for both the uncompensated and compensated case. But at higher frequencies the input referred noise starts to increase because of the frequency dependent factors in the noise expression. Figure 44 also shows that at low frequencies the input referred noise is similar in both cases, but at high frequencies, especially around 3-dB point, noise performance is improved in the compensated architecture. At the 3-dB point the input referred noise for uncompensated case is 29 pA/$\sqrt{Hz}$, and for compensated architecture this value is 26 pA/$\sqrt{Hz}$. For BER of 10^{-12} this implies an electrical receiver sensitivity of -10.14 dBm and optical receiver sensitivity of -34.17 dBm, considering photodetector responsivity of 1 A/W.

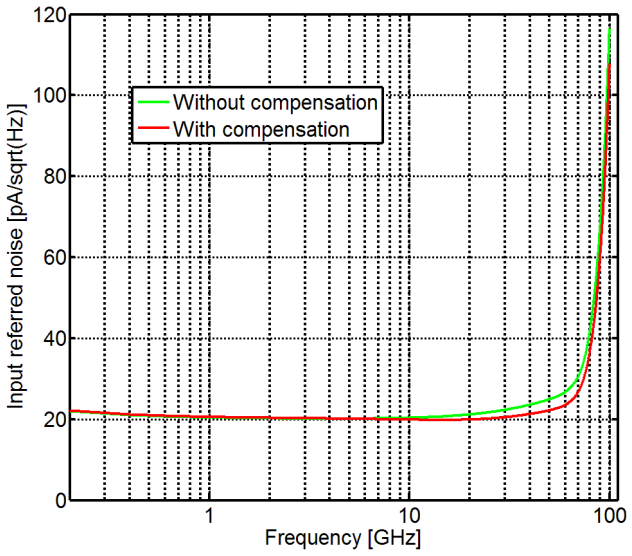


Figure 44: Simulated input referred noise

5.4 Group delay response

The group delay variation is characterized to ensure less data dependent jitter in output data eye due to phase non-linearity. The simulated group delay response as shown in Figure 45 demonstrates ± 2.8 ps of group delay variation within 3-dB bandwidth for the compensated structure. For uncompensated case this value is ± 2.7 ps. Zeros and poles of the transfer function introduce downward and upward slope in the group delay response respectively. Complex poles introduce peaking in the gain response and increase the bandwidth, but the phase response does not get improved by them. On the other hand, zeros improve the gain and phase response simultaneously. Balancing the number of zeros and poles in the architecture and proper placement of them can improve the phase response while increasing the bandwidth and that's exactly how the compensating capacitors and inductors were chosen for the design.

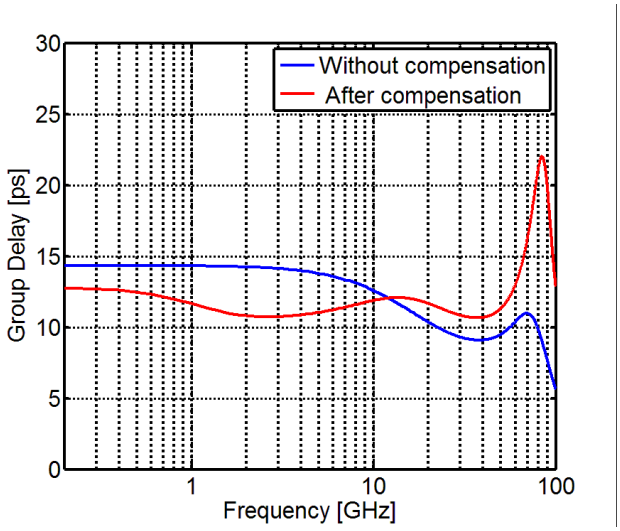


Figure 45: Group delay response

5.5 Eye diagram

Output eye diagram for 400 µA p-p input PRBS current is shown in Figure 46 . Clear eye opening is illustrated in the eye diagram with peak to peak jitter of 1.07 ps. High bandwidth and low group delay variation achieved in the design prevent vertical and horizontal closing of data eye respectively.

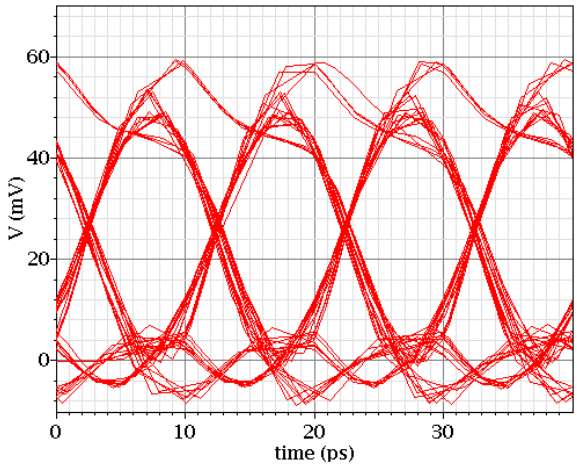


Figure 46: Output eye diagram

5.6 Performance comparison between proposed TIA and others

In this section the performance of proposed TIA is compared with other existing TIA architectures. Table 2 shows the comparison. It's not possible to make a fair comparison between different TIAs, since they are developed in different CMOS technologies. Proposed architecture also marks a sharp difference with other TIAs by data rate. Nonetheless, the comparison gives a rough idea of the effectiveness of proposed architecture in 100 Gb/s data rate. Proposed architecture achieves highest bandwidth and lowest group delay variation among all the TIA architectures in CMOS technology. Input referred noise of proposed TIA is in between all of the architectures. Power consumption is the second lowest which also provides a decent figure of merit.

Table 2: Comparison between proposed TIA with other existing TIA architectures

Paper No.	Process	Bit Rate (Gb/s)	BW (GHz)	Z_T (dBΩ)	GD (ps)	Noise (pA/$\sqrt{Hz}$)	Supply (V)	Power (mW)	Area (mm^2)	BWΩ/P_{DC} (Ω/J)
JSSC 2012 [10]	45 nm SOI	40	33	55	7.8	20.47	1.0	9	0.29	1874.5
ISCAS 2010 [9]	65 nm	40	22	46.7	13 (sim)	30 (sim)	1.2	39.9	0.044	----------
IEEE Tran. 2010 [8]	0.13 µm RF	40	29	50	16	51.8 (sim)	1.5	45.7	0.4	200.7
ISCAS 2012 [11]	65 nm	40	35	52	-----	14	1.2	168	0.825	----------
JSSC 2008 [6]	0.18 µm	40	30.5	51	125	55.7 (sim)	1.8	60.1	0.5382	180.1
JSSC 2008 [7]	90 nm	40	22	66	----	22	1.2	75	0.56	585.3
Proposed Design	65 nm	100	70	42	5.6	26	1.2	24	-----	367.19

Chapter 6

Conclusion

This work provides an overview of the existing transimpedance amplifiers in CMOS technology. A TIA with a maximum 40 Gb/s data rate has been developed to date. Their design details with pros and cons are discussed in detail. The main goal of this research is to enhance the bandwidth of TIA architecture so that it can be operated in 100 Gb/s data rate. But, trade-offs between gain, bandwidth, noise, and group delay variation introduce severe hindrances to attain optimum performance of the TIA. Different TIA architectures such as improved RGC [9], RTRN network [7], nested feedback [11] etc. are studied in detail to improve the frequency response of the TIA. Also, trade-off between gain and group delay variation through analysis are reviewed by studying a group delay optimized TIA [8].

In the proposed work, a transceiver architecture is proposed for next generation 400 Gb/s optical communication system. Currently available IEEE 802.3ba standard permits only parallel 4x25 Gb/s or 10x10 Gb/s parallel communication by wavelength division multiplexing for 100 Gb/s data rate. Inherent cross-talk between channels and high power consumption degrade the performance of transmitter and receiver. To overcome these issues, the number of parallel channels needs to be reduced. Reducing the number of channels requires higher bandwidth channels and circuitries in the network. As the first building block of the receiver, the TIA plays an important role for receiver performance; hence, a TIA in CMOS technology is designed for the next generation 100 Gb/s serial data communication

The proposed TIA is based on differential architecture with an RGC network as input and incorporating a feedback network and peaking inductors for bandwidth enhancement. Capacitive degeneration is also introduced to increase the number of zeros for better phase performance. Total system has been analyzed for transimpedance gain response and noise performance. From simulation results, the proposed architecture shows excellent performance in terms of bandwidth and group delay variation with good transimpedance gain, input referred noise, and power

consumption. The output eye diagram shows clear eye opening with low ISI and peak to peak data jitter demonstrating the feasibility of serial 100 Gb/s data handling capability.

Performance of proposed architecture encourages us to develop the remaining building blocks of the receiver such as limiting amplifier, CDR circuit, etc. Future research will be focused on the aforementioned building blocks. If fabrication is available, the receiver will be fabricated and the performance measured.

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