Fully-differential inverter-based OTA with improved composite transistors

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***Abstract*—The paper deals with fully-differential inverter-based Operational Transconductance Amplifier (OTA) designed using rectangular transistor arrays (RTA) and improved composite transistors (ICT). The two versions of the same OTA are designed and the respective performance has been shown under aggressive supply voltage scaling down to 0.3V. Post-layout simulations referring to 180 nm CMOS process technology have shown how the ICT solution with its proper body bias offer a higher voltage gain, CMRR, PSRR and a lower power consumption compared to the respective RTA version.**

***Index Terms*—CMOS inverter-based amplifiers, rectangular transistor arrays, improved composite transistors, forward-body-biasing, ultra-low-voltage, ultra-low-power**

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I. Introduction

Ultra-deep-submicron technologies support amazing performance enhancements for digital circuits but keep squeezing the available design space for analog circuits. Nonlinear output conductances, reduced voltage gains, gate-leakage mismatches, incite designers to seek alternatives [1]–[5]. In this framework, the possibility to use digital cells such as inverters to implement a traditionally analog function can enable new features in IC design. For instance, analog building blocks such as Operational Transconductance Amplifiers (OTAs) can benefit from the supply voltage scalability of digital gates. This in turn, can be translated into a dramatic reduction of the power consumption so that the IC cell can be powered by harvested source of energy.

Single-ended Inverter-based OTAs have shown these characteristics in previous works [6], [7] using improved composite transistors (ICT) [8], which is an alternative voltage-gain improvement technique to rectangular (RTA) and trapezoidal transistor arrays [9]–[11]. Single-ended OTAs are relatively small and power-efficient when compared to their fully differential counterparts. However, the latter have larger input and output voltage range for the same voltage supply and are more tolerant to common-mode and power supply interfering signals.

This work will present two versions of the same fully-differential inverter-based OTA design using the RTA and ICT techniques. Section II will discuss the CMOS inverter with improved composite transistors and how to scale their properties using transistor arrays. Section III will briefly discuss the fully-differential inverter-based OTA topology originally presented in [12], and how its performance is affected by using parallel units of the same basic inverter cell. The OTA is a variation of the circuit proposed in [13] with improved output voltage excursion. Section IV will show the post-layout simulation results for both the OTAs designs and the comparison with the ultra-low Voltage (ULV) state-of-art topologies. Finally, in Section V the conclusion will be drawn.

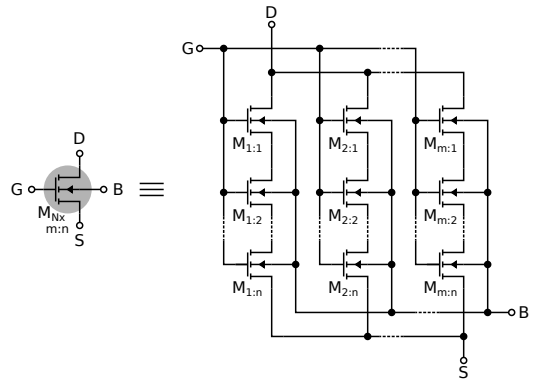


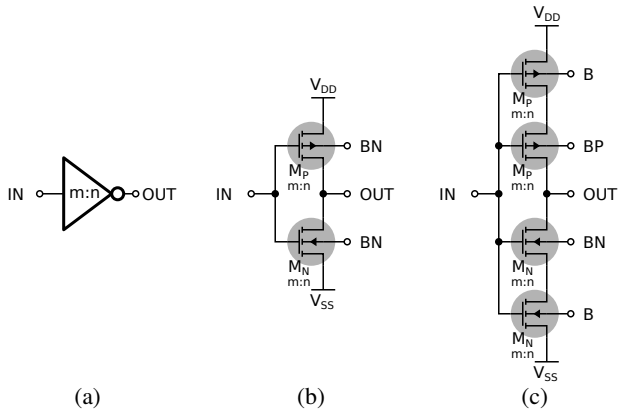
Fig. 1: Rectangular transistor array

II. CMOS inverter with improved composite transistors

Rectangular transistor arrays, such as the one shown in Fig. 1, can be modeled as a single transistor [9] with a higher output impedance [10]. The rectangular array is a m by n matrix of single transistors composed by m parallel columns of n series single transistors. Such transistors can be used to build an inverter as shown in Figure 2. In particular, Figure 2b shows a CMOS inverter in which both the NMOS (pull-down) and P-MOS (pull-up) are made by rectangular transistor arrays [10]. Notice that the designer can choose among several rectangular array by defining the m and n values to set the inverter transconductance G_m, output conductance G_o, voltage gain A_V (G_m/G_o), area and mismatch tolerance [11].

Still relying on rectangular transistor arrays, an inverter with improved composite transistors is shown in Figure 2c. Composite transistors are made of two series transistors with different aspect ratios and the same gate and bulk terminals. Each of these transistors can also be made with rectangular arrays, resulting in a trapezoidal transistor array [9], [11]. Biasing independently the transistors bulk terminals (as shown in Figure 2c), the equivalent output conductance can be made further reduced [6], [8].

Notice that such an inverter can be properly laid-out to be included in an automated digital design flow as any standard



(a) (b) (c)

Fig. 2: (a) Inverter symbol, (b) Inverter made of PMOS (pull-up) and NMOS (pull-down) rectangular transistor arrays and c) respective version with improved composite transistors.

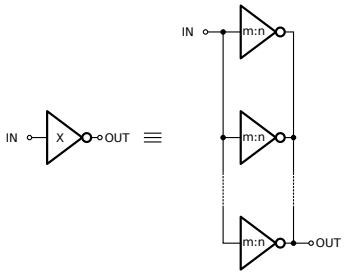


Fig. 3: Equivalent inverter with improved features.

cell. Similarly, an equivalent inverter with improved features can be made by using common-centroid layout technique to combine multiple cells in parallel with shared power supplies, input and output terminals as that in Fig. 3.

This equivalent inverter with improved features in Fig. 3 can be used as a building block of an inverter-based OTA as will be shown in the following Section. By means of a different number of basic m:n inverters in parallel, the OTA characteristics, such as transconductance, gain-bandwidth, power consumption, common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR), can be defined [11]. Then, in order to face the process variability a proper bias circuit to control the common-mode output voltage is also required [2], [11], [14].

III. Inverter-based Fully Differential Amplifier

Figure 5 shows the basic topology of the fully-differential inverter-based OTA [12] that is considering in this paper referring to the TSMC 180 nm process technology and considering inverters made by RTA inverters (as in Figure 2b) and by ICT one (as in Figure 2c) with the body bias reported in

TABLE I: OTA small-signal specs and current consumption

$A_{V_{DF}}$	$A_{V_{CM}}$	G_m	I_{DD}
$\frac{G_{mA}}{G_{oA}+G_{oC}}$	$\frac{G_{mA}}{G_{oA}+G_{oC}+G_{mC}}$	G_{mA}	$2I_{QA}+6I_{QB}$ $+2I_{QC}$

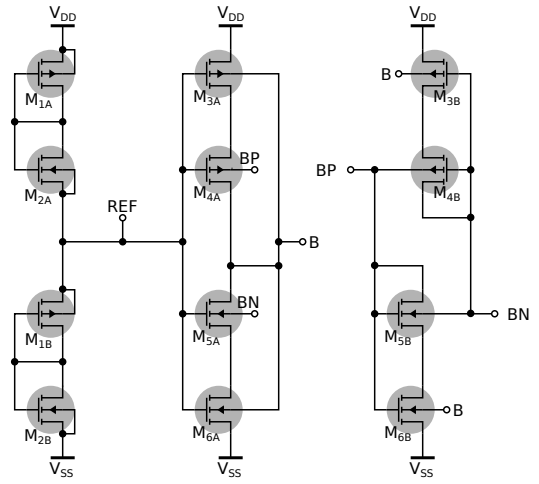


Fig. 4: Inverter with improved composite transistors and the respective body bias circuit.

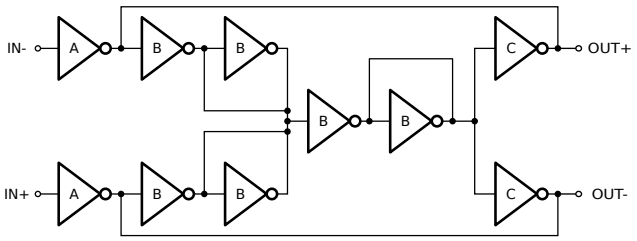


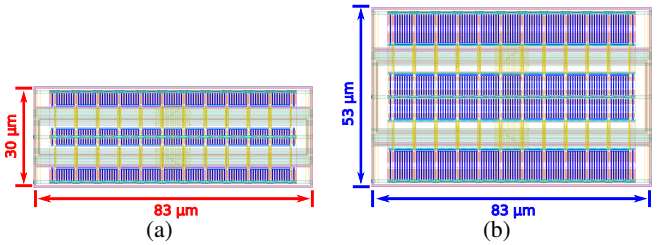
Fig. 5: Basic topology of the considered fully-differential inverter-based OTA [12].

Fig. 4. Each inverter depicted in the circuit diagrams is made of parallel inverters, such as those shown in Fig. 3. The number of parallel inverters and the transistor arrays m and n values define inverters A, B and C transconductances G_{mX}, output conductances G_{oX}, and quiescent current I_{QX}. Table I summarizes the OTA small-signal characteristics, such as differential voltage gain $A_{V_{DF}}$, common-mode voltage gain $A_{V_{CM}}$, and differential transconductance G_m, and total DC current consumption I_{DD}.

The design aims a sub-nanoWatt power consumption while operating at the minimum supply voltage of 0.3 V, room temperature for typical process parameters. Both OTAs and biasing circuits are built with 1:8 transistor arrays consisting, in turn, of single PMOS and NMOS with channel widths of 2.8 μm and 1.2 μm, respectively, and 0.18 μm channel length. All inverters are identically laid out (A=B=C) and made by connecting in parallel two basic inverters, so that, accordingly to Table I, the common-mode voltage gain is unitary and the common-centroid layout technique can be easily used. Fig. 6 shows that RTA and ICT layouts occupy an area of 2490 μm² and 4399 μm² respectively.

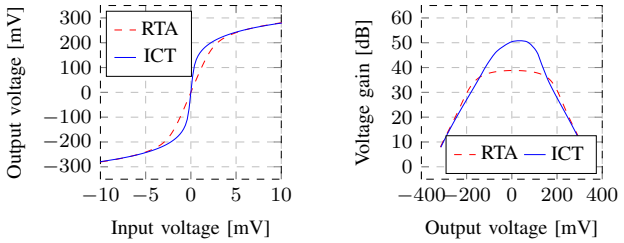
IV. Simulation Results

The post-layout simulation of the RTA and ICT solutions referring to a TSMC 180 nm process technology are reported in this Section. The input-output characteristics and the output



(a) (b)

Fig. 6: Layout of the OTA with (a) Rectangular transistor arrays and (b) with its improved composite transistors version



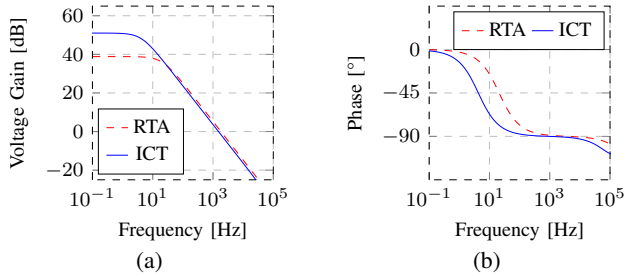
(a) (b)

Fig. 7: OTA DC differential characteristic curves at V_{DD} = 0.4 V: (a) output voltage versus input voltage, and (b) voltage gain versus output voltage

voltage gain versus the differential output voltage for a 0.4 V supply voltage are reported respectively in Fig. 7a e Fig. 7b. The ICT version shows a higher maximum voltage gain, but for a differential output signal amplitudes smaller than 150 mV. This happens because the voltage gain techniques are constrained by the transistors saturation voltage.

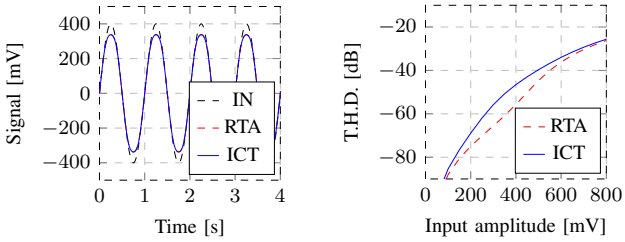
Fig. 8 shows the open-loop differential voltage gain and phase AC simulation results for a 10 pF capacitive load. The RTA (ICT) version has a 39 dB (52 dB) DC voltage gain, a 1.815 Hz (1.517 Hz) GBW and 24.1 nA (20.6 nA) I_{DD}. This translates into a Figure of Merit (FoM = $100 \cdot \text{GBW} \cdot C_L/I_{DD}$) of $74V^{-1}$ for both the OTA versions. Being single-stage OTAs, their phase margin is 90°. As their common-mode voltage gain is unitary, the RTA (ICT) OTA has a 39 dB (52 dB) CMRR. On the basis of their biasing circuit, their common-mode output voltage outputs is $V_{DD}/2$ resulting in a PSRR for the RTA (ICT) OTA of 43 dB (58 dB).

Fig. 9a shows the transient response for a unity gain buffer resistive feedback testbench [2] and a 800 mV peak-to-peak



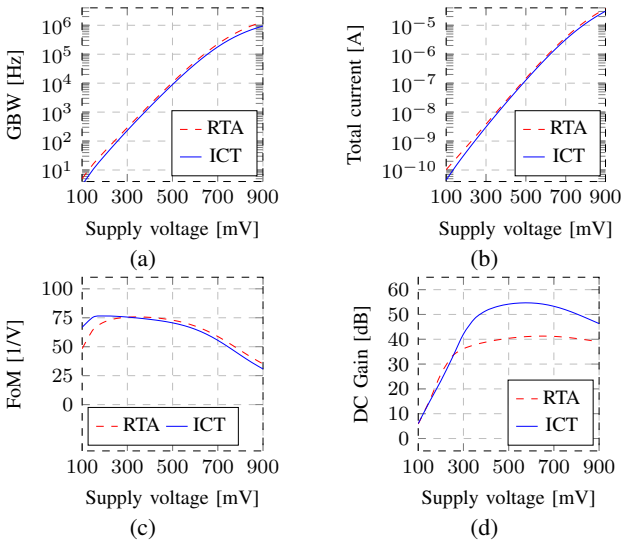
(a) (b)

Fig. 8: OTA small-signal output response at V_{DD} = 0.4 V: (a) voltage gain and (b) phase



(a) (b)

Fig. 9: OTA buffer transient response at V_{DD} = 0.4 V: (a) transient voltages, (b) Total Harmonic Distortion



(a) (b) (c) (d)

Fig. 10: OTA small-signal response versus supply voltage: (a) GBW, (b) total current, (c) FoM, and (d) voltage gain

differential input signal at 0.4 V V_{DD}. Both the OTAs have nearly identical output signals. Fig. 9b shows the Total Harmonic Distortion (THD) versus the differential input-voltage amplitude for both OTAs. As the RTA version has a slightly larger output range (see Fig. 7b), its shows also less distortion.

The biasing circuit does not tune the OTAs transconductance, as other advanced biasing circuits [11], [14], so it varies with the process, supply voltage and temperature. Figure 10 show the GBW, total current (I_{DD}), the Figure of Merit (FoM) and the DC gain versus the supply voltage V_{DD}. Both the GBW (Fig. 10a) and the current consumption (Fig. 10b) grow exponentially with V_{DD}, while transistors operate in weak inversion, so the FoM (Fig. 10c) is above 60 V^{-1} for supply voltages up to 0.6 V. At higher V_{DD}, the FoM sharply declines, as the transistors begin operating in strong inversion. Fig. 10d shows how the voltage gain grows exponentially with supply voltage up to 0.3 V for both of OTA versions. Then it is constrained by the transistors saturation voltage. Anyhow, the ICT version reaches 52 dB at 0.4 V and peaks at 55 dB for 0.6 V. Notice, the possibility to operate into a wide supply voltage range down to 0.3V given by the use of an inverter as basic building block of the OTAs.

Table II summarizes the RTA and ICT OTAs Montecarlo

TABLE II: Monte Carlo simulation results (V_{DD}=0.4V)

	V_{os} [mV]		V_{CM} [mV]		A_V [dB]		GBW [kHz]	
	μ	σ	μ	σ	μ	σ	μ	σ
RTA	0.00	1.98	200.0	2.3	38.9	0.7	1.94	0.73
ICT	0.02	1.63	200.0	2.2	51.3	0.7	1.60	0.61

TABLE III: Performance Comparison

	[10]+	[12]*	[7]*	This work*		Unit
Technology	130	180	180	180	180	nm
Die Area	52000	800	1026	2490	4399	µm²
Mode	FD	FD	SE	FD	FD	-
Technique	RTA	-	ICT	RTA	ICT	-
VDD	0.25	0.3	0.3	0.4	0.4	V
Power	55	10.5	0.27	9.64	8.24	nW
A_V	25	23	54	39	52	dB
CMRR	43	-	54	39	52	dB
PSRR	47	-	54	45	58	dB
V_{os}	0.8	-	8.7	5.9	4.9	mV
T.H.D.	-60	-	-40	-39	-40	dB
@ V_{IN}[1]	19	-	120	550	500	mV
GBW	7.23	8.0	0.21	1.82	1.52	kHz
Phase Margin	90	86	90	90	90	°
C_L	30	10	10	10	10	pF
FoM	143	229	229	74	74	V^{-1}

+ Measured, * Simulated, FD: Fully-Differential, SE: Single-Ended, RTA: Rectangular Transistor Arrays, ICT: Improved Composite Transistors. [1] V_{IN}: differential input peak-to-peak voltage for the measured THD.

simulation results on 1000 runs at 0.4 V V_{DD} considering both global and local process variability. The RTA (ICT) version has 5.4 mV (4.9 mV) offset voltage, considering a 3 σ maximum deviation. The common-mode output voltage V_{CM} standard deviation σ both for the RTA and ICT versions are minimal as the biasing circuit properly corrects global process variability, so the average value μ is close to $V_{DD}/2$. However, the biasing circuit does not correct GBW process variability, so it has a large σ/μ ratio. Additionally, the DC voltage gain A_V is not significantly affected for both the OTAs.

Table III compares the RTA and ICT performance also with the state-of-art ultra-low-voltage single-stage inverter-based OTAs. The OTA presented in [10], a ULV version of the OTA proposed in [13], uses rectangular transistor arrays to decrease process variability. Its voltage gain is low because its limited by the transistors saturation voltage, as a direct result of the low supply voltage, as shown in Fig. 10d. Notice that the former OTA presented in [12] with the same basic topology explored in this paper, has a low voltage gain since it uses minimum channel length transistors and only parallel transistor arrays and a higher FoM.

The most remarkable characteristic of the proposed solutions is the THD. The voltage gain is still comparable to those of their single-ended version, proposed in [7], but has a much better output voltage excursion, as result of its fully-differential design. A better FoM could be achieved by using different number of parallel units and m and n values Additionally, the designs presented in [10], [12] do not have any biasing circuitry to correct global process variability and the biasing circuit power consumption is used in this work to compute this FoM.

V. Conclusion

Although single-ended amplifiers are more power and area efficient than their fully-differential counterparts, these latter ones have an intrinsically larger voltage swing. Thus, the design of fully-differential inverter-based OTAs using RTA and ICT have been shown and their performance have been compared. As the building block of the presented OTAs is an inverter, the solutions can offer a supply voltage scalability being able to operate down to 0.3V with an overall power consumption down to nanoWatt. Post-layout simulations performed referring to 180 nm CMOS process technology, have shown how the ICT solution improves the voltage gain (by 12dB for a supply voltage of 0.4 V), the CMRR (by 13dB) and the PSRR (by 13dB) while the power consumption is slightly reduced.

Acknowledgment

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