Design and Simulation of a 180nm CMOS Single-Stage Differential Pair

Chirag Chiranjeevi
Department of Electronics and Communication Engineering
Manipal Institute of Technology, Manipal
chirag.1840@gmail.com

***Abstract*—This paper presents the design, simulation, and DC analysis of a single-stage CMOS operational amplifier featuring a complementary rail-to-rail input stage and a PMOS active load. The circuit was implemented and simulated using 180nm CMOS technology models in eSim. The chosen topology is designed to achieve a wide input common-mode range. A DC sweep analysis was performed to characterize the amplifier's transfer curve in a unity-gain feedback configuration. The simulation results are used to analyze the amplifier's DC operating characteristics and linear voltage range.**

I. CIRCUIT DETAILS

The circuit diagram is shown in the figure below. For simplicity, the size of all transistors has been set as L=0.18µm, W=100µm. The Bias current is set by the resistor R_B for the current mirror M_5 and M_6 and for the other transistors as well. For the differential input voltage, a reasonable bias value would be 0 V, and the offset voltage V_{off} is also 0 V since the circuit has been designed to be fully symmetric and the transistors are designed to match perfectly.

The amplifier's performance was evaluated under a static DC input condition, with the non-inverting and inverting terminals set to 1.00 V and 0.99 V respectively. This corresponds to a differential input voltage of 10 mV and a common-mode input voltage of 0.995 V. The DC value for differential input voltage and the offset voltage have both been set to 0 V because the design is perfectly symmetrical, so there is no systematic offset. With V_{off} set to 0, the feedback ensures that the voltage difference between the inverting and the non inverting input is equal to the offset voltage of the differential stage

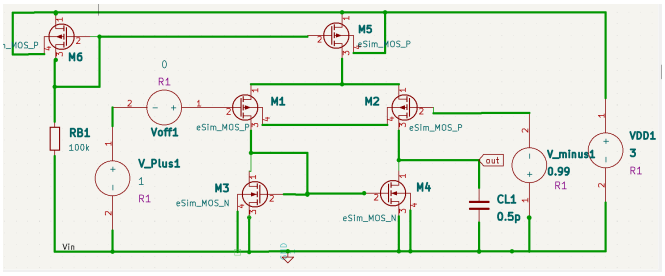

Fig. 1. Circuit Diagram

The waveforms of the expected outputs have been shown further in the paper

II. OUTPUT WAVEFORM

The DC transfer characteristic of the amplifier was analyzed by performing a DC sweep on the non-inverting input voltage source, V_Plus1. The resulting output voltage is plotted against the input voltage sweep as shown in Fig. 2.

The plot's x-axis represents the input voltage sweep from -100 mV to +100 mV around the central DC bias point, while the y-axis shows the corresponding output voltage. The output swings linearly from approximately 0.70 V to 0.82 V in response to this input change. This result demonstrates the expected behavior of the amplifier in its unity-gain feedback configuration, where the output voltage closely follows the inpu

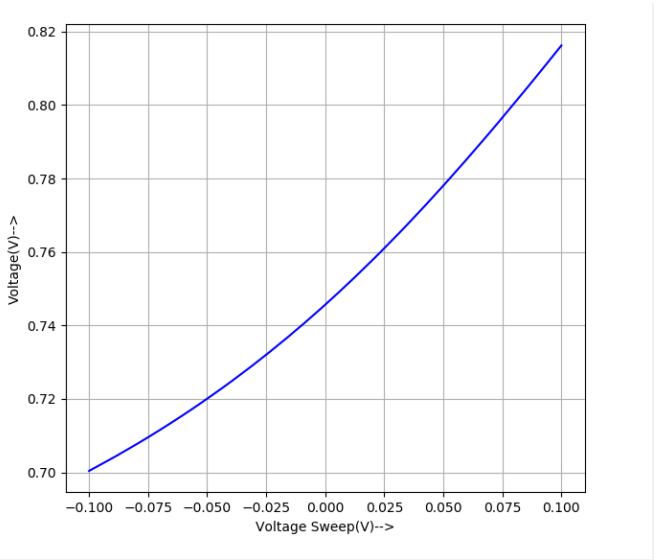

Fig. 2. Plot of output voltage versus differential input voltage for a common mode input voltage of 1V

REFERENCES

[1] CMOS Integrated Circuit Simulation with LTSpice IV - a Tutorial Guide, 1st ed. 2015 Erik Brun