Electronic Circuits & Communication Fundamentals

Statistical Analysis

Chapter No.	Dec. 13	May 14	Dec. 14	May 15	Dec. 15	May 16
Chapter 1	20 Marks	25 Marks	25 Marks	30 Marks	30 Marks	25 Marks
Chapter 2	20 Marks	15 Marks	20 Marks	15 Marks	20 Marks	15 Marks
Chapter 3	05 Marks	10 Marks	-	-	-	15 Marks
Chapter 4	25 Marks	25 Marks	25 Marks	20 Marks	30 Marks	35 Marks
Chapter 5	20 Marks	10 Marks	15 Marks	20 Marks	30 Marks	10 Marks
Chapter 6	10 Marks	10 Marks	10 Marks	10 Marks	05 Marks	05 Marks
Chapter 7	05 Marks	10 Marks	10 Marks	05 Marks	-	-
Chapter 8	10 Marks	15 Marks	10 Marks	10 Marks	10 Marks	05 Marks
Appendix A	-	-	-	10 Marks	-	05 Marks
Repeated Questions	-	15 Marks	14 Marks	15 Marks	35 Marks	60 Marks

Dec. 2013

Chapter 1 : Electronic Circuits [Total Marks : 20]

Q. 1(a) What do you understand by "pinch off" voltage and "cut off" voltage as applied to FET ? **(5 Marks)**

Ans. :

Pinch-off voltage (V_P) :

The "pinch-off" voltage is the value of V_{DS}, at which the drain current reaches its constant saturation value. Any further increase in V_{DS} does not have any effect on the value of I_D. Do not make a confusion between the cut-off and pinch-off. The pinch-off voltage is denoted by V_P.

Cut-off voltage $V_{GS\,(off)}$:

The value of V_{GS} that makes the drain current I_D approximately equal to zero is called as cut-off voltage and it is denoted by $V_{GS\,(off)}$. A JFET must be operated between $V_{GS} = 0$ and $V_{GS\,(off)}$. For this range I_D will change between I_{DSS} and 0 respectively.

Q. 2(a) Determine V_{GSQ}, I_{DQ} and V_{DSQ} and A_V for a voltage divider circuit with $V_{DD} = 18$ V, $R_D = 2.2$ k, $R_1 = 2.1$ M, $R_2 = 330$ k and $R_S = 1.2$ k, $I_{DSS} = 10$ mA, $V_P = -8$ V and $V_{DS} = 40$ µS. **(10 Marks)**

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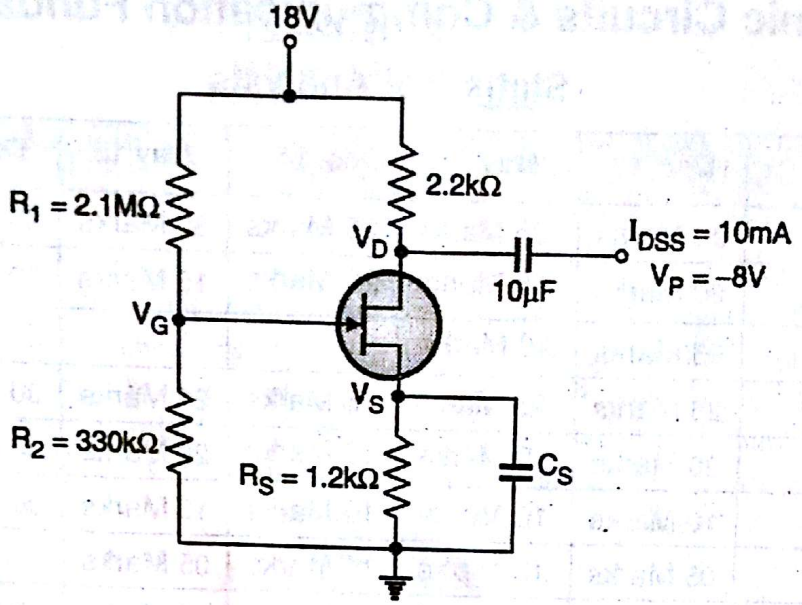
Ans. :



(F-4327) **Fig. 1**

Step 1 : Find expression for V_{GS} :

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{330}{(2100 + 330)} \times 18$$

$$\therefore \quad V_G = 2.45 \text{ Volts} \qquad ...(1)$$

$$V_S = R_S I_D = 1.2 I_D \qquad ...(2)$$

$$\therefore \quad V_{GSQ} = V_G - V_S = (2.45 - 1.2 I_D) \qquad ...(3)$$

Step 2 : Find I_D :

$$I_D = I_{DSS}\left[1 - \frac{V_{GSQ}}{V_P}\right]^2$$

$$\therefore \quad I_D = 10\left[1 + \frac{(2.45 - 1.2 I_D)}{8}\right]^2$$

$$\therefore \quad I_D = \frac{10}{64}[8 + (2.45 - 1.2 I_D)]^2$$

$$6.4 I_D = [10.45 - 1.2 I_D]^2$$

$$6.4 I_D = 109.20 - 25.08 I_D + 1.44 I_D^2$$

$$\therefore \quad 31.48 I_D = 109.20 + 1.44 I_D^2$$

$$\therefore \quad 1.44 I_D^2 - 31.48 I_D + 109.20 = 0$$

$$\therefore \quad I_D = \frac{31.48 \pm \sqrt{(31.48)^2 - (4 \times 1.44 \times 109.20)}}{2 \times 1.44}$$

$$I_D = 17.53 \text{ mA or } 4.32 \text{ mA}$$

For $I_D = 17.53$ A, V_{DS} would be negative, so discard this value and select,

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$$I_{DQ} = 4.32 \text{ A}$$ **Ans.**

Step 3 : Find V_{GSQ} :

From Equation (3), $V_{GSQ} = 2.45 - 1.2\, I_{DQ} = 2.45 - (1.2 \times 4.32)$

$$\therefore \quad V_{GSQ} = -2.734 \text{ V}$$ **...Ans.**

Step 4 : Find V_{DSQ} :

$$V_{DSQ} = V_{DD} - I_{DQ}\,(R_D + R_S)$$

$$\therefore \quad V_{DSQ} = 18 - 4.32\,(2.2 + 1.2)$$

$$\therefore \quad V_{DSQ} = 3.312 \text{ V}$$ **...Ans.**

Step 5 : Find A_V :

$$A_V = -g_m R_D \qquad \text{...(4)}$$

Where, $g_m = g_{mo}\left[1 - \dfrac{V_{GS}}{V_P}\right]$

and $g_{mo} = \left|\dfrac{2\, I_{DSS}}{V_P}\right| = \dfrac{2 \times 10 \text{ mA}}{8} = 2.5 \text{ mS}$

$$\therefore \quad g_m = 2.5 \text{ mS}\left[1 - \left[\frac{-2.734}{-8}\right]\right]$$

$$\therefore \quad g_m = 1.64 \text{ mS}$$

$\therefore$ From Equation (4), $A_V = -1.64 \times 2.2 = -3.608$

$$\therefore \quad A_V = -3.608$$

Q. 3(c) Explain why crystal oscillators are considered to be more stable than other oscillators ?

(5 Marks)

Ans. :

In a crystal oscillator, the frequency of oscillations depends on the physical dimensions of the crystal. As the dimensions remain constant the crystal oscillator frequency remains constant.

Principle of crystal oscillators :

Certain materials such as quartz exhibit a unique property called "piezo electric" property. It states that if mechanical force is applied to a quartz crystal then it generates electric potential. Also if electric field is applied to a crystal it vibrates mechanically. If we apply mechanical vibrations to a quartz crystal then under proper operating conditions we can obtain electrical oscillations from it.

Frequency stability :

The biggest advantage of using a crystal oscillator is its high frequency stability. The frequency of a crystal oscillator remains stable inspite of changes in temperature, voltage, humidity or other parameters.

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Q. 3(d) Compare different biasing circuits with respect to Q-point. Comment on which biasing circuit is better in stability. **(5 Marks)**

Ans. :

Sr. No.	Parameter	Fixed bias	Self bias	Voltage divider bias
1.	Number of dc power supplies	Two	One	One
2.	Expression for V_{GS}	$V_{GS} = -V_{GG}$	$V_{GS} = -I_D R_S$	$V_{GS} = V_G - I_D R_S$
3.	Source resistance	Absent	Present	Present
4.	Negative feedback	Absent	Present	Present
5.	Bias stabilization	Can not be provided	Better than fixed bias	Better than self bias.

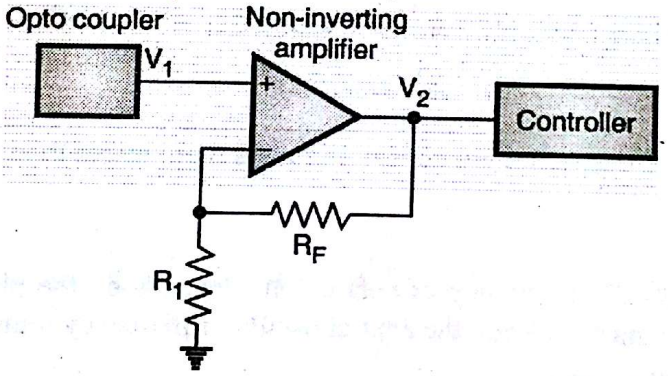
Chapter 2 : Operational Amplifier & its Application [Total Marks : 20]

Q. 1(d) Optical sensor of a package counting system create 1.5 V DC signal when it detects the seal. This voltage need to be amplified and sent to a controller with an input resistance of 5 kΩ. Draw block diagram for the system. Choose correct amplifier to drive this low resistance load and select the resistor values to set the gain. The input voltage range for the controller is +10 V to +30 V DC. **(5 Marks)**

Ans. :

Step 1 : Draw the block diagram of the system :

The block diagram of the desired system is as shown in Fig. 2.



(F-4326) **Fig. 2 : System block diagram**

Step 2 : Calculate R_1 and R_F :

The amplifier selected is non-inverting amplifier. The input V_1 to this amplifier is + 1.5 V from the opto-coupler output and its output V_2 should be in the range + 10 V to + 30 V.

Let $V_2 = 12$ V

Gain $A_V = \frac{V_2}{V_1} = \frac{12}{1.5} = 8$

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But $A_V = 1 + \frac{R_F}{R_1}$

$\therefore \quad 1 + \frac{R_F}{R_1} = 8$

Let $R_1 = 10\ k\Omega$ ...Ans.

$\therefore \quad R_F = 7\ R_1 = 70\ k\Omega$ ...Ans.

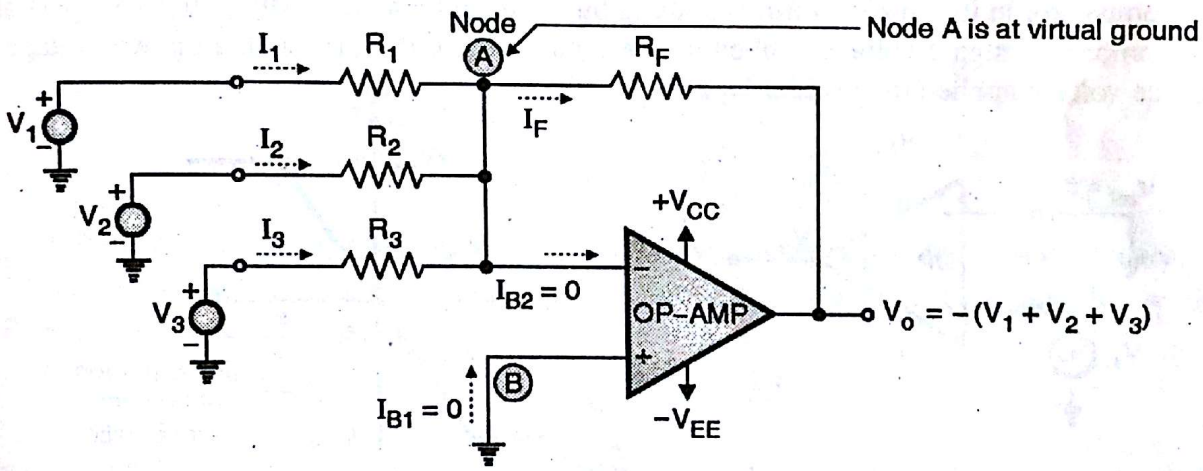
Q. 2(b) Explain how op-amp can be used as a summing, scaling and averaging amplifier in the inverting configuration ? **(10 Marks)**

Ans. :

OP-AMP as Summering amplifier :

Inverting Adder or Inverting Summing Amplifier :

The "inverting summing amplifier" configuration with three inputs V_1, V_2 and V_3. Depending on the relation between the feedback resistor R_F and the three input resistances R_1, R_2 and R_3, the same circuit can be used as either a summing amplifier, scaling amplifier or averaging amplifier. V_1, V_2 and V_3 are three input signals applied simultaneously to the inverting terminal of the OP-AMP through resistors R_1, R_2 and R_3 respectively. V_1, V_2 and V_3 are measured with respect to ground. R_F is the feedback resistor. So the configuration of Fig. 3 is basically an inverting amplifier with three inputs.



(B-355) **Fig. 3 : An inverting adder**

Let the currents through the resistors R_1, R_2 and R_3 be I_1, I_2 and I_3 respectively.

Expression for the output voltage :

Apply KCL at node A of Fig. 3 to write,

$$I_1 + I_2 + I_3 = I_{B2} + I_F \quad ...(1)$$

But as R_i of the OP-AMP is ideally infinite, $I_{B2} = 0$. And $V_A = V_B = 0$ due to virtual ground concept.

$$\text{Hence,} \quad I_1 + I_2 + I_3 = I_F \quad ...(2)$$

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From the input side, $$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1} \text{ as } V_A = 0 \quad ...(3)$$

Similarly, $$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2} \text{ and } I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3}{R_3} \quad ...(4)$$

And from the output side,

$$I_F = \frac{V_A - V_o}{R_F} = -\frac{V_o}{R_F} \quad ...(5)$$

Substituting these values in Equation (2) we get,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_F}$$

$$V_o = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right]$$

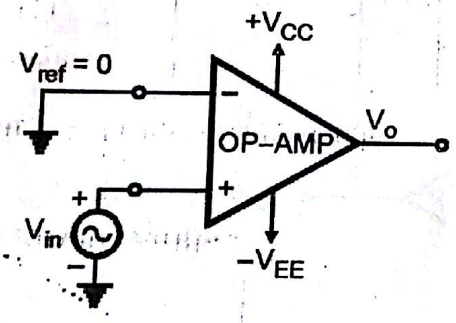
In Equation (2) if we substitute $R_F = R_1 = R_2 = R_3 = R$ then we get,

$$V_o = -(V_1 + V_2 + V_3) \quad ...(7)$$

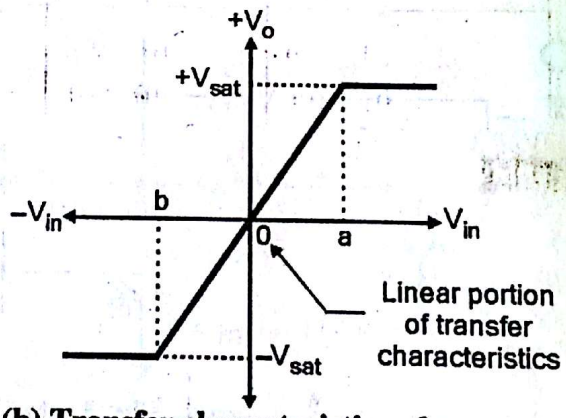
Thus output voltage is the negative sum of the input voltage. Therefore this circuit is called as "Inverting adder" or "Inverting summing amplifier".

OP-AMP as a comparator :

A comparator in its simplest form is nothing but an open loop OP-AMP, with two inputs and one output. It compares a signal voltage applied to one input of the OP-AMP, with a known voltage called the reference voltage applied to the other input.



(a) A basic comparator circuit



(b) Transfer characteristics of a comparator

Fig. 4

The output of a comparator is either positive or negative saturation voltage ($\pm V_{(sat)}$), depending on which input is larger. Fig. 4(a) shows a non-inverting comparator.

This is called as non-inverting comparator because the signal voltage V_{in} is applied to the non-inverting (+) terminal of the OP-AMP. The inverting (–) terminal is connected to ground. So the reference voltage here is $V_{ref} = 0V$. As no feedback is being used, the OP-AMP operates in the open loop mode with a large open loop gain A_V.

For scaling and averaging amplifier :

(i) Scaling amplifier :

Circuit shown in Fig. 5 can be used as a scaling amplifier. This is possible if each input voltage is amplified by a different factor. This can be done if resistors R_1, R_2 and R_3 are different in value.

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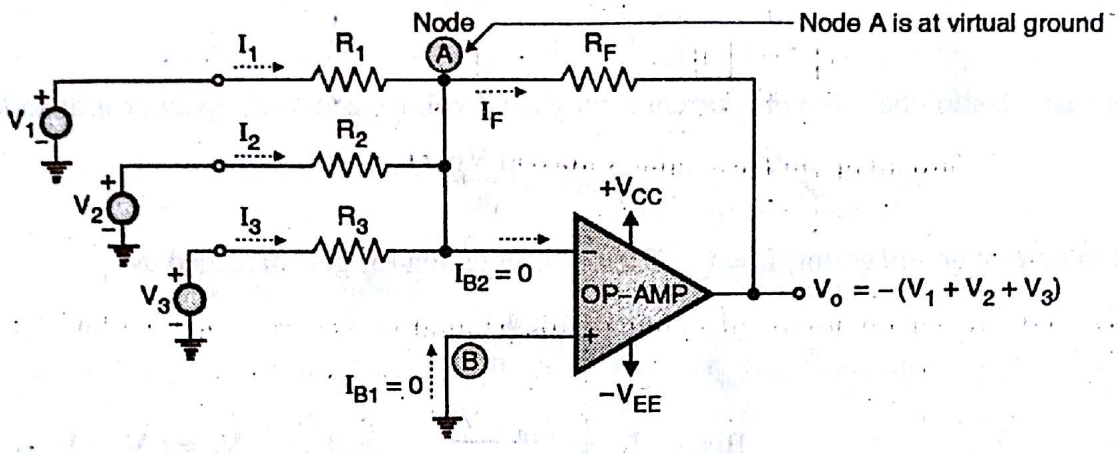
$$V_o = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right] \quad ...(1)$$

Where $R_1 \neq R_2 \neq R_3$

Thus it is possible to "scale" each of the input terminals as per our requirements.



(B-355) **Fig. 5 : An inverting adder**

(iii) Averaging amplifier :

The inverting adder circuit of Fig. 5 can be used as an averaging circuit by setting $R_1 = R_2 = R_3 = R$ and $R_F = \frac{R}{3}$

Substitute these values into Equation (1) to get,

$$V_o = \frac{-R_F}{R}(V_1 + V_2 + V_3) = \frac{-R/3}{R}(V_1 + V_2 + V_3)$$

$$\therefore \quad V_o = \frac{-(V_1 + V_2 + V_3)}{3} \quad ...(2)$$

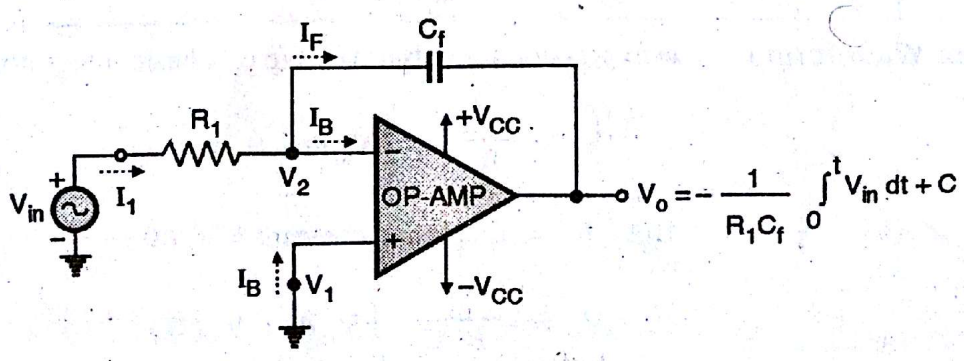
Thus the magnitude of output voltage is equal to the average of the three input voltages.

This principle can be extended for n number of inputs by setting $R_F = R/n$ and $R_1 = R_2 = ... = R_n = R$. Then the output voltage is given by,

$$V_o = \frac{-(V_1 + V_2 + V_3 + ... V_n)}{n}$$

Q. 3(a) Sketch an op-amp integrating circuit together with the circuit waveforms. Explain in brief the circuit operation. **(5 Marks)**

Ans. : The ideal integrator circuit is as shown in Fig. 6. This circuit is obtained by replacing the feedback resistor R_F in the inverting amplifier configuration by "C_F".



(N-77) **Fig. 6 : An ideal integrator circuit**

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Expression for the output voltage :

Referring to the Fig. 6, apply the Kirchhoff's current law at node V_2 to write,

$$I_1 = I_B + I_F \quad ...(1)$$

Due to high input impedance R_i of the OP-AMP, I_B will be negligible as compared to I_F.

$$\therefore \quad I_1 \approx I_F \quad ...(2)$$

The basic relation between the current through and voltage across a capacitor is as follows :

$$I_1 = C \cdot \frac{d V_c}{dt} \quad ...(3)$$

But in case of an integrator, $I_F = I_{CF}$. Therefore Equation (3) gets modified as:

$$I_1 = C_F \frac{d V_c}{dt} \quad ...(4)$$

$$\text{But,} \quad I_1 = \frac{V_{in} - V_2}{R_1} \quad \text{and} \quad V_C = (V_2 - V_o).$$

Substituting these values into Equation (4) we get,

$$\frac{V_{in} - V_2}{R_1} = C_F \frac{d}{dt} (V_2 - V_o). \quad ...(5)$$

Using the concept of "virtual ground" we can write that,

$$V_1 = V_2 = 0 \quad ...(6)$$

Substituting this value into Equation (4) we get,

$$\frac{V_{in}}{R_1} = C_F \frac{d}{dt} (-V_o) \quad ...(7)$$

The output voltage can be obtained by integrating the above equation as :

$$V_o = -\frac{1}{R_1 C_F} \int_0^t V_{in}\, dt + C \quad ...(8)$$

where C is the integration constant and it is proportional to the output voltage V_o at $t = 0$ seconds.

Conclusion :

Equation (8) indicates that the output voltage is negative integration of the input voltage. The negative sign is introduced due to the fact that the basic configuration used is an inverting amplifier. This circuit is therefore called as an inverting integrator.

Input and Output Waveforms : The expression for output voltage of a basic integrator is given by,

$$V_o = \frac{1}{R_1 C_F} \int_0^t V_{in}\, dt + K \quad ...(9)$$

$$\text{But} \quad K = \text{Integration constant} = V_o(0)$$

$$\therefore \quad V_o = -\frac{1}{R_1 C_F} \int_0^t V_{in}\, dt + V_o(0) \quad ...(10)$$

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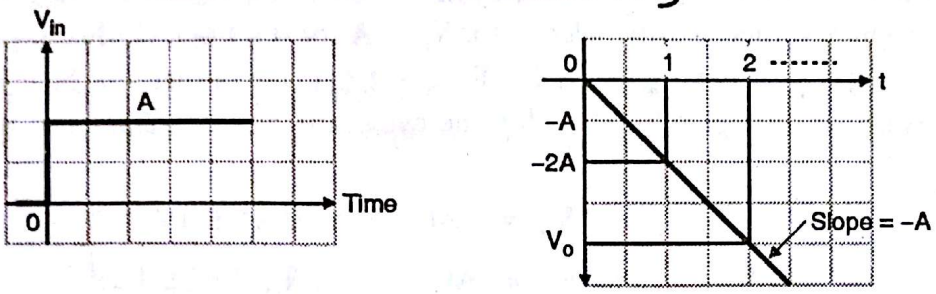
Output for a step input : Let us obtain the output voltage for a step input voltage of amplitude A as shown in Fig. 7(a). This voltage is denoted mathematically as follows :

$$\left.\begin{aligned} V_{in} &= A \quad \text{... for } t \geq 0 \\ \text{and} \quad &= 0 \quad \text{... for } t < 0 \end{aligned}\right\} \qquad ...(11)$$



(a) Step input voltage **(b) Output voltage**

(N-78) **Fig. 7**

Assume that $R_1 C_F = 1$ and substitute the expression of V_{in} into Equation (10) to write,

$$\text{Output voltage} \quad V_o = -1 \int_0^t V_{in}\, dt + V_o(0) \qquad ...(12)$$

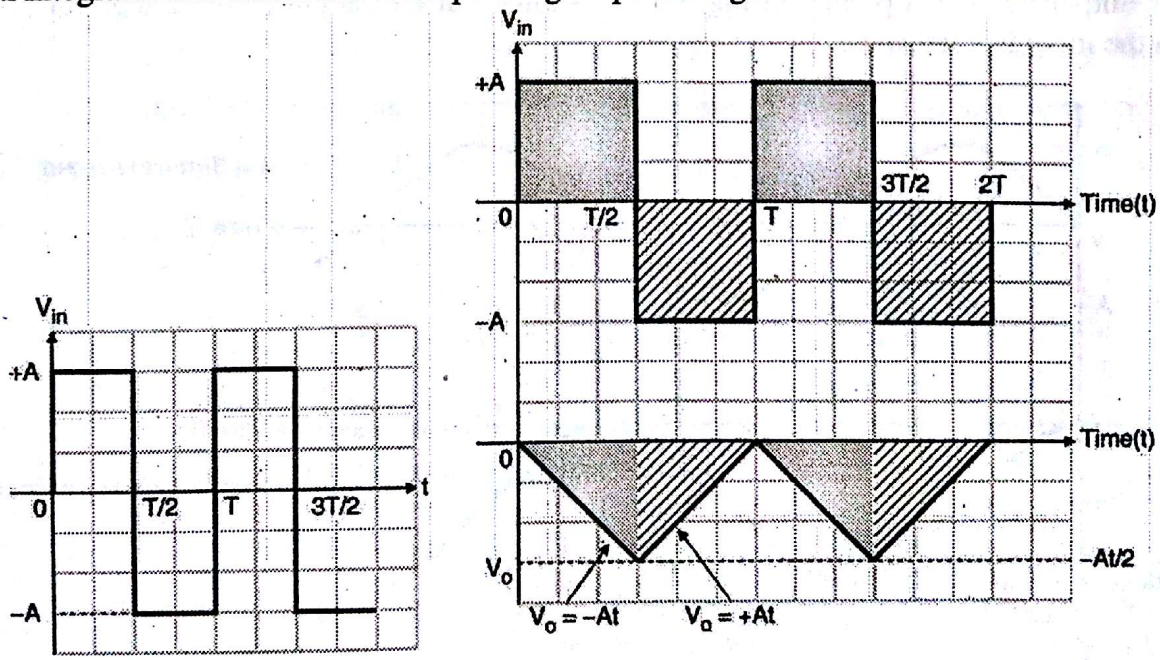
Assume that the initial value of the output voltage $V_o(0)$ is equal to zero.

$$V_o = -1 \int_0^t A\, dt$$

$$V_o = -At \quad (\text{for } t \geq 0) \qquad ...(13)$$

This is the equation of a straight line with a slope equal to – A and zero Y intercept (passing through the origin). Hence the output voltage is as shown in Fig. 7(b). It shows that the output changes linearly with time.

Output for a square wave input : Let us now apply the square wave shown in Fig. 8(a) at the input of an ideal integrator and obtain the corresponding output voltage.



(a) Square wave input **(b) Input output voltage waveform for a square wave input**

(N-79) **Fig. 8**

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The square wave input is mathematically represented as follows:

$$\left.\begin{aligned} V_{in} &= A \quad \text{... for } 0 \le t \le T/2 \\ \text{and} \quad &= -A \quad \text{... for } T/2 < t \le T \end{aligned}\right\} \quad ...(14)$$

This expression is valid only for the first cycle. This expression shows that the square wave is made of many step signals shifted in time. Hence for $V_{in} = A$ for $0 \le t \le T/2$ the output voltage will be a straight line with a slope – A. For $V_{in} = -A$ for $T/2 < t < T$, the output will be again a straight line with a slope of A as shown in Fig. 8(b). Thus for one cycle, the output voltage can be mathematically expressed as :

$$\left.\begin{aligned} V_o &= -At \quad \text{... } 0 \le t \le T/2 \\ \text{and} \quad &= At \quad \text{... } T/2 < t \le T \end{aligned}\right\} \quad ...(15)$$

with $R_1 C_F = 1$.

This is plotted as shown in Fig. 8(b).

Output for a sine wave input :

Here the sinewave input with a peak voltage of A Volts and frequency of f Hz is used. It is as shown in Fig. 9(a) and mathematically represented by,

$$V_{in} = A \sin(2\pi ft) \quad ...(16)$$

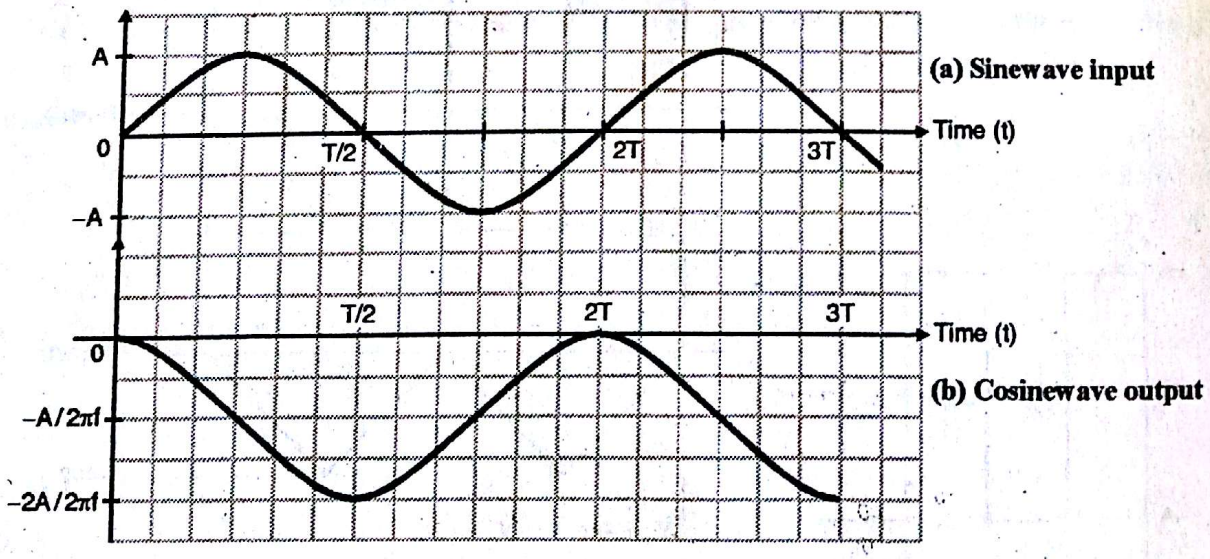
where $f = \frac{1}{T}$ and T = One cycle period.

Assuming the value of $R_1 C_F = 1$, the output voltage is given by,

$$V_o = -1 \int_0^t A \sin(2\pi ft)\, dt = -A \times -\frac{\cos(2\pi ft)}{2\pi f}$$

$$= \frac{-A}{2\pi f}[-\cos(2\pi ft)] \quad ...(17)$$

This output voltage is plotted in Fig. 9(b). It shows that the output of the integrator is a cosine wave when the input is a sinewave.



(N-80) **Fig. 9 : Input and output voltage waveforms for a sinewave input**

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Chapter 3 : Phase Locked Loop (PLL) [Total Marks : 05]

Q. 1(b) With neat block diagram explain how PLL can be used to generate large number of frequencies from a single reference frequency. **(5 Marks)**

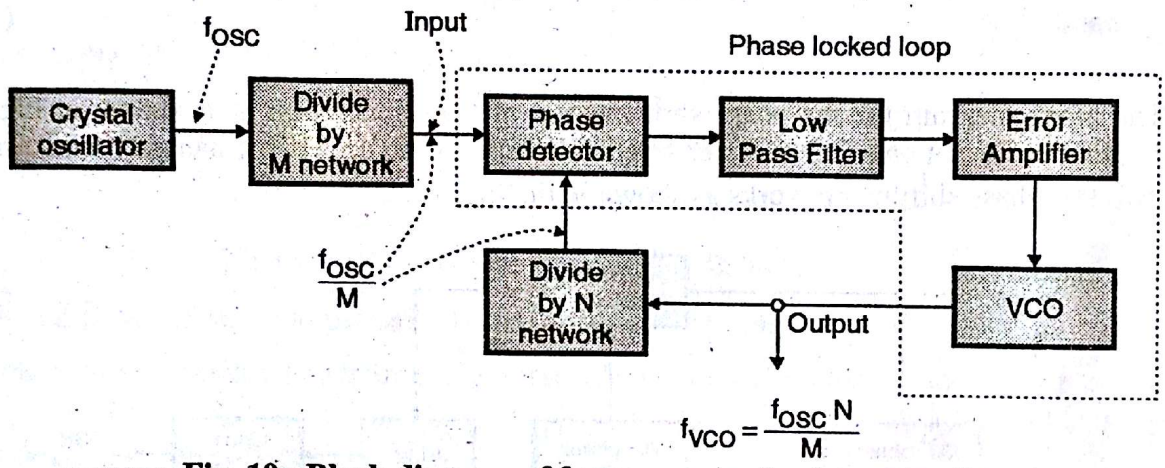
Ans. :

PLL as Frequency Synthesizer :

The block diagram of PLL as frequency synthesizer is as shown in Fig. 10. Note that this circuit is same as the frequency multiplier circuit except for the divide by M network added as shown in Fig. 10.

Operation :

The frequency synthesizer is supposed to produce an output signal, the frequency of which can be precisely adjusted to any value in a prescribed range. The output frequencies of a synthesizer should be very stable. In order to ensure the stability of output frequency, a crystal oscillator of frequency f_{osc} is used. The output frequency of crystal oscillator is divided by M with the help of the divide by M network. Thus the input frequency to PLL is (f_{osc}/M) as shown in Fig. 10.



(K-862) **Fig. 10 : Block diagram of frequency synthesizer using PLL**

The PLL will compare this frequency with the frequency at the output of divide by N network, and will try to adjust this frequency equal to $\frac{f_{osc}}{M}$. In order to obtain the same frequency i.e. (f_{osc}/M) at the output of divide by N network, the VCO frequency should be adjusted to,

$$f_{VCO} = \frac{f_{osc}}{M} \times N \quad ...(1)$$

$$\text{OR} \quad f_{VCO} = \left(\frac{N}{M}\right) f_{osc} \quad ...(2)$$

Chapter 4 : Modulation [Total Marks : 25]

Q. 3(b) Explain the fly wheel effect in class C amplifier. **(5 Marks)**

Ans. :

When we briefly push a fly wheel, it absorbs this energy and continues to rotate for some time. This is known as a fly wheel effect. The same effect is being used in class C amplifier to produce an AM wave. Here the class C amplifier produces a short duration current pulse in each cycle of the carrier. This current pulse is applied to a tuned circuit. The tuned circuit will produce damped oscillations at its output. This is the fly wheel effect present in a class C amplifier.

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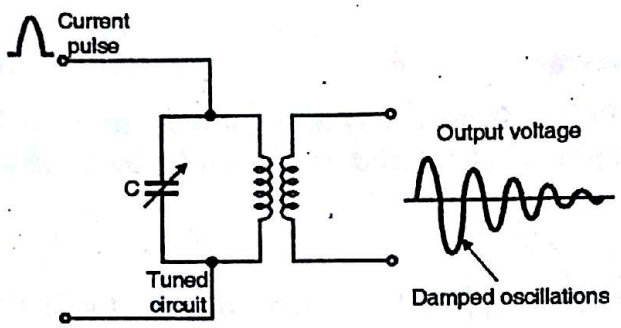
This property states that if we apply a current pulse to a tuned circuit then it generates damped voltage oscillations at its output. This is as shown in Fig. 10(A). The amplitude of oscillations is proportional to the size of current pulse and the decay rate is proportional to the time constant.

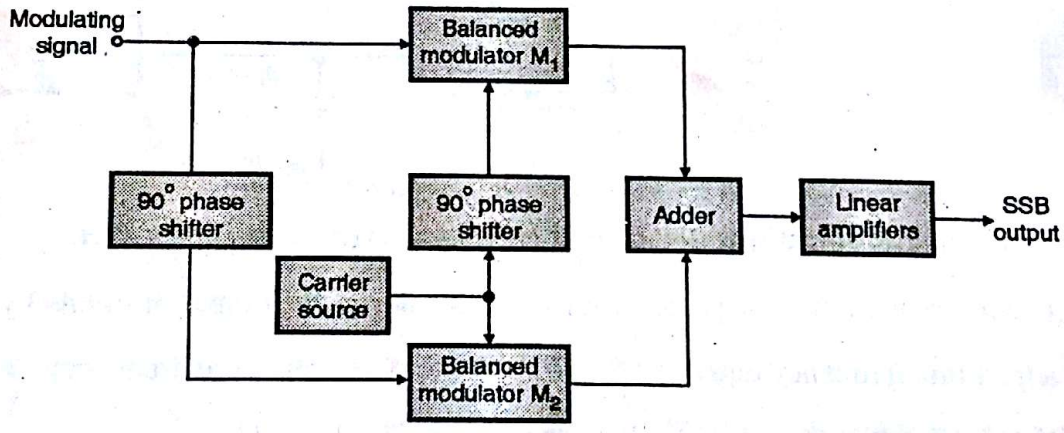


(D-1108) **Fig. 10(A) : The property of tuned circuit**

Q. 4(a) Draw the block diagram of a phase cancellation SSB generation and explain how the carrier and unwanted sideband are supposed. What change is necessary to suppress the other side band ? **(10 Marks)**

Ans. :

The block diagram for the phase shift method of SSB generation is as shown in Fig. 11. This system is used for the suppression of lower sideband. This system uses two balanced modulators M_1 and M_2 and two 90° phase shifting networks as shown in the Fig. 11.



(D-137) **Fig. 11 : Phase shift method to suppress the LSB**

Operation :

The operation of the phase shift method is as follows :

The balanced modulator M_1 has two inputs, the modulating signal without any phase shift and the RF carrier with a 90° phase shift. The other balanced modulator M_2 receives the modulating signal with a 90° phase shift and carrier without any phase shift. At the output of both the balanced modulators we get both the sidebands. The carrier is completely removed.

The upper sidebands (USBs) at the outputs of both the balanced modulators lead the carrier by 90°. But LSB at the output of M_1 leads the carrier by 90° and the LSB at the output of M_2 lags behind the carrier by 90°. Thus the LSBs are out of phase. So when the outputs of M_1 and M_2 are applied to the adder, the LSBs are cancelled out and the output of the adder consists of only the upper sideband.

The linear amplifiers will follow the adder. They are class B or AB type amplifiers used to amplify the USB without introducing any distortion.

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Mathematical proof of sideband suppression :

1. Refer Fig. 8. The inputs to the balanced modulator M_1 are

$$\text{Inputs to } M_1 \begin{cases} \cos \omega_m t & \text{.....Modulating signal as it is} \\ \cos(\omega_c t + 90°) & \text{.....90° phase shifted carrier} \end{cases}$$

2. And the inputs to balanced modulator M_2 are

$$\text{Inputs to } M_2 \begin{cases} \cos(\omega_m t + 90°) & \text{....90° shifted modulating signal} \\ \cos \omega_c t & \text{....carrier as it is} \end{cases}$$

3. So the output of $M_1 = \cos(\omega_c t) \cdot \cos \omega_m t$ ...(1)

$$= \underbrace{\frac{1}{2}\cos[\omega_c t + \omega_c t + 90°]}_{\text{USB with 90° advance}} + \underbrace{\frac{1}{2}\cos[\omega_c t - \omega_m t + 90°]}_{\text{LSB with 90° advance}} \quad \text{...(2)}$$

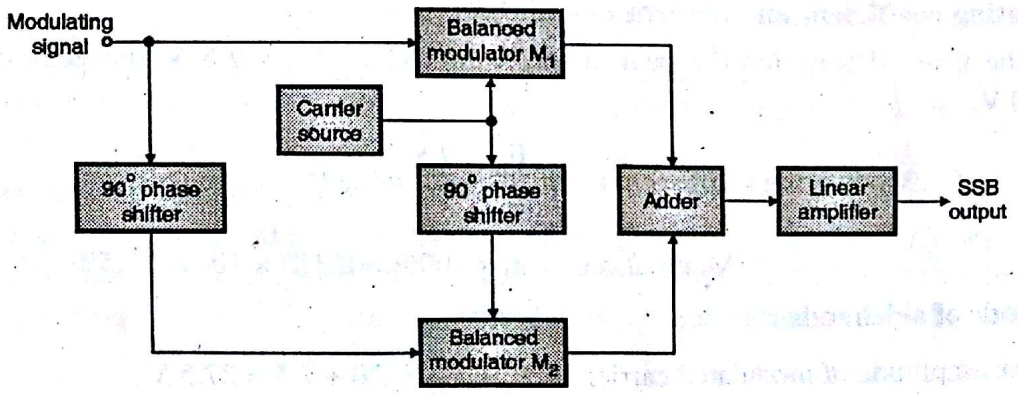
4. And output $M_2 = \cos \omega_c t \cdot \cos(\omega_m t + 90°)$

$$= \underbrace{\frac{1}{2}\cos[\omega_c t + \omega_m t + 90°]}_{\text{USB with 90° advance}} + \underbrace{\frac{1}{2}\cos[\omega_c t - \omega_m t - 90°]}_{\text{LSB with 90° delay}} \quad \text{...(3)}$$

5. Output of the adder = Output of M_1 + output of M_2 = $\cos(\omega_c t + \omega_m t + 90°)$ ...(4)

This output is obtained by adding Equations (2) and (3). The LSBs in the outputs of M_1 and M_2 are 180° out of phase with respect to each other. Hence they are cancelled out when added. So the adder output contains only the upper sideband.

Suppression of the upper sideband : We can suppress the USB and generate the SSB signal consisting of the LSB by arranging the blocks as shown in Fig. 12. Here the modulating and the carrier signals are applied to the upper balanced modulator directly (without any phase shift). Whereas both these signals are 90° phase shifted and then applied to the lower balanced modulator.



(D-138) **Fig. 12 : Phase shift method to suppress the USB**

Mathematical proof for USB suppression :

1. Inputs to M_1 are : $\cos \omega_m t$ and $\cos \omega_c t$
2. Inputs to M_2 are : $\cos(\omega_m t + 90°)$ and $\cos(\omega_c t + 90°)$

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3. Output of $M_1 = \cos \omega_m t \cos \omega_c t$

$$= \frac{1}{2} \cos (\omega_c t + \omega_m t) + \frac{1}{2} \cos (\omega_c t - \omega_m t)$$

$$= \underbrace{\frac{1}{2} \cos (\omega_c + \omega_m) t}_{\text{USB with } 0° \text{ phase shift}} + \underbrace{\frac{1}{2} \cos (\omega_c - \omega_m) t}_{\text{LSB with } 0° \text{ phase shift}} \quad ...(5)$$

4. Output of $M_2 = \cos (\omega_c t + 90°) \cdot \cos (\omega_m t + 90°)$

$$= \underbrace{\frac{1}{2} \cos (\omega_c t + \omega_m t + 180°)}_{\text{USB with } 180° \text{ phase shift}} + \underbrace{\frac{1}{2} \cos (\omega_c t - \omega_m t)}_{\text{LSB with } 0° \text{ phase shift}} \quad ...(6)$$

5. Adder output $= \cos (\omega_c - \omega_m) t$ ...(7)

This output is obtained by adding outputs of M_1 and M_2. The USB in the output of M_1 and that in the output of M_2 are 180° out of phase. So in the adder they cancel each other and only the LSB is obtained.

Q. 5(b) One input to a conventional AM modulator is a 500 kHz carrier with an amplitude of 20 V_P. The second input is a 10 kHz modulating signal that is of sufficient amplitude to cause a change in the output wave of ± 7.5 V_P. Determine :

1. Upper and lower side frequencies
2. Modulation coefficient and percent modulation
3. Peak amplitude of the modulated carried and upper and lower side frequency voltages
4. Expression for the modulated wave
5. Draw the output spectrum. **(10 Marks)**

Ans. :

(a) Upper and lower sideband frequencies :

$$f_{USB} = f_c + f_m = 500 \text{ kHz} + 10 \text{ kHz} = 510 \text{ kHz}$$

$$f_{LSB} = f_c - f_m = 500 \text{ kHz} - 10 \text{ kHz} = 490 \text{ kHz}$$

(b) Modulating coefficient and percent modulation :

From the given description the peak modulating voltage $V_m = 7.5$ V and peak carrier voltage $E_c = 20$ V.

$$\therefore \quad \text{Modulating coefficient } m = \frac{E_m}{E_c} = \frac{7.5}{20} = 0.375$$

$$\% \text{ Modulation} = m \times 100\% = 0.375 \times 100 = 37.5\%$$

(c) Amplitude of sidebands :

$$\text{Peak amplitude of modulated carrier} = E_c + E_m = 20 + 7.5 = 27.5 \text{ V}$$

$$\text{Amplitude of sidebands} = \frac{m E_c}{2} = 0.375 \times \frac{20}{2} = 3.75 \text{ V}$$

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(d) Expression for modulated wave :

$$e_{AM} = E_c [1 + m \sin (2\pi f_m t)] \sin (2\pi f_c t)$$

$$= 20 [1 + 0.375 \sin (2\pi \times 10 \times 10^3 t)] \sin (2\pi \times 500 \times 10^3 t)$$

Chapter 5 : Demodulation [Total Marks : 20]

Q. 1(c) For an FM radio receiver, when the consumer changes the channel, the oscillator frequency changes. The frequency of radio signal coming out of the mixer will be always 10.7 MHz regardless of the channel selected. If the oscillator frequency is 99.2 MHz, what is the frequency of station selected ? If a Hartley tuned oscillator is being used with a variable capacitor in the LC tank circuit, what is the value of capacitance if the total inductance is 2.5 μH. **(5 Marks)**

Ans. :

Part I : Find input signal frequency f_s :

Given : FM radio receiver, I.F. = 10.7 MHz, $f_{osc.}$ = 99.2 MHz

The input frequency f_s is such that,

$$f_s + IF = f_{osc}$$

$$\therefore \quad f_s = f_{osc} - IF = 99.2 \text{ MHz} - 10.7 \text{ MHz}$$

$$= 88.5 \text{ MHz}$$

Part II : Find C :

Given : Hartley oscillator, f_o = 99.2 MHz, $(L_1 + L_2)$ = 2.5 μH.

$$f_o = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}$$

$$\therefore \quad f_o^2 = \frac{1}{4\pi^2 C (L_1 + L_2)} \qquad \therefore \quad C = \frac{1}{4\pi^2 f_o^2 (L_1 + L_2)}$$

$$\therefore \quad C = \frac{1}{4\pi^2 \times (99.2 \times 10^6)^2 \times 2.5 \times 10^{-6}} = 1.03 \text{ pF}$$

Q. 4(b) Draw Foster Seeley discriminator with circuit diagram and explain its working with phasor diagrams. **(10 Marks)**

Ans. : Foster-Seeley Discriminator :

The Foster Seeley discriminator is thus derived from the balanced modulator. Here the primary and the secondary windings both are tuned to the same center frequency "f_c" of the incoming signal. This simplifies the tuning process to a great extent and it will yield better linearity than the balanced slope detector.

Principle of operation :

Even though the primary and secondary tuned circuits are tuned to the same center frequency, the voltages applied to the two diodes D_1 and D_2 are not constant. They vary depending on the frequency of the input signal. This is due to the change in phase shift between the primary and secondary windings depending on the input frequency.

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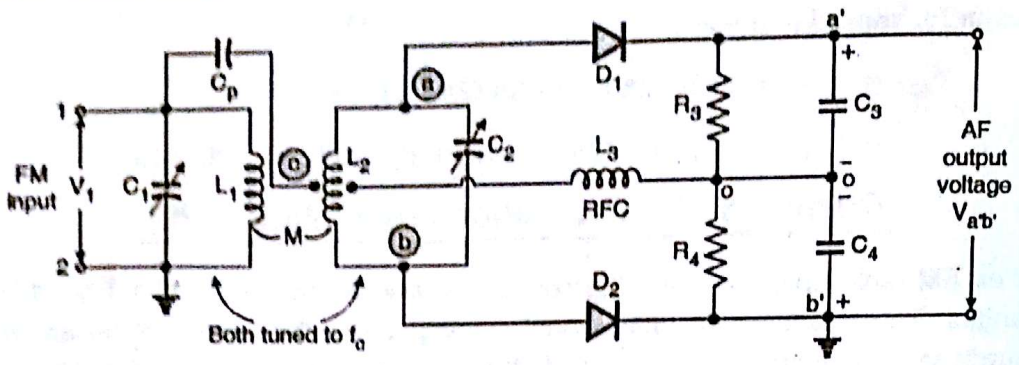

(D-300) **Fig. 13 : Phase discriminator**

Operation : The phase discriminator can be redrawn as shown in Fig. 14 to understand the concept of its operation. The capacitor C_p is a coupling capacitor which passes all the frequencies at the input to the center tap of the transformer secondary. C_4 will bypass resistance R_4 as $R_4 >> X_{C4}$. Therefore voltage across RFC will be equal to the input voltage V_1.

$$V_{RFC} = V_1 \quad ...(1)$$

It can be proved that the secondary voltage V_{ab} gets divided equally across the upper and lower halves of the secondary as shown in Figs. 14 and 15.

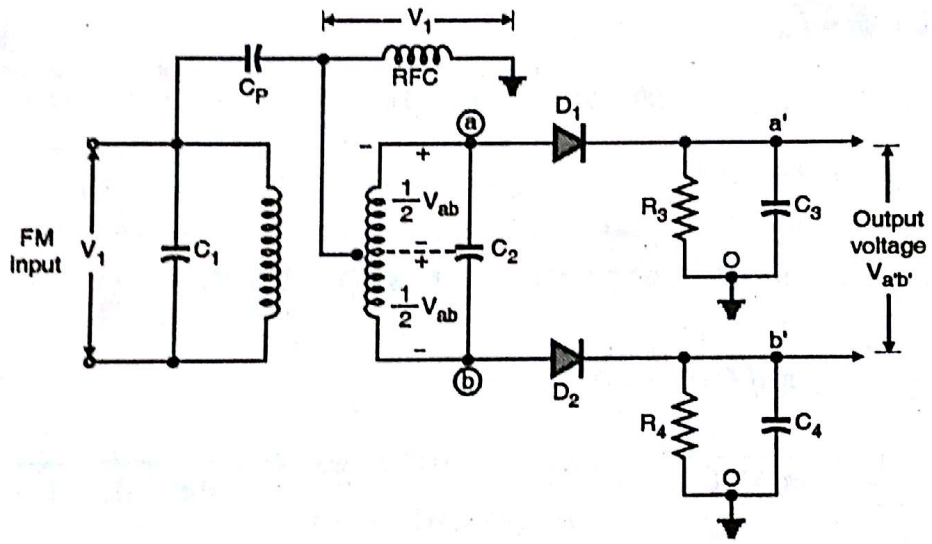

Fig. 14: Phase discriminator redrawn

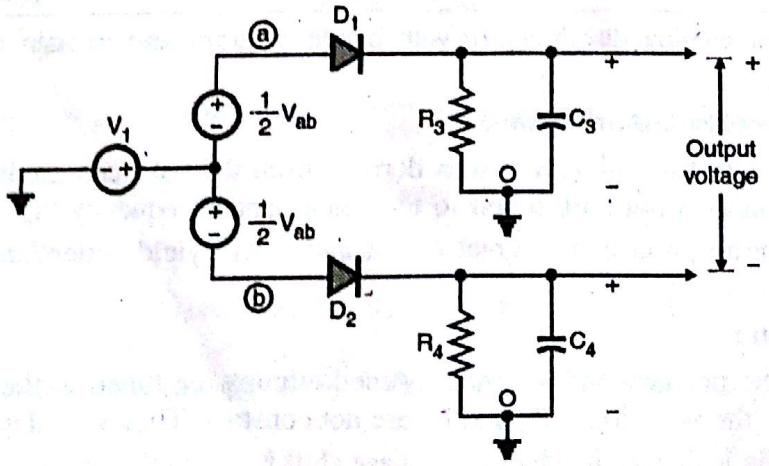

Fig. 15 : Equivalent circuit of phase discriminator

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Thus input to each diode is equal to the vector sum of the primary voltage V_1 and half the secondary voltage i.e $\left(\frac{1}{2}V_{ab}\right)$. Vector sum should be taken because these voltages are not in phase with each other. Phase shift between the primary and secondary voltages is not constant but it depends on the input frequency. The effect of this is as explained below.

Output voltage of the discriminator : Output voltage of the phase discriminator is equal to the difference between the outputs of the two diode rectifiers.

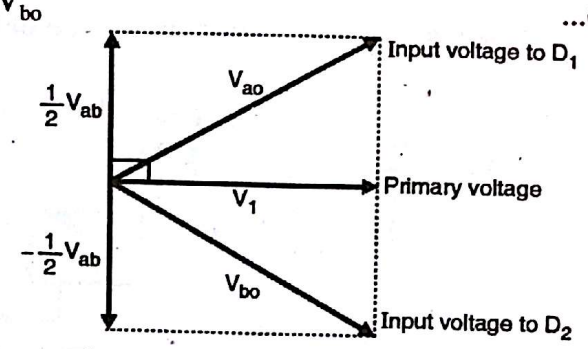
$$\therefore \quad V_o = V_{a'b'} = V_{a'o} - V_{b'o} \qquad ...(2)$$

As the diode drops are not known, we cannot calculate the output exactly. But it is sure that the output will be proportional to the voltage applied at the inputs of diodes D_1 and D_2.

$$\therefore \quad V_o \propto V_{ao} - V_{bo} \qquad ...(3)$$

1. Output voltage at $f_{in} = f_c$:

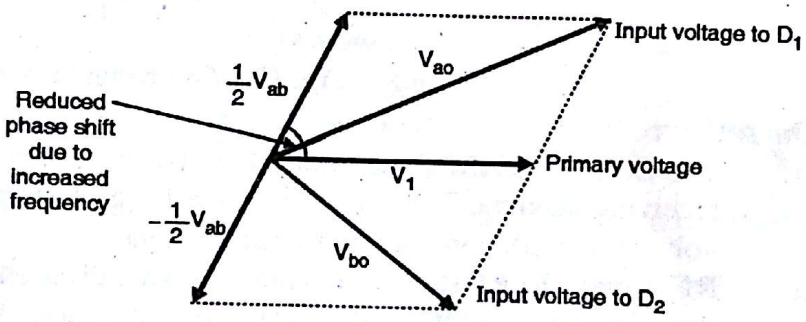
When the input frequency is equal to the center frequency (f_c), the phase shift between the primary and secondary voltages is exactly 90°. Therefore the input voltages to both the diodes will be equal as shown in Fig. 16. Therefore the outputs of both the diodes will be equal. Hence the net output voltage will be zero.



(D-302) **Fig. 16 : Phasor diagram for $f_{in} = f_c$**

2. Output voltage for $f_{in} > f_c$:

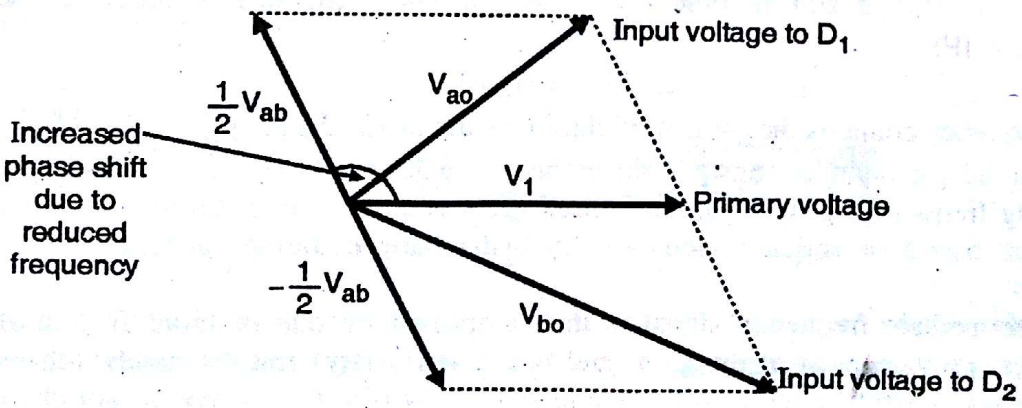
At input frequencies above the center frequency f_c, secondary voltage V_{ab} leads the primary voltage V_1 by less than 90°. Hence input voltage to D_1 i.e. V_{ao} is higher than input to D_2 i.e. V_{bo}. The output voltage will therefore be positive for $f_{in} > f_c$.



(D-303) **Fig. 17 : Phasor diagram for $f_{in} > f_c$**

3. Output voltage for $f_{in} < f_c$:

For input frequencies below the center frequency f_c, the secondary voltage V_{ab} leads the primary voltage V_1 by more than 90° as shown in Fig. 18. Hence input voltage to D_1 is less than input voltage to D_2. Therefore the output voltage will be negative for $f_{in} < f_c$.



(D-303) **Fig. 18 : Phasor diagram for $f_{in} < f_c$**

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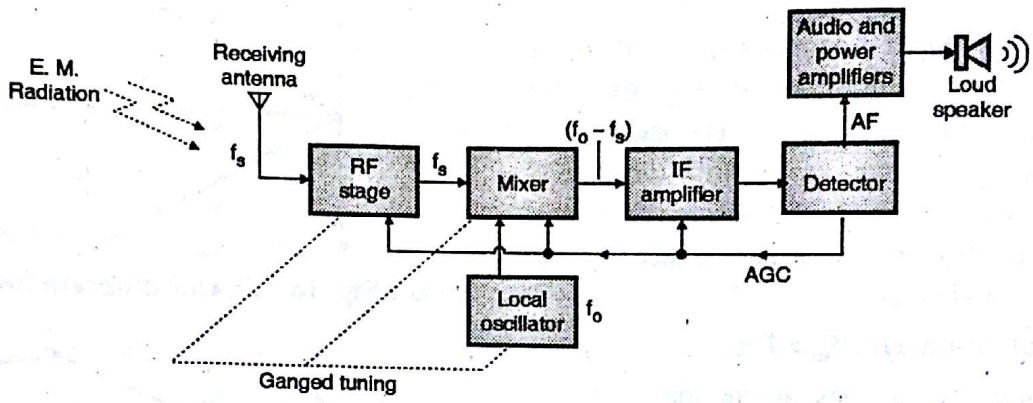
Q. 6(b) Explain in brief the principle of superheterodyne receiver. **(5 Marks)**

Ans. :

Superhetrodyne receiver :

The problems in the TRF receiver are solved in this receiver by converting every selected RF signal to a fixed lower frequency called as the "intermediate frequency (IF)". This frequency contains the same modulation as the original carrier. The IF signal is then amplified and detected to get back the modulating signal. As the "IF" is lower than the lowest RF signal frequency, the possibility of oscillations and instability is minimized.

Also the required value of Q for constant BW does not depend on the frequency of desired signal, because the "IF" is constant and same for all the incoming RF signals. Thus the super-heterodyne receiver solves all the problems associated with the TRF receiver. The radio and TV receivers operate on the principle of superheterodyning. The block diagram of a superheterodyne radio receiver is shown in Fig. 19.



(D-230) **Fig. 19 : The superheterodyne receiver**

Operation :

1. The DSBFC or AM signal transmitted by the transmitter travels through the air and reaches the receiving antenna. This signal is in the form of electromagnetic waves. It induces a very small voltage (few μV) into the receiving antenna.
2. **RF stage:** The RF stage is an amplifier which is used to select the wanted signal and reject other out of many, present at the antenna. It also reduces the effect of noise. At the output of the RF amplifier we get the desired signal at frequency "f_s".
3. **Mixer:** The mixer receives signals from the RF amplifier at frequency (f_s) and from the local oscillator at frequency (f_o) Such that $f_o > f_s$.
4. **Intermediate frequency (IF):** The mixer will mix these signals to produce signals having frequencies f_s, f_o, $(f_o + f_s)$ and $(f_o - f_s)$. Out of these the difference of frequency component i.e. $(f_o - f_s)$ is selected and all others are rejected. This frequency is called as the intermediate frequency (IF).

$$\therefore \text{ I.F. } = (f_o - f_s)$$

This frequency contains the same modulation as the original signal f_s.

5. In order to maintain a constant difference between the local oscillator frequency and the incoming frequency, ganged tuning is used. This is simultaneous tuning of RF amplifier, mixer and local oscillator and it is achieved by using ganged tuning capacitors (Tuning control in radio set).
6. This intermediate frequency signal is then amplified by one or more IF amplifier stages. IF amplifiers provide most of the gain (and hence sensitivity) and the bandwidth requirements of the receiver. Therefore the sensitivity and selectivity of this receiver do not change much with changes in the incoming frequency.

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7. The amplified IF signal is detected by the detector to recover the original modulating signal. This is then amplified and applied to the loudspeaker.

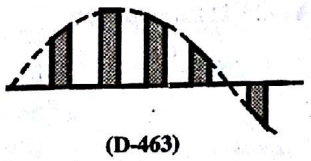
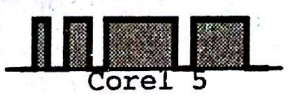
8. AGC means automatic gain control. This circuit controls the gains of the RF and IF amplifiers to maintain a constant output voltage level even when the signal level at the receiver input is fluctuating. This is done by feeding a controlling dc voltage to the RF and IF amplifiers. The amplitude of this dc voltage is proportional to the detector output.

Chapter 6 : Analog Pulse Modulation [Total Marks : 10]

Q. 6(c) Compare PAM, PPM and PWM. **(5 Marks)**

Ans. :

Comparison between PAM, PWM, PPM :

Sr. No	Parameter	PAM	PWM	PPM
1.	Type of carrier	Train of pulses	Train of pulses	Train of pulses
2.	Variable characteristic of the pulsed carrier	Amplitude	Width	Position
3.	Bandwidth requirement	Low	High	High
4.	Noise immunity	Low	High	High
5.	Information is contained in	Amplitude variations	Width variation	Position variation
6.	Transmitted power	Varies with amplitude of pulses	Varies with variation in width	Remains constant
7.	Need to transmit synchronizing pulses	Not needed	Not needed	Necessary
8.	Complexity of generation and detection	Complex	Easy	Complex
9.	Similarity with other modulation systems	Similar to AM	Similar to FM	Similar to PM
10.	Output waveforms	 (D-463)	 (D-463)	(D-463)

Q. 6(d) What is meant by Nyquist rate in sampling ? What is standard frequency for speech signal ? **(5 Marks)**

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Ans. :

Nyquist Rate and Nyquist Interval :

The minimum sampling rate of "2W" samples per second for a signal x (t) having maximum frequency of "W" Hz is called as "Nyquist rate". The reciprocal of Nyquist rate i.e. 1/2W is called as the Nyquist interval.

Nyquist rate = 2W Hz
Nyquist interval = 1/2W seconds

The standard sampling frequency for speech signal is 8 kHz.

Chapter 7 : Digital Modulation Techniques [Total Marks : 05]

Q. 6(a) What are the drawbacks of delta modulation and how are they overcome by ADM ? **(5 Marks)**

Ans. :

Drawbacks of delta modulation :

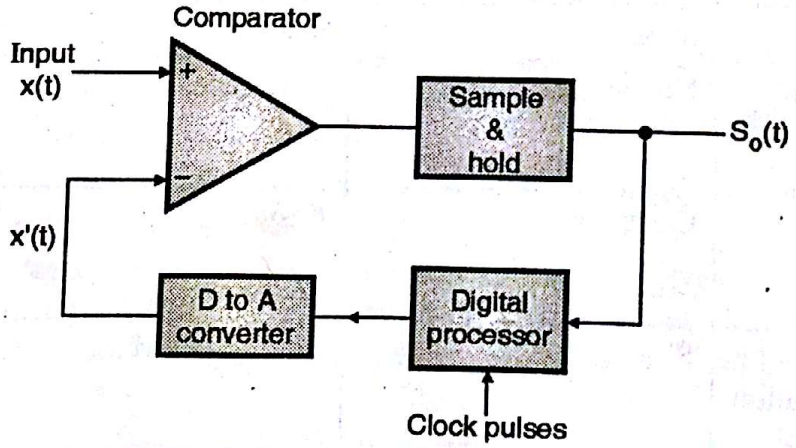
1. The two distortions i.e. slope overload error and granular noise are present.
2. Practically the signaling rate with no slope overload error will be much higher than that of PCM.

The slope overload error can be reduced by using another type of delta modulation, called as adaptive delta modulation (ADM).

Adaptive delta modulation :

ADM Transmitter :

In the ADM system, the step size is not constant. Rather when the slope overload occurs the step size becomes progressive larger and therefore x′ (t) will catch up with x(t) more rapidly. The ADM transmitter is as shown in Fig. 20.



(D-495) **Fig. 20 : ADM transmitter**

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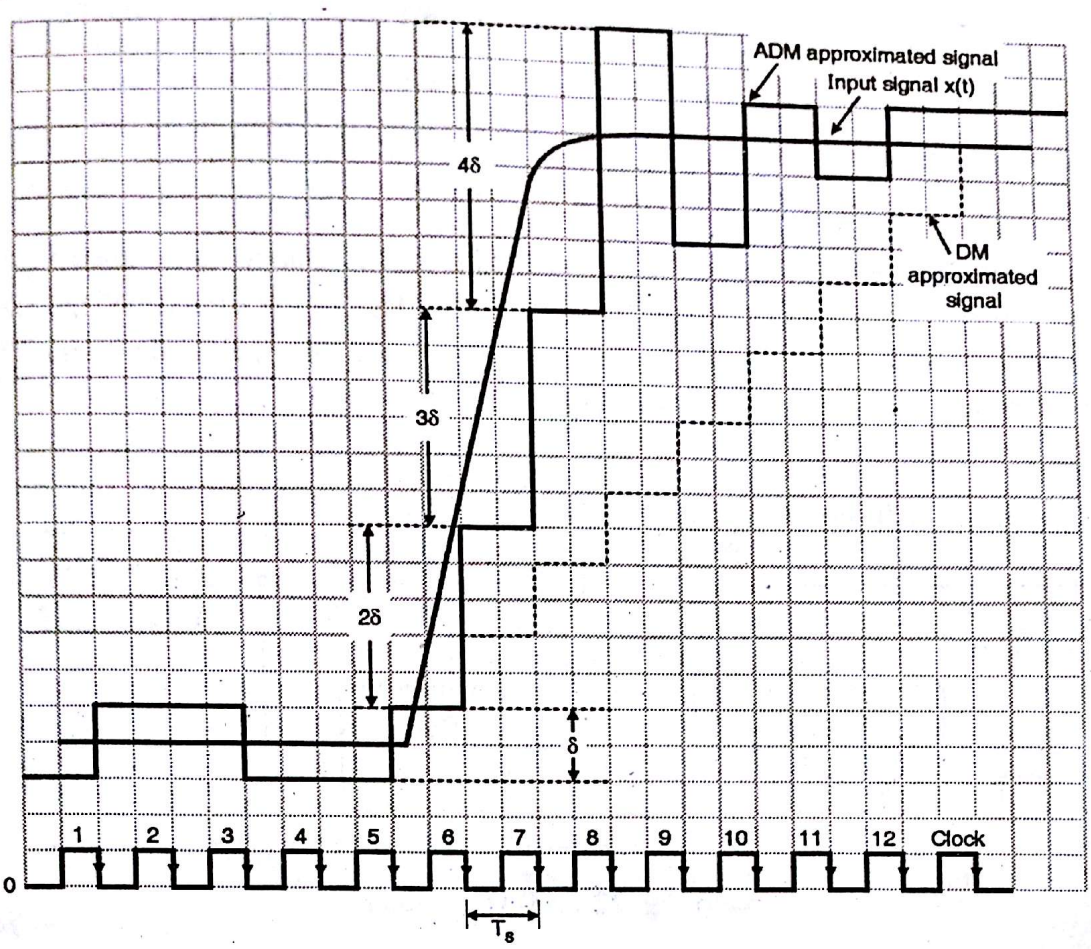
Operation :



(D-496) **Fig. 21 : Waveforms of ADM**

In response to the kth clock pulse trailing edge, the processor generates a step which is equal in magnitude to the step generated in response to the previous i.e. $(k-1)^{th}$ clock edge. If the direction of both the steps is same, then the processor will increase the magnitude of the present step by "δ". If the directions are opposite then the processor will decrease the magnitude of the present step by "δ". $S_o(t)$ in the Fig. 20, i.e. the output of the ADM system is given as,

$$S_o(t) = +1 \text{ if } x(t) > x'(t) \text{ just before } k^{th} \text{ clock edge.}$$

and $$S_o(t) = -1 \text{ if } x(t) < x'(t) \text{ just before the } k^{th} \text{ clock edge.}$$

Then the step size at the sampling instant k is given by,

$$\underset{\substack{\downarrow \\ \text{Step size} \\ \text{at } k^{th} \text{ clock} \\ \text{edge}}}{\delta(k)} = \underset{\substack{\downarrow \\ \text{Step size} \\ \text{at } (k-1)^{th} \\ \text{clock edge}}}{[\delta(k-1)]} \underset{\substack{\downarrow \\ \text{Output at} \\ k^{th} \text{ edge}}}{S_o(k)} + \underset{\substack{\downarrow \\ \text{Basic} \\ \text{step} \\ \text{size}}}{\delta} \underset{\substack{\downarrow \\ \text{Output at } (k-1)^{th} \\ \text{clock edge}}}{S_o(k-1)} \quad ...(1)$$

From the waveforms of Fig. 21. Let us assume k = 6, i.e. consider the 6th clock edge.

$$\therefore \quad k-1 = 5$$

$$\therefore \quad \delta(k-1) = \delta(5) = \delta$$

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$$S_o(k) = S_o(6) = +1$$

$$S_o(k-1) = S_o(5) = +1$$

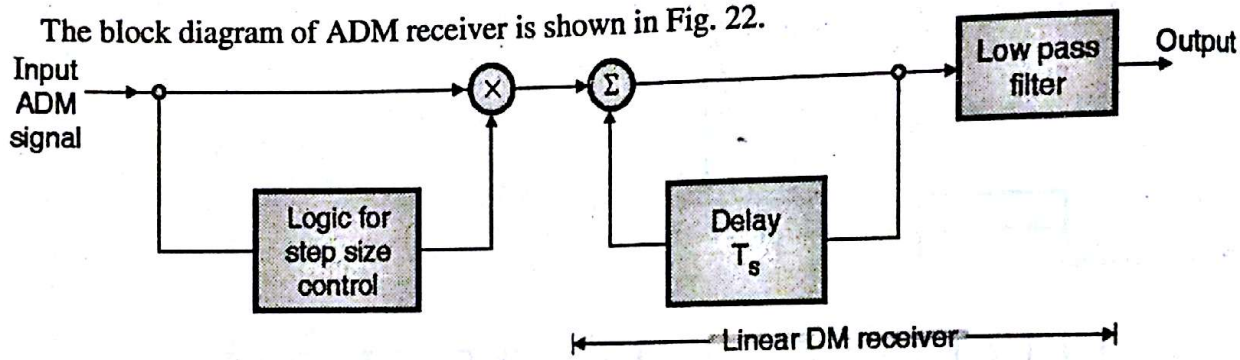
Substitute in Equation (11) to get,

$$\delta(6) = \delta + \delta = 2\delta$$

From the Fig. 21, the step size at the 6th clock edge is 2 δ. Due to variable step size, the slope overload error is reduced. But quantization error is increased. Due to the adjustable step size, the slope overload problem is solved. Hence ADM system has a low bit rate than the PCM system. Therefore the BW required is also less than a comparable PCM system.

ADM Receiver :

The block diagram of ADM receiver is shown in Fig. 22.



(D-497) **Fig. 22 : ADM receiver**

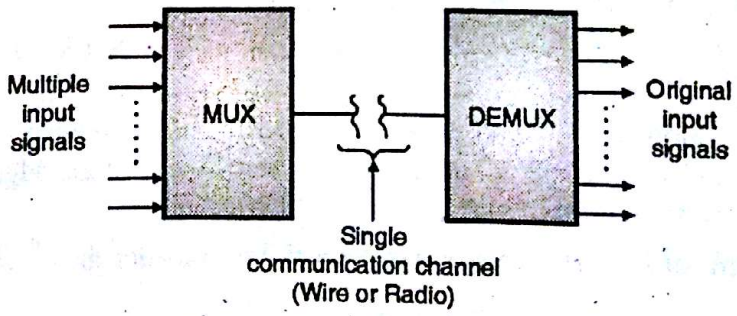
The ADM signal is first converted into a D.M. signal with the help of the step size control logic and then applied to a D.M. receiver. At the output of low pass filter we get the original signal back.

Chapter 8 : Multiplexing [Total Marks : 10]

Q. 5(a) What is multiplexing in communication system ? Draw block diagram of TDM-PCM system and explain. **(10 Marks)**

Ans. :

Multiplexing : The concept of a simple multiplexer is illustrated in Fig. 23. The multiplexer receives a large number of different input signals. Multiplexer has only one output which is connected to the single communication channel. The multiplexer combines all input signals into a single composite signal and transmits it over the communication medium.



(D-499) **Fig. 23 : Concept of multiplexing**

Sometimes the composite signal is used for modulating a carrier before transmission. At the receiving end, of communication link, a demultiplexer is used to sort out the signals into their original form. The operation of demultiplexer is exactly opposite to that of a multiplexer.

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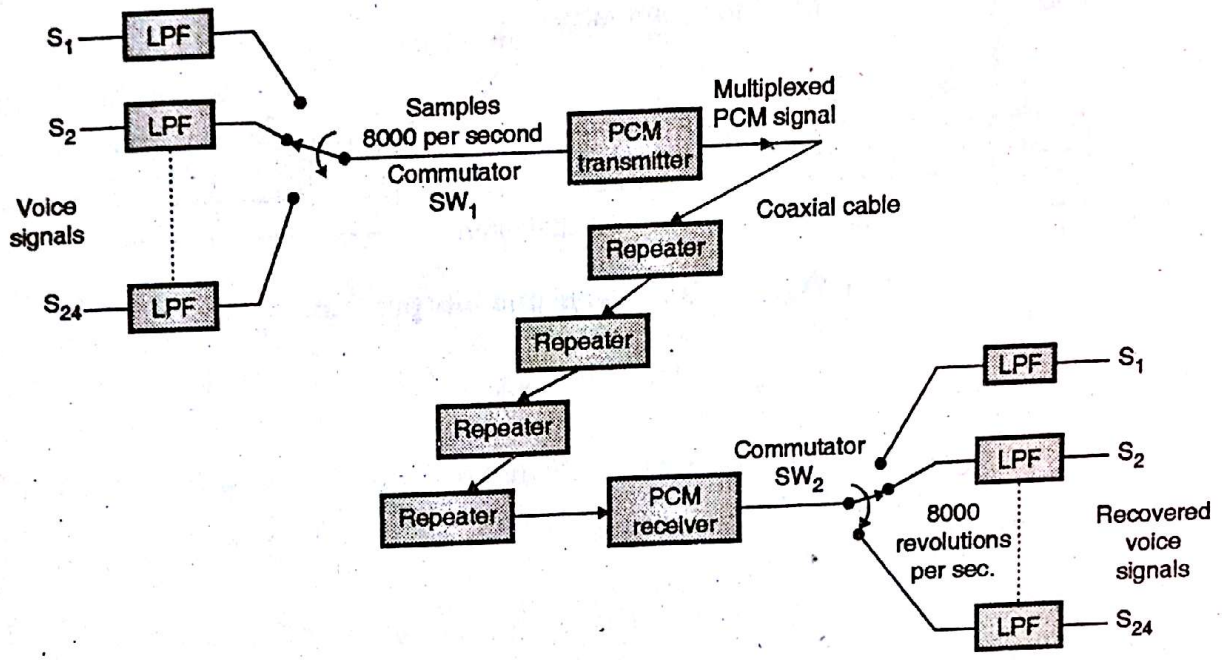
TDM-PCM system : When a large number of PCM signals are to be transmitted over a common channel, multiplexing of these PCM signals is required. Fig. 24 shows the basic time division multiplexing scheme, called as the **T_1 digital system.** This system is used to convey multiple signals over telephone lines using wideband coaxial cable.



(G-1312) **Fig. 24 : Block diagram of a basic PCM-TDM system**

Operation of the T_1 system :

The operation of the PCM-TDM system shown in Fig. 24 is as follows :

This system has been designed to accommodate 24 voice channels marked S_1 to S_{24}. Each signal is bandlimited to 3.3 kHz, and the sampling is done at a standard rate of 8 kHz. This is higher than the Nyquist rate. The sampling is done by the commutator switch SW_1. These voice signals are selected one by one and connected to a PCM transmitter by the commutator switch SW_1.

Each sampled signal is then applied to the PCM transmitter which converts it into a digital signal by the process of A to D conversion and companding. The resulting digital waveform is transmitted over a co-axial cable. Periodically, after every 6000 ft., the PCM-TDM signal is regenerated by amplifiers called "Repeaters". They eliminate the distortion introduced by the channel and remove the superimposed noise and regenerate a clean PCM-TDM signal at their output. This ensures that the received signal is free from the distortions and noise.

At the destination the signal is companded, decoded and demultiplexed, using a PCM receiver. The PCM receiver output is connected to different low pass filters via the commutator switch SW_2. Synchronization between the transmitter and receiver commutators SW_1 and SW_2 is essential in order to ensure proper communication.

Bits/Frame :

The commutators sweep continuously from S_1 to S_{24} and back to S_1 at the rate of 8000 revolutions per second. This will generate 8000 samples per second of each signal (S_1 to S_{24}). Each sample is then encoded (converted) into an eight bit digital word. Thus the digital signal generated during one complete sweep (revolution) of the commutator is given by :

$$1 \text{ Frame} \equiv 1 \text{ revolution}$$

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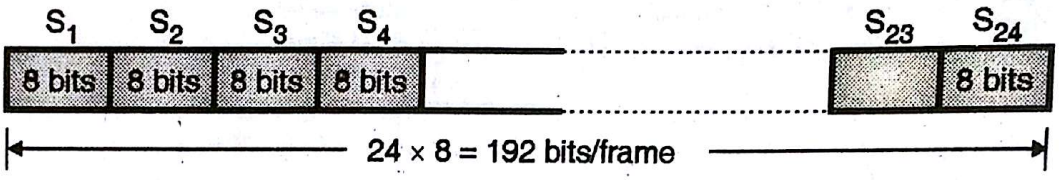
$$= 24 \text{ channels}$$

$$= 24 \times 8 \text{ bits} = 192 \text{ bits}$$

One frame of PAM-TDM is shown in Fig. 25. Each voice signal from S_1 to S_{24} is encoded into eight bits. One frame corresponds to the time corresponding transmission of each signal once. Hence 1-frame corresponds to one-revolution of the commutator.



(G-1313) **Fig. 25 : One frame and bits per frame**

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May 2014

Chapter 1 : Electronic Circuits [Total Marks : 25]

Q. 1(b) Explain Barkhausen's criteria for principle of oscillation. **(5 Marks)**

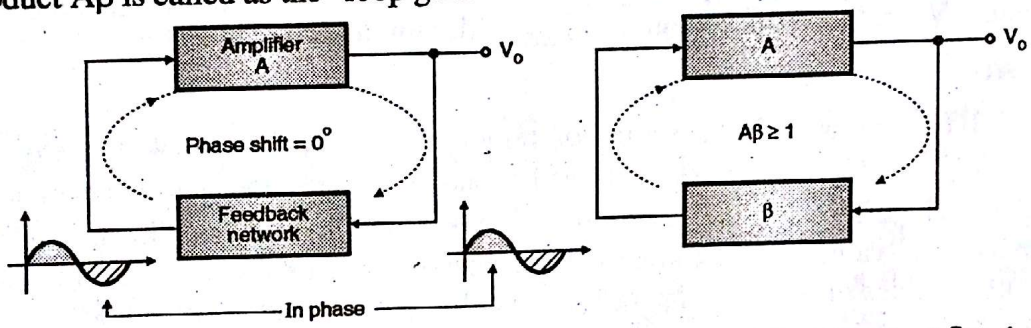
Ans.: Barkhausen criterion :

The Barkhausen criterion states that :

1. An oscillator will operate at that frequency for which the total phase shift introduced, as measured from the input terminals, through the amplifier and feedback network and back again to the input is precisely equal to 0° or 360° or integral multiple of 360°.
2. At the oscillator frequency, the magnitude of the product of open loop gain of the amplifier A and the feedback factor β is equal to or greater than unity.

$$\therefore \ |A\beta| \geq 1$$

The product Aβ is called as the "loop gain". These conditions are shown in Figs. 1(a) and (b).



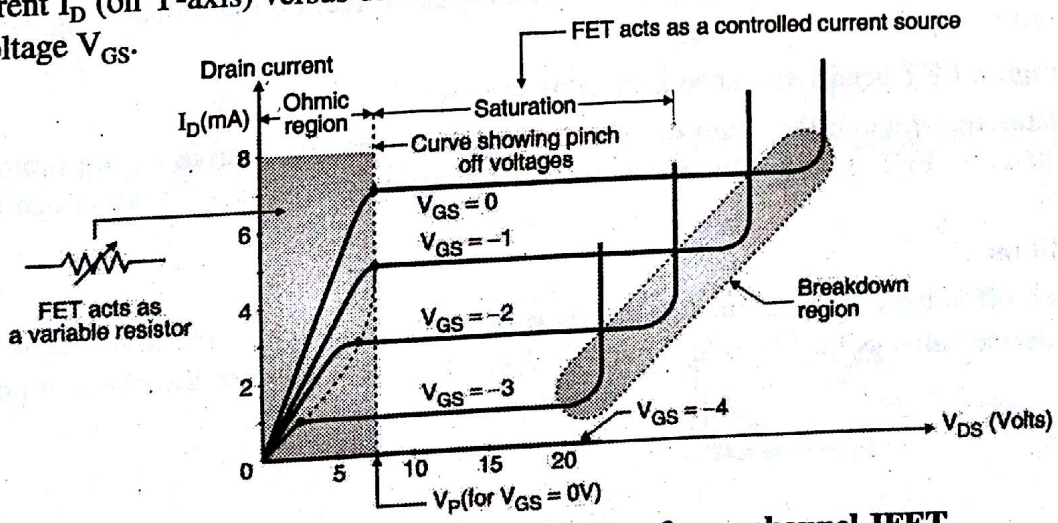
(a) The phase shift around the loop is 0° **(b) Loop gain Aβ ≥ 1**

(N-953) **Fig. 1 : Barkhausen criterion**

Q. 2(a) Sketch a typical drain characteristics for $V_{GS} = 0$ for an n-channel JEFET. Explain the shape of the characteristics, identify regions and indicate the important current and voltage levels. **(10 Marks)**

Ans. : Drain characteristics :

Drain characteristics of an n-channel JFET are as shown in Fig. 2. Drain characteristics is a plot of drain current I_D (on Y-axis) versus drain to source voltage V_{DS} (on X-axis) at different values of gate to source voltage V_{GS}.



(B-272) **Fig. 2 : Drain characteristics of an n-channel JFET**

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The characteristics has been divided into three regions viz. cutoff, saturation and ohmic region.

1. **Cutoff region :** With increase in the negative V_{GS} voltage, the channel width available for conduction decreases. At a certain voltage called "$V_{GS\ (off)}$" the depletion regions touch each other to close the channel completely. Hence the cutoff region corresponds to $I_D = 0$ and $V_{GS} > V_{GS\ (off)}$. In the cutoff region $I_D = 0$ and there is no effect on its value even if we change the drain to source voltage (V_{DS}). The JFET operates as an open circuited switch in this region.

2. **Saturation region :** As shown in Fig. 2, saturation region is that portion of the characteristics where I_D remains fairly constant and does not change with changes in V_{DS}. This "saturation" is entirely different than the "saturation" in a transistor. In order to use the JFET as an amplifier it is operated in the saturation region.

3. **Ohmic region :** The drain current I_D varies with variation in the drain to source voltage V_{DS}, in the ohmic region as shown in Fig. 2. The JFET is therefore said to be operating as a Voltage Variable Resistance (VVR) in the ohmic region. It is equivalent to a closed switch in this region. The resistance offered by the JFET decreases with decrease in the value of negative gate to source bias voltage i.e. negative V_{GS}. The FET resistance in the ohmic region is given by,

$$R_{DS} = V_P / I_{DSS}$$

where, V_P = Pinch off voltage and I_{DSS} = Maximum drain current.

FET breakdown :

When a JFET is operating in the saturation region, I_D does not change with change in V_{DS} upto a certain value of V_{DS}. If V_{DS} is increased further beyond this value, the gate channel junction breaks down due to avalanche effect and the drain current shoots up suddenly as shown in Fig. 2. This can damage the device. The value of breakdown voltage does not remain constant. Infact it decreases with increase in negative values of V_{GS}. The operation in the breakdown region should be avoided in order to protect the JFET against damage.

Effect of negative V_{GS} bias :

With increase in the negative V_{GS} bias the channel width decreases and drain current I_D reduces proportionally. A family of curves for different values of V_{GS} is as shown in Fig. 2. With increase in the negative V_{GS} bias, the breakdown will take place at lower values of V_{DS}.

Pinch off Voltage (V_P) :

The "pinch off" voltage is the value of V_{DS}, at which the drain current reaches its constant saturation value. Any further increase in V_{DS} does not have any effect on the value of I_D. The pinch off voltage is denoted by V_P.

In saturation region FET is equivalent to a current source :

In the saturation region, the drain current remains constant irrespective of the drain to source voltage V_{DS}. Therefore FET is said to be equivalent to a constant current source when operated in the saturation region.

Pinch off condition :

The pinch off voltage V_P is defined as the value of V_{DS} beyond which the drain current becomes constant. V_P is defined always for $V_{GS} = 0$. Refer Fig. 3(a) which demonstrates the effect of positive V_{DS} when $V_{GS} = 0$.

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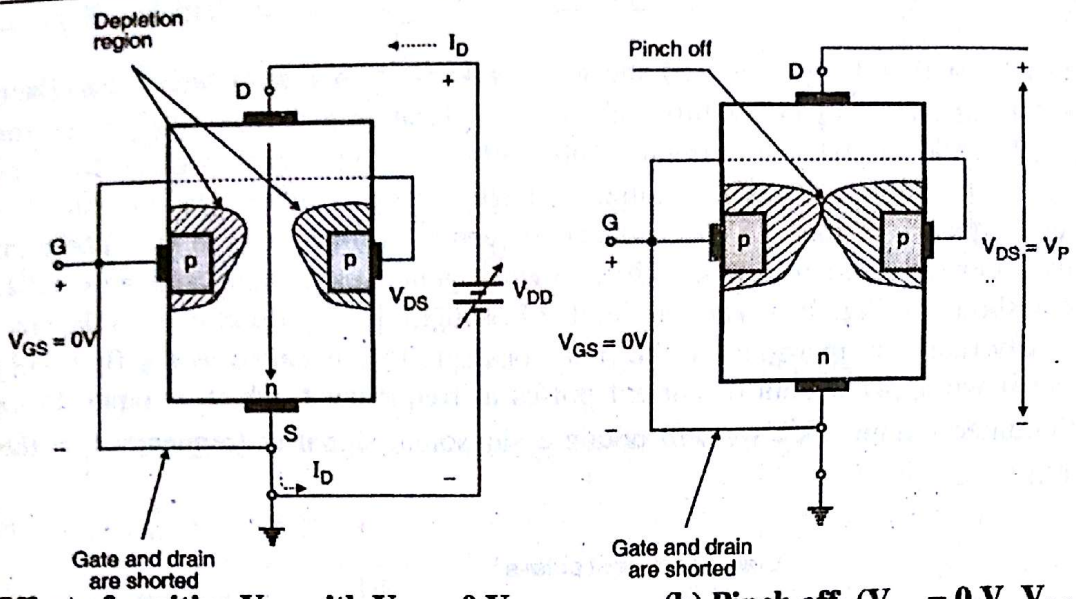


(a) Effect of positive V_{DS} with $V_{GS} = 0$ V **(b) Pinch off ($V_{GS} = 0$ V, $V_{DS} = V_P$)**

(N-924) **Fig. 3**

Q. 2(b) Explain class C BJT power amplifier in detail. Compare it with class A BJT power amplifier. **(10 Marks)**

Ans. :

Class C BJT power amplifiers : Class C amplifiers cannot be used as audio amplifiers. However use the class C amplifier in tuned circuits used in communication. The circuit diagram of class C amplifier is as shown in Fig. 4(a). The LC tuned circuit acts as the load for the transistor Q. The dc source $-V_{BB}$ biases the transistor below the cut off. RFC is a Radio Frequency Choke. It is equivalent to a short circuit for the dc operating conditions but its reactance is very high at radio frequencies. The ac input voltage V_i is applied to the base of the transistor. This voltage is superimposed on $-V_{BB}$ as shown in Fig. 4(b).

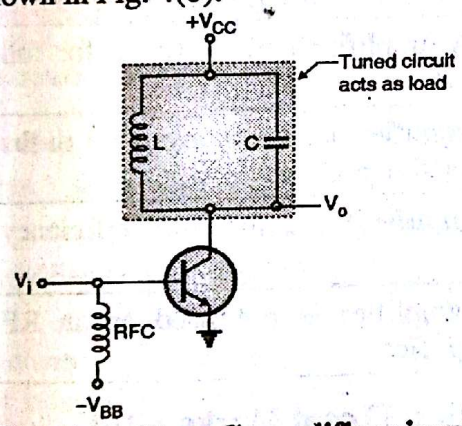
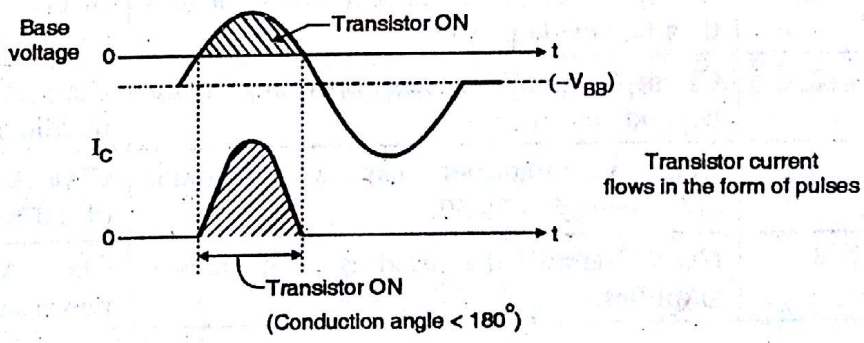
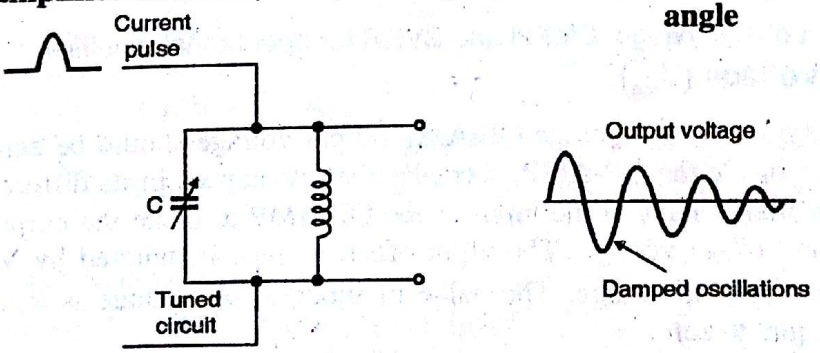


Fig. 4(a) : Class C amplifier circuit



(F-883) **Fig. 4(b) : Transistor biasing and its conduction angle**



(F-884) **Fig. 4(c) : Figure showing the property of tuned circuit**

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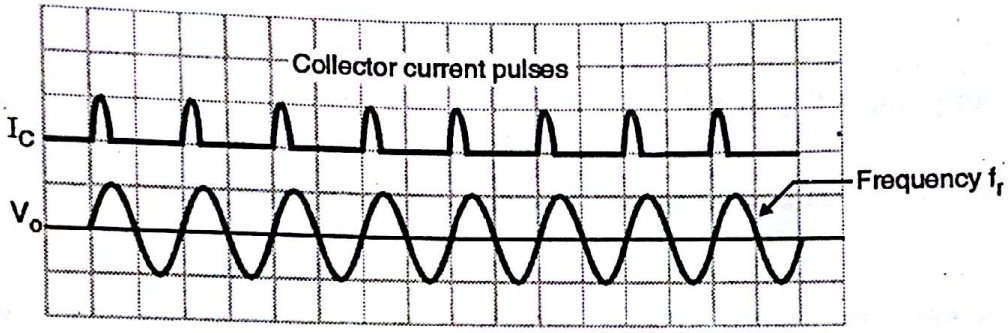
The transistor will be forward biased and will conduct for an angle which is less than 180°. The transistor collector current flows in the form of pulses of duration less than 180°. When these current pulses are applied to the LC resonant circuit a full cycle of output signal is obtained at the resonant frequency of the tuned circuit. Thus the output voltage produced across the LC tuned circuit is a sinewave and its frequency is equal to the resonant frequency of the tuned circuit. The property states that if we apply a current pulse to a tuned circuit then it generates damped voltage oscillations at its output. This is as shown in Fig. 4(c). The amplitude of oscillations is proportional to the size of current pulse and the decay rate is proportional to the time constant. This is called as the flywheel effect in a tuned circuit. So if we apply a train of current pulses at frequency f_r which is equal to the resonant frequency of the tuned circuit, then we will obtain a sinusoidal signal at frequency f_r at the output as shown in Fig. 4(d).



(F-885) **Fig. 4(d) : Output voltage of a class C amplifier**

This shows that the class C operation is limited to use at only one frequency i.e. resonant frequency f_r.

Comparison of Class C and Class A BJT power amplifier :

Sr. No.	Class C	Class A
1.	In class C amplifier current flows for less than half cycle period.	In class A amplifier current flows for full cycle period.
2.	Class C amplifier has operating point beyond cut off.	Class C amplifier has operating point in the middle of active region.
3.	Class C amplifier has a maximum efficiency of > 78.5%.	Class A amplifier has a maximum efficiency of 50%.
4.	Class C amplifier is used as an RF power amplifier.	Class A amplifier is not used as an RF power amplifier.

Chapter 2 : Operational Amplifier & its Application [Total Marks : 15]

Q. 1(a) Explain input offset voltage, CMRR and SVRR for operational amplifier. **(5 Marks)**

Ans. : Input Offset Voltage (V_{ios}) :

Ideally, for a zero input voltage, the OP-AMP output voltage should be zero. This is due to the unavoidable imbalances inside the OP-AMP, specially the imbalances in its differential input stage. So to apply a small differential voltage at the input of the OP-AMP to make the output voltage zero. This voltage is called as input offset voltage. The input offset voltage is denoted by V_{ios}. The input offset voltage is normally in a few mV range. The value of input offset voltage is temperature dependent. Ideally V_{ios} should be equal to zero.

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Common Mode Rejection Ratio (CMRR) :

CMRR of a practical OP-AMP is not ∞ . However it is very high. For IC 741, the CMRR is 90 dB or 31622. Such a high CMRR helps to reject the common mode signals such as noise, successfully. In absence of the input offset voltage, the OP-AMP should respond only to the differential input voltage V_d. But a practical OP-AMP is sensitive to the common mode input $V_{CM} = (V_1 + V_2) / 2$.

$$\therefore \quad V_o = A_d V_d + A_{CM} V_{CM}$$

where A_d = Differential gain and A_{CM} = Common mode gain.

$$\therefore \quad V_o = A_d (V_1 - V_2) + A_{CM} V_{CM} = \left[(V_1 - V_2) + \frac{A_{CM}}{A_d} V_{CM} \right] A_d$$

But (A_{CM} / A_d) = CMRR.

$$\therefore \quad V_o = \left[V_1 - V_2 + \frac{V_{CM}}{CMRR} \right] A_d$$

Supply Voltage Rejection Ratio (SVRR) :

The change in an OP-AMPs input offset voltage (V_{ios}) due to variation in the supply voltage is called as Power Supply Rejection Ratio (PSRR). It is also called as Supply Voltage Rejection Ratio (SVRR) or Power Supply Sensitivity (PSS). Mathematically PSRR is expressed as,

$$PSRR = \frac{\Delta V_{ios}}{\Delta V}$$

where, ΔV_{ios} = Change in input offset voltage and ΔV = Change in the supply voltage.

PSRR is expressed either in microvolts per volt or in decibels. For IC 741C, PSRR = 150 μV/V. The value of PSRR should ideally be equal to zero and practically it should be as small as possible. SVRR is specified assuming that both supply (positive and negative) magnitudes increasing or decreasing simultaneously.

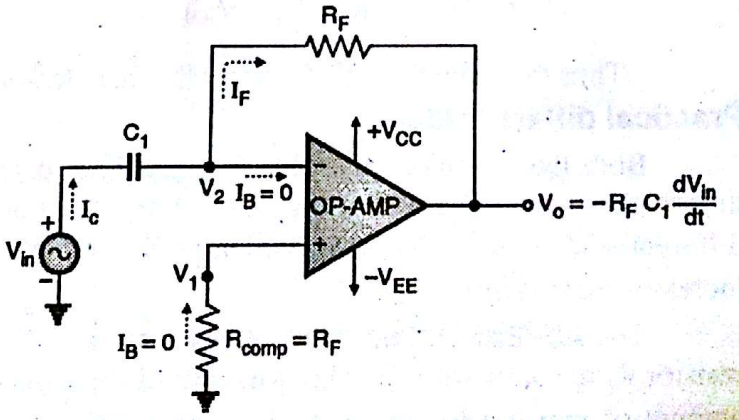
Q. 4(a) Explain ideal as well as practical differentiator using operational amplifier in detail. **(10 Marks)**

Ans. : Ideal differentiator :

The differentiator or differentiating amplifier is as shown in Fig. 5(a).

This circuit will perform the mathematical operation of differentiation on the input voltage waveform and the output is a derivative of the input signal.

The differentiator can be constructed from the basic inverting amplifier by replacing resistance R_1 by capacitor C_1 as shown in Fig. 5(a).



(K-59) **Fig. 5(a) : Basic or Ideal differentiator circuit**

The resistance R_{comp} connected from the non-inverting terminal to ground provides the bias compensation.

Expression for the output voltage :

Assume that an ideal OP-AMP is being used. Hence $V_2 = 0, I_B = 0$

$$V_2 = 0, I_B = 0$$

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Referring to Fig. 5(a) we can write that,

$$I_C = I_B + I_F$$

But since $I_B \approx 0$ the above equation gets modified to,

$$I_C = I_F$$

We know that, $I_C = C\dfrac{d\,V_c}{dt}$

$$I_C = C\frac{d\,V_c}{dt} \quad ...(5)$$

The voltage across C_1 is given by,

$$V_c = V_{in} - V_2 \quad ...(6)$$

Substituting this into Equation (3) we get,

$$I_f = C_1\frac{d}{dt}(V_{in} - V_2) \quad ...(7)$$

Now, obtain the expression for the current I_F.

$$I_F = \frac{V_2 - V_o}{R_F} \quad ...(8)$$

But I_C and I_F are equal because $I_B = 0$ as shown in Fig. 5(a). Therefore, equating the Equations (6) and (7) we get,

$$C_1\frac{d}{dt}(V_{in} - V_2) = \frac{V_2 - V_o}{R_F} \quad ...(9)$$

Using the concept of virtual ground we can write that,

$$V_1 = V_2 = 0 \quad ...(10)$$

Substituting $V_1 = V_2 = 0$ into Equation (8) we get,

$$C_1\frac{d}{dt}(V_{in}) = \frac{-V_o}{R_F}$$

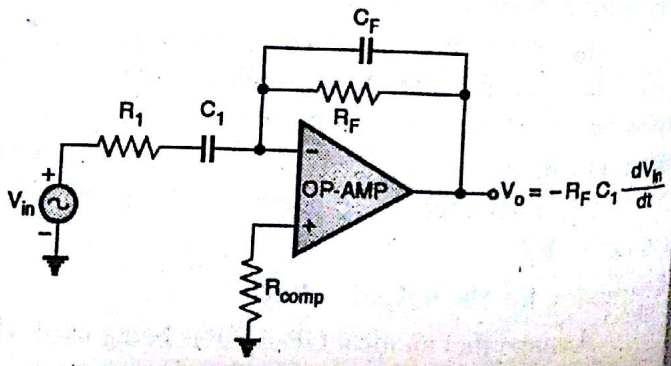
$$\therefore\ V_o = -R_F C_1\frac{d}{dt}(V_{in})$$

Thus the output is $-R_F C_1$ times the time derivative of the input voltage

Practical differentiator :

Both the instability and high frequency noise problems can be corrected by using the practical differentiator circuit shown in Fig. 5(b). Two components i.e. R_1 and C_F have been added to the basic differentiator circuit. Due to reduction in X_{C1} at high frequencies, the gain of the basic differentiator increases drastically.

To stabilize it, we have connected a resistor R_1 in series with C_1. This will control the amount of increase in gain at high frequencies. So the problem of instability is taken care of. In absence of R_1, the gain of differentiator would be so high (at high frequencies) that the noise will completely override the signal. Due to inclusion of R_1 this is avoided.



(K-261) **Fig. 5(b) : Practical differentiator circuit**

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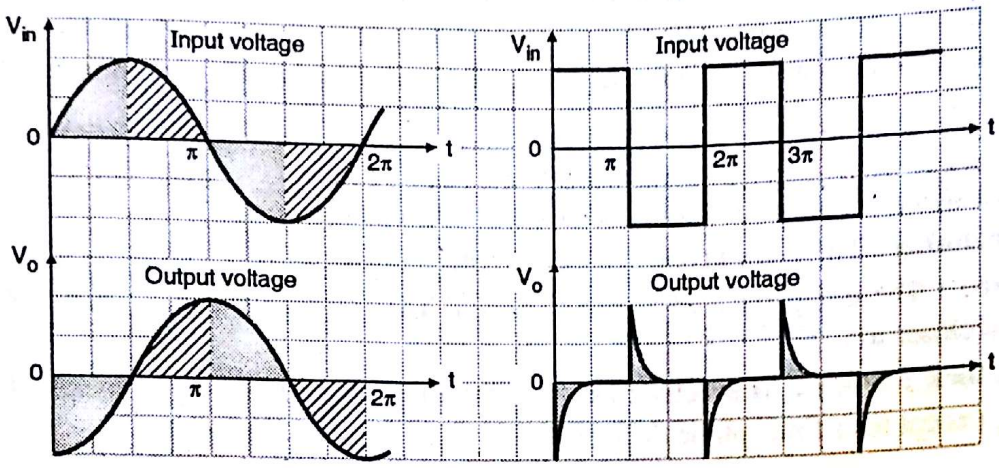
The resistor R_{comp} has been used for bias compensation. The value of R_{comp} should ideally be,

$$R_{comp} = R_1 \parallel R_F \approx R_1 \quad \text{as} \quad R_F >> R_1 \qquad ...(11)$$

The output voltage waveforms of a practical differentiator for different types of input voltages are shown in Fig. 5(c). A sinewave input produces a negative cosine wave at the output and a square wave input produces positive and negative spikes. The waveforms in Fig. 5(c) are drawn for $R_F C_1 = 1$sec.



(K-262) **Fig. 5(c) : Input and output voltage waveforms of a differentiator**

Expression for output voltage of practical differentiator :

The expression for output voltage of a practical differentiator is same as that of the ideal differentiator.

Chapter 3 : Phase Locked Loop (PLL) [Total Marks : 10]

Q. 6(a) Explain PLL as a frequency synthesizer. **(5 Marks)**

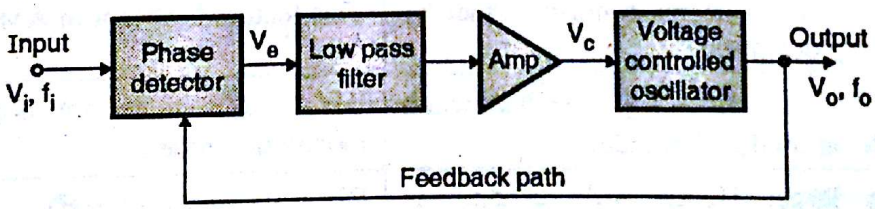
Ans. : Please refer Q.1(b) of Dec. 2013.

Q. 6(b) Explain operating principle of PLL. **(5 Marks)**

Ans. : Phase Locked Loop (PLL) :

As shown in this Fig. 6 the phase locked loop consists of :

1. A phase detector or phase comparator
2. A low pass filter
3. An error amplifier
4. A voltage controlled oscillator (VCO).



(K-831) **Fig. 6 : A basic phase locked loop**

Operation of PLL :

Phase detector / Comparator :

The two inputs to a phase detector or comparator are the input voltage V_s at frequency f_s and the feedback voltage from a voltage controlled oscillator (VCO) at frequency f_o. The phase detector compares these two signals and produces a d.c. voltage V_e which is proportional to the phase difference between f_s and f_o. The output voltage V_e of the phase detector is called as "error voltage". This error voltage is then applied to a low pass filter.

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Low pass filter :

The low pass filter removes the high frequency noise present in the phase detector output and produces a ripplefree dc level. This dc level is amplified to an adequate level and applied to a voltage controlled oscillator. The dc amplifier output voltage is called as the control voltage V_C.

Voltage Controlled Oscillator (VCO) :

The control voltage V_c is applied at the input of a VCO. The output frequency of VCO is directly proportional to the dc control voltage V_c. The VCO frequency "f_o" is compared with the input frequency "f_s" by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency f_s i.e.

$$f_o = f_s$$

The three states of operation through which the VCO undergoes are :

(1) **Free running :** There is no control on VCO output frequency f_o.

(2) **Capture :** The comparison of f_o and f_s begins. The control voltage V_c starts adjusting f_o to bring it closer to f_s.

(3) **Phase lock :** When f_o is exactly equal to f_s the PLL is said to be phase locked. Once locked, $f_o = f_s$ except for a finite phase difference ϕ.

Chapter 4 : Modulation [Total Marks : 25]

Q. 1(d) Compare FM and AM. **(5 Marks)**

Ans. : Comparison between FM and AM :

Sr. No.	FM	AM
1.	Amplitude of FM wave is constant. It is independent of the modulation index.	Amplitude of AM wave will change with the modulating voltage.
2.	Hence transmitted power remains constant. It is independent of m_f.	Transmitted power is dependent on the modulation index.
3.	All the transmitted power is useful.	Carrier power and one sideband power are useless.
4.	FM receivers are immune to noise.	AM receivers are not immune to noise.
5.	It is possible to decrease noise further by increasing deviation.	This feature is absent in AM.
6.	Bandwidth = 2 [$\delta + f_m$]. The bandwidth depends on modulation index.	BW = $2f_m$. It is not dependent on the modulation index.
7.	BW is large. Hence wide channel is required.	BW is much less than FM.
8.	Space wave is used for propagation. So radius of transmission is limited to line of sight.	Ground wave and sky wave propagation is used. Therefore larger area is covered than FM
9.	Hence it is possible to operate several transmitters on same frequency.	Not possible to operate more channels on the same frequency.
10.	FM transmission and reception equipment are more complex.	AM equipments are less complex.

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Q. 3(a) Explain amplitude modulation for more than one modulating signal in following cases :

1. Mathematical equation
2. AM waveform
3. Modulation coefficient
4. Transmission power

(10 Marks)

Ans. :

1. Mathematical equation :

Assume that there are two modulating signals.

$$x_1(t) = E_{m1} \cos \omega_{m1} t$$

and $$x_2(t) = E_{m2} \cos \omega_{m2} t$$

The total modulating signal will be the sum of these two in the time domain.

$$\therefore \text{Total modulating signal} = x_1(t) + x_2(t) = E_{m1} \cos \omega_{m1} t + E_{m2} \cos \omega_{m2} t$$

Let the carrier be $c(t) = E_c \cos \omega_c t$

The instantaneous value of the envelope of AM wave is,

$$A = E_c + x_1(t) + x_2(t) = E_c + E_{m1} \cos \omega_m t + E_{m2} \cos \omega_{m2} t$$

Therefore the AM wave is given by,

$$e_{AM} = A \cos \omega_c t$$

It can be proved that the expression for the DSBFC AM wave is given by,

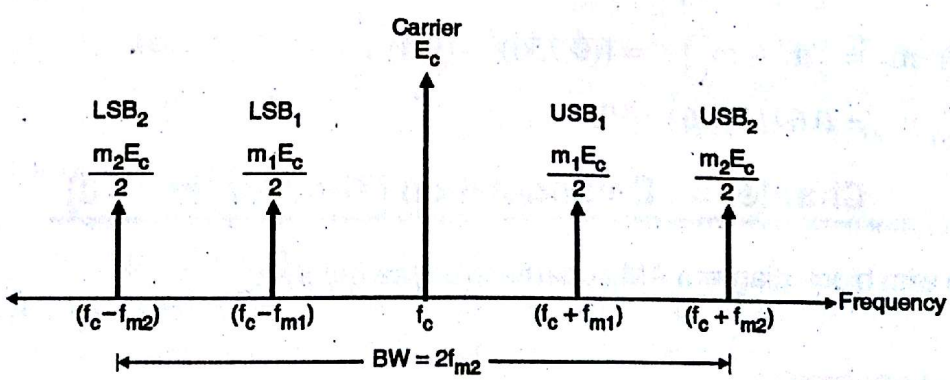
$$e_{AM} = E_c \cos \omega_c t + \frac{m_1 E_c}{2} \cos(\omega_c + \omega_{m1}) t + \frac{m_1 E_c}{2} \cos(\omega_c - \omega_{m1}) t$$

$$+ \frac{m_2 E_c}{2} \cos(\omega_c + \omega_{m2}) t + \frac{m_2 E_c}{2} \cos(\omega_c - \omega_{m2}) t \quad \text{...(1)}$$

Where m_1 and m_2 are the modulation indices corresponding to the two modulating signals $x_1(t)$ and $x_2(t)$ respectively

Equation (1) shows that in the AM wave along with carrier there are four sideband components. There are two USB components at frequencies $(f_c + f_{m1})$ and $(f_c + f_{m2})$ and two LSB components at frequencies $(f_c - f_{m1})$ and $(f_c - f_{m2})$. The frequency spectrum of AM wave is as shown in Fig. 7.

2. AM waveform :



(D-66) **Fig. 7 : Frequency spectrum of AM wave with two modulating signals**

3. Effective modulation index (m_t) :

In general the total modulation index due to the simultaneous modulation by "n" modulating signals is given by,

$$m_t = [m_1^2 + m_2^2 + \ldots\ldots m_n^2]^{1/2}$$

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4. Total Power (P_t) :

The total power in AM wave with a complex modulating signal is given by,

$$P_t = P_c\left[1 + \frac{m_1^2}{2} + \frac{m_2^2}{2} \ldots\ldots + \frac{m_n^2}{2}\right]$$

Q. 4(b) The antenna current of an AM broadcast transmitter, modulated to a depth of 40% by an audio sine wave is 11 A. It increases to 12 A as result of simultaneous modulation by another audio sine wave. What is the modulation index due to this second wave? **(10 Marks)**

Ans. :

Given : $I_{t1} = 11$ A, $m_1 = 0.4$, $I_{t2} = 12$ A

To find : Modulation index due to second wave.

Step 1 : Find I_c :

$$\left[\frac{I_{t1}}{I_c}\right]^2 = 1 + \frac{m_1^2}{2}$$

$$\therefore\ I_c = \frac{I_{t1}}{\left[1 + \frac{m_1^2}{2}\right]^{1/2}} = \frac{11}{\left[1 + \frac{(0.4)^2}{2}\right]^{1/2}} = 10.58 \text{ A}$$

Step 2 : Find m_t :

After modulating with the second signal,

$$I_{t2}^2 = I_c^2\left[1 + \frac{m_t^2}{2}\right]$$

$$m_t = \sqrt{2\left[\left(\frac{I_{t2}}{I_c}\right)^2 - 1\right]} = \sqrt{2\left[\left(\frac{12}{10.58}\right)^2 - 1\right]}$$

$$\therefore\ m_t = 0.756$$

Step 3 : Find m_2 :

$$m_t = \left[m_1^2 + m_2^2\right]^{1/2}$$

$$\therefore\ m_2 = \left[m_t^2 - m_1^2\right]^{1/2} = [(0.756)^2 - (0.4)^2]^{1/2}$$

$$\therefore\ m_2 = 0.6415 = \mathbf{64.15\%}$$

Chapter 5 : Demodulation [Total Marks : 10]

Q. 3(b) Explain with block diagram AM superheterodyne receiver. **(10 Marks)**

Ans. :

Superhetrodyne receiver :

The radio and TV receivers operate on the principle of superheterodyning. The block diagram of a superheterodyne radio receiver is shown in Fig. 8(a).

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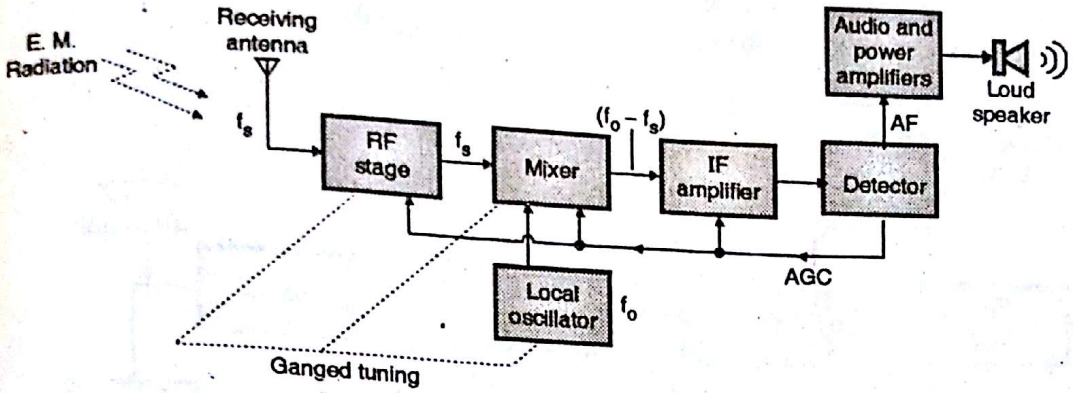

(D-230) **Fig. 8(a) : The superheterodyne receiver**

Operation of superheterodyne receiver :

1. The DSBFC or AM signal transmitted by the transmitter travels through the air and reaches the receiving antenna. This signal is in the form of electromagnetic waves. It induces a very small voltage (few μV) into the receiving antenna.
2. **RF stage :** The RF stage is an amplifier which is used to select the wanted signal and reject other out of many, present at the antenna. It also reduces the effect of noise. At the output of the RF amplifier we get the desired signal at frequency "f_s".
3. **Mixer:** The mixer receives signals from the RF amplifier at frequency (f_s) and from the local oscillator at frequency (f_o) Such that $f_o > f_s$.
4. **Intermediate frequency (IF) :** The mixer will mix these signals to produce signals having frequencies f_s, f_o, $(f_o + f_s)$ and $(f_o - f_s)$. Out of these the difference of frequency component i.e. $(f_o - f_s)$ is selected and all others are rejected. This frequency is called as the intermediate frequency (IF).

$$\therefore \text{ I.F. } = (f_o - f_s)$$

This frequency contains the same modulation as the original signal f_s.

5. In order to maintain a constant difference between the local oscillator frequency and the incoming frequency, ganged tuning is used. This is simultaneous tuning of RF amplifier, mixer and local oscillator and it is achieved by using ganged tuning capacitors (Tuning control in radio set).
6. This intermediate frequency signal is then amplified by one or more IF amplifier stages. IF amplifiers provide most of the gain (and hence sensitivity) and the bandwidth requirements of the receiver. Therefore the sensitivity and selectivity of this receiver do not change much with changes in the incoming frequency.
7. The amplified IF signal is detected by the detector to recover the original modulating signal. This is then amplified and applied to the loudspeaker.
8. AGC means automatic gain control. This circuit controls the gains of the RF and IF amplifiers to maintain a constant output voltage level even when the signal level at the receiver input is fluctuating. This is done by feeding a controlling dc voltage to the RF and IF amplifiers. The amplitude of this dc voltage is proportional to the detector output.

Waveforms at various points of a superheterodyne receiver :

The waveforms at different points of a superheterodyne receivers are as shown in Fig. 8(b). The selected signal is amplified by the RF amplifier. Hence the waveform at its output is an amplified AM signal Local oscillator produces a sinusoidal signal of frequency f_o. Where $f_o = f_s$ + IF. At the mixer output we get an AM signal with IF acting as a carrier. The same signal is then available in the

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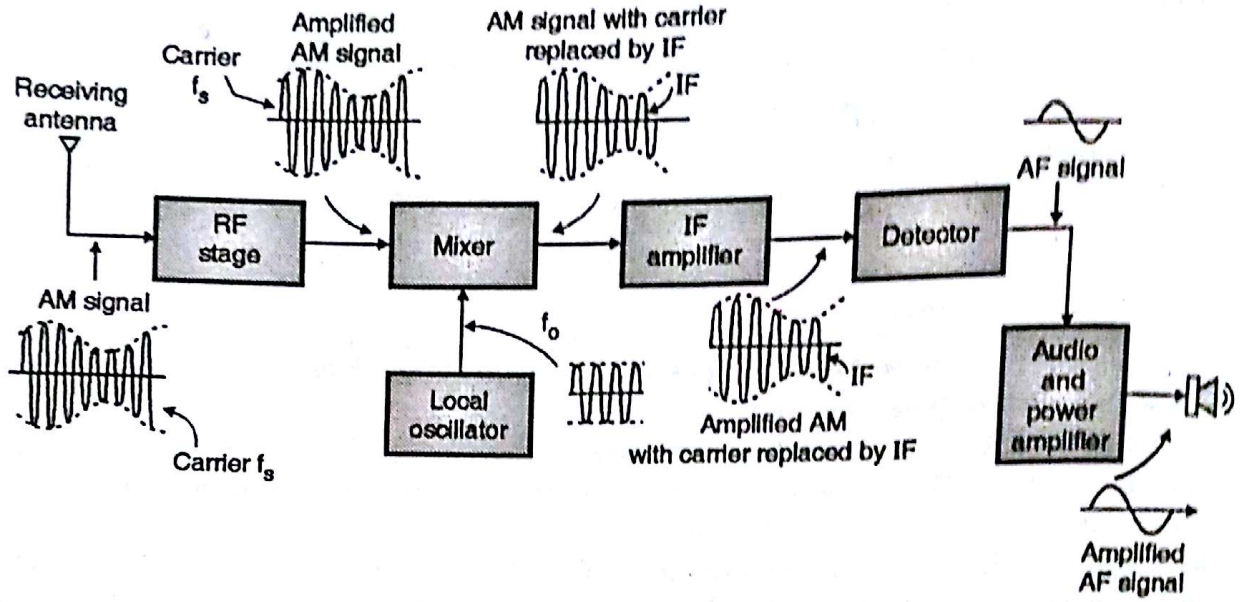
amplified form at the output of the IF amplifier. This waveform is applied to a detector, which removes the IF and produces an AF signal at the detector output. This AF signal is amplified by the audio and power amplifier. Hence we get the amplified version of the AF signal.



(D-232) **Fig. 8(b) : Superheterodyne receiver with waveforms shown at intermediate points**

Chapter 6 : Analog Pulse Modulation [Total Marks : 10]

Q. 5(a) State sampling theorem. What happens if the sampling is done at less than 2 f_{max}. **(10 Marks)**

Ans. : Sampling theorem for low pass signal :

Statement :

A continuous time signal x (t) can be completely represented in its sampled form and recovered back from the sampled form if the sampling frequency $f_s \geq 2W$ where "W" is the maximum frequency of the continuous time signal x (t).

Aliasing or Foldover error :

If the signal x (t) is not strictly bandlimited and / or if the sampling frequency f_s is less than 2W, then an error called aliasing or foldover error is observed. The adjacent spectrums overlap if $f_s < 2W$. This is shown in Fig. 9(b). The signal x (t) is not strictly bandlimited. The spectrum of signal x(t) is shown in Fig. 9(b). The spectrum X_δ (f) of the discrete time signal x_δ (t) is shown in Fig. 9(b) which is nothing but the sum of X (f).

Consider the two replicas of X (f) which are centered about the frequencies f_s and $-f_s$. If we use a reconstruction filter with its pass-band extending from $-f_s / 2$ to $+f_s / 2$ then its output will not be an undistorted version of the original signal x (t). Some distortion will be present in the filter output. The distortion occurs due to the overlapping of the adjacent spectrums as shown in Fig. 9(b).

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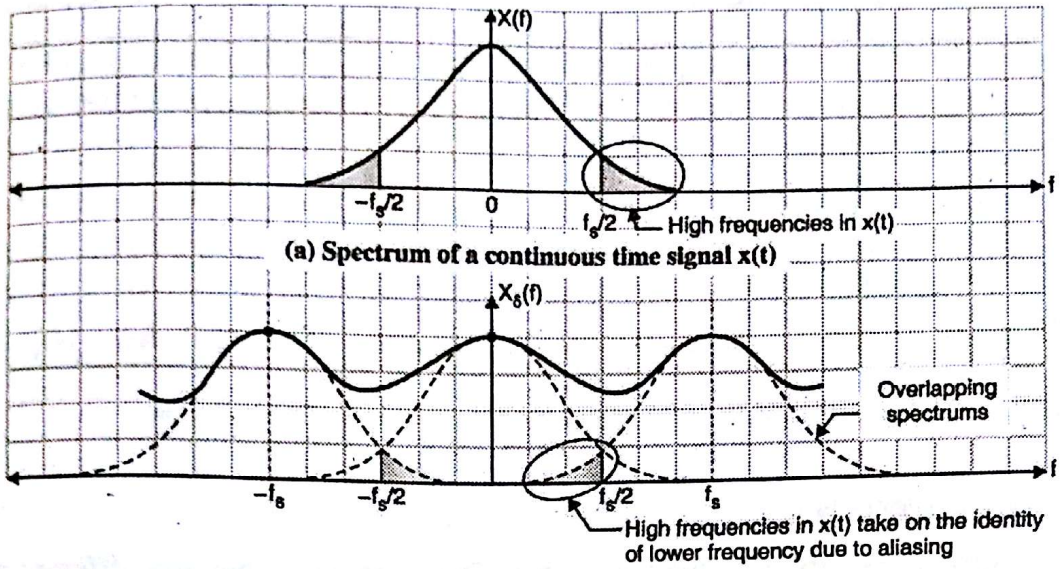


(b) Spectrum of the sampled version of x(t) with $f_s < 2W$

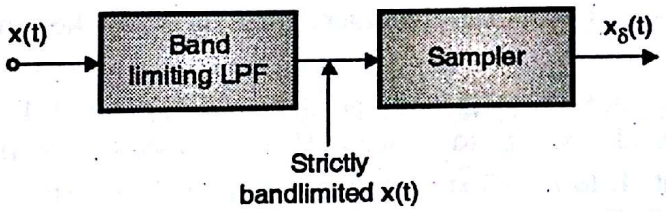
(D-415) **Fig. 9**

Due to this overlapping, it is seen that the portions of the frequency shifted replicas are "folded over" inside the desired spectrum. Due to this "fold over", high frequencies in X (f) are reflected into low frequencies in X_δ (f). This can be understood by comparing the shaded portions of the spectra shown in Figs. 9(a) and (b).

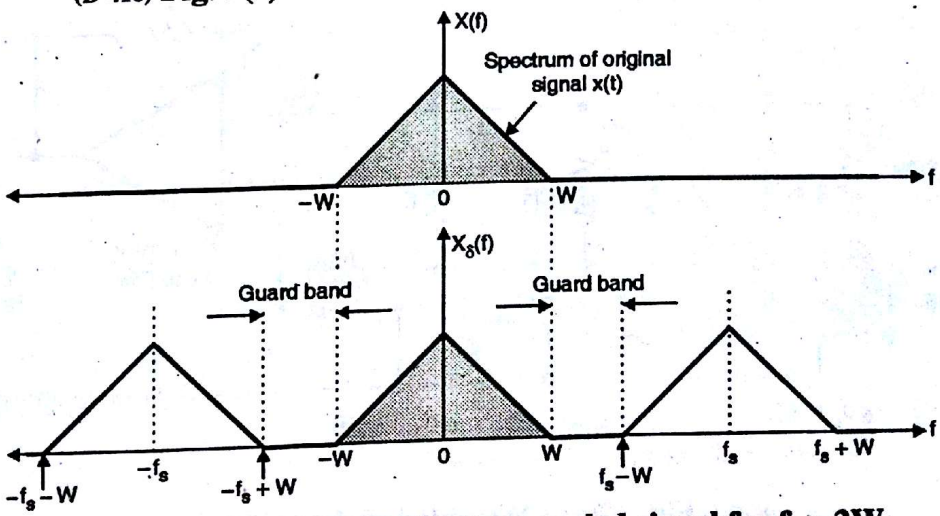
Effect of aliasing :

Due to aliasing some of the information contained in the original signal x (t) is lost in the process of sampling. Aliasing can be completely eliminated if we take the following action :

Use a bandlimiting low pass filter and pass the signal x (t) through it before sampling as shown in Fig. 9(c). This filter has a cutoff frequency at $f_c = W$, therefore it will strictly bandlimit the signal x (t) before sampling takes place. This filter is also called as antialiasing filter or prealias filter.



(D-416) **Fig. 9(c) : Use of a bandlimiting filter to eliminate aliasing**



(D-417) **Fig. 9(d) : Spectrum of a sampled signal for $f_s > 2W$**

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Increase the sampling frequency f_s to a great extent i.e. $f_s >>> 2W$. Due to this, even though $x(t)$ is not strictly bandlimited, the spectrums will not overlap. A guard band is created between the adjacent spectrums as shown in Fig. 9(d).

Thus aliasing can be prevented by :

1. Using an antialiasing or prealiasing filter and
2. Using the sampling frequency $f_s > 2W$.

Chapter 7 : Digital Modulation Techniques [Total Marks : 10]

Q. 6(c) List different types of ADC's and explain binary weighted ADC in detail. **(10 Marks)**

Ans. :

Types of A to D converters :

There are various circuits available for the A to D conversions. They use different principles of operation for conversion. Some of them are :

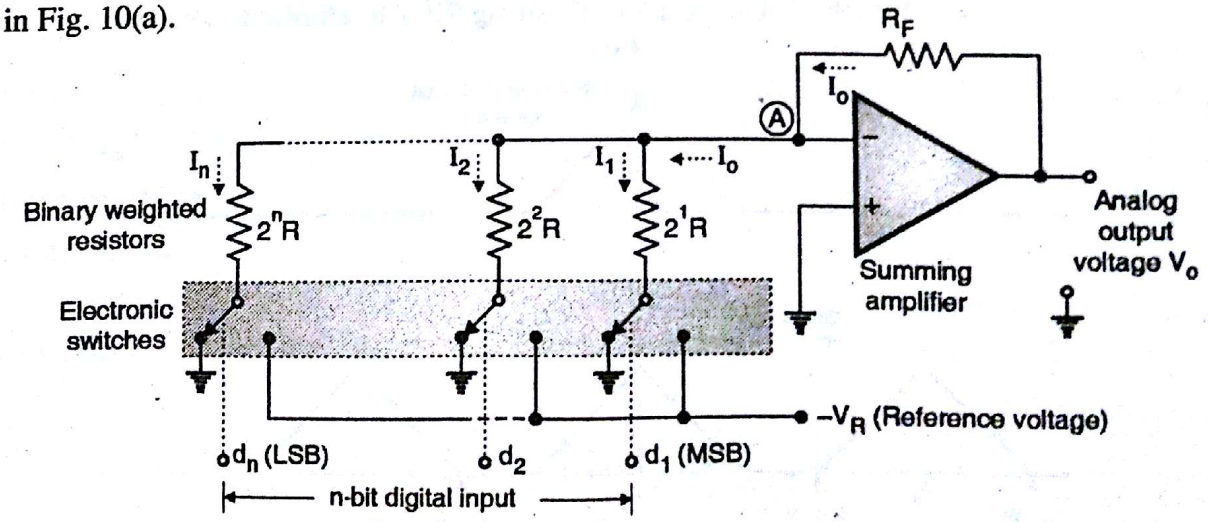
1. Flash type or simultaneous ADC
2. Tracking or servo type
3. Single slope A to D converter
4. Counter type ADC
5. Successive approximation A to D converter
6. Dual slope A to D converter (Integrator type)

Binary weighted resistor DAC :

The circuit diagram of binary weighted resistor type DAC is as shown in Fig. 10(a). This circuit uses a resistive network of binary weighted resistors followed by a summing amplifier. The resistors $2^1 R, 2^2 R \ldots, 2^n R$ are from the network of binary weighted resistors. There are "n" number of electronic switches used, one per digital bit. They are Single Pole Double Throw (SPDT) type switches. The position of the moving arm of a switch is controlled by the binary input bit applied to it.

For example, if the binary bit $d_1 = 1$, then the first SPDT switch will connect resistor 2^1R to a negative reference voltage ($-V_R$) and when the binary input d_1 is "0" then this switch will connect this resistor to ground.

Thus an n-bit digital word will decide the positions of all the SPDT switches and connect their corresponding binary weighted resistors to either $-V_R$ or ground. Depending upon the positions of various switches, the currents I_1 to I_n will start flowing through the resistors 2^1R to 2^nR respectively as shown in Fig. 10(a).



(K-582) **Fig. 10(a) : Weighted resistor DAC**

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Expression for analog output voltage :

Let the n-bit digital input word to the DAC be $d_1\ d_2 \ldots d_n$ with d_1 as MSB (Most Significant Bit) and d_n as LSB (Least Significant Bit). Let R_F be the feedback resistor and I_o be the output current. Let the OP-AMP in Fig. 10(a) be an ideal OP-AMP so that the current flowing into its input terminals is zero due to infinite input resistance. Assuming the OP-AMP of Fig. 10(a) to be ideal, the output current I_o can be expressed as the sum of individual currents through the weighted resistors.

$$\therefore\ I_o = I_1 + I_2 + \ldots\ldots + I_n = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots\ldots + \frac{V_R}{2^n R} d_n \qquad \ldots(1)$$

$d_1, d_2, \ldots\ldots, d_n$ can have a value of either "0" or "1".

$$\therefore\ I_o = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n}\right] \qquad \ldots(2)$$

The output voltage V_o is given by,

$$V_o = I_o R_F = V_R \cdot \frac{R_F}{R}\left[d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n}\right] \qquad \ldots(3)$$

This is the required expression for output voltage. Now comparing Equations (2) and (3),

$$K = \frac{R_F}{R} \text{ and } V_{FS} = V_R.$$

So if $R_F = R$ then $K = 1$.

$$_o = V_R\left[d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots + d_n 2^{-n}\right] \qquad \ldots(4)$$

By substituting the values of d_1, d_2 ..... d_n in Equation (3) we can obtain the value of corresponding analog output voltage V_o.

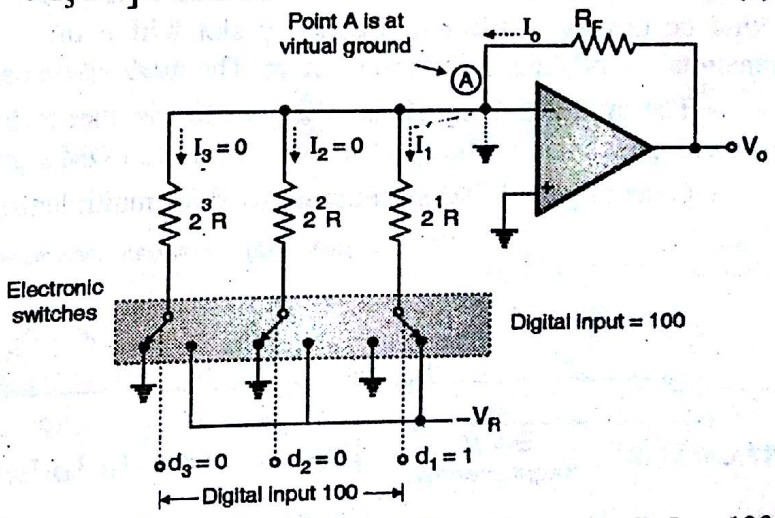
Output voltage waveform of a 3-Bit DAC :

The circuit of DAC shown in Fig. 10(a) uses an "inverting" summing amplifier. Therefore the use of a negative reference voltage ($-V_R$) gives a positive analog output voltage. Now to plot the output voltage V_o, we are going to use Equation (3). In this equation substitute $K = (R_F / R) = 1$ and $n = 3$.

That means the digital word at the DAC input is 3-bit long.

$$\therefore\ V_o = V_R\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right] \qquad \ldots(5)$$

Calculate V_o for any one combination of $d_1\ d_2\ d_3$. Let $d_1\ d_2\ d_3 = 100$, then the equivalent circuit of DAC is as shown in Fig. 10(b). The two switches corresponding to the inputs d_2 and d_3, connect the resistors 2^2R and 2^3R to ground. As point A is at virtual ground potential, the currents I_2 and I_3 will be equal to zero as shown in Fig. 10(b).



(K-583) **Fig. 10(b) : Equivalent circuit of DAC for digital input $d_1\ d_2\ d_3 = 100$**

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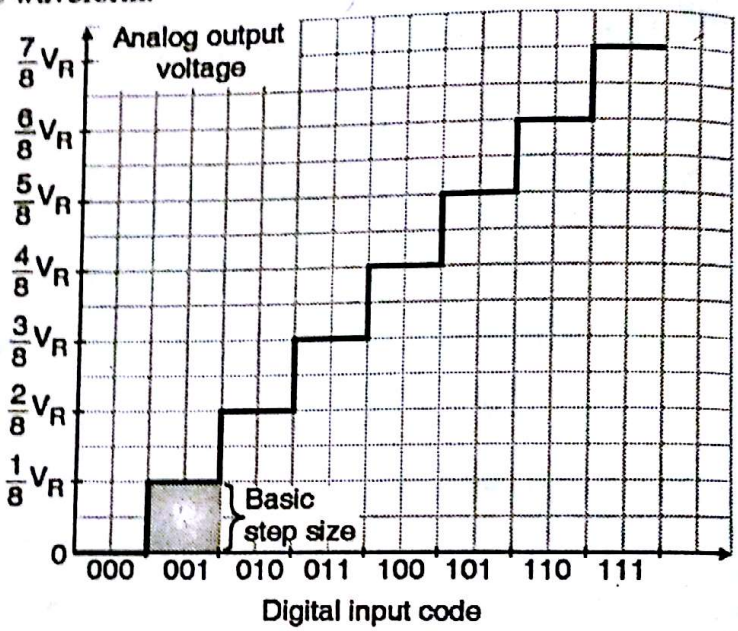
However the switch corresponding to d_1 will connect the resistor 2^1R to $-V_R$ and due to potential difference between A and $-V_R$, current I_1 will flow. Substituting the values of d_1, d_2 and d_3 into Equation (5) we can obtain the analog output voltage V_o as :

$$V_o = V_R\,[1\times 2^{-1}+0\times 2^{-2}+0\times 2^{-3}] = \frac{V_R}{2}$$

Similarly, we can obtain the output voltage for all the possible input digital words from 000 to 111, as shown in Table 1. The graph of digital input code versus output voltage V_o is plotted in Fig. 10(c). Thus the DAC output is a staircase waveform.

Table 1

Digital input			Analog output Voltage V_o
d_1	d_2	d_3	
0	0	0	0
0	0	1	$V_R/8$
0	1	0	$2\,V_R/8$
0	1	1	$3\,V_R/8$
1	0	0	$4\,V_R/8$
1	0	1	$5\,V_R/8$
1	1	0	$6\,V_R/8$
1	1	1	$7\,V_R/8$



(K-584) **Fig. 10(c) : Staircase output for DAC**

Chapter 8 : Multiplexing [Total Marks : 15]

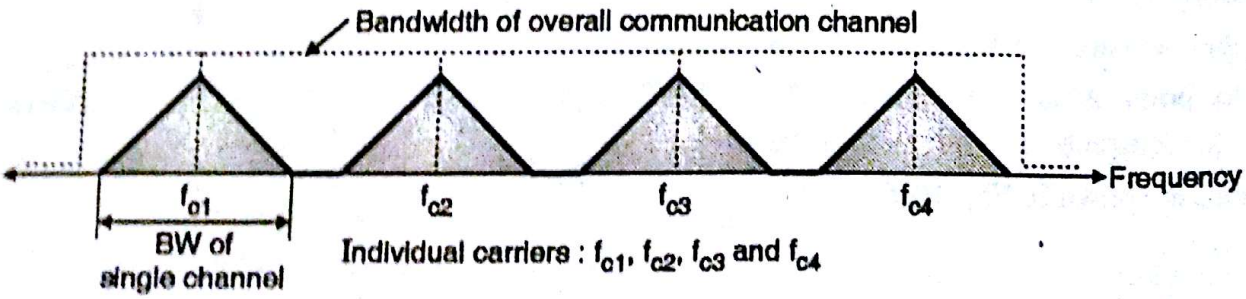
Q. 1(c) Explain principle of FDM. **(5 Marks)**

Ans.: Frequency Division Multiplexing (FDM) :

The operation of FDM is based on sharing the available bandwidth of a communication channel among the signals to be transmitted. That means many signals are transmitted simultaneously with each signal occupying a different frequency slot within the total available bandwidth. Each signal to be transmitted modulates a different carrier. The modulation can be AM, SSB, FM or PM.

The modulated signals are then added together to form a composite signal which is transmitted over a single channel. The spectrum of composite FDM signal is shown in Fig. 11(a).

Generally the FDM systems are used for multiplexing the analog signals.



(L-107) **Fig. 11(a) : Spectrum of FDM signal**

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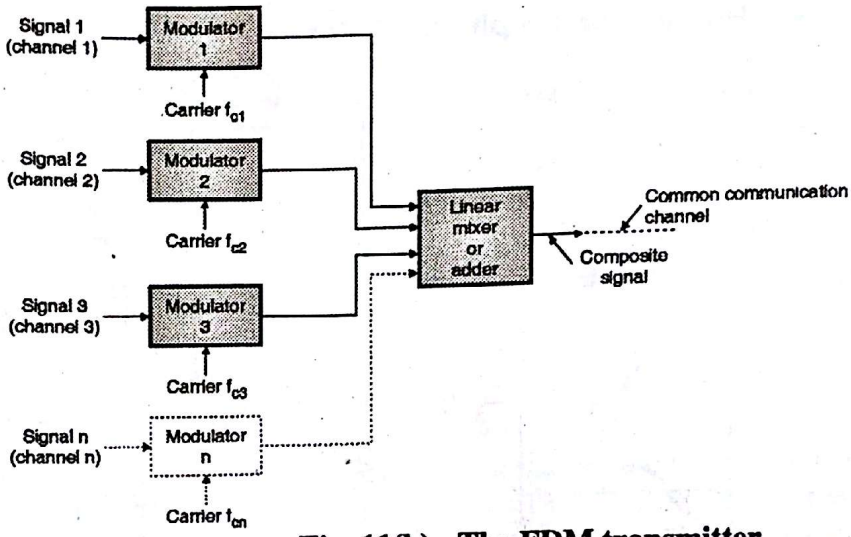
1. FDM transmitter :

Fig. 11(b) shows the block diagram of an FDM transmitter. The signals which are to be multiplexed will each modulate a separate carrier. The type of modulation can be AM, SSB, FM or PM. The modulated signals are then added together to form a complex signal which is transmitted over a single channel.

Each signal modulates a separate carrier. The modulator outputs will contain the sidebands of the corresponding signals. The modulator outputs are added together in a linear mixer or adder. The linear mixer is different from the normal mixers. Here the sum and difference frequency components are not produced.

But only the algebraic addition of the modulated outputs will take place. Different signals are thus added together in the time domain but they have their own separate identity in the frequency domain.

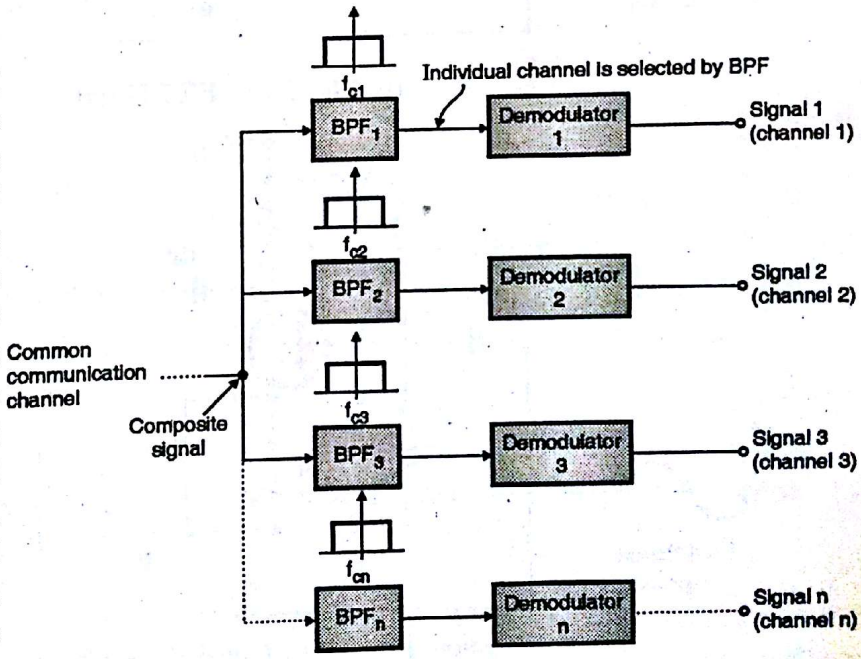
This is as shown in the Fig. 11(a). The composite signal at the output of mixer is transmitted over the single communication channel as shown in Fig. 11(b). This signal can be used to modulate a radio transmitter if the FDM signal is to be transmitted through air.



(L-108) **Fig. 11(b) : The FDM transmitter**

2. FDM receiver :

The block diagram of an FDM receiver is as shown in Fig. 11(c). The composite signal is applied to a group of band pass filters (BPF). Each BPF has a center frequency corresponding to one of the carriers used in the transmitter i.e. f_{c1}, f_{c2}, ... f_{cn} etc. The BPFs have an adequate bandwidth to pass all the channel information without any distortion. Each filter will pass through only its channel and reject all the other channels. Thus all the multiplexed channels are separated out. The channel demodulator then removes the carrier and recovers the original signal back.



(L-109) **Fig. 11(c) : FDM receiver**

Q. 5(b) What is multiplexing in communication system ? Draw black diagram of TDM-PCM system and explain ? **(10 Marks)**

Ans. : **Please refer Q. 5(a) of Dec. 2013.**

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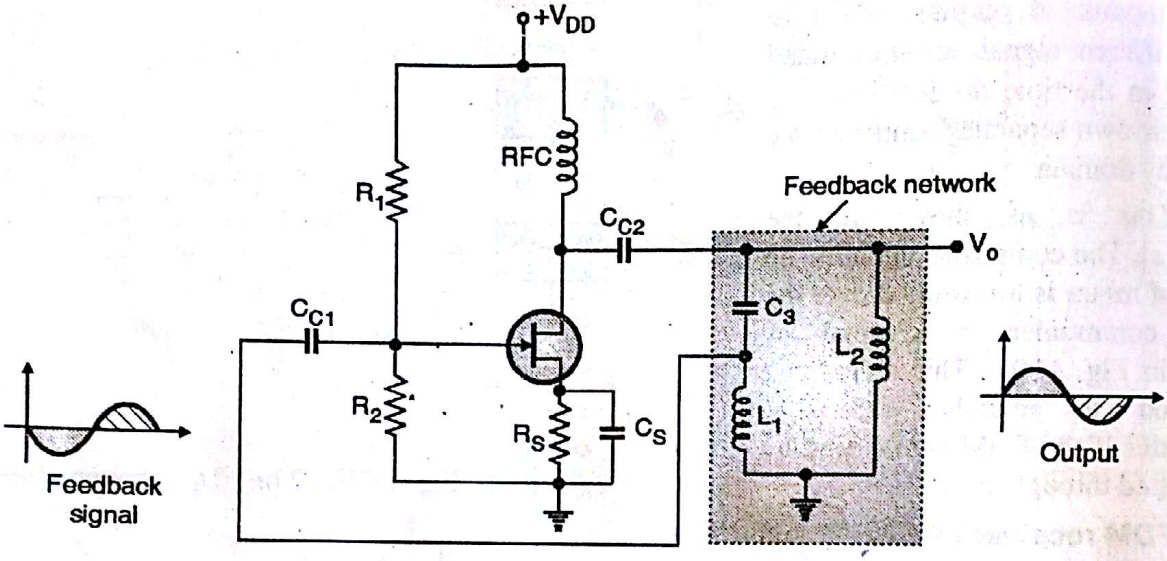
Dec. 2014

Chapter 1 : Electronic Circuits [Total Marks : 25]

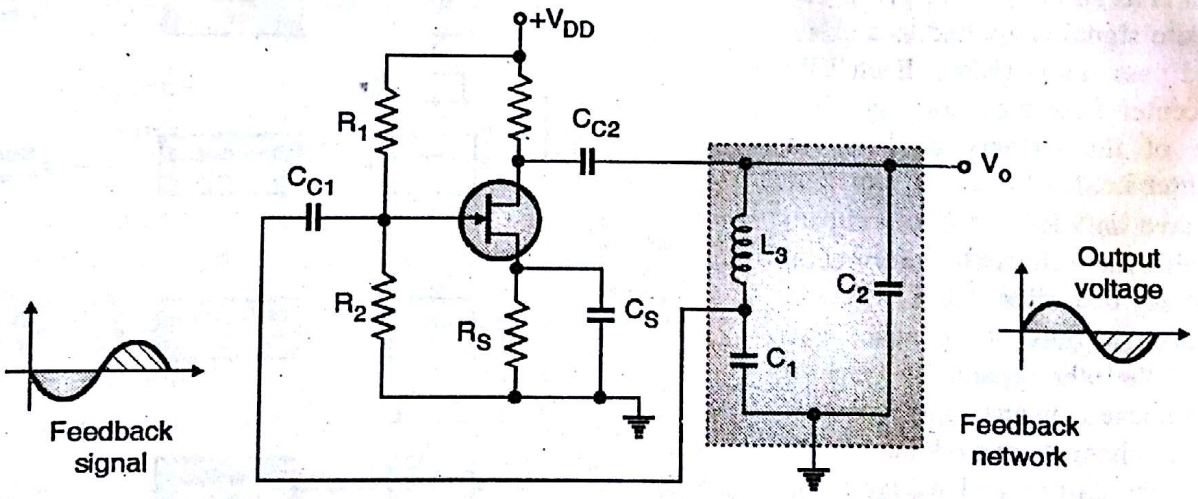
Q. 1(c) Draw FET based Hartley and Colpitt Oscillator. What is the frequency of oscillation if

1. $L_1 = 10$ mH, $L_2 = 10$ mH and $C = 0.1$ μF for Hartley tank circuit.
2. $L = 10$ mH, $C_1 = 0.1$μF and $C_2 = 0.1$ μF for Colpitt tank circuit. **(5 Marks)**

Ans. : Hartley and Colpitt oscillator :



(F-811) **Fig. 1(a) : FET Hartley oscillator**



(F-818) **Fig. 1(b) : Colpitt's oscillator using FET**

1. For Hartley tank circuit :

Given : $L_1 = L_2 = 10$ mH, $C = 0.1$ μF

The oscillator frequency for a Hartley oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}} = \frac{1}{2\pi\sqrt{0.1 \times 10^{-6}\,[(10 \times 10^{-3}) + (10 \times 10^{-3})]}} = \mathbf{3.558\ kHz}$$

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2. For Colpitt tank circuit :

Given : $L = 10$ mH, $C_1 = 0.1\ \mu F$, $C_2 = 0.1\ \mu F$

The oscillator frequency for a colpitt oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$\text{Where} \quad C = \frac{C_1 C_2}{C_1 + C_2} = \frac{(0.1 \times 0.1)}{(0.1 + 0.1)} = 5 \times 10^{-8}\ F$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{10 \times 10^{-3} \times 5 \times 10^{-8}}} = \mathbf{7.117\ kHz}$$

Q. 2(a) With proper circuit diagrams and transfer characteristics indicating Q-points do comparison of JFET bias circuits in detail. **(10 Marks)**

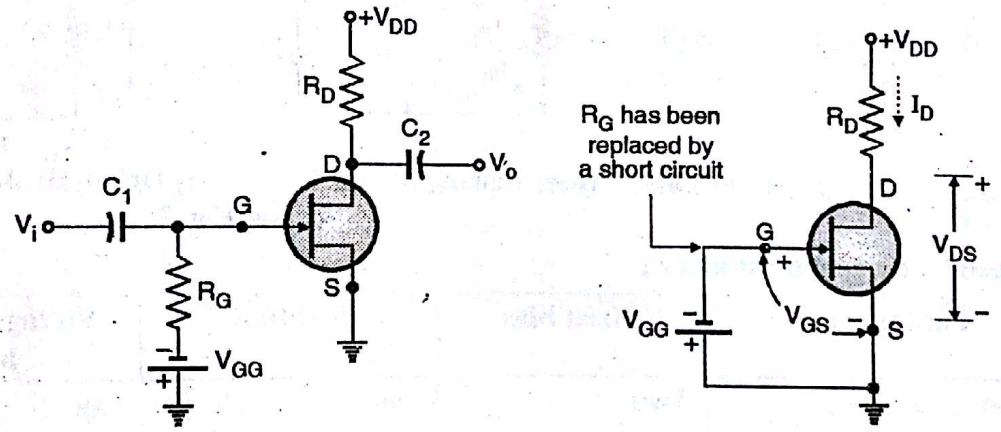
Ans. : JFET biasing :

Biasing is a process of applying external dc voltages of appropriate amplitudes and polarities to various terminals of FET. Biasing is essential to operate the FET in the desired region of operation such as cut off, saturation or ohmic regions.

The commonly used biasing circuits for FET are :

1. Fixed bias configuration :

The simplest biasing arrangement for the n-channel JFET is fixed bias configuration as shown in Fig. 2(a). The capacitors C_1 and C_2 are the coupling capacitors which are used for coupling the ac signal to the input of the circuit and amplified ac signal from the output of the circuit. However for the dc analysis, these capacitors are equivalent to "open circuits".



(a) Fixed bias configuration for n channel JFET **(b) Simplified fixed bias configuration for dc analysis**

(F-1650(a)) **Fig. 2**

For dc analysis $I_G = 0$. Therefore the voltage drop across R_G i.e. $I_G R_G = 0$. This will allow us to replace R_G by a short circuit for the dc analysis. The simplified fixed bias configuration used for the dc analysis is as shown in Fig. 2(b).

2. Self bias configuration :

The self bias configuration for FET is as shown in Fig. 2(c). This configuration needs only one dc power supplies. This is its advantage over the fixed bias circuit.

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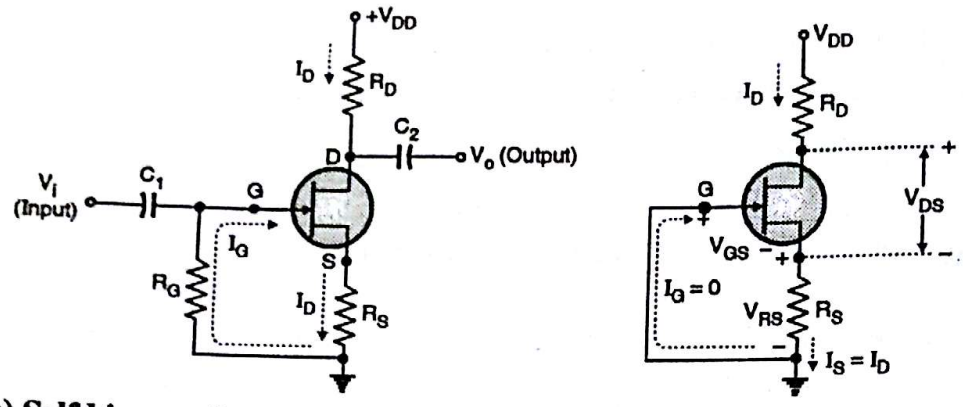


(c) Self bias configuration (d) Simplified DC equivalent circuit

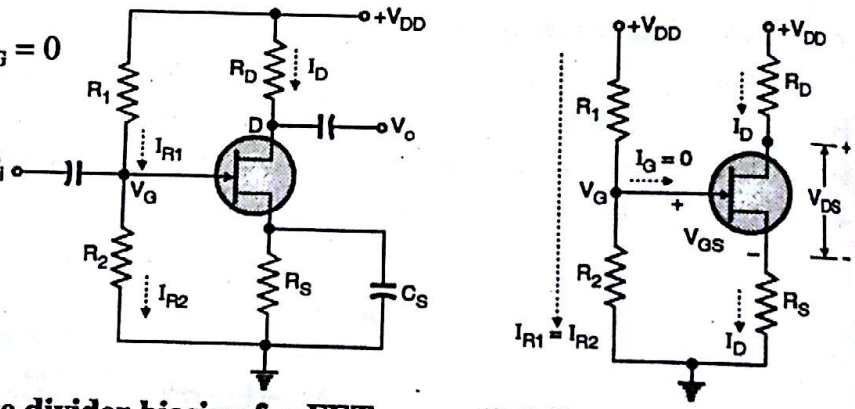
(F-1656) Fig. 2

3. Voltage Divider Biasing For a JFET :

The voltage divider biasing for a JFET amplifier is as shown in Fig. 2(e). This configuration is exactly same as the one used for biasing the transistor but its dc analysis will be entirely different. In the dc analysis of this circuit assume that $I_G = 0$. The coupling capacitors C_1, C_2 and C_S are assumed to be "open circuit" for the dc analysis. In addition the source voltage V_{DD} is separated into two equivalent sources. The simplified voltage divider biasing circuit for dc analysis is as shown in Fig. 2(f). As shown in Fig. 2(f) we can write that,

$$I_{R1} = I_{R2} \quad \text{because} \quad I_G = 0$$

$$\text{and} \quad I_{R1} = I_{R2} = \frac{V_{DD}}{(R_1 + R_2)}$$



(e) Voltage divider biasing for FET (f) DC equivalent circuit

(F-1669) Fig. 2

4. Comparison of biasing techniques :

Sr. No.	Parameter	Fixed bias	Self bias	Voltage divider bias
1.	Number of dc power supplies	Two	One	One
2.	Expression for V_{GS}	$V_{GS} = -V_{GG}$	$V_{GS} = -I_D R_S$	$V_{GS} = V_G - I_D R_S$
3.	Source resistance	Absent	Present	Present
4.	Negative feedback	Absent	Present	Present
5.	Bias stabilization	Cannot be provided	Better than fixed bias	Better than self bias.

Q. 3(a) Sketch a block representation for an n-channel JFET, showing bias voltages, depletion regions, and current directions. Label the device terminals and explain its operation. Explain the effect of increasing levels of negative gate-source voltage. Also sketch a typical drain characteristics for $V_{GS} = 0$ for an n-channel JFET. Explain the shape of the characteristic, identify the regions, and indicate the important current and voltage levels. **(10 Marks)**

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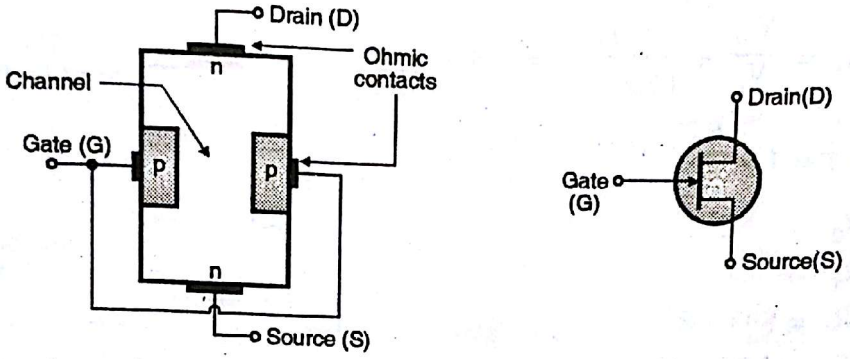
Ans. : n-channel JFET :

The structure of an n-channel field effect transistor is as shown in Fig. 3(a). A semiconductor bar of n-type material is taken and ohmic contacts are made to the two ends of the bar. These are the terminals named drain (D) and source (S) as shown in Fig. 3(a). On both sides of n-type bar, heavily doped (p) regions have been formed by alloying or by diffusion to create a p-n junction. Both these p regions are connected together and via an ohmic contact the gate terminal is brought out.

The supply voltage is connected between the drain and source terminals of a JFET hence current is caused to flow along the length of the n-type bar. This current is due to the majority carriers which in this case are electrons. Fig. 3(b) shows the symbol for the n-type JFET. The arrow on gate terminal indicates the conventional current directions.



(a) Structure of n-channel JFET **(b) Symbol of n-channel JFET**

(B-263) **Fig.3**

Channel : Channel is the n-type material between the two gate regions. The majority carriers (electrons here) move through this channel from source to drain. Since the channel is made of n-type material, this FET is called as n-channel JFET. The electrons enter the channel through the "source" terminal and leave through the "drain" terminal.

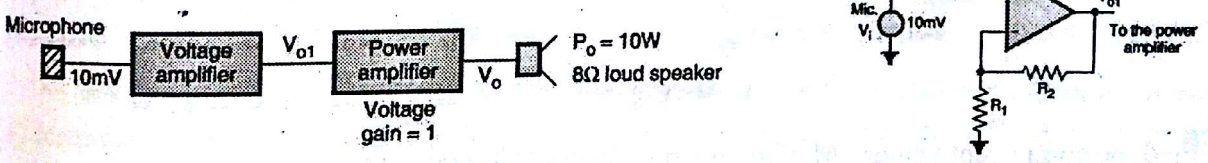
Drain characteristics (Output characteristics) : Please refer Q. 2(a) of Dec. 2013.

Chapter 2 : Operational Amplifier & its Application [Total Marks : 20]

Q. 1(d) A public address system is connected to a microphone that has a maximum output voltage of 10 mV. The microphone is connected to a 10 Watts audio amplifier system that is driving an 8 Ohm speaker. The voltage amplifier is a non inverting op-amp circuit. Calculate the maximum voltage gain for the voltage amplifier stage and determine the resistor values to obtain the desired gain. Assume the power amplifier stage has a voltage gain of 1. **(5 Marks)**

Ans. :

Step 1 : Draw circuit diagram :



(a) Public address system **(b) Voltage amplifier**

(D-1543) **Fig. 4**

Step 2 : Calculate V_o and V_{o1} : Output voltage of the power amplifier is given by,

$$P_o = \frac{V_o^2}{R_L}$$

$$\therefore V_o = \sqrt{P_o \times R_L} = \sqrt{10 \times 8} = 8.94 \text{ Volts} \quad ...(1)$$

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Voltage gain of the power amplifier is 1. Hence the output voltage of the voltage amplifier given by,

$$V_{o1} = \frac{V_o}{\text{Voltage gain of P.A.}} = \frac{V_o}{1}$$

$$\therefore V_{o1} = V_o = 8.94 \text{ Volts}$$

Step 3 : Find R_1 and R_2 and A_V : Voltage gain of voltage amplifier is,

$$A_V = 1 + \frac{R_2}{R_1}$$

$$\text{and } V_{o1} = A_V \times V_i$$

$$\therefore A_V = \frac{V_{o1}}{V_i} = \frac{8.94}{10 \times 10^{-3}} = 894.4$$

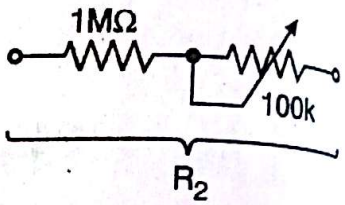
$$\therefore 894.4 = 1 + \frac{R_2}{R_1}$$

$$\therefore \frac{R_2}{R_1} = 893.4$$

$$R_2 = 893.4\, R_1$$

Let $\mathbf{R_1 = 1.2\ k\Omega}$

$\therefore$ $\mathbf{R_2 = 1072\ k\Omega}$



(D-1544) **Fig. 4(c)**

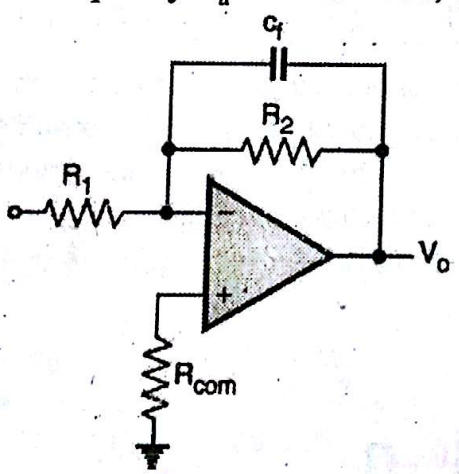
R_2 as a combination of a 1 MΩ fix value resistance and a 100 kΩ preset as shown in Fig. 4(c).

Q. 2(b) Find R_1 and R_2 in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when ω = 10,000 rad/s. Use capacitance of 0.01μF. **(10 Marks)**

Ans. :

Given : Maximum gain = 20 dB, 3 dB frequency ω_a = 10000 rad/s, c_f = 0.01 μF.

Step 1 : Draw the circuit diagram



(D-1545) **Fig. 5**

Step 2 : Find the component values : Maximum gain is nothing but dc gain.

$\therefore$ DC gain = 20 dB = $20 \log_{10} |A_V|$

$\therefore |A_V| = 10$

But $|A_V| = \frac{R_2}{R_1}$

$\therefore R_2 = 10\, R_1$ ...(1)

Also ω_a = 10000 rad/sec.

$$\therefore \quad f_a = \frac{10000}{2\pi} = 1591.55 \text{ Hz}$$

$$\text{But} \quad f_a = \frac{1}{2\pi R_2 c_f}$$

$$c_f = 0.01 \ \mu F \qquad \text{(Given)}$$

$$\therefore \quad R_2 = \frac{1}{2\pi f_a c_f} = \frac{1}{10000 \times 0.01 \times 10^{-6}}$$

$$\therefore \quad \mathbf{R_2 = 10 \ k\Omega}$$

Substituting in Equation (1) we get,

$$10 \ k\Omega = 10 \ R_1$$

$$\therefore \quad \mathbf{R_1 = 1 \ k\Omega}$$

Q. 3(c) Draw and explain op-amp non inverting comparator. Draw input and output waveforms for V_{ref} positive and also for V_{ref} negative. **(5 Marks)**

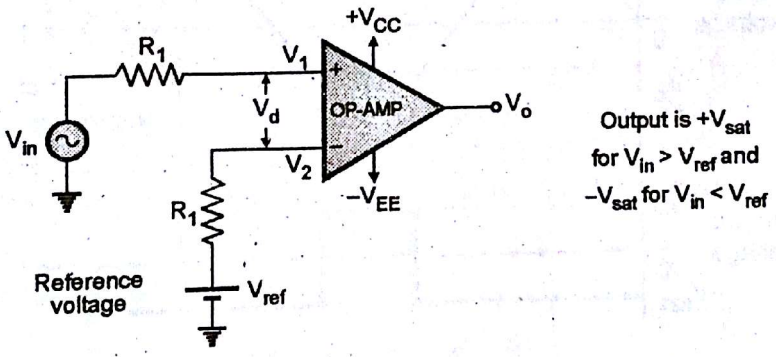
Ans. :

Op-amp non inverting comparator :

The schematic diagram of a non-inverting comparator is as shown in Fig. 6(a). A positive dc reference voltage is applied to the inverting terminal (–) and an ac sinusoidal signal is applied to the non-inverting (+) terminal. As the ac signal is connected to the non-inverting (+) terminal, this comparator is called as non-inverting comparator.

Operation of the circuit : As the current through resistors R_1 is almost zero, the voltage drop across them will be equal to zero. Hence $V_1 = V_{in}$ and $V_2 = V_{ref}$. Hence the differential input voltage V_d is given by,

$$V_d = V_1 - V_2 = V_{in} - V_{ref}$$



(K-436)**Fig. 6(a) : A non-inverting comparator**

When V_{in} is less than V_{ref} the inverting (–) terminal is at higher potential than the non-inverting (+) terminal. Therefore the differential input voltage V_d is negative and the OP-AMP output will swing to the $-V_{(sat)}$ Volts. When V_{in} is greater than V_{ref} the non-inverting (+) terminal is at higher potential than the inverting (–) terminal. Therefore the differential input voltage V_d is positive and the OP-AMP output will swing to $+V_{(sat)}$ Volts as shown in Fig. 6(b).

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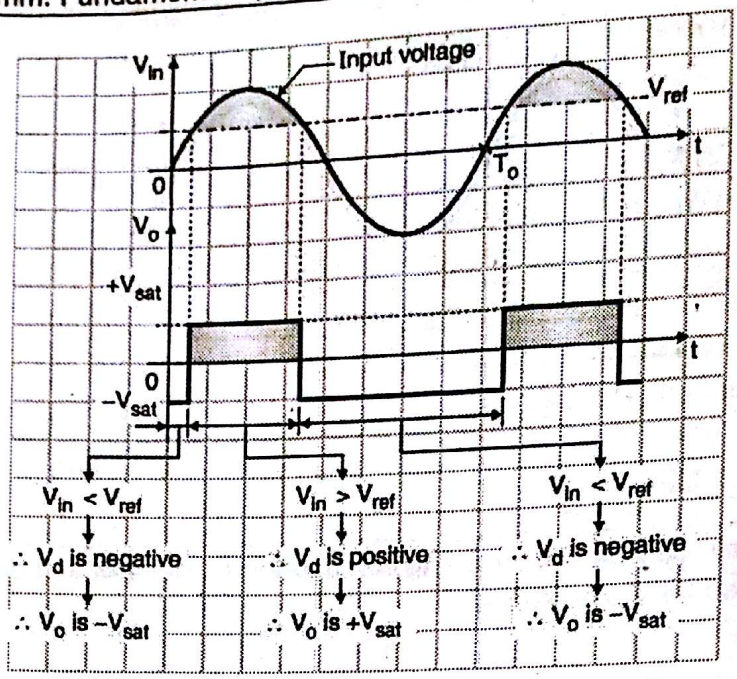
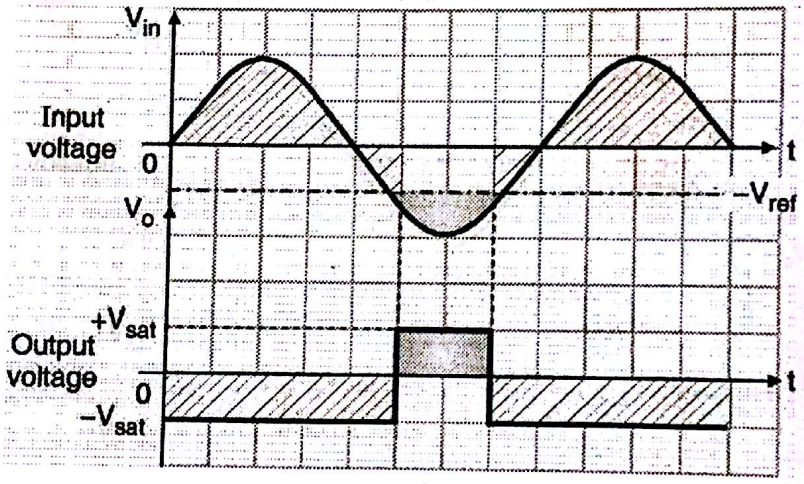


(K-437)Fig. 6(b) : Input and output voltage waveforms

If the reference voltage is made negative ($-V_{ref}$) and applied to the inverting (–) terminal then the input and output voltage waveforms are modified as shown in Fig. 6(c). If the OP-AMP is capable of operating on the single polarity supply i.e. only on + V_{CC} then the output waveform of such a comparator will be unipolar. Then we will get either + V_{sat} or GND at the comparator output. OP-AMP ICs such as IC LM 324 is capable of working on a single polarity supply.



(K-438)Fig. 6(c) : Waveforms for a non-inverting comparator with negative reference voltage

Chapter 4 : Modulation [Total Marks : 25]

Q. 3(b) Draw the spectrum of an amplitude modulated wave and explain its components. **(5 Marks)**

Ans. : Amplitude modulated wave :

The expression for the AM wave shows that it consists of three terms :

1. First term is nothing else but the unmodulated carrier signal.
2. The second term is a sinusoidal signal at frequency ($f_c + f_m$). This is called as the upper sideband (USB). Its amplitude is $\frac{m E_c}{2}$.

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3. The third term represents a sinusoidal signal at frequency $(f_c - f_m)$. It is called as the lower sideband (LSB). Its amplitude is $\frac{m E_c}{2}$.

Hence the frequency spectrum of an A.M. wave is as shown in Fig. 7. It is a single sided spectrum i.e. the spectrum plotted for only the positive values of frequency.

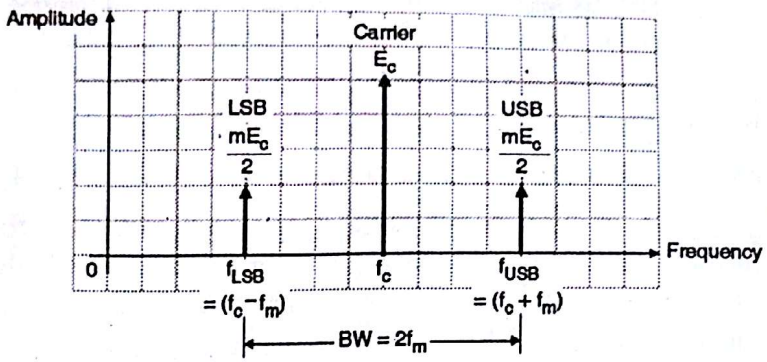


Fig. 7 : Single sided frequency spectrum of AM wave

Q. 4(b) What is DSBSC wave? Explain its generation using balanced modulator. **(10 Marks)**

Ans. :

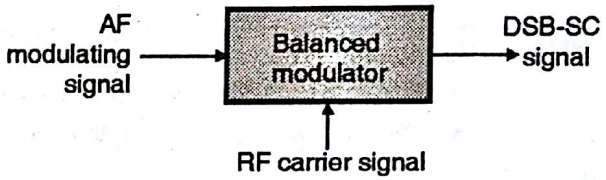
DSBSC wave :

Double-sideband Suppressed-Carrier Transmission (DSB-SC) is transmission in which frequencies produced by Amplitude Modulation (AM) are symmetrically spaced above and below the carrier frequency and the carrier level is reduced to the lowest practical level, ideally being completely suppressed

Balanced modulator :

The nonlinear modulators are also known as the balanced modulators. The balanced modulators are used to suppress the unwanted carrier in an AM wave.

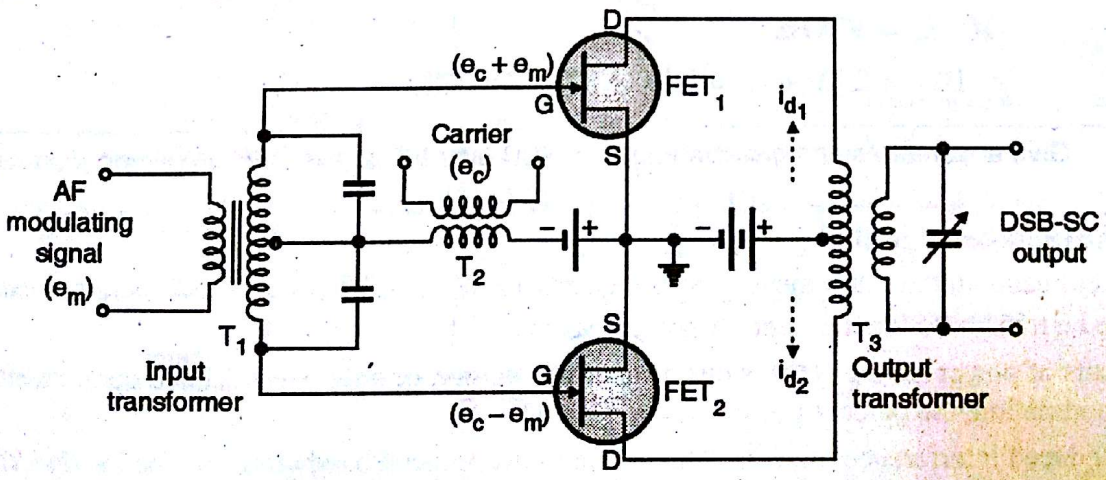
The carrier and modulating signals are applied to the inputs of the balanced modulator and we get the DSB signal with suppressed carrier at the output of the balanced modulator. Thus the output consists of the upper and lower sidebands only.



(D-120) **Fig. 8(a) : Block diagram of balanced modulator**

The principle of operation of a balanced modulator states that if two signals at different frequencies are passed through a "nonlinear resistance" then at the output we get an AM signal with suppressed carrier. The device having a nonlinear resistance can be a diode or a JFET or even a bipolar transistor.

Balanced modulator using FETs :



(D-125) **Fig. 8(b) : Balanced modulator using FETs**

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The balanced modulator using FETs is as shown in Fig. 8(b). The carrier voltage is applied "in phase" to the two gates via the transformers T_2 and T_1.

However the modulating signal appears 180° out of phase at the gates of the two FETs. This is because the input transformer T_1 is a centre tapped transformer.

Mode I (Operation in the absence of modulating signal) :

In the absence of modulating signal, both the FETs conduct simultaneously due to the same carrier voltage applied to their gates. Both the FETs are identical in all respect to each other. Their drain currents are equal in magnitude but opposite in direction through the primary of output transformer T_3 as shown in the Fig. 8(b). Due to this their magnetic fields cancel each other, inducing a zero secondary voltage. Thus the output of transformer T_3 is zero. The carrier is thus suppressed.

Mode II (Carrier and modulating signal both present) :

When the modulating signal is applied alongwith the carrier, the drain currents of the two FETs flow due to the combined effect of carrier and the modulating signal. The FET currents due to carrier are equal and opposite and hence cancel each other.

However FET currents due to the modulating signal are equal but not opposite so they do not cancel out. This is because the modulating signal is applied 180° out of phase to the two FETs. Hence at the output of the circuit we get a DSB-SC signal. For the 100 % suppression of the carrier, both the FETs must have the identical characteristics i.e. it should be a matched pair and the transformer centre taps must be exactly at the centre of the windings. Practically this is not possible hence carrier will be heavily suppressed but not completely removed.

Q. 5(b) The maximum deviation allowed in a FM broadcast system is 75 kHz. If the modulating signal is a single tone sinusoidal of frequency 15 kHz, find the bandwidth of the FM signal. How does the bandwidth change if the modulating frequency is doubled ? **(5 Marks)**

Ans. :

Given : $\Delta f = 75$ kHz, $f_m = 15$ kHz

To find : 1. Bandwidth of FM signal.

2. Bandwidth of FM signal if modulating frequency is doubled.

Step 1 : Calculate bandwidth :

$$BW = 2\,[\Delta f + f_m] = 2\,[75 + 15] = \mathbf{180\ kHz}$$

Step 2 : Calculate BW if modulating frequency is doubled :

If $f_m = 30$ kHz

$$\therefore\ BW = 2\,[\Delta f + f_m] = 2\,[75 + 30] = \mathbf{210\ kHz}$$

Q. 6(c) Give advantages and disadvantages of SSB over full carrier DSB amplitude modulated wave. **(5 Marks)**

Ans. : Advantages of SSB :

1. Less bandwidth requirement as SSB requires a BW of f_m. This will allow more number of signals to be transmitted in the same frequency range.
2. Lots of power saving. This is due to the transmission of only one sideband component. At 100 % modulation, the percent power saving is 83.33 %.
3. Reduced interference of noise. This is due to the reduced bandwidth. As the bandwidth increases, the amount of noise added to the signal will increase.

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Disadvantages of SSB :

1. The generation and reception of SSB signal is complicated as discussed later on.
2. The SSB transmitter and receiver need to have excellent frequency stability. A slight change in frequency will hamper the quality of transmitted and received signal. SSB therefore is not generally used for the transmission of good quality music. It is used for speech transmission.

Chapter 5 : Demodulation [Total Marks : 15]

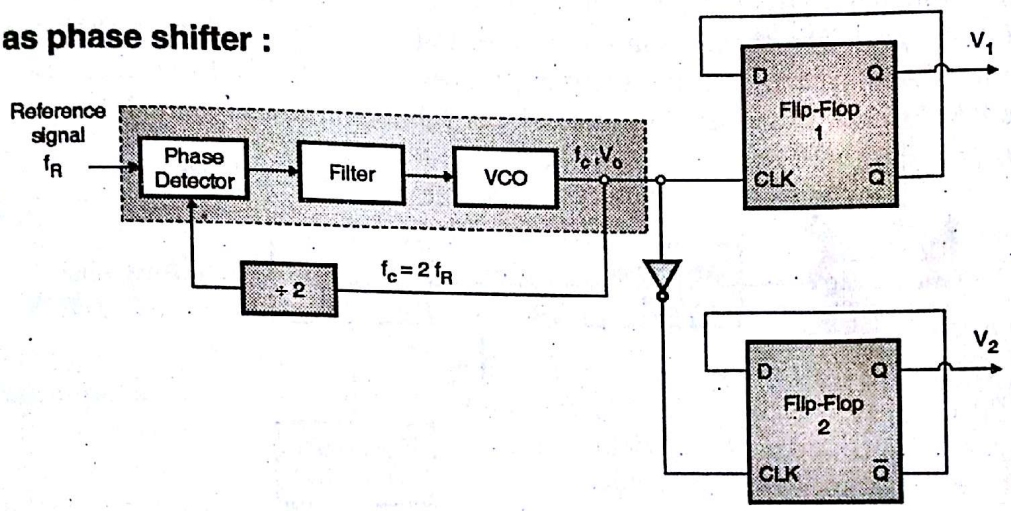
Q. 4(a) Explain the working of a superheterodyne receiver with the help of a neat block diagram. Show the waveforms at the output of each block. **(10 Marks)**

Ans. : **Please refer Q. 3(b) of May 2014.**

Q. 6(b) With neat circuit diagram explain the use of PLL as phase shifter. **(5 Marks)**

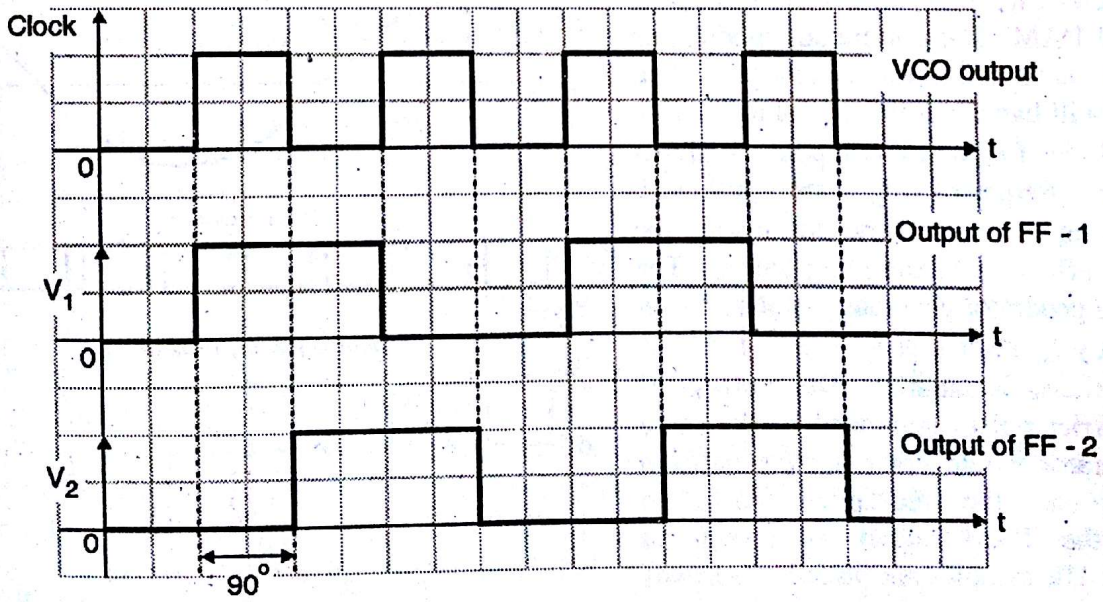
Ans. :

Use of PLL as phase shifter :



(K-866) **Fig. 9(a) : PLL used as a phase shifter**

In many modulation techniques, we require 90° phase shift of local oscillator. The phase shifter circuit that introduces a phase shift of 90° using PLL is as shown in Fig. 9(a).



(K-867) **Fig. 9(b) : Timing diagram for the phase shifter**

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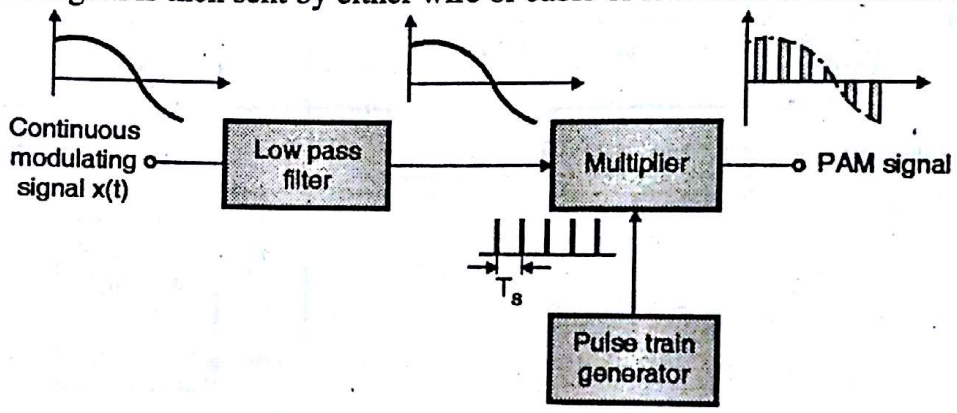
The input signal to the circuit has a frequency f_R. The PLL doubles this frequency so that the frequency of VCO output voltage is $f_c = 2 f_R$. The VCO output signal is used as the clock signal for flip-flop- 1. This flip-flop responds to the positive clock edges and produces a voltage V_1 that has a frequency of $f_c/2$ or f_R as shown in Fig. 9(b). This is because the flip-flop divides clock frequency of 2. The VCO output is inverted and applied to the clock input of second flip-flop. The output of F/F - 2 i.e. V_2 is shown in Fig. 9(b). The signals V_1 and V_2 differ in phase by 90°. F/F-2 responds to the negative edges of VCO output.

Chapter 6 : Analog Pulse Modulation [Total Marks : 10]

Q. 5(a) Draw the PAM, PWM and PPM waveforms in time domain assuming a sinusoidal modulating signal. Explain them in brief. **(10 Marks)**

Ans. : Pulse Amplitude Modulation (PAM) :

In the PAM system, the amplitude of the pulsed carrier is changed in proportion with the instantaneous amplitude of the modulating signal x(t). So the information is contained in the amplitude variation of PAM signal. The carrier is in the form of train of narrow pulses as shown in Fig. 10(b). If you compare the PAM system with the sampling process, you will find that these two processes are identical. The PAM signal is then sent by either wire or cable or it is used to modulate a carrier.

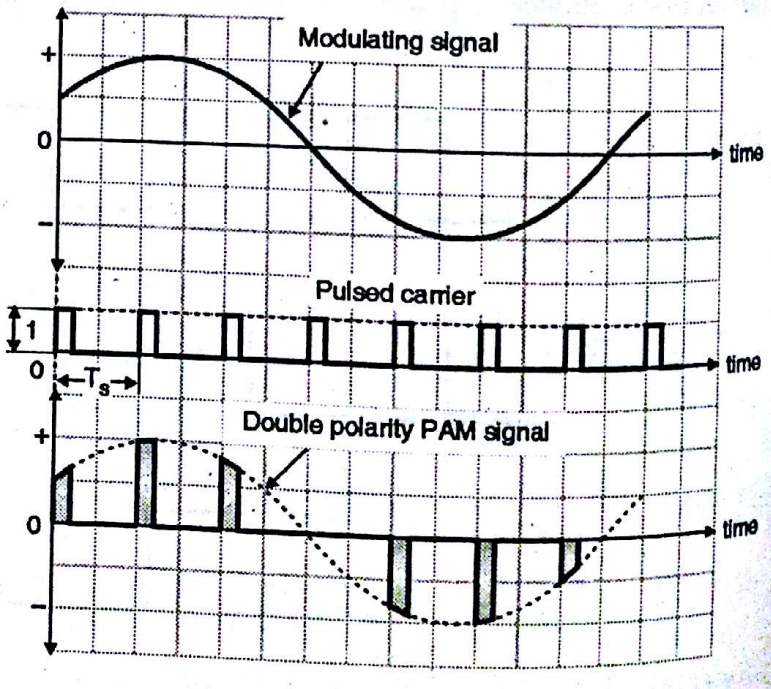


(L-181) **Fig. 10(a) : Generation of PAM**

There are two types of PAM :

1. Generation of natural PAM :

Refer Fig. 10(a) shows the generation of natural PAM. The continuous modulating signal x(t), is passed through a low pass filter. The LPF will bandlimit this signal to f_m. That means all the frequency components higher than the frequency f_m are removed. Bandlimiting is necessary to avoid the "aliasing" effect in the sampling process. The pulse train generator generates a pulse train at a frequency f_s, such that $f_s \geq 2f_m$. Thus the Nyquist criteria is satisfied. The rectangular narrow carrier pulses generated by the pulse train generator would carry out the uniform "sampling" in the multiplier block, to generate the PAM signal as shown in Fig. 10(b). The samples are placed T_s seconds away from each other.



(L-182) **Fig. 10(b) : Waveform of natural PAM**

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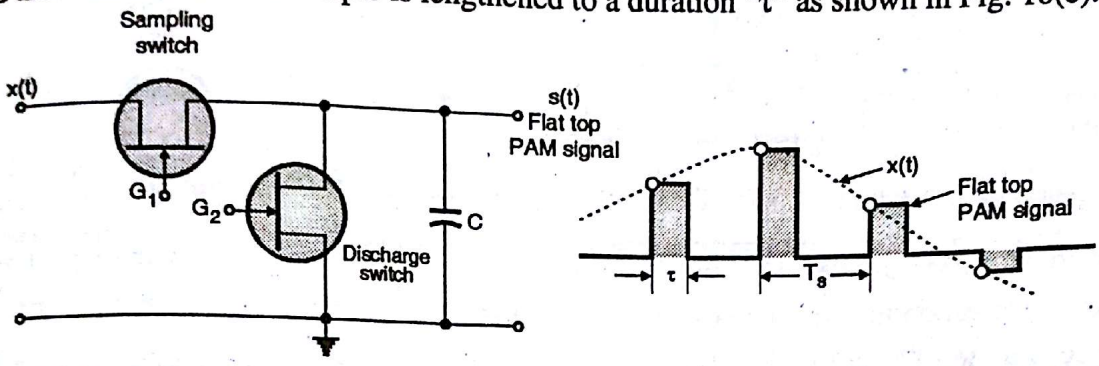
The "information" in the modulating signal is contained in the "Amplitude variations" of the pulsed carrier. Natural PAM is sometimes called as chopper sampled PAM because the waveform of the sampled signal appears to be chopped off from the continuous time signal x(t).

2. **Flat top PAM :**

The natural PAM is rarely employed in practice. Instead the flat top PAM is employed in practice. In the flat top PAM technique, the analog signal x(t) is sampled instantaneously at the rate $f_s = \frac{1}{T_s}$ and the duration of each sample is lengthened to a duration "τ" as shown in Fig. 10(c).



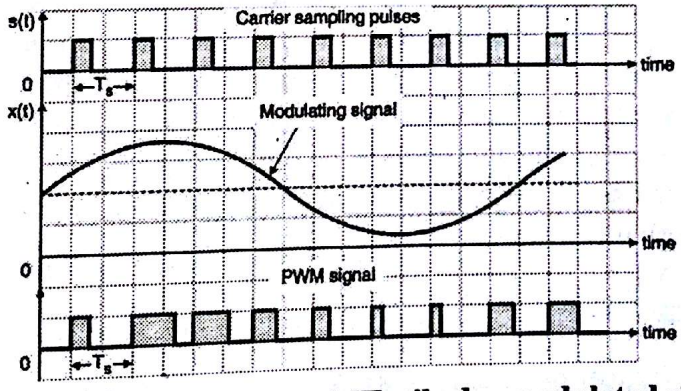
(c) Sample and hold circuit to obtain the flat top PAM **(d) Flat top PAM signal**

(D-449) **Fig. 10**

Thus the amplitudes of these pulses are constant and equal to the corresponding sampled values. The flat top PAM can be obtained by using the sample and hold circuit shown in Fig. 10(c).

Pulse Width Modulation (PWM) or Pulse Duration Modulation (PDM) :

The other type of a pulse analog modulation is the pulse width modulation (PWM). In PWM, the width of the carrier pulses varies in proportion with the amplitude of modulating signal. The waveforms of PWM are as shown in Fig. 10(e). As seen from the waveforms, the amplitude and the frequency of the PWM wave remains constant. Only the width changes. That is why the "information" is contained in the width variation. As the noise is normally "additive" noise, it changes the amplitude of the PWM signal. At the receiver, it is possible to remove these unwanted amplitude variations very easily by means of a limiter circuit. As the information is contained in the width variation, it is unaffected by the amplitude variations introduced by the noise. Thus the PWM system is more immune to noise than the PAM signal.



(D-454) **Fig. 10(e) : PWM signal [Trail edge modulated signal]**

Pulse Position Modulation (PPM) : In PPM the amplitude and width of the pulsed carrier remains constant but the position of each pulse is varied in proportion with the amplitudes of the sampled values of the modulating signal. The position of the pulses is changed with respect to the position of reference pulses. The PPM pulses can be derived from the PWM pulses as shown in Fig. 10(f). With increase in the modulating voltage the PPM pulses shift further with respect to reference. The vertical dotted lines

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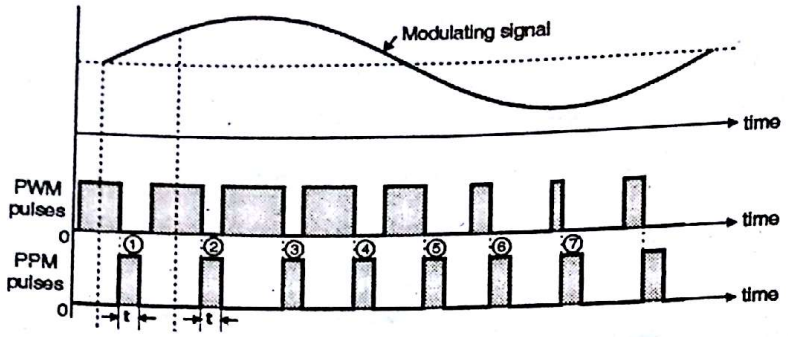
drawn in Fig. 10(f) are treated as reference lines to measure the shift in position of PPM pulses. The leading edge of each PPM pulse coincides with the trailing pulse of a PWM pulse.



(D-460) **Fig. 10(f) : PPM pulses generated from PWM signal**

The PPM pulses marked 1, 2 and 3 etc. in Fig. 10(f) go away from their respective reference lines. This is corresponding to increase in the modulating signal amplitude. Then as the modulating voltage decreases the PPM pulses 4, 5, 6, 7 come progressively closer to their respective reference lines.

Chapter 7 : Digital Modulation Techniques [Total Marks : 10]

Q. 1(a) Mention five important specifications of ADC/DAC that are looked at while selecting them for any application. **(5 Marks)**

Ans. : Specifications for DAC (D/A Accuracy and Resolution) :

1. **Resolution :** Resolution is defined as the smallest possible change in the analog output voltage. Resolution should be as high as possible. Its value depends on the number of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution. Resolution of a DAC can be defined in two different ways : The first definition of resolution is the number of different analog output voltage values that can be provided by a DAC. For an n-bit DAC,

$$\text{Resolution} = 2^n$$

Hence the resolution of a 4-bit DAC is $2^4 = 16$ and that of a 3-bit DAC is $2^3 = 8$. Hence resolution increases with the increase in number of bits. Resolution is defined in an alternative way as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input. To calculate the resolution with this definition, we need to know the full scale analog output voltage V_{FS} and the number of digital inputs "n". The full scale analog output voltage V_{FS} is defined as the output voltage corresponding to the digital input with all digits 1. Therefore the resolution is given by,

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

where n = Number of digital inputs.

2. **Accuracy :** Accuracy of a DAC indicates how close the analog output voltage is to its theoretical value. In short it indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the values of resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output. That means maximum output voltage. e.g. if the full scale output is 15 V and accuracy is ± 0.1 percent then the maximum error is given by $0.001 \times 15 = 0.015$ V or 15 mV.

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3. **Linearity :** The relationship between the digital input and analog output is expected to be linear. However practically it is not so due to the error in the values of resistors used for the resistive networks.

4. **Settling time :** Theoretically the analog output voltage should change instantaneously as soon as there is a change in the digital input. Practically the analog output of a D to A converter does not change instantaneously. Due to the resistors and OP-AMP in the circuit, oscillations are observed at the output. The time required to settle the analog output within 1/2 LSB of the final value, from the instant of change in digital input is called as settling time. The settling time should be as short as possible.

5. **Speed :** It is defined as the time taken by a DAC to perform a conversion from digital to analog. It is also defined as the number of conversions that can be performed per second. The speed of DAC should be as high as possible.

Q. 5(c) How is adaptive delta modulation superior to delta modulation ? **(5 Marks)**

Ans. : Adaptive Delta Modulation (ADM) :

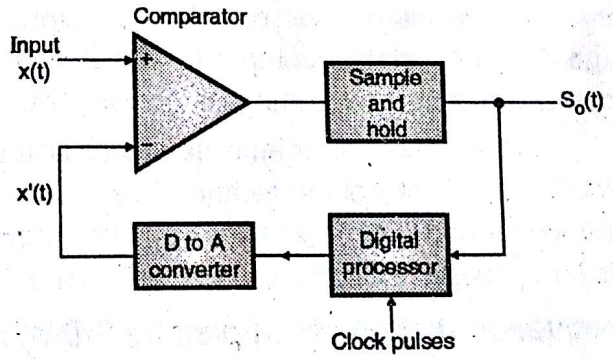
In the ADM system, the step size is not constant. Rather when the slope overload occurs the step size becomes progressive larger and therefore x′ (t) will catch up with x (t) more rapidly. Whenever the slope of input signal is large, the step size of the staircase approximated signal x′ (t) is increased. On the other hand when the input signal is varying slowly the step size is reduced. Thus the step size is adapted as per the level of input signal.

There are various types of ADM systems available depending on the type of scheme used for adjusting the step size. In one type a discrete set of values is provided for the step size whereas in another type a continuous range of step size variation is provided. We will discuss the first type here.

ADM Transmitter :

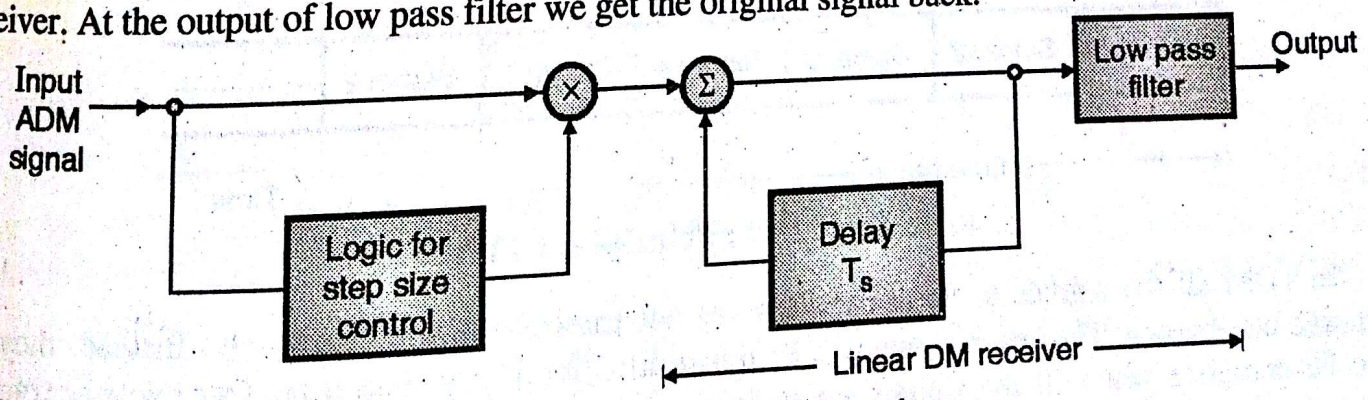
In the ADM system, the step size is not constant. Rather when the slope overload occurs the step size becomes progressive larger and therefore x′(t) will catch up with x(t) more rapidly. The ADM transmitter is as shown in Fig. 11(a).

If you compare this block diagram with that of the linear delta modulator, then you will find that except for the counter being replaced by the digital processor, the remaining blocks are identical.



(D-495) **Fig. 11(a) : ADM transmitter**

ADM Receiver : The block diagram of ADM receiver is shown in Fig. 11(b). The ADM signal is first converted into a D.M. signal with the help of the step size control logic and then applied to a D.M. receiver. At the output of low pass filter we get the original signal back.



(D-497) **Fig. 11(b) : ADM receiver**

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Advantages of Adaptive Delta Modulation :

The advantages of ADM over DM are as follows :

1. Reduction in slope overloads distortion and granular noise.
2. Improvement in signal to noise ratio.
3. Wide dynamic range due to variable step size.
4. Better utilization of bandwidth as compared to delta modulation.
5. Low signaling rate.
6. Simplicity of implementation.

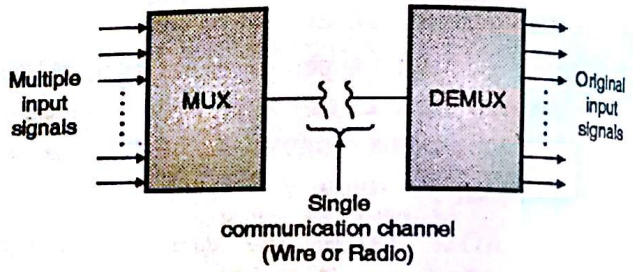
Chapter 8 : Multiplexing [Total Marks : 10]

Q. 6(a) What do you understand by signal multiplexing ? Explain TDM and FDM with suitable examples. **(10 Marks)**

Ans. : Multiplexing :

Multiplexing is the process of simultaneously transmitting two or more individual signals over a single communication channel. Due to multiplexing it is possible to increase the number of communication channels so that more information can be transmitted. The typical applications of multiplexing are in telemetry and telephony or in the satellite communication.

The concept of a simple multiplexer is shown in Fig. 12(a). The multiplexer receives a large number of different input signals. Multiplexer has only one output which is connected to the single communication channel. The multiplexer combines all input signals into a single composite signal and transmits it over the communication medium.



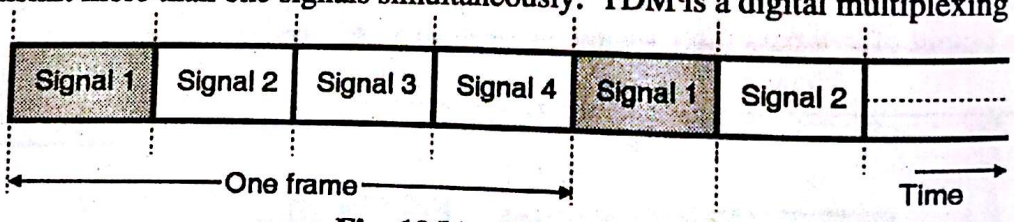
(L-105) **Fig. 12(a) : Concept of multiplexing**

Sometimes the composite signal is used for modulating a carrier before transmission. At the receiving end, of communication link, a demultiplexer is used to separate out the signals into their original form. The operation of demultiplexer is exactly opposite to that of a multiplexer. Demultiplexing is the process which is exactly opposite to that of multiplexing.

Frequency Division Multiplexing (FDM) : Please refer Q. 1(c) of May 2014.

Time Division Multiplexing (TDM) :

The process called multiplexing is used in order to utilize common transmission channel or medium to transmit more than one signals simultaneously. TDM is a digital multiplexing process.



(L-122) **Fig. 12(b) : Principle of TDM**

In TDM all the signals to be transmitted are not transmitted simultaneously. Instead, they are transmitted one-by-one. Thus each signal will be transmitted for a very short time. One cycle or frame is said to be complete when all the signals are transmitted once on the transmission channel. The TDM principle is illustrated in Fig. 12(b).

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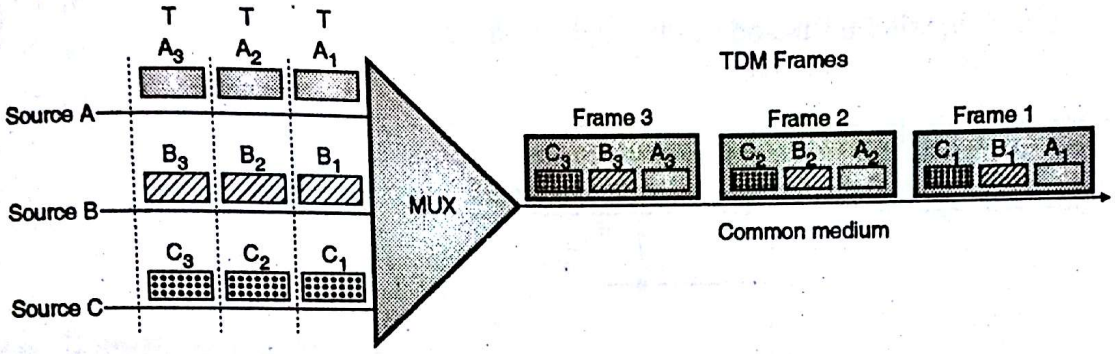
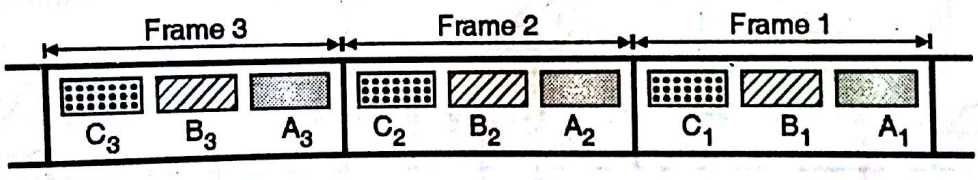
As shown in the Fig. 12(b) one transmission of each channel completes one cycle of operation called as a "Frame". The TDM system can be used to multiplex analog or digital signals, however it is more suitable for the digital signal multiplexing. The concept of TDM will be more clear as shown in Fig. 12(b). The data flow of each source (A, B or C) is divided into units (say A_1, A_2 or B_1, C_1 etc.)

Then one unit from each source is taken and combined to form one frame. The size of each unit such as A_1, B_1 etc. can be 1 bit or several bits.



(L-123) **Fig. 12(c) : TDM system**

Fig. 12(d) shows the frames of TDM signal. For 3 inputs being multiplexed, a frame of TDM will consist of 3 units i.e. one unit from each source. Similarly for n number of inputs, each TDM frame will consist of n units.



(L-124) **Fig. 12(d) : TDM frames**

The TDM signal in the form of frames is transmitted on the common communication medium.

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May 2015

Chapter 1 : Electronic Circuits [Total Marks - 30]

Q. 1(a) Draw and explain FET based Hartley and Colpitt oscillator. (5 Marks)

Ans. :

FET based Hartley oscillator :

Fig. 1-Q. 1(a) shows the Hartley oscillator using FET.

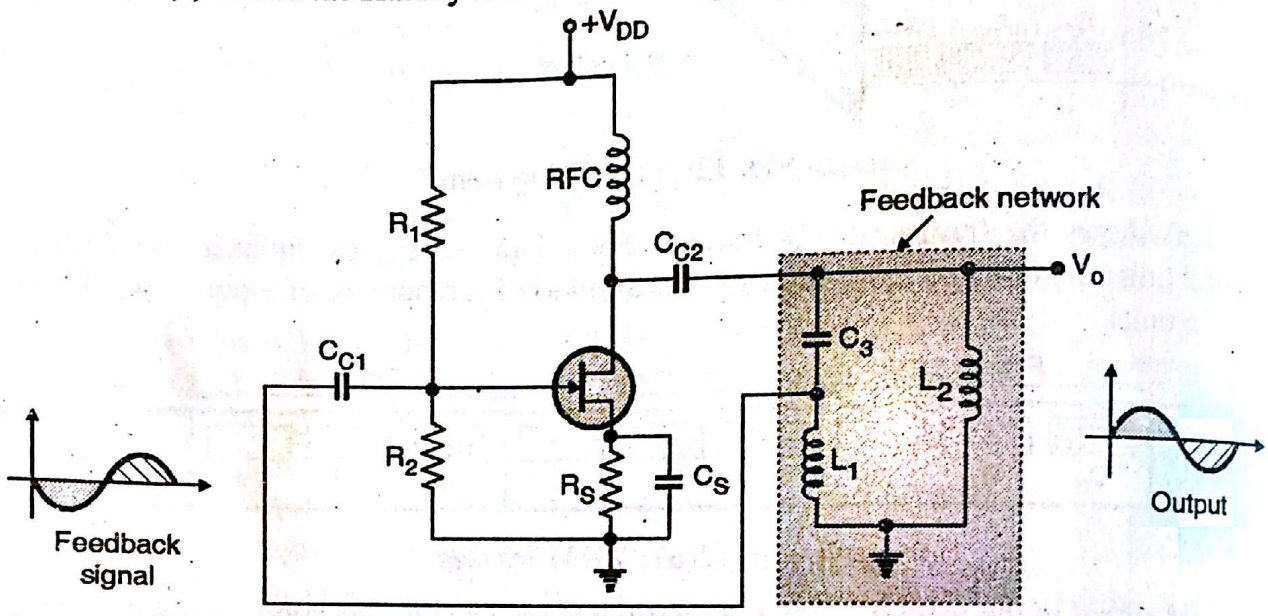

Fig. 1-Q. 1(a) : FET Hartley oscillator

Circuit description :

R_1, R_2 and R_S are used to properly bias the n-channel JFET used here. C_{C1} and C_{C2} are the coupling capacitors and C_S is the bypass capacitor. The amplifier configuration is C_S hence the phase shift between input and output will be 180°. The feedback network provides the additional 180° phase shift required to satisfy the condition for positive feedback.

Expression for the frequency of oscillations :

Here we have, $X_1 = \omega L_1$, $X_2 = \omega L_2$ and $X_3 = \dfrac{-1}{\omega C_3}$

$$X_1 + X_2 + X_3 = 0$$

$$\therefore \quad \omega L_1 + \omega L_2 - \frac{1}{\omega C_3} = 0$$

$$\therefore \quad \omega L_1 + \omega L_2 = \frac{1}{\omega C_3}$$

$$\therefore \quad \omega (L_1 + L_2) = \frac{1}{\omega C_3}$$

$$\therefore \quad \omega^2 = \frac{1}{(L_1 + L_2) C_3},$$

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$$\therefore \omega = \frac{1}{\sqrt{(L_1 + L_2) C_3}}$$

$$\text{But } \omega = 2\pi f,$$

$$\therefore f = \frac{1}{2\pi\sqrt{C_3 (L_1 + L_2)}} \text{ without mutual inductance} \quad ...(1)$$

Note that we have not considered the effect of mutual inductance M between the two inductors L_1 and L_2. If the inductors are not wound on the same core then the mutual inductance between them is zero and Equation (1) is valid.

But if they are wound on the same core then we have to consider the mutual inductance M. The expression for oscillator frequency will then be :

$$f = \frac{1}{2\pi\sqrt{C_3 (L_1 + L_2 + 2M)}} \text{ with mutual inductance} \quad ...(2)$$

FET based Colpitt oscillator :

Fig. 2-Q. 1(a) shows the Colpitt's oscillator using FET. R_1, R_2 and R_S are the biasing resistors for the FET. C_{C1} and C_{C2} are the coupling capacitor while C_S is the bypass capacitor. FET is operated in the CS configuration. Therefore the phase shift introduced is 180°. The feedback network consists of C_1, C_2 and L_3 which introduces an additional phase shift of 180° in order to make the total phase shift equal to 0°. Thus the condition for the positive feedback is satisfied.

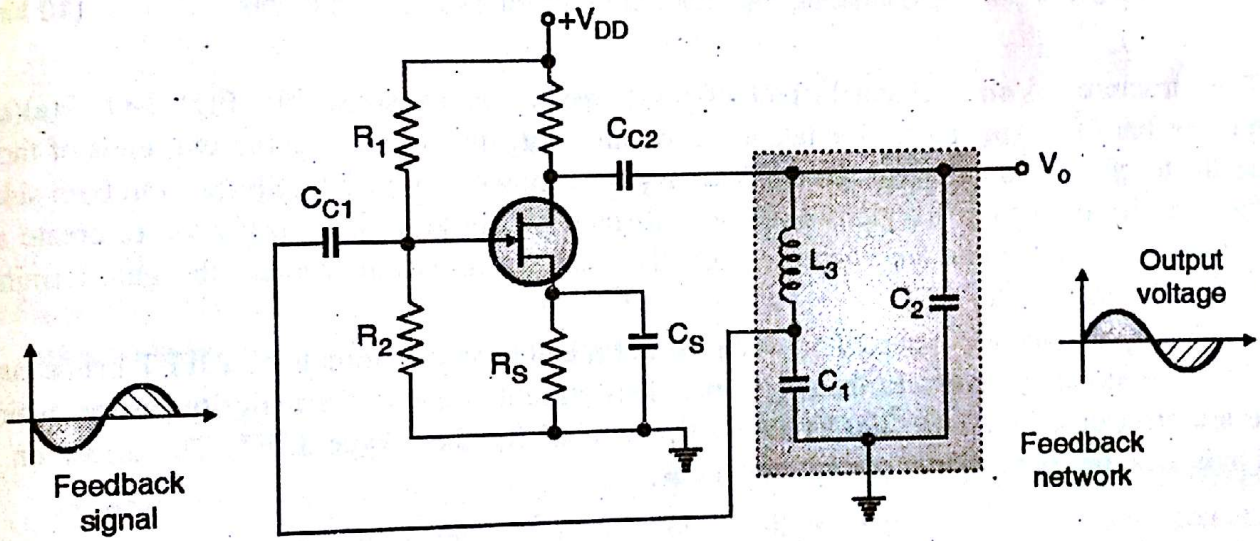


Fig. 2-Q. 1(a) : Colpitt's oscillator using FET

The expression for frequency of oscillations is obtained as follows :

$$X_1 = \frac{-1}{\omega C_1}, \qquad X_2 = \frac{-1}{\omega C_2}, \qquad X_3 = \omega L_3$$

We know that, $X_1 + X_2 + X_3 = 0$

$$\therefore \frac{-1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L_3 = 0$$

$$\therefore \frac{-(C_2 + C_1)}{\omega C_1 C_2} = -\omega L_3$$

$$\therefore \quad \omega^2 = \frac{C_1 + C_2}{L_3 C_1 C_2} \quad \text{...(3)}$$

Let, $C = \frac{C_1 C_2}{C_1 + C_2}$, hence Equation (3) gets converted as,

$$\omega^2 = \frac{1}{C L_3}$$

$$\therefore \quad \omega = \frac{1}{\sqrt{C L_3}}$$

$$\text{and} \quad f = \frac{1}{2\pi\sqrt{C L_3}} \quad \text{...(4)}$$

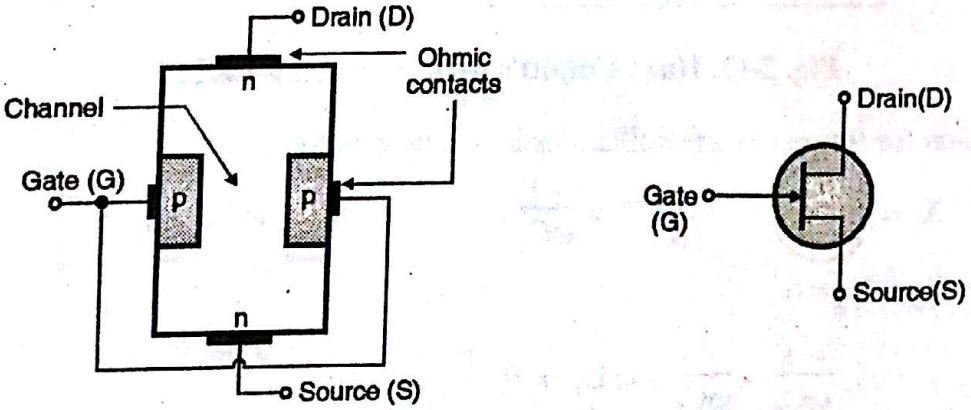
$$\text{where,} \quad C = \frac{C_1 C_2}{C_1 + C_2}$$

Q. 2(a) Sketch a block representation for an n-channel JFET, showing bias voltages, depletion regions, and current directions. Label the device terminals and explain its operation. Explain the effect of increasing levels of negative gate-source voltage. Also sketch a typical drain characteristics for $V_{GS} = 0$ for an n-channel JFET. Explain the shape of the characteristic, identify the regions and indicate the important current and voltage levels. **(10 Marks)**

Ans. :

The structure of an n-channel field effect transistor is as shown in Fig. 1-Q. 2(a)(a). A semiconductor bar of n-type material is taken and ohmic contacts are made to the two ends of the bar. These are the terminals named drain (D) and source (S) as shown in Fig. 1-Q. 2(a)(a). On both sides of n-type bar, heavily doped (p) regions have been formed by alloying or by diffusion to create a p-n junction. Both these p regions are connected together and via an ohmic contact the gate terminal is brought out.

The supply voltage is connected between the drain and source terminals of a JFET hence current is caused to flow along the length of the n-type bar. This current is due to the majority carriers which in this case are electrons. Fig. 1-Q. 2(a)(b) shows the symbol for the n-type JFET. The arrow on gate terminal indicates the conventional current directions.



(a) Structure of n-channel JFET **(b) Symbol of n-channel JFET**

Fig. 1-Q. 2(a)

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Channel :

Channel is the n-type material between the two gate regions. The majority carriers (electrons here) move through this channel from source to drain. Since the channel is made of n-type material, this FET is called as n-channel JFET. The electrons enter the channel through the "source" terminal and leave through the "drain" terminal.

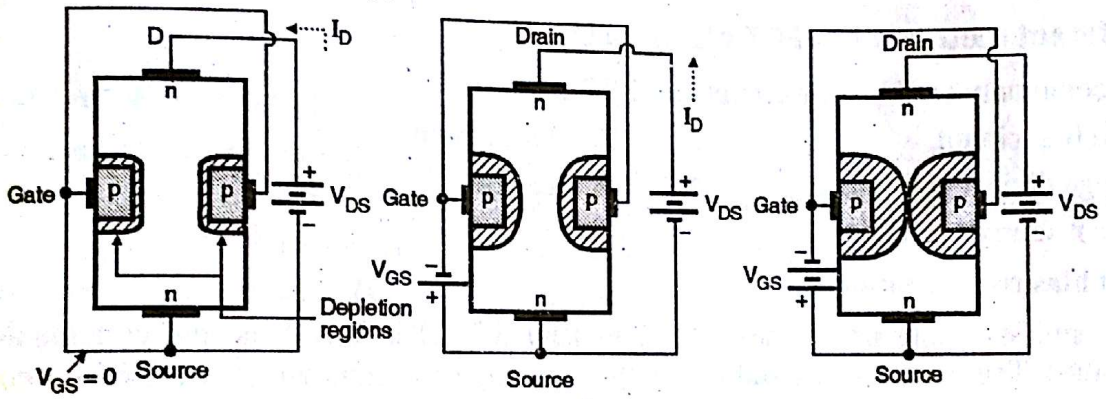
Operation of n- channel JFET :

A positive voltage is applied between the drain and source terminals of a JFET, i.e. V_{DS} is positive and a negative voltage is applied between the gate and source terminals i.e. V_{GS} is negative.

The operation of JFET is explained for different values of V_{GS} as follows :

1. Operation of n-channel JFET with $V_{GS} = 0$:

Now let us see the effect of gate to source voltage V_{GS} on the operation of a n-channel JFET. Refer to Fig. 2-Q. 2(a)(a) in which gate is connected to source making $V_{GS} = 0$. Due to the supply voltage V_{DS}, current starts flowing through the channel. The drain current is controlled solely by the resistance of the semiconductor material between drain and source. The n-type material has a finite resistance. Therefore the drain current flow, causes a voltage drop along the channel. This voltage drop will reverse bias the gate to source p-n junction.



(a) Operation with no bias voltage **(b) Operation with a small negative gate source bias** **(c) Operation with a large negative gate source bias**

Fig. 2-Q. 2(a)

The depletion region of the reverse biased p-n junction penetrates more into the n-type bar because it is lightly doped as compared to the heavily doped p-type gate. The penetration of the depletion region into n-type bar depends on the magnitude of reverse bias voltage. Due to the depletion regions the width of the "Channel" available for conduction is reduced, as shown in Fig. 2-Q. 2(a)(a).

Source saturation current I_{DSS} :

The value of drain current corresponding to $V_{GS} = 0V$ is called as the source saturation current and it is denoted by I_{DSS}. I_{DSS} corresponds to the maximum drain current because the channel is widest for $V_{GS} = 0V$.

2. Operation of a n-channel JFET for small negative V_{GS} :

Now a small negative voltage is applied between the gate and source terminals as shown in Fig. 2-Q. 2(a)(b). Due to the reverse voltage applied across the gate source junction, the penetration of the depletion region into n-type material increases further. This will reduce the channel width further. Due to reduced channel width less number of electrons can pass through to drain from source. Therefore drain current I_D reduces with increase in $-V_{GS}$.

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3. Operation of n-channel JFET for large value of negative V_{GS} :

As the negative voltage V_{GS} is further increased, the depletion regions spread more into the n-type bar. At a certain value of negative V_{GS}, the depletion regions touch each other as shown in Fig. 2-Q. 2(a)(c). At this point the channel width is zero and therefore the drain current $I_D = 0$. This gate to source voltage at which the drain current is cutoff is called as $V_{GS\,(off)}$.

Thus with increase in the negative gate to source voltage, the channel becomes more and more narrow and drain current I_D reduces. Thus for $V_{GS} = 0$, maximum drain current I_{DSS} will flow through JFET. The drain current then reduces with increase in the negative gate to source bias. Thus JFET is a voltage controlled device.

Cutoff voltage $V_{GS\,(off)}$:

The value of V_{GS} that makes the drain current I_D approximately equal to zero is called as cutoff voltage and it is denoted by $V_{GS\,(off)}$. A JFET must be operated between $V_{GS} = 0$ and $V_{GS\,(off)}$. For this range I_D will change between I_{DSS} and 0 respectively.

Drain characteristics of an n-channel JFET : Please refer Q. 2(a) of May 2014.

Q. 3(a) Explain the different methods of biasing JFET along with their characteristics in detail. **(10 Marks)**

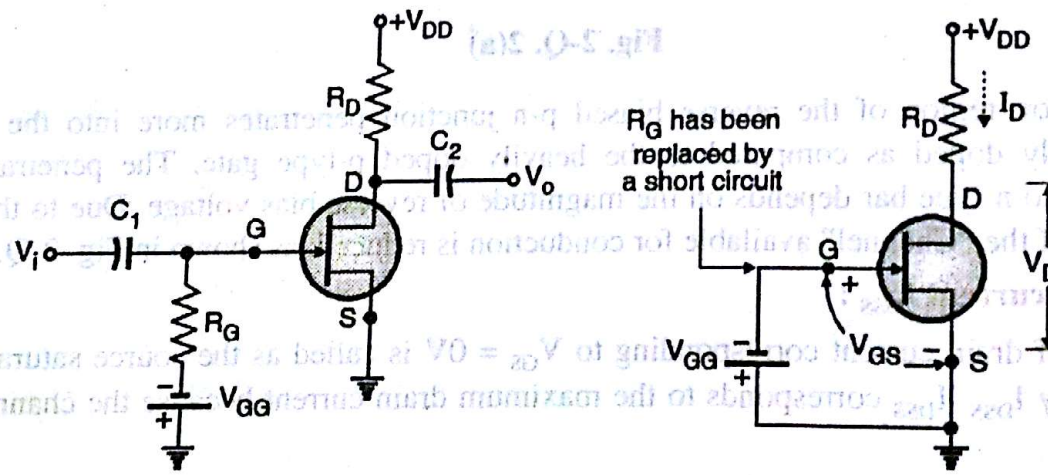
Ans. : Different methods of JFET biasing :

The commonly used biasing circuits for FET are :

1. Fixed bias circuit.
2. Self bias circuit.
3. Voltage divider bias circuit.
4. Source bias.
5. Current source biasing.

1. Fixed bias configuration :

The simplest biasing arrangement for the n-channel JFET is fixed bias configuration as shown in Fig. 1-Q. 3(a)(a). The capacitors C_1 and C_2 are the coupling capacitors which are used for coupling the ac signal to the input of the circuit and amplified ac signal from the output of the circuit. However for the dc analysis, these capacitors are equivalent to "open circuits".



(a) Fixed bias configuration for n channel JFET **(b) Simplified fixed bias configuration for dc analysis**

Fig. 1-Q. 3(a)

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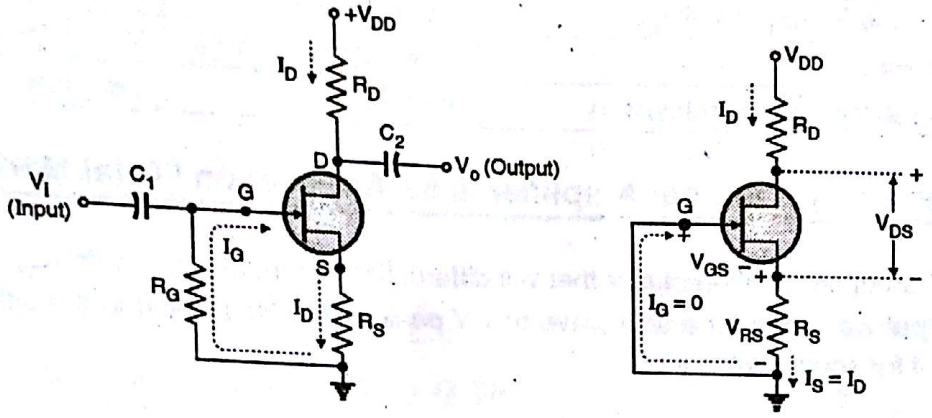
For dc analysis $I_G = 0$. Therefore the voltage drop across R_G i.e. $I_G R_G = 0$. This will allow us to replace R_G by a short circuit for the dc analysis.

2. Self bias configuration :

The self bias configuration for FET is as shown in Fig. 2-Q. 3(a). This configuration needs only one dc power supplies. This is its advantage over the fixed bias circuit.



(a) Self bias configuration **(b) Simplified DC equivalent circuit**

Fig. 2-Q. 3(a)

DC Analysis of the self bias circuit :

For the dc analysis, capacitors C_1 and C_2 will be considered as open circuits and the resistor R_G will be replaced by a short circuit as $I_G = 0$ as explained earlier. The simplified DC equivalent circuit is as shown in Fig. 2-Q. 3(a)(b). We will use this circuit for the analysis of self bias circuit.

3. Voltage divider biasing for a JFET :

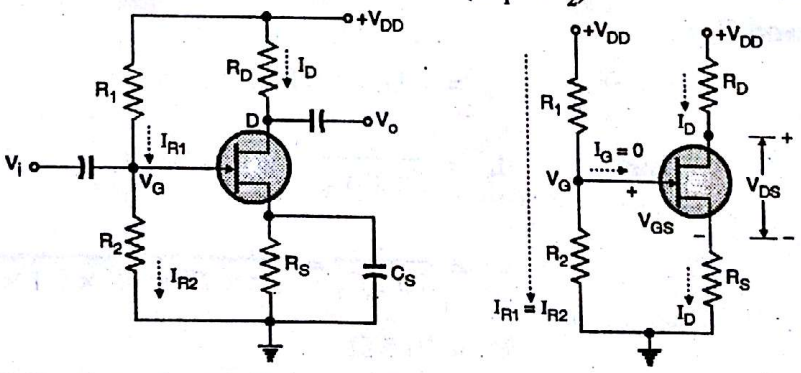
The voltage divider biasing for a JFET amplifier is as shown in Fig. 3-Q. 3(a)(a). This configuration is exactly same as the one used for biasing the transistor but its dc analysis will be entirely different. In the dc analysis of this circuit we will assume that $I_G = 0$. The coupling capacitors C_1, C_2 and C_S are assumed to be "open circuit" for the dc analysis. In addition the source voltage V_{DD} is separated into two equivalent sources.

The simplified voltage divider biasing circuit for dc analysis is as shown in Fig. 3-Q. 3(a)(b). Looking at Fig. 3-Q. 3(a)(b) we can write that,

$$I_{R1} = I_{R2} \quad \text{because} \quad I_G = 0$$

and

$$I_{R1} = I_{R2} = \frac{V_{DD}}{(R_1 + R_2)} \qquad ...(1)$$



(a) Voltage divider biasing for FET **(b) DC equivalent circuit**

Fig. 3-Q. 3(a)

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Q. 6(c) Compare class A and class C power amplifiers. **(5 Marks)**

Ans. : Comparison of class A and class C power amplifiers :

Sr. No.	Parameter	Class A	Class C
1.	Conduction angle of collector current.	360° or full cycle.	Less than 180°.
2.	Position of Q point on the load line.	At the center.	Below the X-axis.
3.	Distortion in output voltage	No distortion.	More than A, B and AB.
4.	Efficiency.	Lowest 25% to 50%.	Very high (95%).
5.	Power dissipation in transistors	Very high	Very low

Chapter 2 : Operational Amplifier & its Application [Total Marks 15]

Q. 2(b) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz. Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator. Also repeat it for square wave input. **(10 Marks)**

Ans. :

Part I : Design of the differentiator :

Given : $f_{max} = 1$ kHz.

The steps to be followed to design a differentiators are :

Step 1 : Select "f_a" equal to the highest frequency of the input signal.

Step 2 : Assume a value of $C_1 < 1\ \mu F$ and calculate R_F.

Step 3 : Select $f_b = 20\ f_a$ and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Step 1 : Select "f_a" and calculate R_F :

$$f_a = 1 \text{ kHz as the highest input frequency is 1 kHz.}$$

$$\text{Let} \quad C_1 = 0.1\ \mu F.$$

$$\text{But} \quad f_a = \frac{1}{2\pi R_F C_1}$$

$$\therefore \quad R_F = \frac{1}{2\pi f_a C_1} = \frac{1}{2\pi \times 1 \times 10^3 \times 0.1 \times 10^{-6}}$$

$$\therefore \quad R_F = 1.59\ k\Omega$$ ...Ans.

Step 2 : Calculate R_1 and C_F :

$$f_b = 20\ f_a = 20 \text{ kHz}$$

$$\text{But} \quad f_b = \frac{1}{2\pi R_1 C_1}$$

$$\therefore \quad R_1 = \frac{1}{2\pi f_b C_1} = \frac{1}{2\pi \times 20 \times 10^3 \times 0.1 \times 10^{-6}}$$

$$\therefore \quad R_1 = 79.5\ \Omega$$ ...Ans.

Let us use the standard value of 82 Ω.

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As $R_1 C_1 = R_F C_F$

$$C_F = \frac{82 \times 0.1 \times 10^{-6}}{1.59 \times 10^3} = 0.00515\ \mu F$$ ...Ans.

Let C_F be 0.005 μF. And finally,

$$R_{comp} = R_F = 1.59\ k\Omega \approx 1.5\ k\Omega.$$

Thus the component values are as follows :

$R_1 = 82\ \Omega$

$R_{comp} = 1.5\ k\Omega$

$C_F = 0.005\ \mu F$

$R_F = 1.59\ k\Omega$

$C_1 = 0.1\ \mu F$

The circuit diagram is as shown in Fig. 1-Q. 2(b).

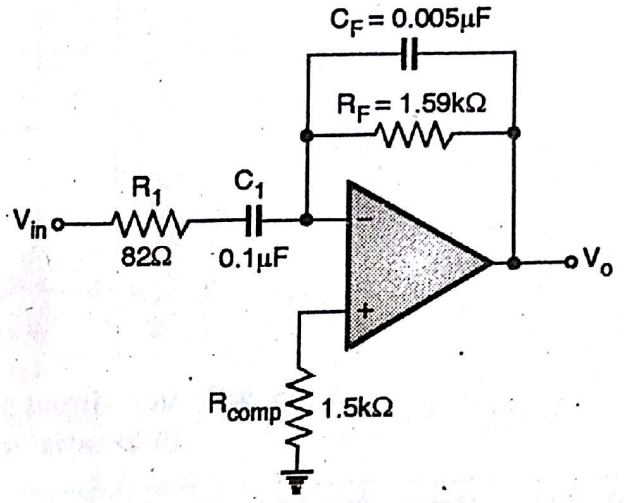

Fig. 1-Q. 2(b) : Designed circuit

Part II : To draw the waveforms :

For an inverting differentiator,

$$V_o = -R_F C_1 \frac{d V_{in}}{dt} \quad ...(1)$$

But, $V_{in} = 1 \sin (2\pi \times 100\ t)$

$$= 2 \sin (200\pi t) \quad ...(2)$$

From the Fig. 2-Q. 2(b) values of R_F and C_1 are :

$R_F = 1.59\ k\Omega$ and

$C_1 = 0.005 \times 10^{-6}\ F$

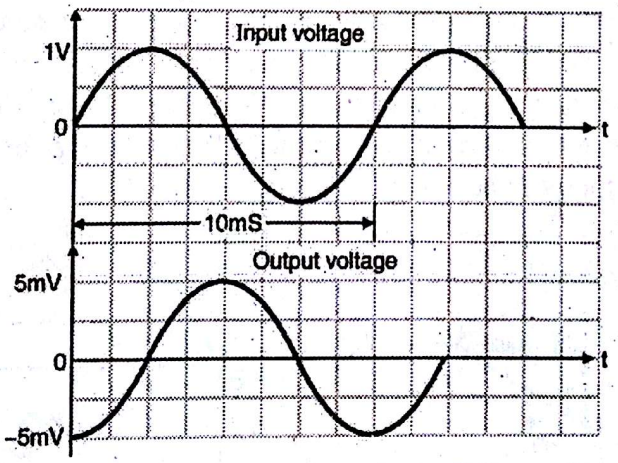

Fig. 2-Q. 2(b) : Waveforms for a differentiator

Substituting these values into Equation (1) we get,

$$V_o = -1.59 \times 10^{+3} \times 0.005 \times 10^{-6} \cdot \frac{d}{dt}[1 \sin (200\pi\ t)]$$

$$= 7.95 \times 10^{-6} \times 200\ \pi\ [\cos (200\ \pi\ t)]$$

$$= -5 \times 10^{-3} \cos (200\ \pi\ t)$$ ...Ans.

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This is a cosine wave with a peak voltage of 5 mV and frequency of 100 Hz. The input and output waveforms are as shown in Fig. 2-Q. 2(b).

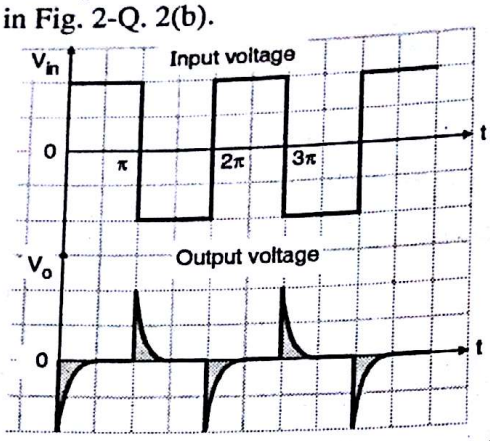


Fig. 3-Q. 2(c) : Input and output voltage waveforms of a differentiator for a square wave input

Q. 3(c) Draw and explain op-amp inverting comparator. Draw input and output waveforms for $V_{ref} > 0$ and also for $V_{ref} < 0$. **(5 Marks)**

Ans. : Inverting comparator :

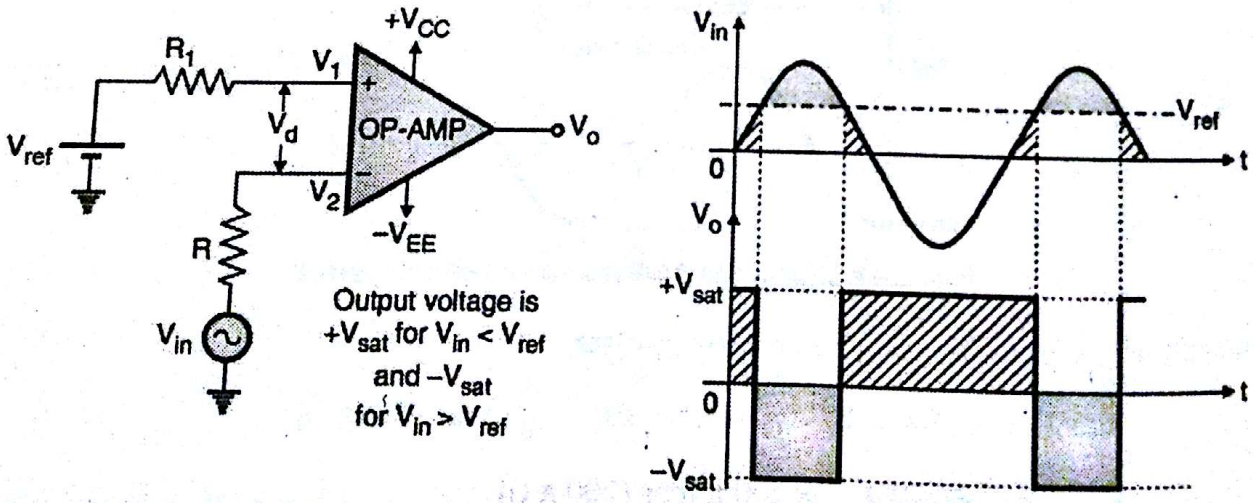
The schematic diagram of an inverting comparator is as shown in Fig. 1-Q. 3(c)(a) and the relevant waveforms are as shown in Fig. 1-Q. 3(c)(b). Note that the reference voltage V_{ref} has now been applied to the non-inverting (+) terminal and the input voltage is applied to the inverting (–) terminal.

Operation of the circuit : Assume the OP-AMP to have a very high input resistance. Hence the currents flowing through the resistors R_1 and R of Fig. 1-Q. 3(c)(a) is very small. Hence the voltage drop across them is close to zero.

$$\therefore \quad V_1 = V_{ref} \text{ and } V_2 = V_{in}$$

$$\therefore \text{ Differential input voltage } \quad V_d = V_1 - V_2 = (V_{ref} - V_{in})$$

When V_{in} is less than V_{ref}, the voltage at the non-inverting (+) terminal is higher than the voltage at the inverting (–) terminal. This makes the differential input voltage V_d positive and the OP-AMP output will swing to + $V_{(sat)}$. When V_{in} is greater than V_{ref}, the voltage at the inverting (–) terminal is greater than the voltage at the non-inverting (+) terminal. Therefore the differential input voltage V_d is negative and the OP-AMP output will be – $V_{(sat)}$.



(a) Inverting comparator **(b) Input and output voltage waveforms**

Fig. 1-Q. 3(c)

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If the reference voltage is made negative ($-V_{ref}$) then the input and output voltage waveforms gets modified as shown in Fig. 2-Q. 3(c).

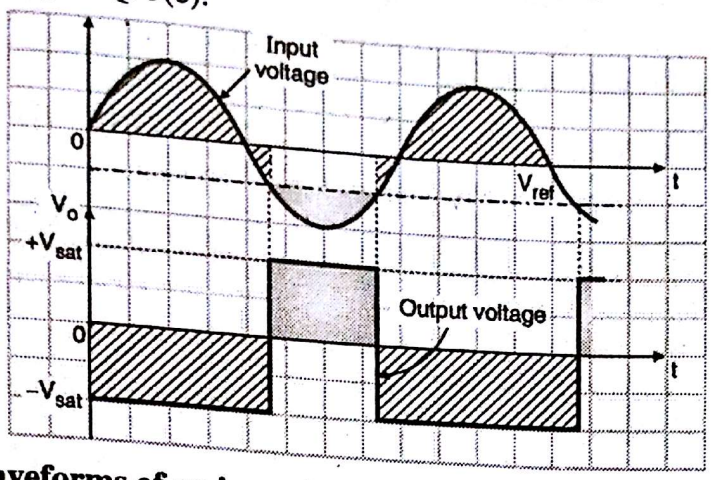

Fig. 2-Q. 3(c) : Waveforms of an inverting comparator for a negative reference voltage

Chapter 4 : Modulation [Total Marks - 20]

Q. 1(d) Discuss the factors that influence modulation index of an FM wave. **(5 Marks)**

Ans. : The modulation index of an FM wave is defined as :

$$m_f = \frac{\text{Maximum frequency deviation}}{\text{Modulating frequency}} \quad ...(1)$$

$$\therefore \quad m_f = \frac{\delta}{f_m} \quad ...(2)$$

The factors that influence modulation index are deviation (δ) and modulating frequency (f_m). The modulation index (m_f) is very important in FM because it decides the bandwidth of the FM wave (discussed later on). The modulation index also decides the number of sidebands having significant amplitudes. In AM the maximum value of the modulation index m is 1. But for FM the modulation index can be greater than 1. The modulation index m_f is measured in radians.

Q. 4(b) What is DSBSC wave ? Explain its generation using balanced modulator. **(10 Marks)**

Ans. : DSB-SC or DSB or AM-SC Signal :

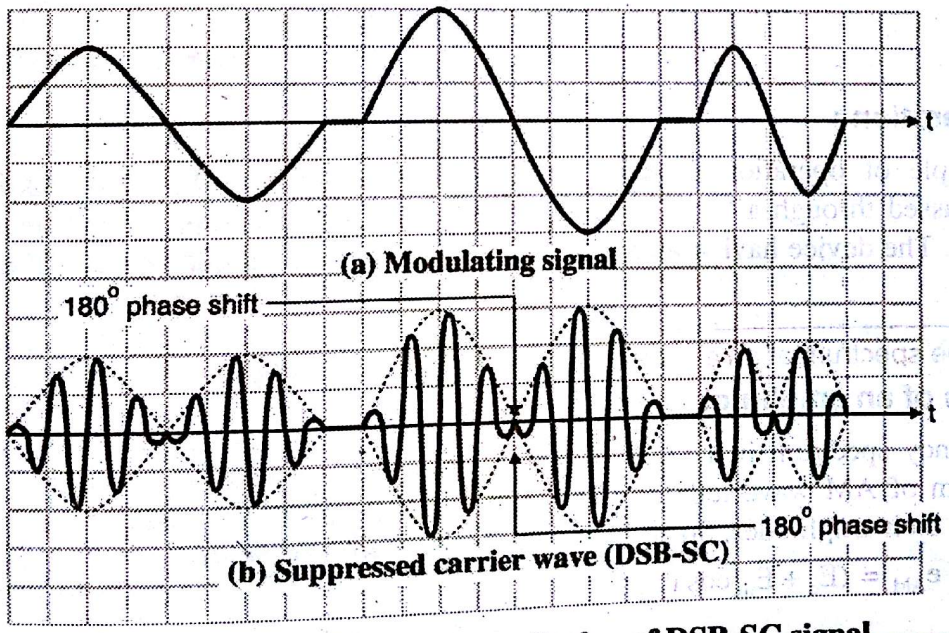

Fig. 1-Q. 4(b) : Time domain display of DSB-SC signal

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From the AM wave (DSB-FC) if only the carrier component is suppressed then the remaining signal is called as DSBSC (double sideband suppressed carrier) signal. The time domain display of DSB-SC signal is as shown in Fig. 1-Q. 4(b) and the spectrum of this signal is as shown in Fig. 2-Q. 4(b). If m = 1 then the percent power saving in DSBSC is given by,

$$\% \text{ Power saving} = \frac{[m^2/2]\,P_c \times 100}{\left[1+\frac{m^2}{2}\right]P_c} = \frac{0.5}{1.5} \times 100 \times = 66.667\%$$

Thus DSB-SC is a power efficient system as compared to DSB-FC.

However as both the sidebands are being transmitted, the BW of DSB-SC system is still 2 f_m i.e. same as that of AM wave.

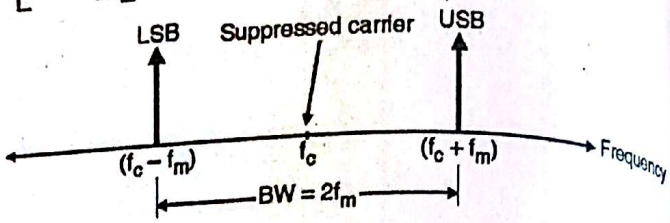

Fig. 2-Q. 4(b) : Frequency spectrum of DSB-SC signal

DSB-SC signal :

1. The spectrum of DSB signal contains only two sidebands but the carrier is not present. Hence some power saving does take place.
2. But the bandwidth of DSB signal is same as that of DSB-FC signal i.e. BW = 2 f_m. Hence DSB-SC system is equally bad when it comes to the bandwidth requirement is concerned.

Generation of DSB-SC using balanced modulator :

The nonlinear modulators are also known as the balanced modulators.

The balanced modulators are used to suppress the unwanted carrier in an AM wave.

The carrier and modulating signals are applied to the inputs of the balanced modulator and we get the DSB signal with suppressed carrier at the output of the balanced modulator.

Thus the output consists of the upper and lower sidebands only.

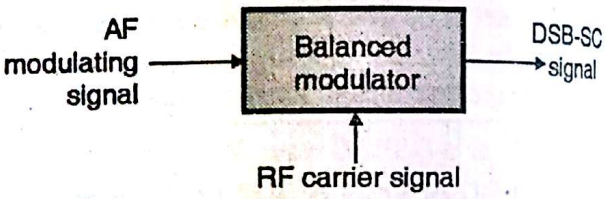

Fig. 3-Q. 4(b) : Block diagram of balanced modulator

Principle of operation :

The principle of operation of a balanced modulator states that if two signals at different frequencies are passed through a "nonlinear resistance" then at the output we get an AM signal with suppressed carrier. The device having a nonlinear resistance can be a diode or a JFET or even a bipolar transistor.

Q. 6(b) Draw the spectrum of an amplitude modulated wave and explain its components. **(5 Marks)**

Ans. : Spectrum of an amplitude modulated wave :

The frequency spectrum is a graph of amplitude on Y axis versus frequency on X axis. The frequency spectrum of AM wave tells us about which frequency components are present in the AM wave and what are their amplitudes. So consider the equation for AM wave.

$$e_{AM} = (E_c + E_m \cos \omega_m t) \cos \omega_c t$$

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$$E_c = \left[1 + \frac{E_m}{E_c}\cos\omega_m t\right]\cos\omega_c t$$

As per the definition of the modulation index, $m = E_m / E_c$.

$$\therefore \quad e_{AM} = E_c(1 + m\cos\omega_m t)\cos\omega_c t \qquad ...(1)$$

Simplifying we get,

$$e_{AM} = E_c\cos\omega_c t + m E_c \cos\omega_m t \cos\omega_c t \qquad ...(2)$$

For the second term in the above expression use the following standard identity :

$$2\cos A\cos B = \cos(A+B) + \cos(A-B)$$

Therefore Equation (2) gets simplified as follows :

$$e_{AM} = \underbrace{E_c\cos\omega_c t}_{\text{Carrier}} + \underbrace{\frac{m E_c}{2}\cos(\omega_c + \omega_m)t}_{\text{Upper sideband}} + \underbrace{\frac{m E_c}{2}\cos(\omega_c - \omega_m)t}_{\text{Lower sideband}} \qquad ...(3)$$

Observations :

The expression for the AM wave shows that it consists of three terms :

1. First term is nothing else but the unmodulated carrier signal.
2. The second term is a sinusoidal signal at frequency ($f_c + f_m$). This is called as the upper sideband (USB). Its amplitude is $\frac{m E_c}{2}$.
3. The third term represents a sinusoidal signal at frequency ($f_c - f_m$). It is called as the lower sideband (LSB). Its amplitude is $\frac{m E_c}{2}$.

Hence the frequency spectrum of an A.M. wave is as shown in Fig. Q. 6(b). Note that it is a single sided spectrum i.e. the spectrum plotted for only the positive values of frequency.

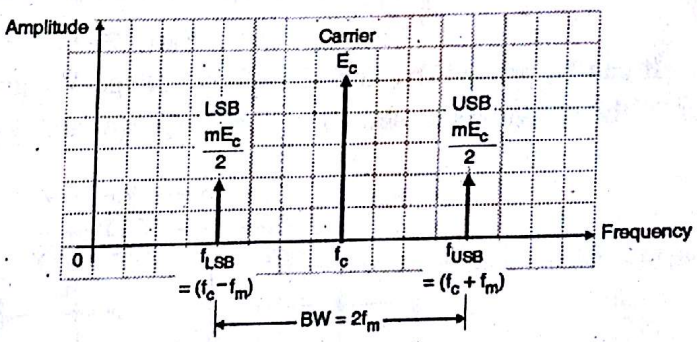

Fig. Q. 6(b) : Single sided frequency spectrum of AM wave

Chapter 5 : Demodulation [Total Marks - 20]

Q. 4(a) Draw Foster Seeley discriminator with circuit diagram and explain its working with phasor diagrams. **(10 Marks)**

Ans. : Foster Seeley discriminator :

The phase discriminator or Foster Seeley discriminator is as shown in Fig. 1-Q. 4(a). If you compare this circuit with the balanced slope detector circuit then you will find that the diode and load arrangement is same in both the circuits. But the method of applying the input voltage to the diodes

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which is proportional to the frequency deviation is entirely different. The Foster Seeley discriminator is thus derived from the balanced modulator.

Here the primary and the secondary windings both are tuned to the same center frequency "f_c" of the incoming signal. This simplifies the tuning process to a great extent and it will yield better linearity than the balanced slope detector.

Principle of operation :

Even though the primary and secondary tuned circuits are tuned to the same center frequency, the voltages applied to the two diodes D_1 and D_2 are not constant.

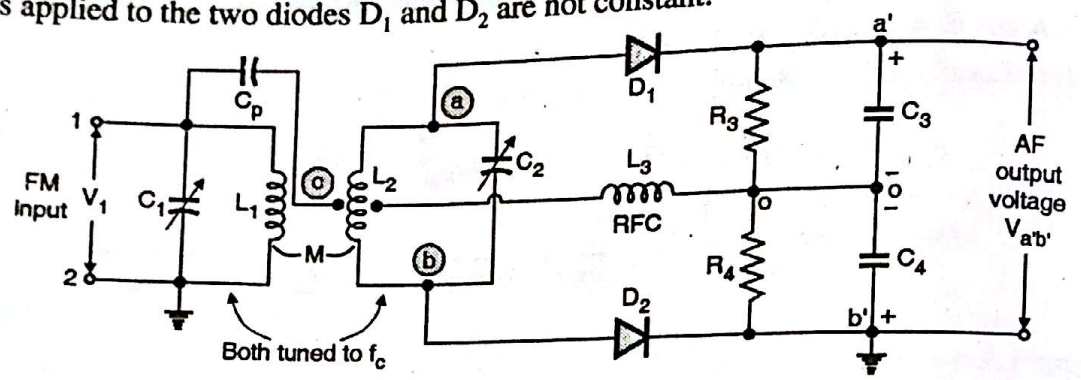

Fig. 1-Q. 4(a) : Phase discriminator

They vary depending on the frequency of the input signal. This is due to the change in phase shift between the primary and secondary windings depending on the input frequency.

Operation : The phase discriminator can be redrawn as shown in Fig. 2-Q. 4(a) to understand the concept of its operation. The capacitor C_p is a coupling capacitor which passes all the frequencies at the input to the center tap of the transformer secondary. C_4 will bypass resistance R_4 as $R_4 >> X_{C4}$. Therefore voltage across RFC will be equal to the input voltage V_1.

$$V_{RFC} = V_1 \quad ...(1)$$

It can be proved that the secondary voltage V_{ab} gets divided equally across the upper and lower halves of the secondary as shown in Figs. 2-Q. 4(a) and 3-Q. 4(a).

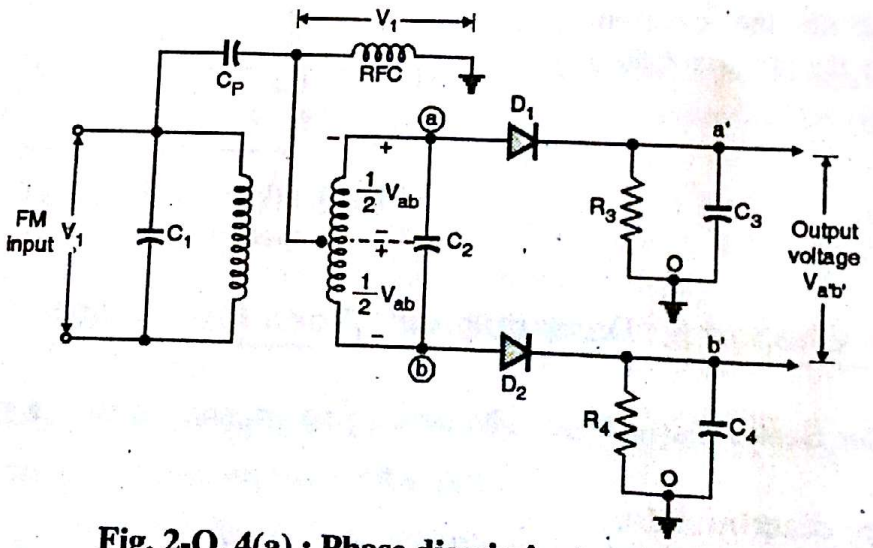

Fig. 2-Q. 4(a) : Phase discriminator redrawn

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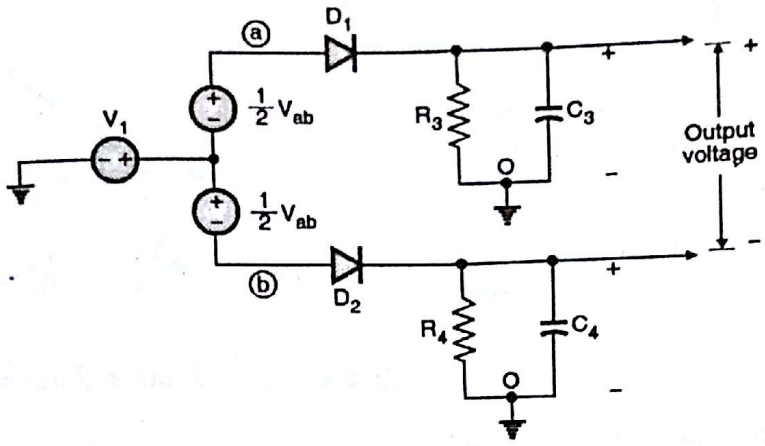

Fig. 3-Q. 4(a) : Equivalent circuit of phase discriminator

Thus input to each diode is equal to the vector sum of the primary voltage V_1 and half the secondary voltage i.e. $\left(\frac{1}{2}V_{ab}\right)$. Vector sum should be taken because these voltages are not in phase with each other. Phase shift between the primary and secondary voltages is not constant but it depends on the input frequency. The effect of this is as explained below.

Output voltage of the discriminator :

Output voltage of the phase discriminator is equal to the difference between the outputs of the two diode rectifiers.

$$\therefore \quad V_o = V_{a'b'} = V_{a'o} - V_{b'o} \qquad ...(2)$$

As the diode drops are not known, we cannot calculate the output exactly. But it is sure that the output will be proportional to the voltage applied at the inputs of diodes D_1 and D_2.

$$\therefore \quad V_o \propto V_{ao} - V_{bo} \qquad ...(3)$$

1. Output voltage at $f_{in} = f_c$:

When the input frequency is equal to the center frequency (f_c), the phase shift between the primary and secondary voltages is exactly 90°.

Therefore the input voltages to both the diodes will be equal as shown in Fig. 4-Q. 4(a). Therefore the outputs of both the diodes will be equal. Hence the net output voltage will be zero.

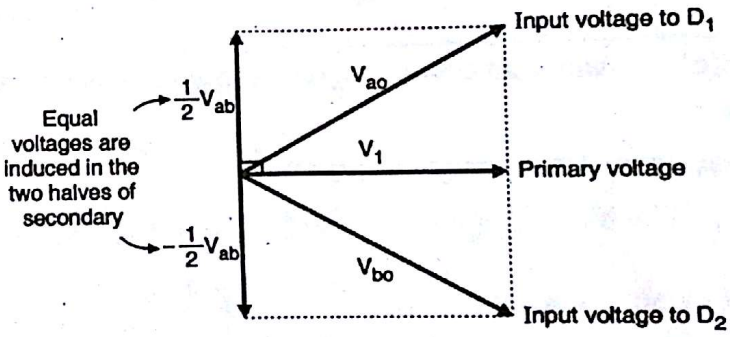

Fig. 4-Q. 4(a) : Phasor diagram for $f_{in} = f_c$

2. Output voltage for $f_{in} > f_c$:

At input frequencies above the center frequency f_c, secondary voltage V_{ab} leads the primary voltage V_1 by less than 90°.

Hence input voltage to D_1 i.e. V_{ao} is higher than input to D_2 i.e. V_{bo}. The output voltage will therefore be positive for $f_{in} > f_c$.

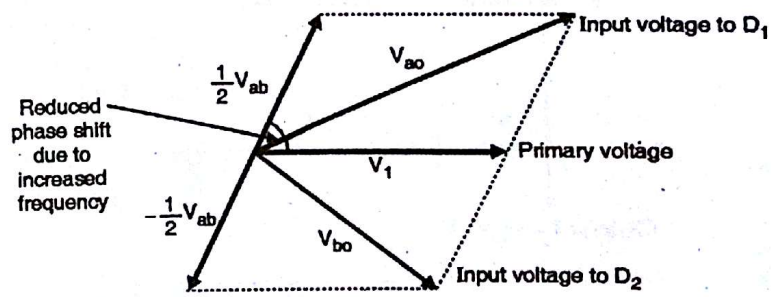

Fig. 5-Q. 4(a) : Phasor diagram for $f_{in} > f_c$

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3. Output voltage for $f_{in} < f_c$:

For input frequencies below the center frequency f_c, the secondary voltage V_{ab} leads the primary voltage V_1 by more than 90° as shown in Fig. 6-Q. 4(a).

Hence input voltage to D_1 is less than input voltage to D_2. Therefore the output voltage will be negative for $f_{in} < f_c$.

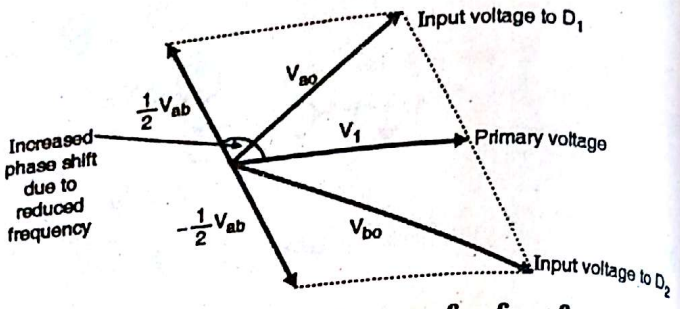

Fig. 6-Q. 4(a) : Phasor diagram for $f_{in} < f_c$

Q. 5(b) In an AM radio receiver the loaded Q of the antenna circuit at the input to the mixer is 100. If the intermediate frequency is 455 kHz, calculate the image frequency and its rejection at 1 MHz. **(5 Marks)**

Ans. :

Given : $Q = 100$, $IF = 455$ kHz, $f_s = 1$ MHz $= 1000$ k.

Step 1 : **Calculate image frequency :**

$$f_{si} = f_s + 2\,IF = 1000000 + 2\,(455 \times 10^3)$$

$$= 1910 \text{ kHz}$$ ...Ans.

Step 2 : **Calculate image frequency ratio :**

$$\rho = \frac{f_{si}}{f_s} - \frac{f_s}{f_{si}} = \frac{1910}{1000} - \frac{1000}{1910} = 1.386$$

Image frequency rejection ratio $\alpha = \sqrt{1 + Q^2 \rho^2}$

$$= \sqrt{1 + (100^2 \times 1.386^2)}$$

$$\therefore \alpha = 138.6$$ ...Ans.

Q. 5(c) With neat circuit diagram explain the use of PLL in frequency translator. **(5 Marks)**

Ans. :

Frequency translator using PLL :

The block diagram of PLL used as a frequency translator is shown in Fig. 1-Q. 5(c).

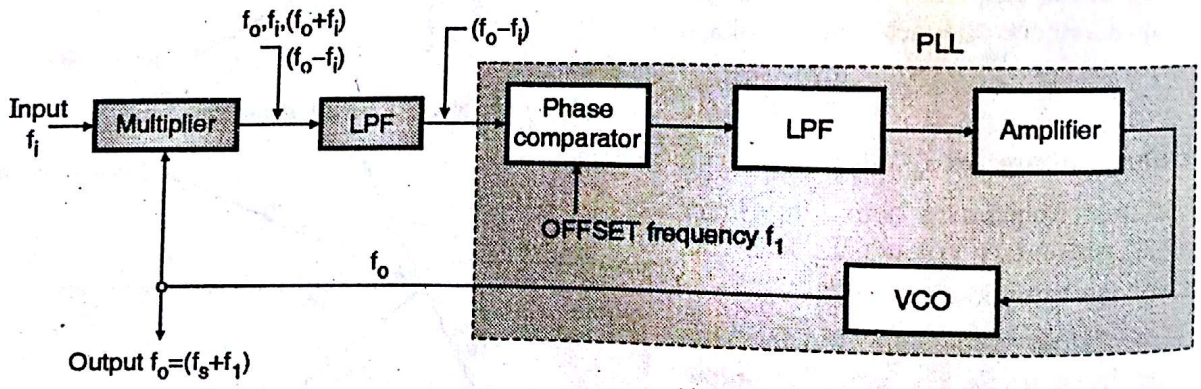

Fig. 1-Q. 5(c) : PLL for frequency translation

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A multiplier (or a mixer) alongwith a low pass filter is connected externally at the input of a PLL as shown in Fig. 1-Q. 5(c). The input signal f_i, the frequency of which is to be translated is connected at the input of the mixer.

The other input to the mixer is coming from the VCO output, at frequency f_o. At the mixer output, we get the following frequency components :

f_o, f_i, $(f_o + f_i)$ and $(f_o - f_i)$.

The low pass filter will allow only the $(f_o - f_i)$ component to pass through it and blocks all the other components.

This signal and the offset frequency signal at frequency f_1 are applied to the phase comparator. When the PLL is in the locked state, it will try to adjust the VCO frequency such that,

$$f_o - f_i = f_1 \quad \text{or} \quad f_o = (f_1 + f_i) \qquad ...(1)$$

Thus the frequency of the output signal is automatically adjusted to $(f_1 + f_i)$. The input frequency is thus shifted (or offsetted) by f_1 Hz. This frequency translator can be implemented using PLL 565 as shown in Fig. 2-Q. 5(c).

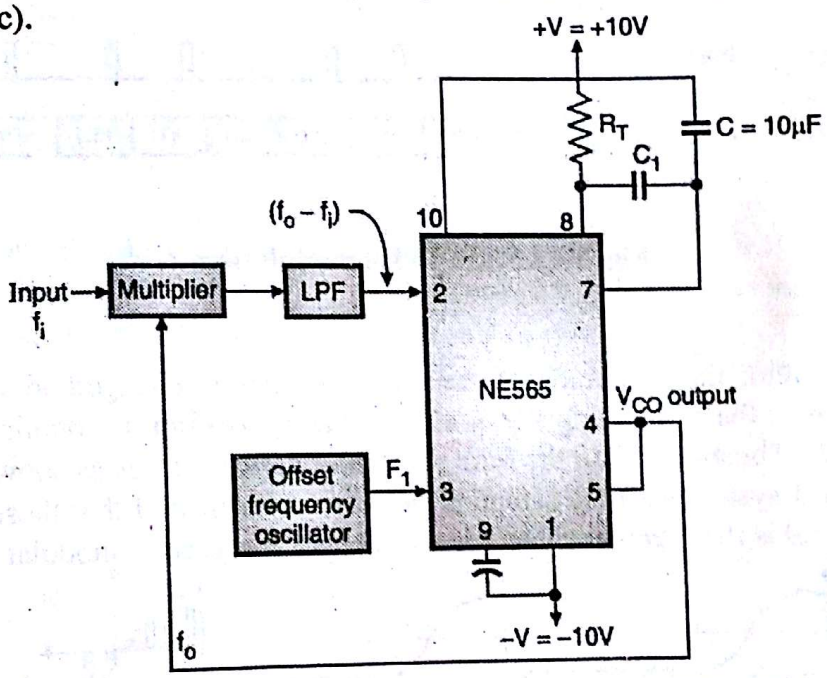

Fig. 2-Q. 5(c) : Frequency translator using PLL 565

Chapter 6 : Analog Pulse Modulation [Total Marks - 10]

Q. 5(a) Draw the PAM, PWM and PPM waveforms in time domain assuming a sinusoidal modulating signal. Explain them in brief. **(10 Marks)**

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Ans. :

Waveforms :

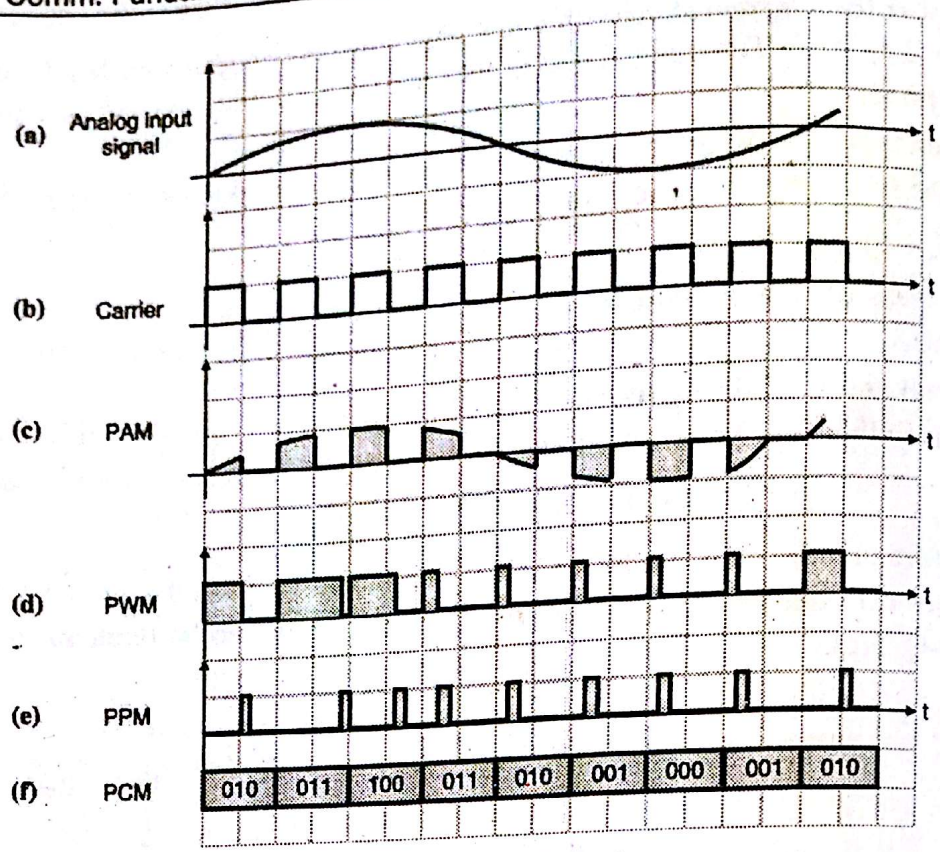

Fig. 1-Q. 5(a) : Pulse modulation

1. PAM :

In the PAM system, the amplitude of the pulsed carrier is changed in proportion with the instantaneous amplitude of the modulating signal x(t). So the information is contained in the amplitude variation of PAM signal. The carrier is in the form of train of narrow pulses as shown in Fig. 2-Q. 5(a). If you compare the PAM system with the sampling process, you will find that these two processes are identical. The PAM signal is then sent by either wire or cable or it is used to modulate a carrier.

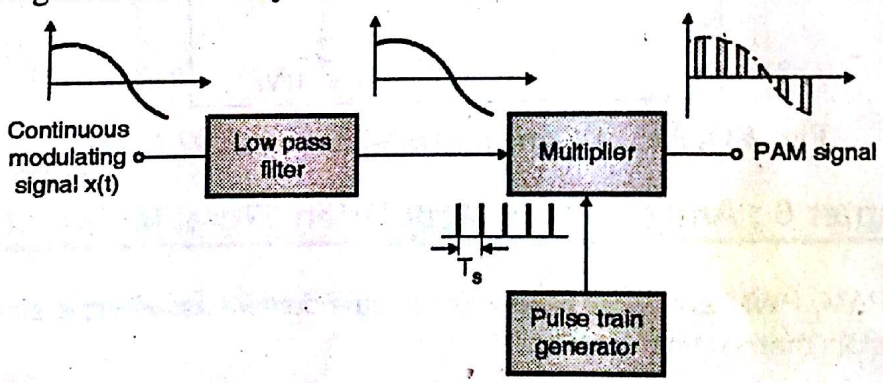

Fig. 2-Q. 5(a) : Generation of PAM

2. PWM :

The other type of a pulse analog modulation is the pulse width modulation (PWM). In PWM, the width of the carrier pulses varies in proportion with the amplitude of modulating signal. The waveforms of PWM are as shown in Fig. 3-Q. 5(a). As seen from the waveforms, the amplitude and the frequency of the PWM wave remains constant. Only the width changes. That is why the "information" is contained in the width variation. This is similar to FM. As the noise is normally "additive" noise, it changes the amplitude of the PWM signal.

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At the receiver, it is possible to remove these unwanted amplitude variations very easily by means of a limiter circuit. As the information is contained in the width variation, it is unaffected by the amplitude variations introduced by the noise. Thus the PWM system is more immune to noise than the PAM signal.

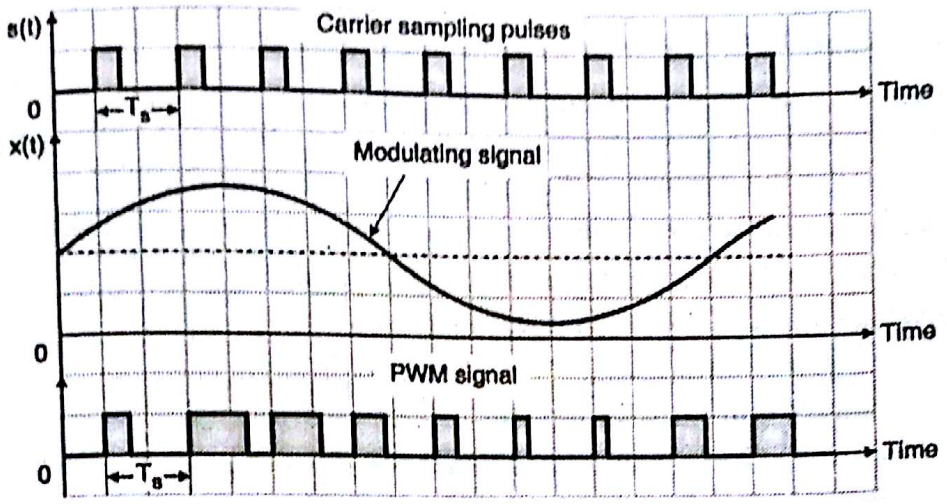

Fig. 3-Q. 5(a) : PWM signal [Trail edge modulated signal]

3. PPM :

In PPM the amplitude and width of the pulsed carrier remains constant but the position of each pulse is varied in proportion with the amplitudes of the sampled values of the modulating signal. The position of the pulses is changed with respect to the position of reference pulses. The PPM pulses can be derived from the PWM pulses as shown in Fig. 4-Q. 5(a). Note that with increase in the modulating voltage the PPM pulses shift further with respect to reference. The vertical dotted lines drawn in Fig. 5-Q. 5(a) are treated as reference lines to measure the shift in position of PPM pulses. The leading edge of each PPM pulse coincides with the trailing pulse of a PWM pulse.

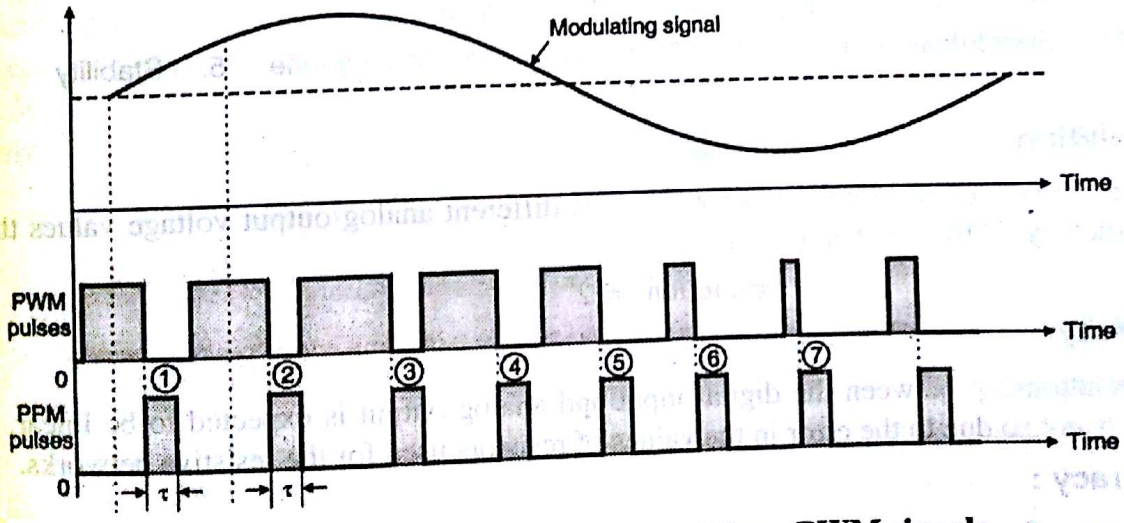

Fig. 5-Q. 5(a) : PPM pulses generated from PWM signal

The PPM pulses marked 1, 2 and 3 etc. in Fig. 5-Q. 5(a) go away from their respective reference lines. This is corresponding to increase in the modulating signal amplitude. Then as the modulating voltage decreases the PPM pulses 4, 5, 6, 7 come progressively closer to their respective reference lines.

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Chapter 7 : Digital Modulation Techniques [Total Marks - 05]

Q. 1(c) How is adaptive delta modulation superior to delta modulation ? **(5 Marks)**

Ans. :

Adaptive delta modulation is superior to delta modulation :

In the ADM system, the step size is not constant. Rather when the slope overload occurs the step size becomes progressive larger and therefore x′ (t) will catch up with x (t) more rapidly. Whenever the slope of input signal is large, the step size of the staircase approximated signal x′ (t) is increased.

On the other hand when the input signal is varying slowly the step size is reduced.

1. Thus the step size is adapted as per the level of input signal.
2. Reduction in slope overload distortion and granular noise.
3. Improvement in signal to noise ratio.
4. Wide dynamic range due to variable step size.
5. Better utilization of bandwidth as compared to delta modulation.
6. Low signaling rate.
7. Simplicity of implementation.

Chapter 8 : Multiplexing [Total Marks - 10]

Q. 6(a) What do you understand by signal multiplexing ? Explain TDM and FDM with suitable examples. **(10 Marks)**

Ans. : **Please refer Q. 6(a) of Dec. 2014.**

Appendix-A : D/A and A/D Converters[Total Marks : 10]

Q. 1(b) Comment on the following ADC / DAC specifications :

1. Resolution 2. Linearity 3. Accuracy 4. Settling time 5. Stability **(5 Marks)**

Ans. :

1. Resolution :

The definition of resolution is the number of different analog output voltage values that can be provided by a DAC. For an n-bit DAC,

$$\text{Resolution} = 2^n \quad ...(1)$$

2. Linearity :

The relationship between the digital input and analog output is expected to be linear. However practically it is not so due to the error in the values of resistors used for the resistive networks.

3. Accuracy :

Accuracy of a DAC indicates how close the analog output voltage is to its theoretical value. In short it indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the values of resistors used in the ladder, and the precision of the reference voltage used.

4. Settling time :

The time required to settle the analog output within 1/2 LSB of the final value, from the instant of change in digital input is called as settling time. The settling time should be as short as possible.

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5. **Stability :** The ideal requirement is that the analog output voltage of D to A converter should not change due to changes in temperature. But practically the analog output is a function of temperature. It is so because the resistance values and OP-AMP parameters change with changes in temperature.

Q. 3(b) Explain any one technique used of conversion of analog signal to digital with ADC. **(5 Marks)**

Ans. :

Counter type ADC :

Principle of operation :

For this type of A to D converter, we use a D to A converter i.e. DAC. Here the digital input to this DAC is adjusted until the DAC's output comes within ± (1/2) LSB of the analog output of DAC i.e. V_A.(This V_A is to be converted into a digital form by the ADC). The circuit diagram of counter type ADC is as shown in Fig. 1-Q. 3(b).

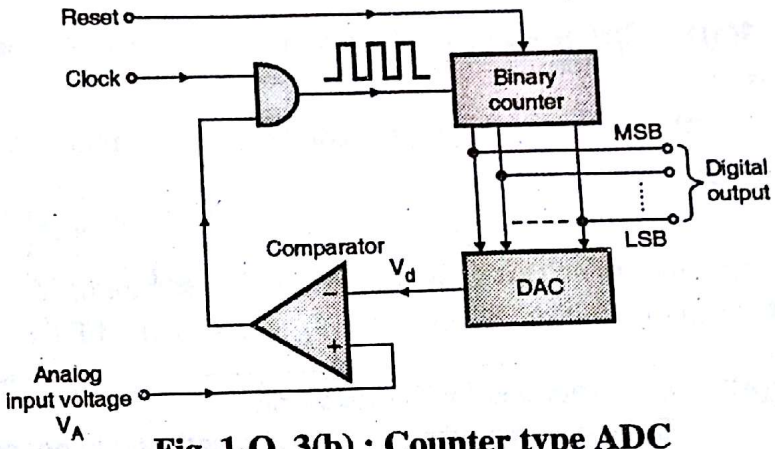

Fig. 1-Q. 3(b) : Counter type ADC

Operation : Fig. 1-Q. 3(b) shows an n-bit counter type ADC. The counter is Reset to zero first, by applying a reset pulse. Then after releasing the Reset pulse, the Clock pulses are applied to the counter through an AND gate. Initially the DAC output is zero. Therefore the analog input voltage V_A is higher than the DAC output V_d i.e. ($V_A > V_d$). The comparator output is high and the AND gate is enabled. Thus the clock pulses are allowed to pass through the AND gate to the counter. The counter starts counting these clock pulses, its output goes on increasing. As the counter output acts as input to DAC, the DAC output (which is a staircase waveform) also increases. As long as DAC output $V_d < V_A$, this process will continue, as the comparator output remains high enabling the AND gate, so that the clock pulses are allowed to pass through to the counter. However as soon as the DAC output is higher than the input analog voltage ($V_d > V_A$), the comparator output becomes low. This will disable the AND gate and stop the clock pulses. Thus the counting stops as shown in Fig. 2-Q. 3(b). The digital output of the counter then represents the analog input voltage V_A. When the analog input voltage is changed to a new value, a second reset pulse is applied to the counter to clear it and the counting begins again as shown in Fig. 2-Q. 3(b).

Waveform :

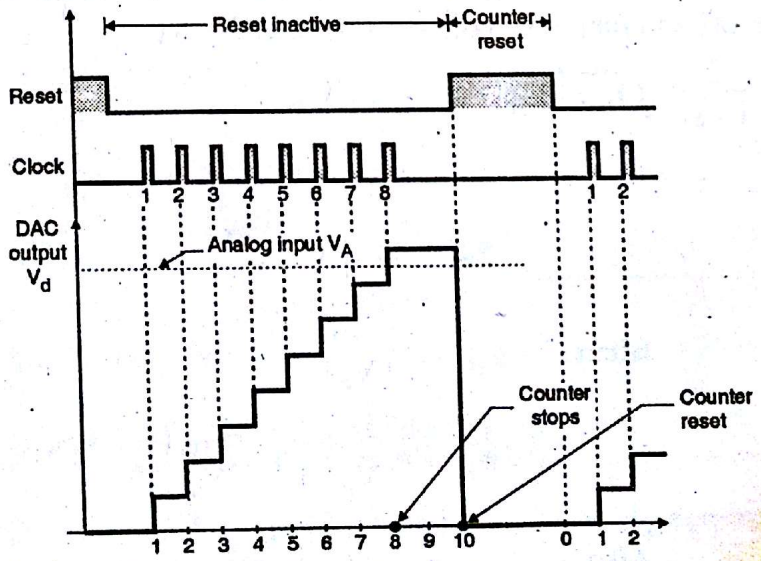

Fig. 2-Q. 3(b) : Waveforms for counter type ADC

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Dec. 2015

Chapter 1 : Electronic Circuits [Total Marks - 30]

Q. 1(a)1. Give reasons for the following : FET is called as a square law device. **(5 Marks)**

Ans. :

We know that the expression for drain current of a JFET is as follows :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

This shows that I_D is proportional to square of V_{GS} which is the controlling input parameter. Due to this square relationship between I_D and V_{GS}, the FET is called as a square law device.

Q. 1(a)2. Give reasons for the following :
Barkhausens criteria should be satisfied to get oscillations. **(5 Marks)**

Ans. :

An oscillator is basically an "amplifier" which does not have any ac input but it operates on the principle of positive feedback to generate an ac signal on its own at its output. Thus it is clear that an amplifier can work as an oscillator if positive feedback is made to exist. However positive feedback not always guarantees oscillations. An amplifier will work as an oscillator if and only if it satisfies a set of conditions called the "Barkhausen Criterion".

Q. 2(a) Draw and explain JFET characteristics. Also show that for a JFET, $g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}$ **(10 Marks)**

Ans. : **Please refer Q. 2(a) of May 2014.**

Pinch off Voltage(V_P)

The pinch off voltage is the value of V_{DS}, at which the drain current reaches its constant saturation value .Any further increase in V_{DS} dose not have any effect on the value of I_D Do not make a confusion between the cut off and pinch off voltage is denoted by Vp .

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}$$

We know that,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

where, $$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

$$\therefore g_m = \frac{2 I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \quad ...(1)$$

Also $$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad ...(2)$$

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$$\therefore \left[1-\frac{V_{GS}}{V_P}\right]^2 = \frac{I_{DS}}{I_{DSS}}$$

$$\therefore \left[1-\frac{V_{GS}}{V_P}\right] = \sqrt{\frac{I_{DS}}{I_{DSS}}} \quad ...(3)$$

Substituting Equation (3) into Equation (1) we get,

$$g_m = \frac{2\,I_{DSS}}{|V_P|} \times \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$\therefore g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}$$ **...Proved**

Q. 3(d) Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points :

(a) $V_{GS} = -0.5$ V, $V_{GS} = -1.5$ V

(b) $V_{GS} = -2.5$ V **(5 Marks)**

Ans. :

Given : $I_{DSS} = 8$ mA, $V_P = -4$ V

To find : g_m for $V_{GS} = -0.5$ V

g_m for $V_{GS} = -1.5$ V

g_m for $V_{GS} = -2.5$ V

Step 1 : Calculate transconductance g_m :

$$g_m = g_{m0}\left[1-\frac{V_{GS}}{V_P}\right]$$

where, $$g_{m0} = \frac{-2\,I_{DSS}}{V_P} = \frac{-2\times 8\times 10^{-3}}{-4} = 4\times 10^{-3}$$

g_m for $V_{GS} = -0.5$ V :

$$g_m = 4\times 10^{-3}\left[1-\frac{-0.5}{-4}\right] = 3.5 \text{ mS}$$ **...Ans.**

g_m for $V_{GS} = -1.5$ V :

$$g_m = 4\times 10^{-3}\left[1-\frac{-1.5}{-4}\right] = 2.5 \text{ mS}$$ **...Ans.**

g_m for $V_{GS} = -2.5$ V :

$$g_m = 4\times 10^{-3}\left[1-\frac{-2.5}{-4}\right] = 1.5 \text{ mS}$$ **...Ans.**

Q. 6(d) Compare different biasing techniques for JFET. **(5 Marks)**

Ans. : Please refer Q. 3(d) of Dec. 2013.

Chapter 2 : Operational Amplifier & its Application [Total Marks - 20]

Q. 1(b) With neat diagram explain any one application of zero-crossing detector. **(5 Marks)**

Ans. : Applications of zero-crossing detector :

1. Square wave generators.
2. In the mains supply synchronizing circuit.

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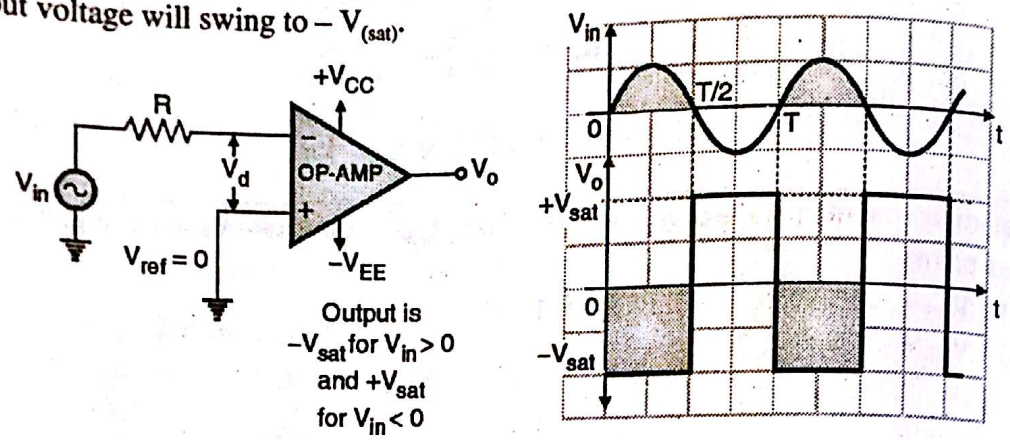
3. Microprocessor based triggering circuit for thyristors.

Zero-crossing detector as square wave generator : Zero crossing detector is as shown Fig. Q. 1(b)(a). As you can see, zero crossing detector is nothing but the basic comparator circuit with zero reference voltage applied to the non-inverting terminal.

Circuit operation : Refer to the waveforms shown in Fig. Q. 1(b)(b). When the input sinewave crosses zero and becomes positive at instant t = 0, the differential input voltage V_d becomes negative and the output voltage will swing to $-V_{(sat)}$.



(a) Zero crossing detector **(b) Input and output voltage waveforms**

Fig. Q. 1(b)

When the sine wave again crosses zero and becomes negative at instant t = T/2, the differential input voltage becomes positive and the output voltage will swing to + $V_{(sat)}$ as now the (+) terminal is more positive than the (–) terminal. The zero crossing detector thus switches its output from one state to the other every time when the input voltage crosses the zero. The zero crossing detector is also known as a sine wave to square wave converter.

Q. 2(b) With respect to op-amp explain the ideal characteristics and concept of virtual ground. Explain how op-amp can be used as an averaging amplifier in inverting configuration. Also draw neat circuit diagrams to :

1. Convert sine wave to square wave using op-amp.
2. Detect the crossing of zero's in the generated square wave. **(10 Marks)**

Ans. : The important characteristics of an ideal OP-AMP :

1. Infinite voltage gain ($A_V = \infty$) :

The open loop (without any feedback) gain of an ideal OP-AMP is denoted by A_V. It is the differential voltage gain and its value for an ideal OP-AMP is ∞.

$$V_o = A_V \times V_d \quad ...(1)$$

As $A_V = \infty$, the differential voltage V_d required to obtain the maximum output voltage ($\pm V_{CC}$) will be negligible i.e. $V_d \approx 0V$.

2. Infinite input resistance ($R_i = \infty$) :

The input resistance is also called as differential input resistance and it is defined as the total resistance measured between the two input terminals of an op-amp (see Fig. 1-Q. 2(b)).

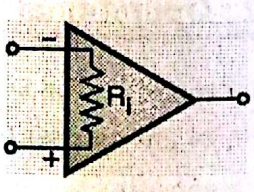


Fig. 1-Q. 2(b) : Differential input resistance

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The input resistance R_i of an ideal OP-AMP is infinite. Due to this, the current flowing in each input terminal will be zero i.e. $I_{B1} = I_{B2} = 0$. Due to infinite input resistance, almost any source can drive it and the source does not get loaded.

3. Zero output resistance ($R_o = 0$) :

The output resistance of an OP-AMP is the resistance viewed from its output terminal as shown in Fig. 2-Q. 2(b).

The output resistance R_o of an ideal OP-AMP is zero. Due to zero output resistance, the ideal OP-AMP can drive infinite number of other devices.

Further there will not be any change in its output voltage due to change in load current. That means its voltage regulation will be good.

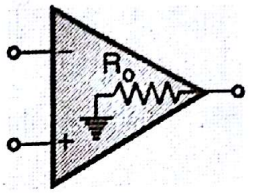

Fig. 2-Q. 2(b) : Output resistance

4. Zero offset voltage :

In practical OP-AMPs a small output voltage is present even though both the inputs V_1 and V_2 are having a zero value. This voltage is called as the offset voltage. For ideal OP-AMPs the offset voltage is zero. That means output voltage will be zero when input voltage is zero.

5. Infinite bandwidth :

Bandwidth of an amplifier is the range of frequencies over which all the signal frequencies are amplified almost equally. The bandwidth of an ideal OP-AMP is infinite. So it can amplify any frequency signal from 0 to ∞ Hz. Thus the gain of an ideal amplifier is constant from 0 frequency (dc signal) to ∞ Hz.

6. Infinite CMRR :

For an OP-AMP, the Common Mode Rejection Ratio (CMRR) is defined as the ratio of differential gain to common mode gain. CMRR is ∞ for an ideal OP-AMP. Thus the output voltage corresponding to the common mode noise is zero.

Virtual ground :

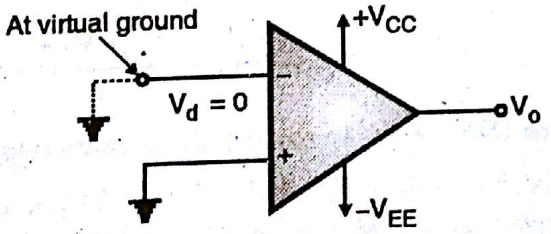

Fig. 3-Q. 2(b) : Concept of virtual ground

If the non-inverting (+) terminal of OP-AMP is connected to ground as shown in Fig. 3-Q. 2(b), then due to the "virtual short" existing between the two input terminals, the inverting (–) terminal will also be at ground potential. Hence it is said to be at "virtual ground". Similarly if the inverting (–) terminal is connected to ground, then the non-inverting (+) terminal will be at "virtual ground" potential.

The concept of virtual ground has been used extensively in analyzing various closed loop configurations, specially we use this concept in the inverting amplifier analysis.

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Averaging circuit :

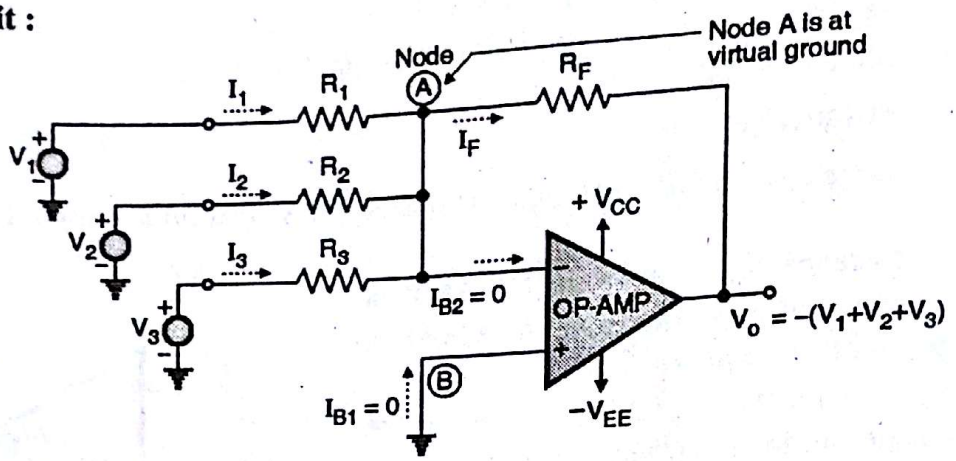

Fig. 4-Q. 2(b) : An inverting adder

The inverting adder circuit of Fig. 4-Q.2(b) can be used as an averaging circuit by setting $R_1 = R_2 = R_3 = R$ and $R_F = R/3$. Substitute these values into Equation (2) to get,

$$\left.\begin{aligned} &\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_F} \\ &\text{OR} \\ &V_o = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right] \end{aligned}\right\} \quad (2)$$

$$V_o = \frac{-R_F}{R}(V_1 + V_2 + V_3) = \frac{-R/3}{R}(V_1 + V_2 + V_3)$$

$$\therefore \quad V_o = \frac{-(V_1 + V_2 + V_3)}{3} \quad ...(3)$$

Thus the magnitude of output voltage is equal to the average of the three input voltages. This principle can be extended for n number of inputs by setting

$R_F = R/n$ and $R_1 = R_2 = ... = R_n = R$.

Then the output voltage is given by,

$$V_o = \frac{-(V_1 + V_2 + V_3 + ... + V_n)}{n}$$

ZCD as square wave generator (Sine wave to square wave convertor) :

Zero crossing detector is as shown in Fig. 5-Q. 2(b)(a). As you can see, zero crossing detector is nothing but the basic comparator circuit with a zero reference voltage applied to the non-inverting terminal.

Circuit operation :

Refer to the waveforms shown in Fig. 5-Q. 2(b)(b). When the input sinewave crosses zero and becomes positive at instant t = 0, the differential input voltage V_d becomes negative and the output voltage will swing to $-V_{(sat)}$.

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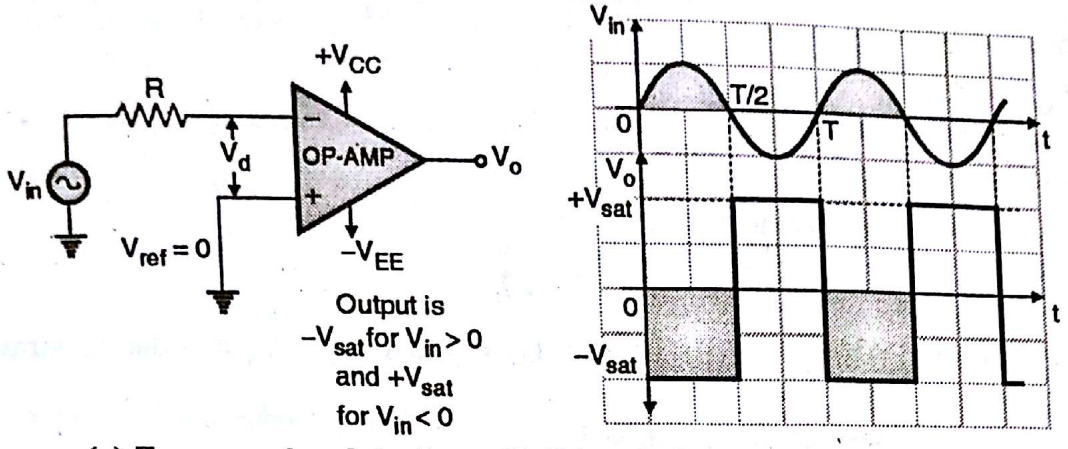

(a) Zero crossing detector **(b) Input and output voltage waveforms**

Fig. 5-Q. 2(b)

When the sinewave again crosses zero and becomes negative at instant t = T/2, the differential input voltage becomes positive and the output voltage will swing to + $V_{(sat)}$ as now the (+) terminal is more positive than the (–) terminal. The zero crossing detector thus switches its output from one state to the other everytime when the input voltage crosses the zero. The zero crossing detector is also known as a sinewave to square wave converter.

Q. 3(a) Explain how operational amplifier can be used for addition of two AC signals with one DC signal. **(5 Marks)**

Ans. :

Inverting summing amplifier :

Fig. Q. 3(a) shows the "inverting summing amplifier" configuration with three inputs V_1, V_2 and V_3. Depending on the relation between the feedback resistor R_F and the three input resistances R_1, R_2 and R_3 we can use the same circuit shown in Fig. Q. 3(a) as a summing amplifier, scaling amplifier or averaging amplifier.

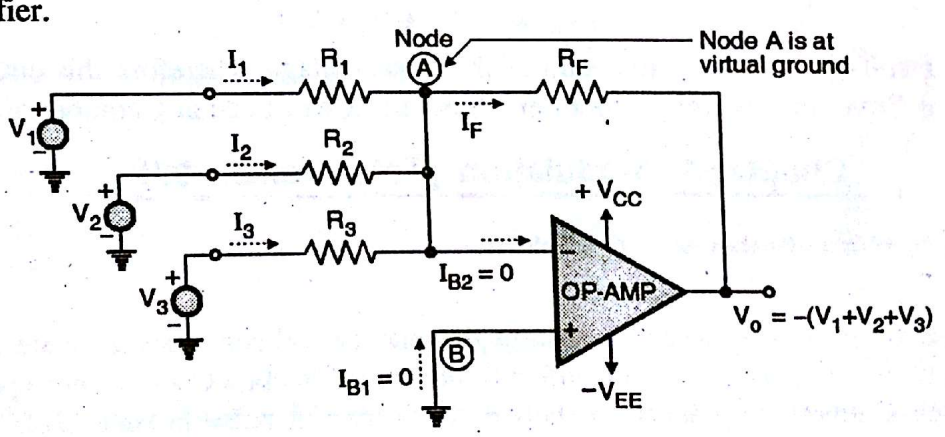

Fig. Q. 3(a) : An inverting adder

V_1, V_2 and V_3 are three input signals applied simultaneously to the inverting terminal of the OP-AMP through resistors R_1, R_2 and R_3 respectively. V_1, V_2 and V_3 are measured with respect to ground. R_F is the feedback resistor connected between the output terminal and the inverting input terminal of OP-AMP.

The non-inverting input terminal is connected to ground. So the configuration of Fig. Q. 3(a) is basically an inverting amplifier with three inputs. Let the currents through the resistors R_1, R_2 and R_3 be I_1, I_2 and I_3 respectively.

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For the analysis of this circuit we assume that the OP-AMP is ideal. Hence its input resistance is $R_i = \infty$. Therefore the currents I_{B1} and I_{B2} are zero. In addition to this, Node A is at virtual ground potential.

Expression for the output voltage :

Apply KCL at node A of Fig. Q. 3(a) to write,

$$I_1 + I_2 + I_3 = I_{B2} + I_F \quad ...(1)$$

But as R_i of the OP-AMP is ideally infinite, $I_{B2} = 0$ and $V_A = V_B = 0$ due to virtual ground concept.

$$\text{Hence,} \quad I_1 + I_2 + I_3 = I_F \quad ...(2)$$

On the input side,

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1} \text{ as } V_A = 0 \quad ...(3)$$

Similarly,

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2} \text{ and } I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3}{R_3} \quad ...(4)$$

And on the output side,

$$I_F = \frac{V_A - V_o}{R_F} = -\frac{V_o}{R_F} \quad ...(5)$$

Substituting these values in Equation (2) we get,

$$\left.\begin{aligned} &\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_F} \\ &\text{OR} \\ &V_o = -\left[\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right] \end{aligned}\right\} \quad ...(6)$$

In Equation (6) if we substitute $R_F = R_1 = R_2 = R_3 = R$ then we get,

$$V_o = -(V_1 + V_2 + V_3) \quad ...(7)$$

Thus output voltage is the negative sum of the input voltage. Therefore this circuit is called as "Inverting adder" or "Inverting summing amplifier". Similarly we can add any number of inputs

Chapter 4 : Modulation [Total Marks - 30]

Q. 3(b) Explain fly wheel effect in class C amplifier. **(5 Marks)**

Ans. :

When we briefly push a fly wheel, it absorbs this energy and continues to rotate for some time. This is known as a fly wheel effect. The same effect is being used in class C amplifier to produce an AM wave. Here the class C amplifier produces a short duration current pulse in each cycle of the carrier. This current pulse is applied to a tuned circuit. The tuned circuit will produce damped oscillations at its output. This is the fly wheel effect present in a class C amplifier.

Property of a tuned circuit :

To understand the high level modulation, we must know an important property of a tuned circuit.

This property states that if we apply a current pulse to a tuned circuit then it generates damped voltage oscillations at its output.

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This is as shown in Fig. 1-Q. 3(b). The amplitude of oscillations is proportional to the size of current pulse and the decay rate is proportional to the time constant. This is called as the flywheel effect in a tuned circuit.

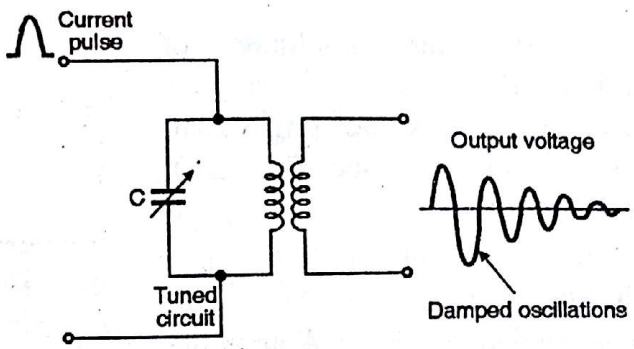

Fig. 1-Q. 3(b) : The property of tuned circuit

High level collector modulator circuit :

A high level collector modulator circuit is as shown in Fig. 2-Q. 3(b). This circuit shows the output stage of a transmitter. It is a high power RF (Radio frequency) class C amplifier. The class C amplifier conducts for only a portion of the positive half cycles of the carrier signal applied at the base of transistor Q_1.

Operation of the circuit :

The transistor Q_1 receives the RF carrier signal at its base. However the transistor will conduct only for a portion of the positive half cycles of the carrier signal because it has been biased to operate as class C amplifier.

Thus the collector current of Q_1 is in the form of current pulses. This is as shown in Fig. 3-Q. 3(b)(b). These current pulses are supplied to the tuned circuit.

The high power audio amplifier amplifies the modulating signal to a high power level.

The secondary winding of the modulating transformer T_1 is connected in series with the dc supply voltage V_{CC}.

Therefore the modulating voltage will add or subtract from V_{CC} as shown in Fig. 3-Q. 3(b)(b).

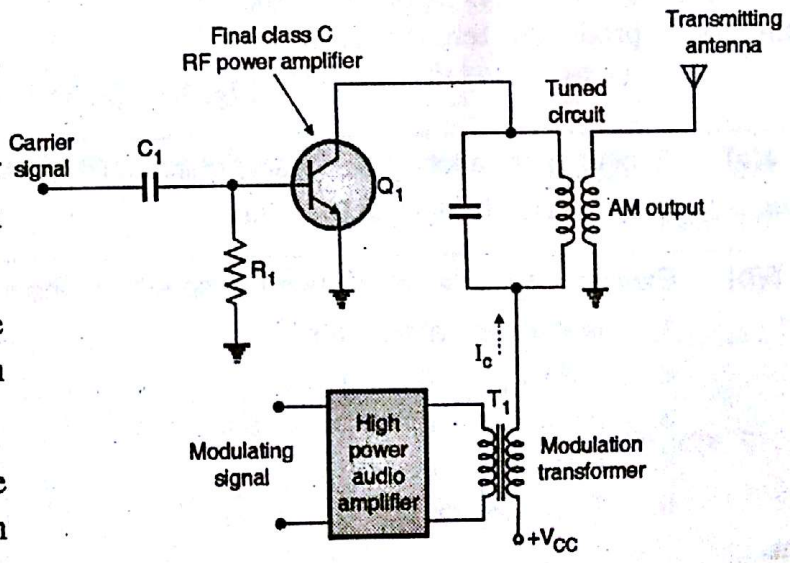

Fig. 2-Q. 3(b) : High level collector modulator

This varying supply voltage is then applied to the class C amplifier consisting of transistor Q_1.

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Naturally the amplitude of collector current pulses will vary in accordance with the modulating signal. This is as shown in the Fig. 3-Q. 3(b)(b).

These current pulses pass through the tuned circuit. They will cause the tuned circuit to oscillate at the desired output frequency as per the flywheel effect discussed earlier.

As per the property of the tuned circuit, the AM wave is produced at the output of the tuned circuit. This is as shown in Fig. 3-Q. 3(b)(b).

It won't be possible to obtain the 100% modulation using this circuit. The reason is that to get 100 % modulation $E_m = V_{CC}$.

When the modulating signal goes negative it subtracts from the V_{CC}. At the negative peak point the subtraction is zero, so zero voltage is applied to the transistor Q_1 producing zero output.

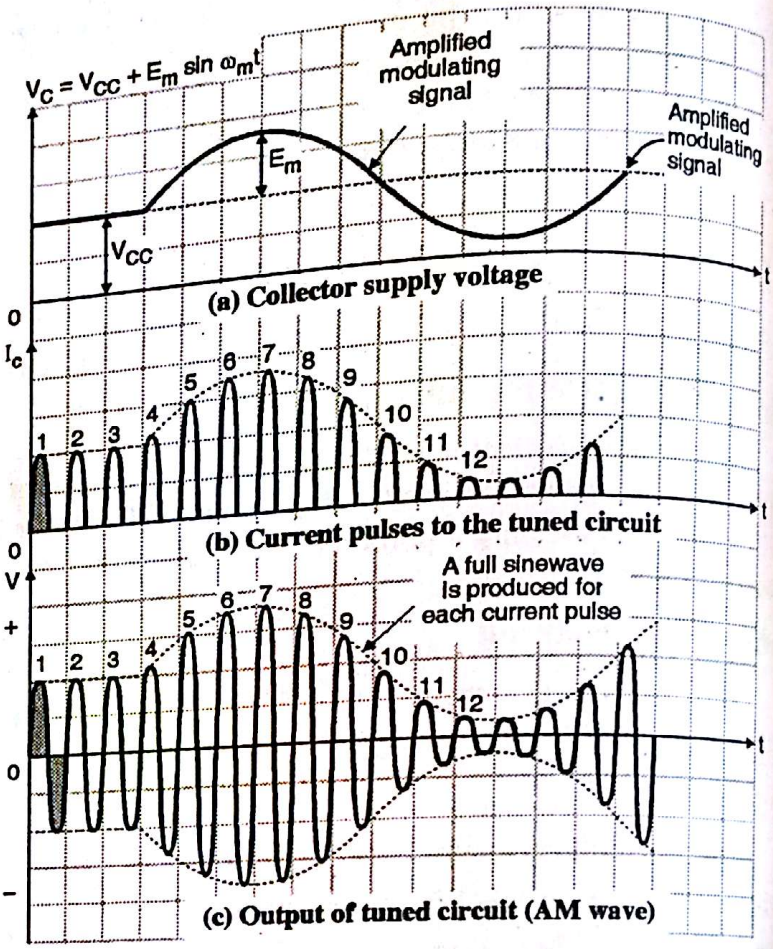

Fig. 3-Q. 3(b) : Waveforms of collector modulator circuit

Q. 4(a) Explain generation of SSB using phase shift method. **(10 Marks)**

Ans. : **Please refer Q. 4(a) of Dec. 2013.**

Q. 5(b) Explain amplitude modulation for more than one modulating signal in the following cases :

1. Mathematical equation
2. AM waveform
3. AM amplitude and power spectrum
4. Modulation coefficient
5. Transmission power

(10 Marks)

Ans. :

1. Mathematical equation in time domain :

Assumptions :

Let the modulating signal be sinusoidal and be represented as,

$$e_m = E_m \cos \omega_m t \quad ...(1)$$

where "e_m" is the instantaneous amplitude of the modulating signal, E_m is the peak amplitude, $\omega_m = 2\pi f_m$ and f_m = Frequency of the modulating signal.

Let the carrier signal also be sinusoidal at a much higher frequency than that of the modulating signal. The instantaneous carrier signal e_c is given by,

$$e_c = E_c \cos \omega_c t \quad ...(2)$$

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where E_c = Peak carrier amplitude,

f_c = Carrier frequency and $\omega_c = 2\pi f_c$.

The AM wave is expressed by the following expression,

$$e_{AM} = A \cos(2\pi f_c t) \quad ...(3)$$

where A = Envelope of AM wave

Where A represents the instantaneous value of the envelope. The modulating signal either adds or gets subtracted from the peak carrier amplitude E_c as shown in Fig. 1-Q. 5(b). Hence we can represent the instantaneous value of envelope as,

$$A = E_c + e_m$$

$$= E_c + E_m \cos(2\pi f_m t) \quad ...(4)$$

Hence the AM wave is given by,

$$e_{AM} = A \cos(2\pi f_c t) = [E_c + E_m \cos(2\pi f_m t)] \cos(2\pi f_c t)$$

$$\therefore \quad e_{AM} = E_c \left[1 + \frac{E_m}{E_c} \cos(2\pi f_m t)\right] \cos(2\pi f_c t)$$

Let $m = E_m / E_c$ be the modulation index.

$$\therefore \quad e_{AM} = E_c [1 + m \cos(2\pi f_m t)] \cos(2\pi f_c t) \quad ...(5)$$

This expression represents the time domain representation of an AM signal.

2. AM wave :

Fig. 1-Q. 5(b) shows the amplitude modulated wave when the modulating signal is a sinusoidal signal.

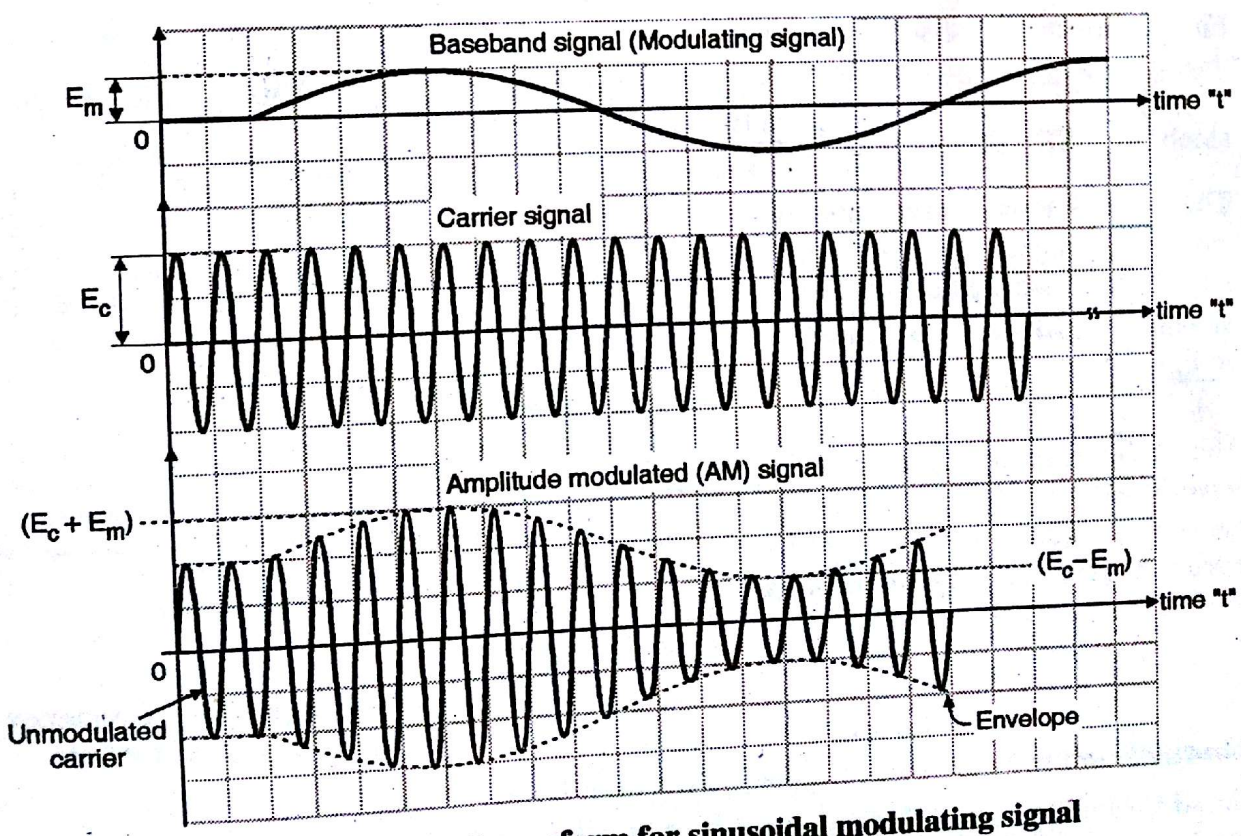

Fig. 1-Q. 5(b) : AM waveform for sinusoidal modulating signal

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3. Am amplitude and power spectrum :

The frequency spectrum is a graph of amplitude on Y axis versus frequency on X axis. The frequency spectrum of AM wave tells us about which frequency components are present in the AM wave and what are their amplitudes. So consider the equation for AM wave.

$$e_{AM} = (E_c + E_m \cos \omega_m t) \cos \omega_c t$$

$$E_c = \left[1 + \frac{E_m}{E_c} \cos \omega_m t\right] \cos \omega_c t \quad ...(6)$$

As per the definition of the modulation index, $m = E_m / E_c$.

$$\therefore \quad e_{AM} = E_c (1 + m \cos \omega_m t) \cos \omega_c t \quad ...(7)$$

Simplifying we get,

$$e_{AM} = E_c \cos \omega_c t + m E_c \cos \omega_m t \cos \omega_c t$$

For the second term in the above expression use the following standard identity :

$$2 \cos A \cos B = \cos (A + B) + \cos (A - B)$$

Therefore Equation (7) gets simplified as follows :

$$e_{AM} = \underbrace{E_c \cos \omega_c t}_{\text{Carrier}} + \underbrace{\frac{m E_c}{2} \cos (\omega_c + \omega_m) t}_{\text{Upper sideband}} + \underbrace{\frac{m E_c}{2} \cos (\omega_c - \omega_m) t}_{\text{Lower sideband}} \quad ...(8)$$

Observations :

The expression for the AM wave shows that it consists of three terms :

1. First term is nothing else but the unmodulated carrier signal.
2. The second term is a sinusoidal signal at frequency ($f_c + f_m$). This is called as the upper sideband (USB). Its amplitude is $\frac{m E_c}{2}$.
3. The third term represents a sinusoidal signal at frequency ($f_c - f_m$). It is called as the lower sideband (LSB). Its amplitude is $\frac{m E_c}{2}$.

Hence the frequency spectrum of an A.M. wave is as shown in Fig. 2-Q. 5(b). Note that it is a single sided spectrum i.e. the spectrum plotted for only the positive values of frequency.

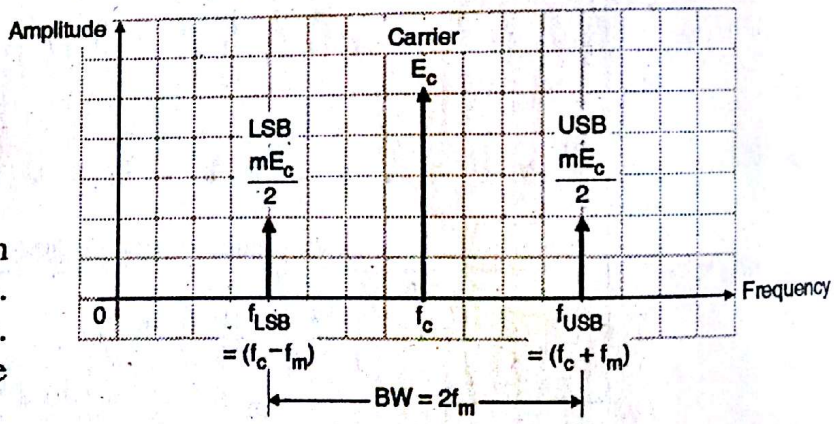

Fig. 2-Q. 5(b) : Single sided frequency spectrum of AM wave

4. Modulation Index :

In AM wave the modulation index (m) is defined as the ratio of amplitudes of the modulating and carrier waves as follows :

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$$m = \frac{E_m}{E_c} \quad (9)$$

When $E_m \leq E_c$ the modulation index "m" has values between 0 and 1 and no distortion is introduced in the AM wave. But if $E_m > E_c$ then m is greater than 1. This will distort the shape of AM signal. The distortion is called as "over modulation."

The modulation index is also called as modulation factor, modulation coefficient or degree of modulation. However if modulation index is expressed as percentage it is called as "percentage modulation."

$$\therefore \ \% \text{ Modulation} = \frac{E_m}{E_c} \times 100 \quad (10)$$

Note that "m" is a dimensionless quantity.

5. Transmission power :

The total power in an AM wave is given by,

$$P_t = [\text{Carrier Power}] + [\text{Power in USB}] + [\text{Power in LSB}] \quad ...(11)$$

$$\therefore \ P_t = \frac{E_{carr}^2}{R} + \frac{E_{USB}^2}{R} + \frac{E_{LSB}^2}{R} \quad ...(12)$$

Where E_{carr}, E_{USB} and E_{LSB} are the rms values of the carrier and sideband amplitudes respectively and R is the characteristic resistance of antenna in which the total power is dissipated. The total transmitted power in AM is thus the rms power.

Q. 6(c) Write short note on generation of FM by Armstrong method. **(5 Marks)**

Ans. : Generation of FM by Armstrong method :

In this method the FM is obtained through phase modulation. A crystal oscillator can be used hence the frequency stability is very high. This method is widely used in practice. The block diagram of the Armstrong method is as shown in Fig. Q. 6(c).

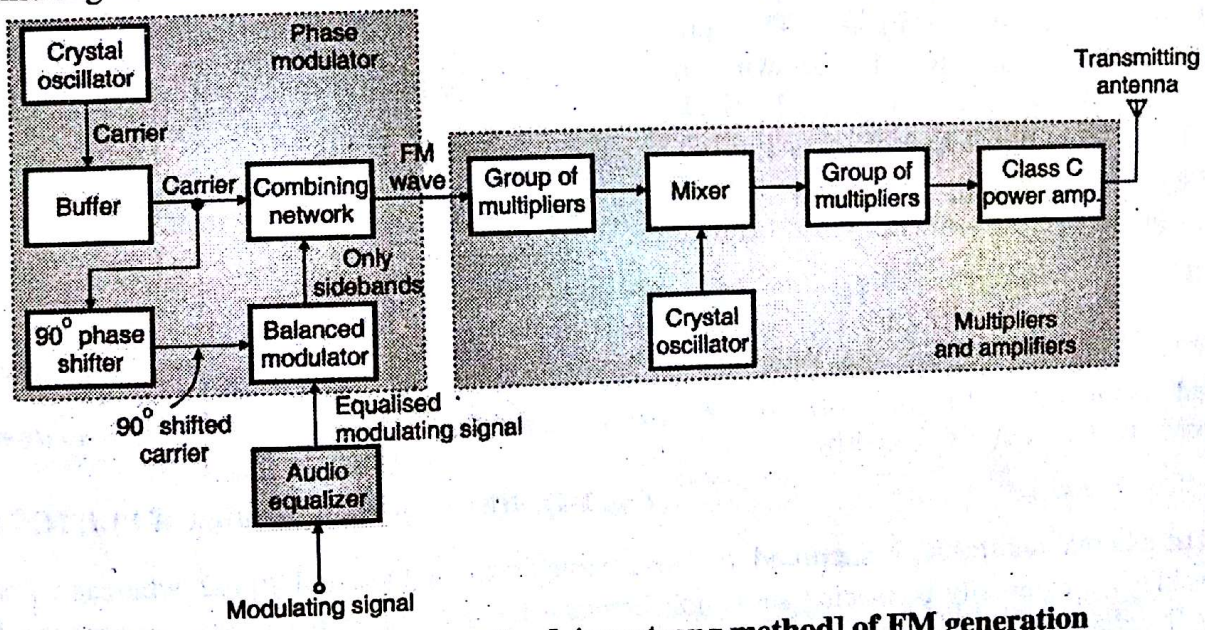

Fig. Q. 6(c) : Indirect method Armstrong method] of FM generation

The Armstrong method uses the phase modulation to generate frequency modulation.

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Operation of the Armstrong method :

Now refer to Fig. Q. 6(c). The operation of the Armstrong method is as follows :

1. The crystal oscillator generates the carrier at low frequency typically at 1 MHz. This is applied to the combining network and a 90° phase shifter.
2. The modulating signal is passed through an audio equalizer to boost the low modulating frequencies, for the reason discussed earlier. The modulating signal is then applied to a balanced modulator.
3. The balanced modulator produces two sidebands such that their resultant is 90° phase shifted with respect to the unmodulated carrier.
4. The unmodulated carrier and 90° shifted sidebands are added in the combining network.
5. As discussed earlier, at the output of the combining network we get FM wave. This FM wave has a low carrier frequency f_c and low value of the modulation index m_f.
6. The carrier frequency and the modulation index are then raised by passing the FM wave through the first group of multipliers. The carrier frequency is then raised by using a mixer and then the f_c and m_f both are raised to the required high values using the second group of multipliers. The effect of multiplication and mixing is as discussed earlier.
7. The FM signal with high f_c and high m_f is then passed through a class C power amplifier to raise the power level of the FM signal.

Chapter 5 : Demodulation [Total Marks - 30]

Q. 1(c) With neat circuit diagram explain the use of PLL as a phase shifter. **(5 Marks)**

Ans. : **Please refer Q. 6(b) of Dec. 2014.**

Q. 4(b) Discuss the operating principle of PLL and explain its use as frequency translator. **(10 Marks)**

Ans. : PLL IC - SE/NE 565 :

SE/NE 565 is available in 14-pin DIP and 10 pin metal can package. The pin configuration of this IC is shown in Fig. 1-Q.4(b)(a) and the functional block diagram is shown in Fig. 2-Q.4(b).

The free running frequency of VCO (i.e. when inputs 2, 3 are grounded) is given by,

$$f_o = \frac{0.3}{R_T C_T} \text{ Hz} \quad ...(1)$$

Where R_T and C_T are the externally connected components to pins (8) or (9) respectively as shown in Fig. 2-Q.4(b).

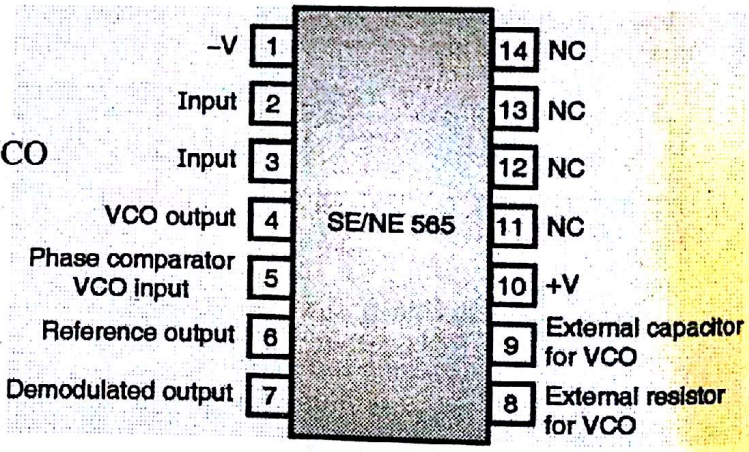


Fig. 1-Q. 4(b) : Pin configuration of PLL IC - 565

The external resistor R_T is supposed to have a value between 2 kΩ and 20 kΩ, whereas C_1 can be of any value. An externally connected short link between the pins (4) and (5) will connect the VCO output to the phase detector input, so as to compare f_s and f_o. The 3.6 kΩ internal resistance will form an R-C filter with the externally connected capacitor C between pins (7) and (10). This capacitor should be sufficiently large to minimize the variations in the demodulated output at pin (7). The VCO free running

frequency f_o is adjusted externally with R_T and C_T, to be at the centre of the input frequency range. The 565 PLL is capable of locking to and tracking an input signal over ± 60 % bandwidth with respect to f_o (center frequency). The lock range f_L of the PLL is given by

$$\text{Lock range :} \quad f_L = \pm \frac{8 f_o}{V} \text{ Hz} \qquad ...(2)$$

where f_o = Free running frequency of VCO in Hz

and V = (+V) – (– V) volts.

The expression for the capture range is given by :

$$\text{Capture range :} \quad f_C = \pm \left[\frac{f_L}{(2\pi)(3.6) \times 10^3 \times C} \right]^{1/2} \qquad ...(3)$$

where C is expressed in farads.

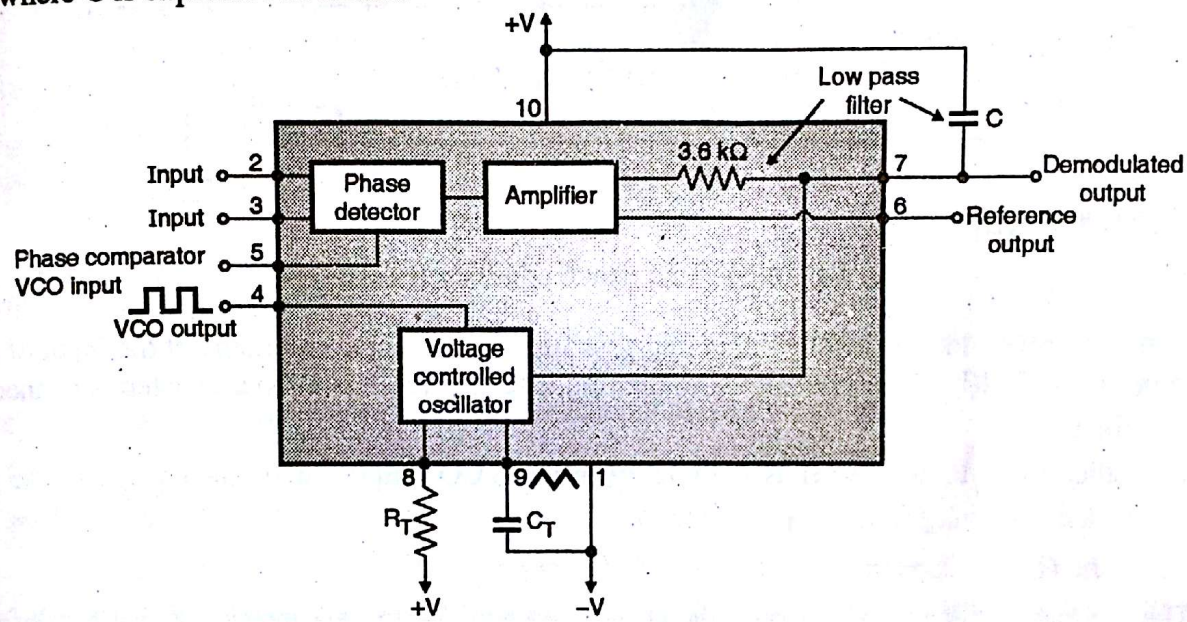
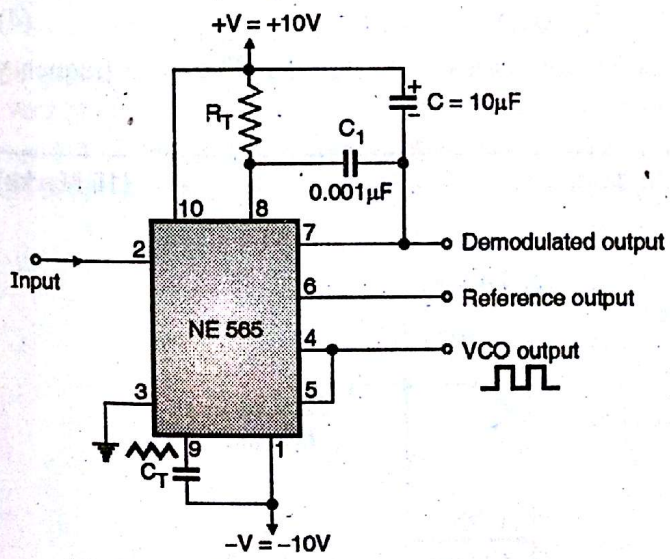
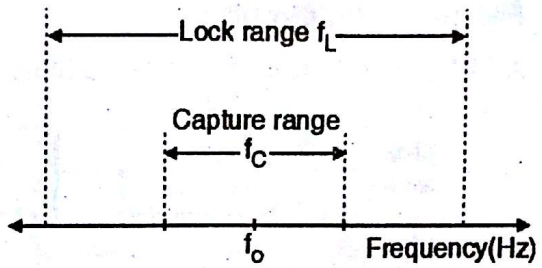


Fig. 2-Q. 4(b) : Functional block diagram of PLL - IC 565

Connection diagram of PLL 565 :



(a) Connection diagram of PLL 565



(b) Relationship between f_o, f_L and f_C

Fig. 3-Q. 4(b)

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The connection diagram of PLL IC 565 is as shown in Fig. 3-Q. 4(b)(a) and the lock and capture ranges are shown in Fig. 3-Q. 4(b)(b). The lock range f_L given by Equation (2) increases with increase in the input voltage but decreases with increase in the supply voltage. Pins (2) and (3) are the input pins for PLL 565 and we can couple the input signal directly to them. As seen from Fig. 3-Q. 4(b)(b), the capture range f_C is always less than the lock range f_L.

PLL as frequency translator :

The block diagram of PLL used as a frequency translator is shown in Fig. 4-Q. 4(b).

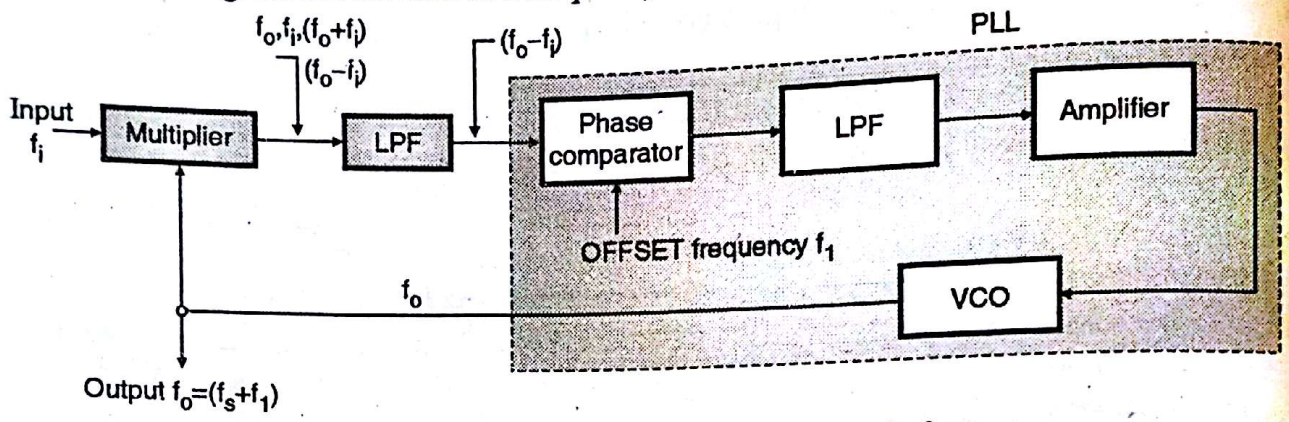

Fig. 4-Q. 4(b) : PLL for frequency translation

A multiplier (or a mixer) alongwith a low pass filter is connected externally at the input of a PLL as shown in Fig. 4-Q. 4(b). The input signal f_i, the frequency of which is to be translated is connected at the input of the mixer.

The other input to the mixer is coming from the VCO output, at frequency f_o. At the mixer output, we get the following frequency components :

$$f_o,\ f_i,\ (f_o + f_i) \quad \text{and} \quad (f_o - f_i).$$

The low pass filter will allow only the $(f_o - f_i)$ component to pass through it and blocks all the other components. This signal and the offset frequency signal at frequency f_1 are applied to the phase comparator. When the PLL is in the locked state, it will try to adjust the VCO frequency such that,

$$f_o - f_i = f_1 \text{ or } f_o = (f_1 + f_i) \quad ...(4)$$

Thus the frequency of the output signal is automatically adjusted to $(f_1 + f_i)$. The input frequency is thus shifted (or offsetted) by f_1 Hz.

Q. 5(a) With neat diagram explain the circuit for FM detection. **(10 Marks)**

Ans. : FM detection circuit :

A PLL can be used as FM demodulator as shown in Fig. 1-Q.5(a).

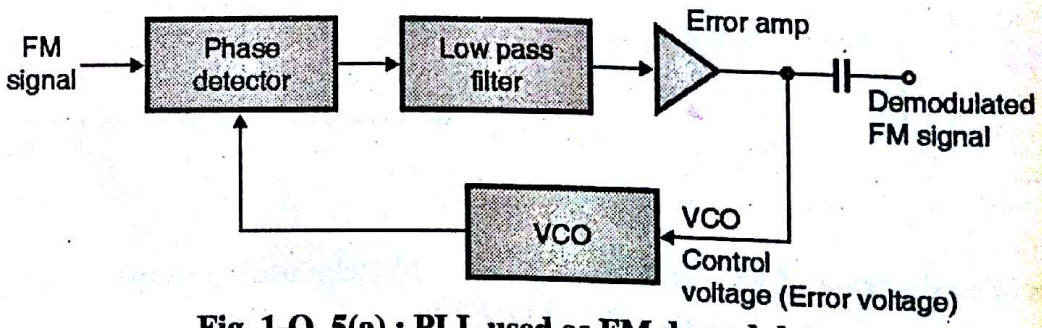

Fig. 1-Q. 5(a) : PLL used as FM demodulator

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Operation :

The FM signal which is to be demodulated is applied at the input of the PLL. As the PLL is locked to the FM signal, the VCO starts tracking the instantaneous frequency in the FM input signal.

The error voltage produced at the output of the amplifier is proportional to the deviation of input frequency from the centre frequency of FM. Thus the ac component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output.

The FM demodulator using PLL ensures a highly linear relationship, between the instantaneous input frequency and VCO control voltage (error amplifier output).

The FM demodulator using IC 565 is as shown in Fig. 2-Q. 5(a). The block diagram of FM detector using PLL (Fig. 1-Q. 5(a)) has simply been implemented using IC 565 here.

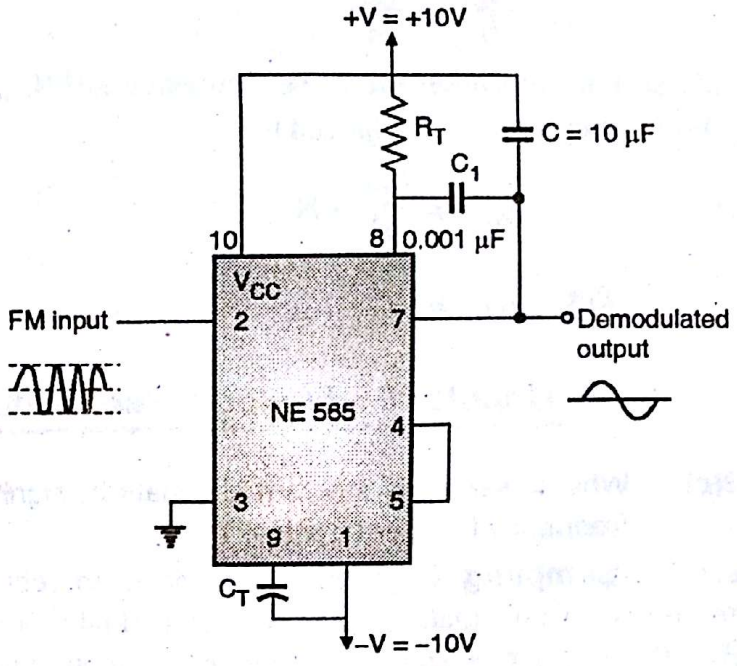

Fig. 2-Q. 5(a) : FM detector using PLL 565

Q. 6(a) Explain application of PLL as frequency synthesizer. **(5 Marks)**

Ans. :

PLL as frequency synthesizer :

The block diagram of PLL as frequency synthesizer is as shown in Fig. Q. 6(a). Note that this circuit is same as the frequency multiplier circuit except for the divide by M network added as shown in Fig. Q. 6(a) on the input side after the crystal oscillator.

Operation :

The frequency synthesizer is supposed to produce an output signal, the frequency of which can be precisely adjusted to any value in a selected range. The output frequencies of a synthesizer should be very stable. In order to ensure the stability of output frequency, a crystal oscillator of frequency f_{osc} is used. The output frequency of crystal oscillator is divided by M with the help of the frequency divide by M network. Thus the input frequency to PLL is (f_{osc}/M) as shown in Fig. Q. 6(a).

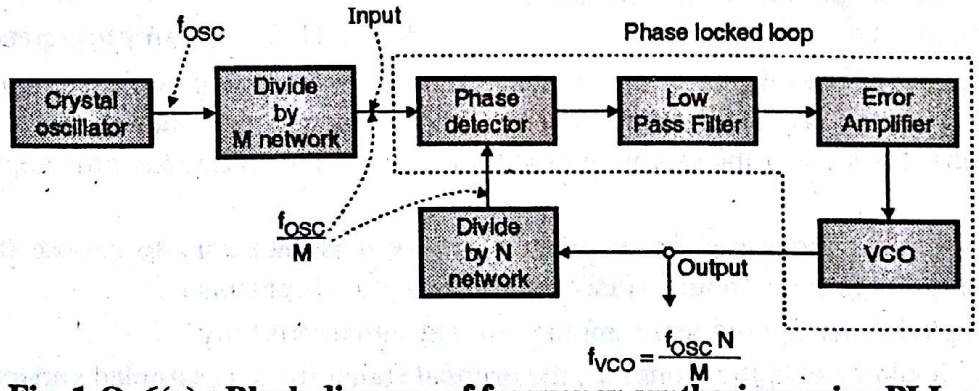

Fig. 1-Q. 6(a) : Block diagram of frequency synthesizer using PLL

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The PLL will compare this frequency with the frequency at the output of divide by N network, and will try to adjust this frequency equal to $\frac{f_{osc}}{M}$. But the frequency at divide by N network is f_{VCO}/N.

$$\therefore \frac{f_{VCO}}{N} = \frac{f_{osc}}{M} \quad ...(1)$$

In order to obtain the same frequency i.e. (f_{osc}/M) at the output of divide by N network, the VCO frequency should be adjusted to,

$$f_{VCO} = \frac{f_{osc}}{M} \times N \quad ...(2)$$

$$\text{OR} \quad f_{VCO} = \left(\frac{N}{M}\right) f_{osc} \quad ...(3)$$

Chapter 6 : Analog Pulse Modulation [Total Marks - 05]

Q. 3(c) What is sampling theorem and state its significance in communication. What is the standard frequency for speech signal ? **(5 Marks)**

Ans. : **Sampling theorem :** In order to represent the original message signal "faithfully" (without loss of information), it is necessary to take as many samples of the original signal as possible. Higher the number of samples, closer is the representation. The number of samples depends on the "sampling rate" and the maximum frequency of the signal to be sampled.

Statement :

1. If a finite energy signal x (t) contains no frequencies higher than "W" Hz (i.e. it is a band limited signal) then it is completely determined by specifying its values at the instants of time which are spaced (1/2W) seconds apart.
2. If a finite energy signal x (t) contains no frequency components higher than "W" Hz then it may be completely recovered from its samples which are spaced (1/2W) seconds apart

Significance of sampling theorem :

In the pulse modulation and digital modulation systems, the signal to be transmitted must be in the discrete time form.

If the message signal is coming from a digital source (e.g. a digital computer) then it is in the proper for a digital communication system to be processed.

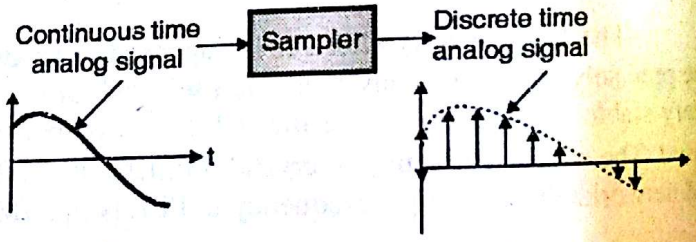

Fig. 1-Q. 3(c) : Sampling process

But this is not always the case. The message signal can be analog in nature (e.g. speech or video signal). In such a case it has to be first converted into a discrete time signal. We use the "sampling process" to do this. Thus using the sampling process we convert a continuous time signal into a discrete time signal.

For the sampling process to be of practical utility it is necessary to choose the sampling rate properly. The sampling process should satisfy the following requirements :

1. Sampled signal should represent the original signal faithfully.
2. We should be able to reconstruct the original signal from its sampled version.

The standard sampling frequency for speech signal is 8 kHz.

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Chapter 8 : Multiplexing [Total Marks - 10]

Q. 1(d) Explain with suitable example what do you understand by signal multiplexing ? **(5 Marks)**

Ans. : **Please refer Q. 6(a) of Dec. 2014.**

Q. 6(b) With block diagram explain TDM-PCM system **(5 Marks)**

Ans. : **Please refer Q. 5(a) of Dec. 2013.**

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May 2016

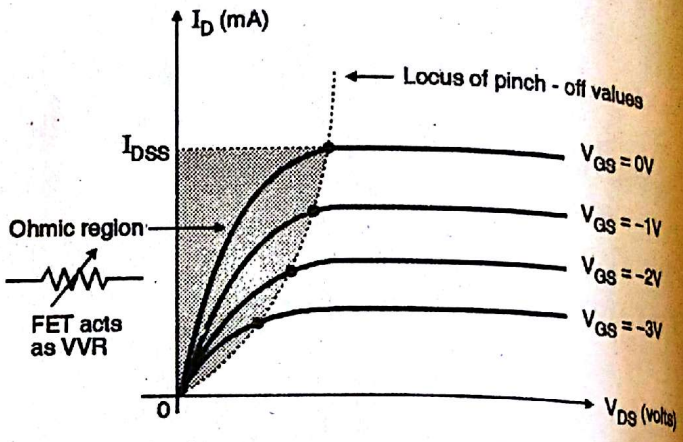
Chapter 1 : Electronic Circuits [Total Marks : 25]

Q. 1(a) Justify that JFET can be used as a voltage variable resistor. **(5 Marks)**

Ans. :

JFET can be used as a voltage variable resistor :

The field effect transistor can be operated as a voltage variable resistor (VVR).Refer to the drain characteristics of a JFET shown in Fig. 1. The region before "pinch off" is called as ohmic region. In this region the JFET acts as a variable resistor. The drain to source resistance R_{DS} in this region is dependent on the gate to source voltage. As V_{GS} becomes less negative, more drain current flows and R_{DS} decreases. For higher negative gate voltage, I_D decreases and R_{DS} will increase. Thus the JFET acts as a voltage variable resistor (VVR).



(B-1634) **Fig. 1 : Ohmic region in which FET acts as VVR**

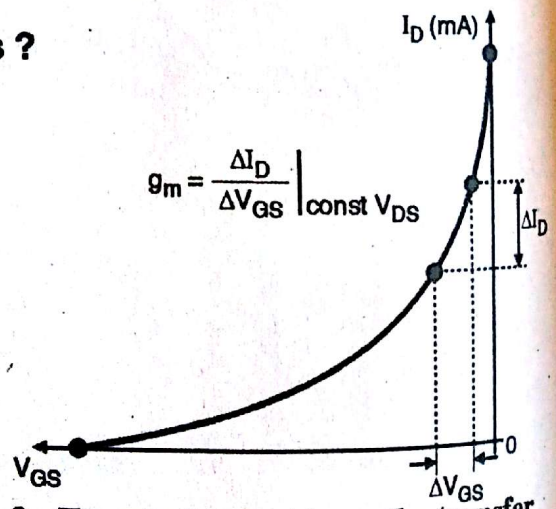
Q. 2(a) Derive an expression for trans-conductance for JFET. **(10 Marks)**

Ans. : The transconductance g_m is defined as the ratio of change in drain current to the corresponding change in gate to source voltage, at a constant value of drain to source voltage. It is calculated at a particular operating point.

$$\therefore \quad g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{\text{constant } V_{DS}} \quad ...(1)$$

How to obtain 'g_m' from the transfer characteristics ?

Transconductance can be obtained from the transfer characteristics of the JFET. Transconductance is the slope of transfer characteristics. Slope of the transfer characteristics is not constant. It depends on the value of V_{GS}. Therefore g_m has larger value near the top of the transfer characteristics. The units for transconductance will be mA/V or mS.



(F-2917) **Fig. 2 : To calculate g_m from the transfer characteristics of JFET**

Mathematical expression for g_m :

The transconductance can be calculated from the following equation which states that,

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$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] \quad ...(2)$$

In Equation (2) g_{m0} is the value of g_m for $V_{GS} = 0$.

The expression for g_{m0} is given by,

$$g_{m0} = \frac{-2\,I_{DSS}}{V_P} \quad ...(3)$$

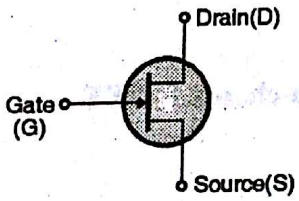
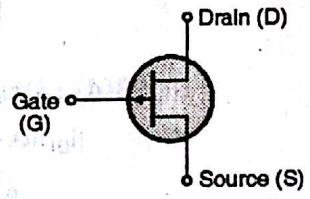
Typically g_m varies between 0.25 mS and 2mS.

Q. 3(d) Determine the magnitude of g_m for a JFET with I_{DSS} = 8 mA and V_P = – 4 V at dc bias points V_{GS} = – 0.5 V and also at V_{GS} = – 2.5 V. **(5 Marks)**

Ans. : Please refer Q. 3(d) of Dec. 2015.

Q. 6(d) Compare n-channel and p-channel JFET with respect to their device features and voltage current characteristics. **(5 Marks)**

Ans. :

Sr. No.	n-channel JFET	p-channel JFET
1.	n-type semiconductor bar is being used with two P-type gate regions.	P-type semiconductor bar is being used with two n-type gate regions.
2.	In n-channel current flows due to electrons.	In p-channel, current flows due to holes.
3.	 (B-263) **Fig. 3(a)**	 (B-2545(a)) **Fig. 3(b)**
4.	V_{GS} is negative for an n-channel JFET	V_{GS} is positive for p-channel JFET.
5.	Drain characteristics : Refer Fig. 3(c)	Drain characteristics : Refer Fig. 3(d)
6.	Transfer characteristics : Refer Fig. 3(e)	Transfer characteristics : Refer Fig. 3(f)

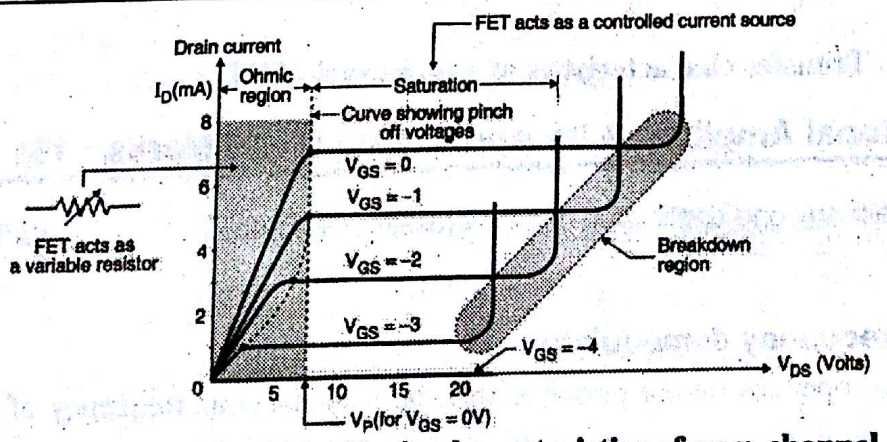


Fig. 3(c) : Drain characteristics of an n-channel JFET

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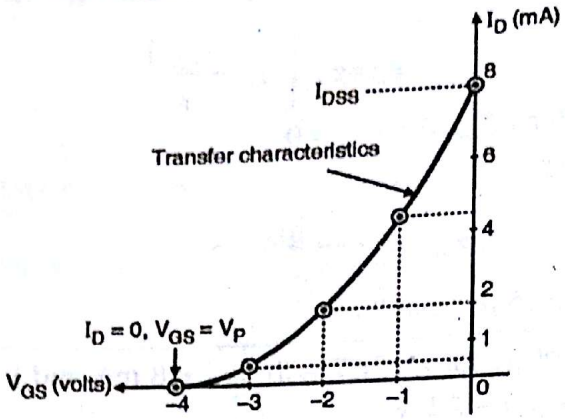

Fig. 3(e) : Transfer characteristics of a JFET

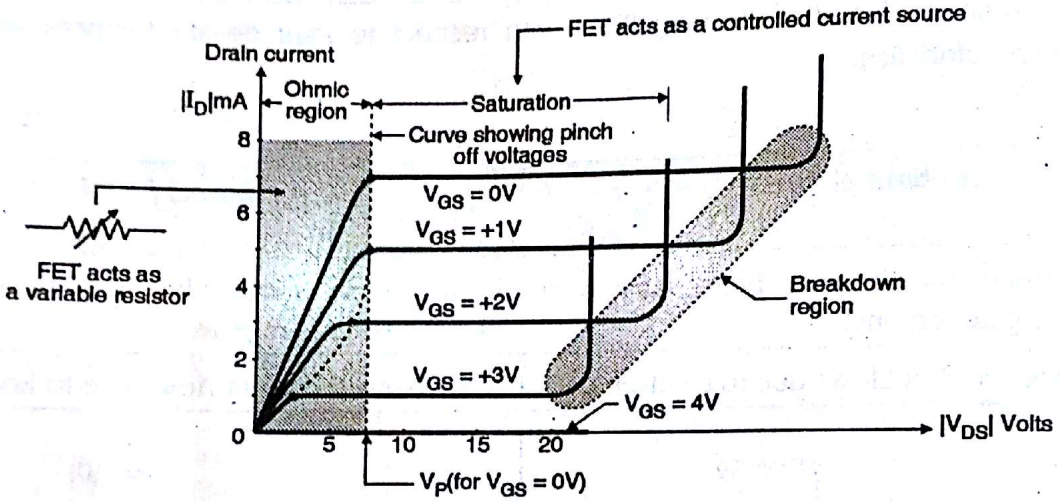

Fig. 3(d) : Drain characteristics of a p-channel JFET

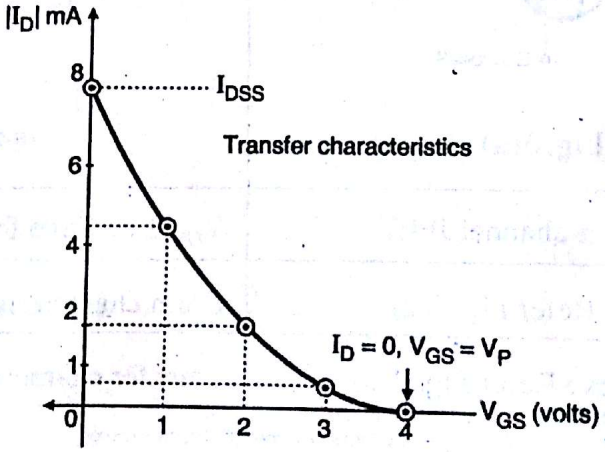

Fig. 3(f) : Transfer characteristics of a p-channel JFET

Chapter 2 : Operational Amplifier & its Application [Total Marks : 15]

Q. 1(b) With neat diagram explain any one application of zero-crossing detector. **(5 Marks)**

Ans. :

Zero crossing detector as frequency demodulator :

The zero crossing detector operates on the principle that the instantaneous frequency of an FM wave is approximately given by,

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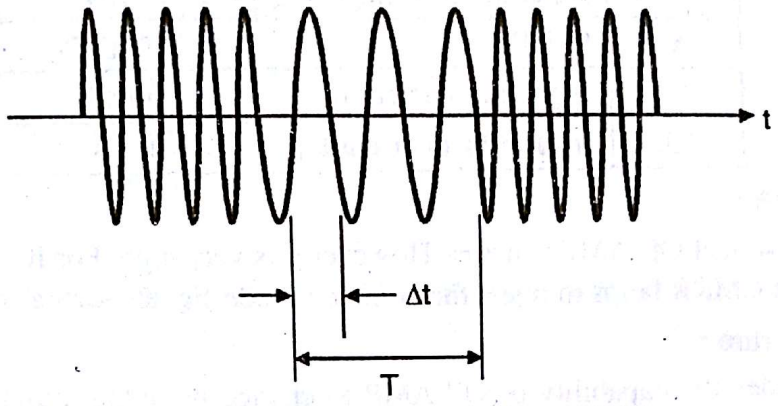
$$f_i \approx \frac{1}{2\Delta t} \quad ...(1)$$

Where Δt is the time difference between the adjacent zero crossover points of the FM wave as shown in Fig. 4.



(D-311) **Fig. 4 : Definitions of T and Δt for an FM wave**

Consider a time duration T as shown in Fig. 4. The time T is chosen such that it satisfies the following two conditions :

1. T should be small as compared to (1 / W) where W is the bandwidth of the message signal
2. T should be large as compared to $(1 / f_c)$ where f_c is the carrier frequency of the FM wave.

Let the number of zero crossings during interval T be denoted by n_o. Hence Δt i.e. the time between the adjacent zero crossing points is given by,

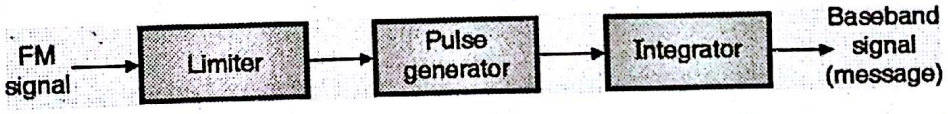
$$\Delta t = \frac{T}{n_o} \quad ...(2)$$

Therefore the instantaneous frequency is given by,

$$f_i = \frac{1}{2\,\Delta t} = \frac{n_o}{2T} \quad ...(3)$$

By definition of the instantaneous frequency, we know that there is a linear relation between f_i and message signal x (t). Hence we can recover x (t) if n_o is known.

This can be achieved by using a zero crossing detector of Fig. 5..



(D-312) **Fig. 5 : Block diagram of zero crossing detector**

Q. 2(b) List down various parameters of Opamp alongwith their typical values for IC741. Also explain what the significance of CMRR and slew rate is ? **(10 Marks)**

Ans. :

Typical values for IC741 :

Sr. No.	Characteristics	Value for IC 741
1.	Input resistance R_i	2 MΩ
2.	Output resistance R_o	75 Ω
3.	Voltage gain A_V	2×10^5
4.	Bandwidth B.W.	1 MHz

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Sr. No.	Characteristics	Value for IC 741
5.	CMRR	90 dB
6.	Slew rate S	0.5 V/μS
7.	Input offset voltage V_{ios}	2 mV
8.	PSRR	150 μV/V
9.	Input bias current I_B	50 nA
10.	Input offset current I_{ios}	6 nA

Significance of CMRR :

CMRR of a practical OP-AMP is not ∞. However it is very high. For IC 741, the CMRR is 90 dB or 31622. Such a high CMRR helps to reject the common mode signals such as noise, successfully.

Significance of slew rate :

Slew rate decides the capability of OP-AMP to change its output rapidly, hence it decides the highest frequency of operation of a given OP-AMP. The value of slew rate depends on the change in voltage gain. Therefore it is generally specified at unity (+ 1) gain. Slew rate should be ideally ∞ and practically as high as possible. Slew rate of 741 OP-AMP is only 0.5 V/μS, which is its biggest drawback. Therefore it cannot be used for high frequency applications.

Q. 3(a) Explain how operational amplifier can be used for taking average of three signals. **(5 Marks)**

Ans. : Please refer Q. 2(b) of Dec. 2013.

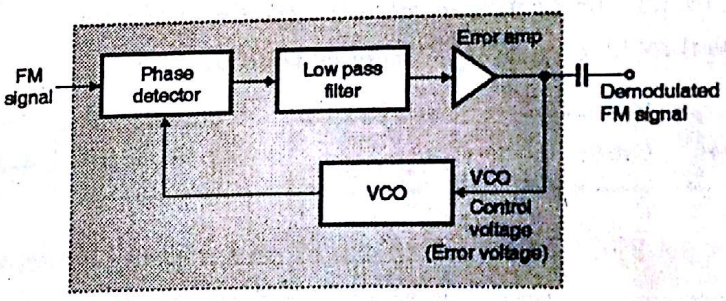
Chapter 3 : Phase Locked Loop (PLL) [Total Marks : 15]

Q. 1(c) With neat block diagram explain how PLL can be used to generate large number of frequencies from a single reference frequency. **(5 Marks)**

Ans. : Please refer Q. 1(b) of Dec. 2013.

Q. 4(b) Explain the use of PLL as FM detector. **(10 Marks)**

Ans. : A PLL can be used as FM demodulator as shown in Fig. 6.



(K-864)**Fig. 6 : PLL used as FM demodulator**

Operation :

The FM signal which is to be demodulated is applied at the input of the PLL. As the PLL is locked to the FM signal, the VCO starts tracking the instantaneous frequency in the FM input signal. The error voltage produced at the output of the amplifier is proportional to the deviation of input frequency from the centre frequency of FM. Thus the ac component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output. The FM demodulator using PLL ensures a highly linear relationship, between the instantaneous input frequency and VCO control voltage (error amplifier output).

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Chapter 4 : Modulation [Total Marks : 35]

Q. 3(b) Explain fly wheel effect in class C amplifier. **(5 Marks)**

Ans. : Please refer Q. 3(b) of Dec. 2015.

Q. 4(a) Explain generation of SSB using phase shift method. **(10 Marks)**

Ans. : Please refer Q. 4(a) of Dec. 2013.

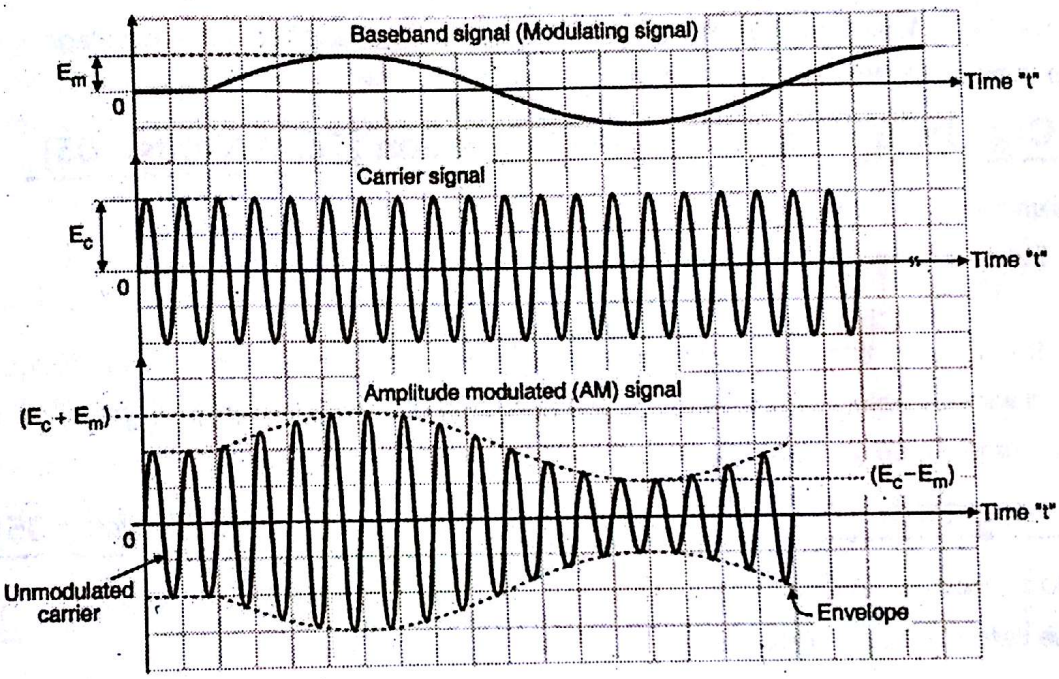
Q. 5(b) Explain the concept of amplitude modulation. **(10 Marks)**

Ans. ;

Amplitude modulation (AM) or Amplitude Modulation with Full Carrier (AM-FC) is the process of changing the amplitude of a high frequency sinusoidal carrier signal in proportion with the instantaneous value of modulating signal.

How does an AM wave look like ?

Fig. 7 shows the amplitude modulated wave when the modulating signal is a sinusoidal signal.



(D-12) **Fig. 7 : AM waveform for sinusoidal modulating signal**

Observations :

1. The frequency of the sinusoidal carrier is much higher than that of the modulating signal.
2. In AM the instantaneous amplitude of the sinusoidal high frequency carrier is changed in proportion to the instantaneous amplitude of the modulating signal. This is the principle of AM.
3. The time domain display of AM signal is as shown in Fig. 7. This AM signal is transmitted by a transmitter. The information in the AM signal is contained in the amplitude variations of the carrier of the envelope shown by dotted lines in Fig. 7.
4. Note that the frequency and phase of the carrier remain constant.
5. AM is used in the applications such as radio transmission, TV transmission etc.

Q. 6(a) Write short note on generation of FM by Armstrong method. **(5 Marks)**

Ans. : Please refer Q. 6(c) of Dec. 2015.

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Q. 6(c) Explain the necessity and significance of modulation in communication. **(5 Marks)**

Ans. :

Need of modulation :

The baseband transmission has many limitations which can be overcome using modulation. In the process of modulation, the baseband signal is "translated" i.e. shifted from low frequency side to high frequency side of the frequency spectrum. This frequency shift is proportional to the frequency of carrier.

Significance of modulation :

1. Reduction in the height of antenna
2. Avoids mixing of signals
3. Increases the range of communication
4. Multiplexing becomes possible
5. Improves quality of reception.

Chapter 5 : Demodulation [Total Marks : 10]

Q. 5(a) Explain superheterodyne receiver in detail alongwith the waveforms at each stage. **(10 Marks)**

Ans. : Please refer Q. 3(b) of May 2014.

Chapter 6 : Analog Pulse Modulation [Total Marks : 05]

Q. 3(c) Explain Nyquist criteria. **(5 Marks)**

Ans. : Please refer Q. 6(d) of Dec. 2013.

Chapter 8 : Multiplexing [Total Marks : 05]

Q. 1(d) Explain with suitable example what do you understand by signal multiplexing ? **(5 Marks)**

Ans. : Please refer Q. 5(b) of May 2014.

Appendix-A : D/A and A/D Converters [Total Marks : 05]

Q. 6(b) Mention important specifications of ADC and DAC required for communication. **(5 Marks)**

Ans. : Please refer Q. 1(a) of Dec. 2015.

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Dec. 2013

Q. 1 (a) What do you understand by "pinch off" voltage and "cut off" voltage as applied to FET ? **(5 Marks)**

(b) With neat block diagram explain how PLL can be used to generate large number of frequencies from a single reference frequency. **(5 Marks)**

(c) For an FM radio receiver, when the consumer changes the channel, the oscillator frequency changes. The frequency of radio signal coming out of the mixer will be always 10.7 MHz regardless of the channel selected. If the oscillator frequency is 99.2 MHz, what is the frequency of station selected ? If a Hartley tuned oscillator is being used with a variable capacitor in the LC tank circuit, what is the value of capacitance if the total inductance is 2.5 μH. **(5 Marks)**

(d) Optical sensor of a package counting system create 1.5 V DC signal when it detects the seal. This voltage need to be amplified and sent to a controller with an input resistance of 5 kΩ. Draw block diagram for the system. Choose correct amplifier to drive this low resistance load and select the resistor values to set the gain. The input voltage range for the controller is +10 V to +30 V DC. **(5 Marks)**

Q. 2 (a) Determine V_{GSQ}, I_{DQ} and V_{DSQ} and A_V for a voltage divider circuit with $V_{DD} = 18$ V, $R_D = 2.2$ k, $R_1 = 2.1$ M, $R_2 = 330$ k and $R_S = 1.2$ k, $I_{DSS} = 10$ mA, $V_P = -8$ V and $V_{DS} = 40$ μS. **(10 Marks)**

(b) Explain how op-amp can be used as a summing, scaling and averaging amplifier in the inverting configuration ? **(10 Marks)**

Q. 3 (a) Sketch an op-amp integrating circuit together with the circuit waveforms. Explain in brief the circuit operation. **(5 Marks)**

(b) Explain the fly wheel effect in class C amplifier. **(5 Marks)**

(c) Explain why crystal oscillators are considered to be more stable than other oscillators ? **(5 Marks)**

(d) Compare different biasing circuits with respect to Q-point. Comment on which biasing circuit is better in stability. **(5 Marks)**

Q. 4 (a) Draw the block diagram of a phase cancellation SSB generation and explain how the carrier and unwanted sideband are supposed. What change is necessary to suppress the other side band ? **(10 Marks)**

(b) Draw Foster Seeley discriminator with circuit diagram and explain its working with phasor diagrams. **(10 Marks)**

Q. 5 (a) What is multiplexing in communication system ? Draw block diagram of TDM-PCM system and explain. **(10 Marks)**

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(b) One input to a conventional AM modulator is a 500 kHz carrier with an amplitude of 20 V_P. The second input is a 10 kHz modulating signal that is of sufficient amplitude to cause a change in the output wave of ± 7.5 V_P. Determine :

1. Upper and lower side frequencies
2. Modulation coefficient and percent modulation
3. Peak amplitude of the modulated carried and upper and lower side frequency voltages
4. Expression for the modulated wave **(10 Marks)**
5. Draw the output spectrum.

Q. 6 (a) What are the drawbacks of delta modulation and how are they overcome by ADM ? **(5 Marks)**

(b) Explain in brief the principle of superheterodyne receiver. **(5 Marks)**

(c) Compare PAM, PPM and PWM. **(5 Marks)**

(d) What is meant by Nyquist rate in sampling ? What is standard frequency for speech signal ? **(5 Marks)**

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May 2014

Q. 1 (a) Explain input offset voltage, CMRR and SVRR for operational amplifier. **(5 Marks)**

(b) Explain Barkhausen's criteria for principle of oscillation. **(5 Marks)**

(c) Explain principle of FDM. **(5 Marks)**

(d) Compare FM and AM. **(5 Marks)**

Q. 2 (a) Sketch a typical drain characteristics for $V_{GS} = 0$ for an n-channel JEFET. Explain the shape of the characteristics, identify regions and indicate the important current and voltage levels. **(10 Marks)**

(b) Explain class C BJT power amplifier in detail. Compare it with class A BJT power amplifier. **(10 Marks)**

Q. 3 (a) Explain amplitude modulation for more than one modulating signal in following cases :

(i) Mathematical equation (ii) AM waveform
(iii) Am amplitude and power spectrum (iv) Modulation coefficient
(v) Transmission power **(10 Marks)**

(b) Explain with block diagram AM superheterodyne receiver. **(10 Marks)**

Q. 4 (a) Explain ideal as well as practical differentiator using operational amplifier in detail. **(10 Marks)**

(b) The antenna current of an AM broadcast transmitter, modulated to a depth of 40% by an audio sine wave is 11A. It increase to 12 A as result of simultaneous modulation by another audio sine wave. What is the modulation index due to this second wave. **(10 Marks)**

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Q. 5 (a) State sampling theorem. What happens if the sampling is done at less than 2 f_{max}. **(10 Marks)**

(b) What is multiplexing in communication system ? Draw black diagram of TDM-PCM system and explain ? **(10 Marks)**

Q. 6 (a) Explain PLL as a frequency synthesizer. **(5 Marks)**

(b) Explain operating principle of PLL. **(5 Marks)**

(c) List different types of ADC's and explain binary weighed ADC in detail. **(10 Marks)**

Dec. 2014

Q. 1 Solve the following : **(20 Marks)**

(a) Mention five important specifications of ADC/DAC that are looked at while selecting them for any application.

(b) Discuss the factors that influence modulation index of an FM wave.

(c) Draw FET based Hartley and Colpitt Oscillator. What is the frequency of oscillation if

(i) L_1= 10 mH, L_2 = 10 mH and C=0.1μF for Hartley tank circuit

(ii) L=10 mH, C_1 = 0.1μF and C_2 = 0.1 μF for Colpitt tank circuit.

(d) A public address system is connected to a microphone that has a maximum output voltage of 10mV. The microphone is connected to a 10 watt audio amplifier system that is driving an 8 Ohm speaker. The voltage amplifier is a noninverting op-amp circuit. Calculate the maximum voltage gain for the voltage amplifier stage and determine the resistor values to obtain the desired gain. Assume the power amplifier stage has a voltage gain of 1

Q. 2. (a) With proper circuit diagrams and transfer characteristics indicating Q-points do comparison of JFET bias circuits in detail. **(10 Marks)**

(b) Find R_1 and R_2 in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when ω = 10,000 rad/s. Use capacitance of 0.01μF. **(10 Marks)**

Q. 3 (a) Sketch a block representation for an n-channel JFET, showing bias voltages, depletion regions and current directions. Label the device terminals and explain its operation. Explain the effect of increasing levels of negative gate-source voltage.

Also sketch a typical drain characteristics .for V_{GS} = 0 for an n-channel JFET. Explain the shape of the characteristic, identify the regions and indicate the important current and voltage levels. **(10 Marks)**

(b) Draw the spectrum of an amplitude modulated wave and explain its components. **(5 Marks)**

(c) Draw and explain opamp non inverting comparator. Draw input and output waveforms for V_{ref} positive and also for V_{ref} negative. **(5 Marks)**

Q. 4 (a) Explain the working of a superheterodyne receiver with the help of a neat block diagram. Show the waveforms at the output of each block. **(10 Marks)**

(b) What is DSBSC wave? Explain its generation using balanced modulator. **(10 Marks)**

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Q. 5 (a) Draw the PAM, PWM and PPM waveforms in time domain assuming a sinusoidal modulating signal. Explain them in brief. **(10 Marks)**

(b) The maximum deviation allowed in a FM broadcast system is 75kHz. If the modulating signal is a single tone sinusoidal of frequency 15kHz, find the bandwidth of the FM signal. How does the bandwidth change if the modulating frequency is doubled?

(c) How is adaptive delta modulation superior to delta modulation? **(5 Marks)**

Q. 6 (a) What do you understand by signal multiplexing? Explain TDM and FDM with suitable examples. **(10 Marks)**

(b) With neat circuit diagram explain the use of PLL as phase shifter. **(5 Marks)**

(c) Give advantages and disadvantages of SSB over full carrier DSB amplitude modulated wave. **(5 Marks)**

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May 2015

Q. 1 (a) Draw and explain FET based Hartley and Colpitt oscillator. **(5 Marks)**

(b) Comment on the following ADC / DAC specifications :

1. Resolution 2. Linearity 3. Accuracy
4. Settling time 5. Stability **(5 Marks)**

(c) How is adaptive delta modulation superior to delta modulation? **(5Marks)**

(d) Discuss the factors that influence modulation index of an FM wave. **(5 Marks)**

Q. 2 (a) Sketch a block representation for an n-channel JFET, showing bias voltages, depletion regions, and current directions. Label the device terminals and explain its operation. Explain the effect of increasing levels of negative gate-source voltage. Also sketch a typical drain characteristics for $V_{GS} = 0$ for an n-channel JFET. Explain the shape of the characteristic, identify the regions and indicate the important current and voltage levels. **(10 Marks)**

(b) Design an op-amp differentiator that will differentiate an input signal with $f_{max} = 100$ Hz. Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator. Also repeat it for square wave input. **(10 Marks)**

Q. 3 (a) Explain the different methods of biasing JFET along with their characteristics in detail. **(10 Marks)**

(b) Explain any one technique used of conversion of analog signal to digital with ADC. **(5 Marks)**

(c) Draw and explain op-amp inverting comparator. Draw input and output waveforms for $V_{ref} > 0$ and also for $V_{ref} < 0$. **(5 Marks)**

Q. 4 (a) Draw Foster Seeley discriminator with circuit diagram and explain its working with phasor diagrams. **(10 Marks)**

(b) What is DSBSC wave ? Explain its generation using balanced modulator. **(10 Marks)**

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Q. 5 (a) Draw the PAM, PWM and PPM waveforms in time domain assuming a sinusoidal modulating signal. Explain them in brief. **(10 Marks)**

(b) In an AM radio receiver the loaded Q of the antenna circuit at the input to the mixer is 100. If the intermediate frequency is 455 kHz, calculate the image frequency and its rejection at 1 MHz. **(5 Marks)**

(c) With neat circuit diagram explain the use of PLL in frequency translator. **(5 Marks)**

Q. 6 (a) What do you understand by signal multiplexing ? Explain TDM and FDM with suitable examples. **(10 Marks)**

(b) Draw the spectrum of an amplitude modulated wave and explain its components. **(5 Marks)**

(c) Compare class A and class C power amplifiers. **(5 Marks)**

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Dec. 2015

Q. 1 (a)1. Give reasons for the following : FET is called as a square law device. **(5 Marks)**

(a)2. Give reasons for the following :
Barkhausens criteria should be satisfied to get oscillations. **(5 Marks)**

(b) With neat diagram explain any one application of zero-crossing detector. **(5 Marks)**

(c) With neat circuit diagram explain the use of PLL as a phase shifter. **(5 Marks)**

(d) Explain with suitable example what do you understand by signal multiplexing ? **(5 Marks)**

Q. 2 (a) Draw and explain JFET characteristics. Also show that for a JFET,

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} \cdot I_{DS}}$$ **(10 Marks)**

(b) With respect to op-amp explain the ideal characteristics and concept of virtual ground. Explain how op-amp can be used as an averaging amplifier in inverting configuration. Also draw neat circuit diagrams to :

1. Convert sine wave to square wave using op-amp.
2. Detect the crossing of zero's in the generated square wave. **(10 Marks)**

Q. 3 (a) Explain how operational amplifier can be used for addition of two AC signals with one DC signal. **(5 Marks)**

(b) Explain fly wheel effect in class C amplifier. **(5 Marks)**

(c) What is sampling theorem and state its significance in communication. What is the standard frequency for speech signal ? **(5 Marks)**

(d) Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points :

(a) $V_{GS} = -0.5$ V, (b) $V_{GS} = -1.5$ V

(c) $V_{GS} = -2.5$ V **(5 Marks)**

Q. 4 (a) Explain generation of SSB using phase shift method. **(10 Marks)**

(b) Discuss the operating principle of PLL and explain its use as frequency translator. **(10 Marks)**

Q. 5 (a) With neat diagram explain the circuit for FM detection. **(10 Marks)**

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(b) Explain amplitude modulation for more than one modulating signal in the following cases : (10 Marks)

1. Mathematical equation
2. AM waveform
3. AM amplitude and power spectrum
4. Modulation coefficient
5. Transmission power

Q. 6 (a) Explain application of PLL as frequency synthesizer. (5 Marks)

(b) With block diagram explain TDM-PCM system. (5 Marks)

(c) Write short note on generation of FM by Armstrong method. (5 Marks)

(d) Compare different biasing techniques for JFET. (5 Marks)

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May 2016

Q. 1 (a) Justify that JFET can be used as a voltage variable resistor. (5 Marks)

(b) With neat diagram explain any one application of zero-crossing detector. (5 Marks)

(c) With neat block diagram explain how PLL can be used to generate large number of frequencies from a single reference frequency. (5 Marks)

(d) Explain with suitable example what do you understand by signal multiplexing ? (5 Marks)

Q. 2 (a) Derive an expression for trans-conductance for JFET. (10 Marks)

(b) List down various parameters of Opamp alongwith their typical values for IC741. Also explain what the significance of CMRR and slew rate is ? (10 Marks)

Q. 3 (a) Explain how operational amplifier can be used for taking average of three signals. (5 Marks)

(b) Explain fly wheel effect in class C amplifier. (5 Marks)

(c) Explain Nyquist criteria. (5 Marks)

(d) Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at dc bias points $V_{GS} = -0.5$ V and also at $V_{GS} = -2.5$ V. (5 Marks)

Q. 4 (a) Explain generation of SSB using phase shift method. (10 Marks)

(b) Explain the use of PLL as FM detector. (10 Marks)

Q. 5 (a) Explain superheterodyne receiver in detail alongwith the waveforms at each stage. (10 Marks)

(b) Explain the concept of amplitude modulation. (10 Marks)

Q. 6 (a) Write short note on generation of FM by Armstrong method. (5 Marks)

(b) Mention important specifications of ADC and DAC required for communication. (5 Marks)

(c) Explain the necessity and significance of modulation in communication. (5 Marks)

(d) Compare n-channel and p-channel JFET with respect to their device features and voltage current characteristics. (5 Marks)

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