
Report : timing
-path full
-delay min
-max_paths 1
Design : Switch
Version: 0-2018.06-SP4
Date : Mon Dec 20 17:24:05 2021

Operating Conditions: ff1p16v125c Library: saed32hvt_ff1p16v125c
Wire Load Model Mode: enclosed

Startpoint: pe_u/pe0/Rpipe_reg[0]
(rising edge-triggered flip-flop clocked by ideal_clk)
Endpoint: pe_u/pe1/Rpipe_reg[0]
(rising edge-triggered flip-flop clocked by ideal_clk)
Path Group: ideal_clk
Path Type: min

Des/Clust/Port	Wire Load Model	Library

Switch	8000	saed32hvt_ff1p16v125c
PEtotal	8000	saed32hvt_ff1p16v125c

Point	Incr	Path

clock ideal_clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
pe_u/pe0/Rpipe_reg[0]/CLK (DFFX1_LVT)	0.00	0.00 r
pe_u/pe0/Rpipe_reg[0]/Q (DFFX1_LVT)	0.05	0.05 r
pe_u/pe0/Rpipe[0] (PE_0)	0.00	0.05 r
pe_u/pe1/R[0] (PE_14)	0.00	0.05 r
pe_u/pe1/Rpipe_reg[0]/D (DFFX1_LVT)	0.00	0.05 r
data arrival time		0.05
clock ideal_clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
pe_u/pe1/Rpipe_reg[0]/CLK (DFFX1_LVT)	0.00	0.00 r
library hold time	0.01	0.01
data required time		0.01

data required time		0.01
data arrival time		-0.05

slack (MET)		0.04