Top.tb

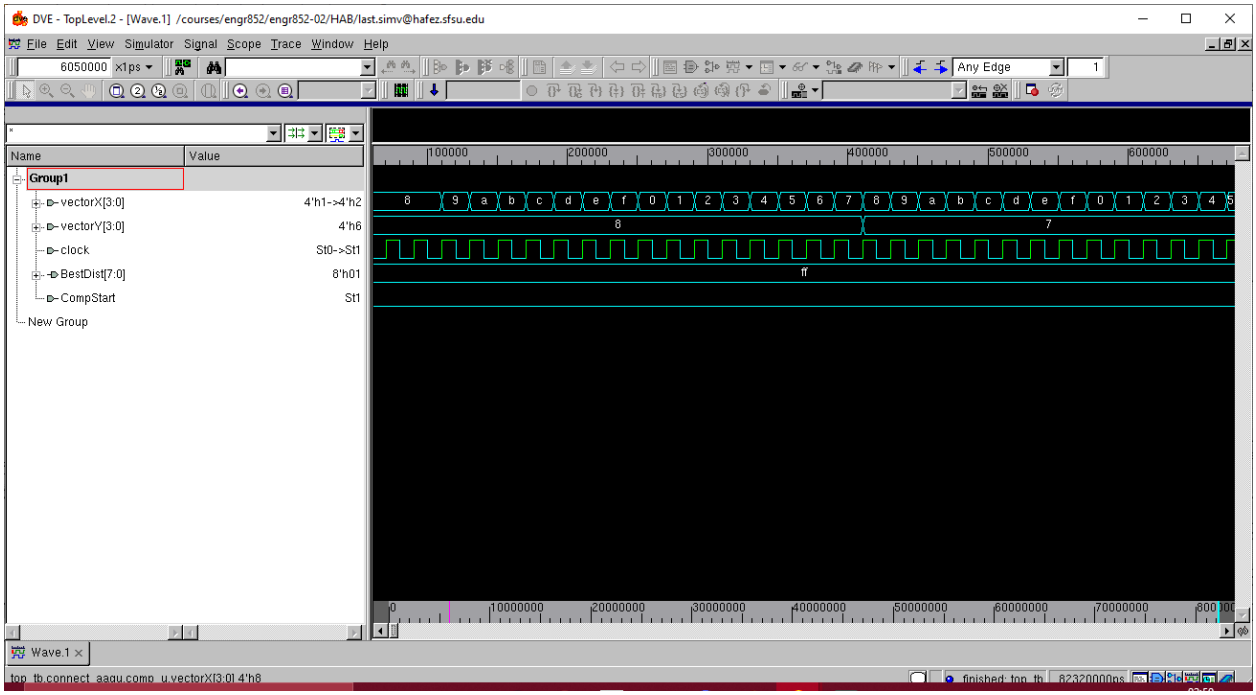
```
`timescale 1ns/1ps
module top_tb();
reg clock;
wire [7:0] AddressR;
wire [9:0] AddressS1, AddressS2;
reg [7:0] Rmem[255:0];
reg       [7:0] Smem[960:0];
reg [7:0] R, S1, S2;
reg start;

wire [7:0] BestDist;
wire [3:0] motionX, motionY;
wire [127:0] Accumulate;
wire [15:0] S1S2mux,newDist,PEready;
wire [3:0] VectorX, VectorY;
wire CompStart;

    //Switch connect (.clock(clock), .start(start), .BestDist(BestDist), .motionX(motionX),
.motionY(motionY),.R(R), .S1(S1), .S2(S2), .AddressR(AddressR), .AddressS1(AddressS1),
.AddressS2(AddressS2));


initial begin
$dumpfile("PE_dump1.vcd");
$dumpvars;
$readmemh("ref_memory.hex",Rmem);
$readmemh("search_memory.hex",Smem);
clock= 0;
start=0;
#100 start=1;

#(4111*2*10) $finish;
end

always #10 clock = ~clock;



always @(posedge clock)
 begin
          R <= Rmem[AddressR];
          S1 <= Smem[AddressS1];
          S2 <= Smem[AddressS2];
```

end

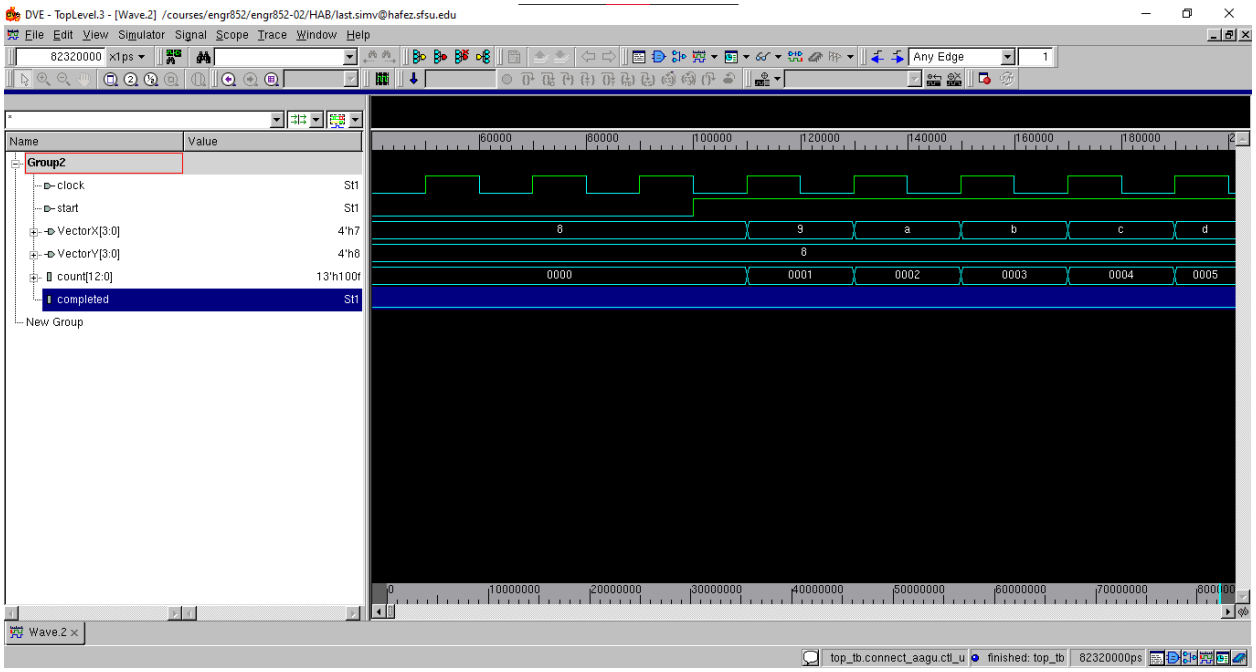
Switch connect_aagu (.clock(clock), .start(start), .BestDist(BestDist), .motionX(motionX), .motionY(motionY),.R(R), .S1(S1), .S2(S2), .AddressR(AddressR), .AddressS1(AddressS1), .AddressS2(AddressS2));

endmodule

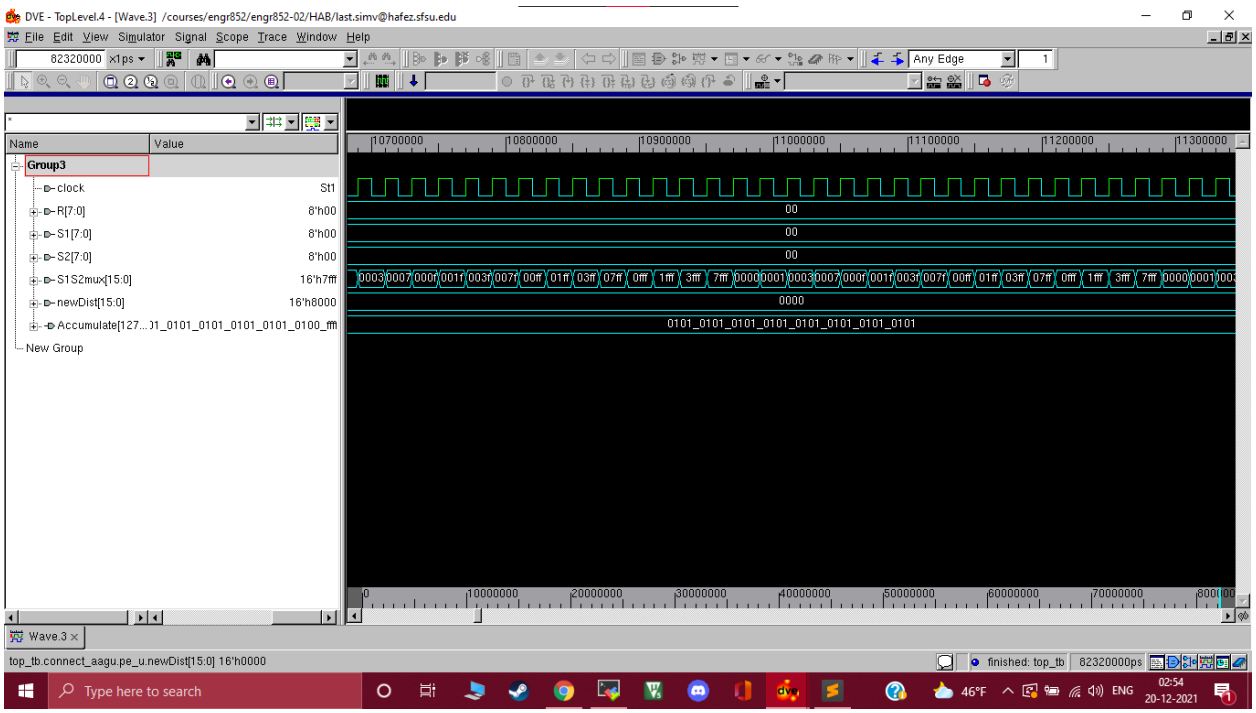
COMPARATOR VALUES



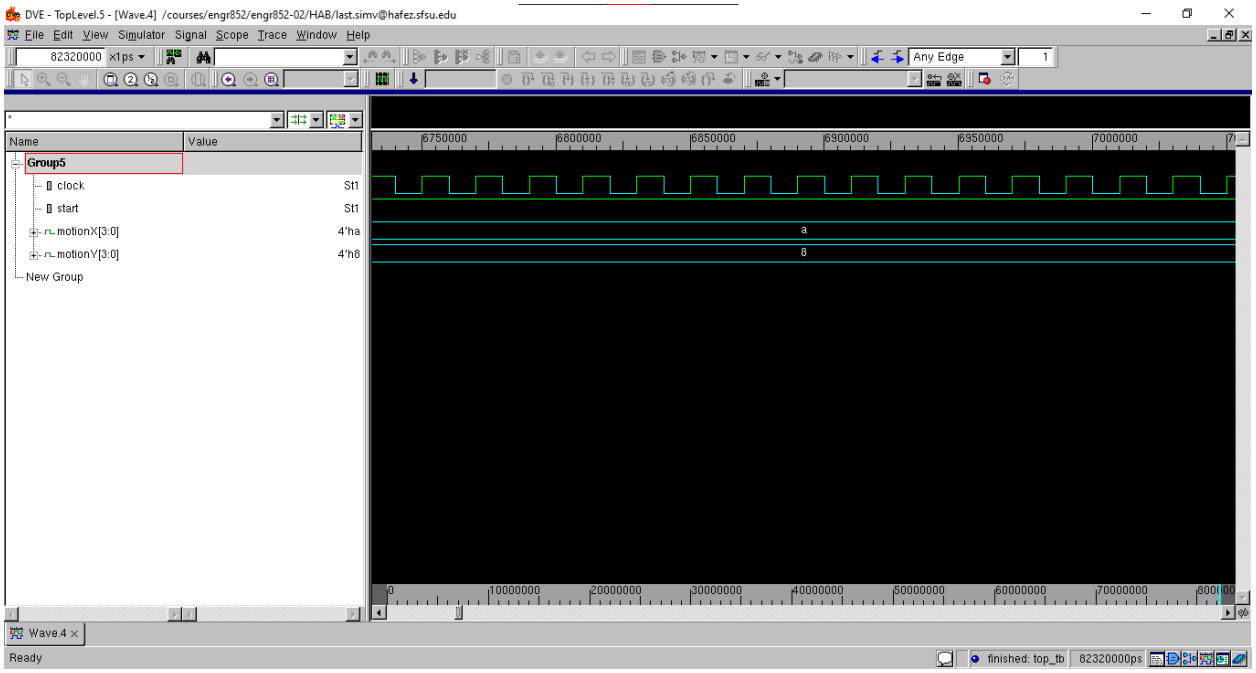
CONTROL UNIT



Processing Element



FINAL Values



****

Report : timing
-path full
-delay max
-max_paths 1
Design : Switch
Version: O-2018.06-SP4
Date : Mon Dec 20 17:26:45 2021
****

Operating Conditions: ff1p16v125c Library: saed32hvt_ff1p16v125c
Wire Load Model Mode: enclosed

Startpoint: ctl_u/count_reg[4]
(rising edge-triggered flip-flop clocked by ideal_clk)
Endpoint: comp_u/BestDist_reg[0]
(rising edge-triggered flip-flop clocked by ideal_clk)
Path Group: ideal_clk
Path Type: max

Des/Clust/Port	Wire Load Model	Library
Switch	8000	saed32hvt_ff1p16v125c

control 8000 saed32hvt_ff1p16v125c
Comparator 8000 saed32hvt_ff1p16v125c

Point	Incr	Path
clock ideal_clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
ctl_u/count_reg[4]/CLK (DFFSSRX1_LVT)	0.00	0.00 r
ctl_u/count_reg[4]/QN (DFFSSRX1_LVT)	0.05	0.05 f
ctl_u/U71/Y (AND2X1_LVT)	0.03	0.07 f
ctl_u/U69/Y (AND3X1_LVT)	0.04	0.11 f
ctl_u/U67/Y (AND3X1_LVT)	0.03	0.15 f
ctl_u/U44/Y (AND2X1_LVT)	0.04	0.19 f
ctl_u/U18/Y (AND2X1_LVT)	0.04	0.23 f
ctl_u/PEready[6] (control)	0.00	0.23 f
comp_u/PEready[6] (Comparator)	0.00	0.23 f
comp_u/U23/Y (NOR3X0_LVT)	0.03	0.26 r
comp_u/U25/Y (NAND4X0_LVT)	0.02	0.28 f
comp_u/U3/Y (INVX1_LVT)	0.02	0.30 r
comp_u/U61/Y (AO222X1_LVT)	0.05	0.36 r
comp_u/U70/Y (OR3X1_LVT)	0.03	0.38 r
comp_u/U69/Y (AO221X1_LVT)	0.04	0.42 r
comp_u/U122/Y (OR3X1_LVT)	0.03	0.45 r
comp_u/U121/Y (AO222X1_LVT)	0.04	0.50 r
comp_u/U130/Y (AO21X1_LVT)	0.03	0.53 r
comp_u/U129/Y (OA22X1_LVT)	0.03	0.55 r
comp_u/U139/Y (AND2X1_LVT)	0.02	0.57 r
comp_u/U138/Y (OAI222X1_LVT)	0.04	0.61 f
comp_u/U136/Y (OA221X1_LVT)	0.02	0.63 f
comp_u/U47/Y (AO221X1_LVT)	0.02	0.65 f
comp_u/U45/Y (OA221X1_LVT)	0.02	0.67 f
comp_u/U44/Y (AO21X1_LVT)	0.02	0.69 f
comp_u/U141/Y (AO22X1_LVT)	0.02	0.71 f
comp_u/U140/Y (NAND2X0_LVT)	0.02	0.73 r
comp_u/U38/Y (INVX1_LVT)	0.04	0.77 f
comp_u/U58/Y (AO221X1_LVT)	0.03	0.80 f
comp_u/BestDist_reg[0]/D (DFFX1_HVT)	0.00	0.80 f
data arrival time	0.80	
clock ideal_clk (rise edge)	3.85	3.85
clock network delay (ideal)	0.00	3.85
comp_u/BestDist_reg[0]/CLK (DFFX1_HVT)	0.00	3.85 r
library setup time	-0.02	3.82
data required time		3.82
data required time		3.82
data arrival time		-0.80
slack (MET)		3.02