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Report : timing

-path full
-delay max
-max\_paths 1
Design: Switch

Version: 0-2018.06-SP4

Date : Mon Dec 20 17:26:45 2021

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Operating Conditions: ff1p16v125c Library: saed32hvt\_ff1p16v125c

Wire Load Model Mode: enclosed

Startpoint: ctl\_u/count\_reg[4]

(rising edge-triggered flip-flop clocked by ideal\_clk)

Endpoint: comp\_u/BestDist\_reg[0]

Des/Clust/Port Wire Load Model Library

(rising edge-triggered flip-flop clocked by ideal\_clk)

Path Group: ideal\_clk

Path Type: max

Switch	8000	saed32hvt ff1p16v125c	
control	8000	saed32hvt ff1p16v125c	
Comparator 8000		saed32hvt_ff1p16v125c	
'			
Point		Incr	Path
clock ideal_clk (rise edge)		0.00	0.00
clock network delay (ideal)		0.00	0.00
ctl_u/count_reg[4]/CLK (DFFSSRX1_LVT)		0.00	0.00 r
ctl_u/count_reg[4]/QN (DFFSSRX1_LVT)		0.05	0.05 f
ctl_u/U71/Y (AND2X1_LVT)		0.03	0.07 f
ctl_u/U69/Y (AND3X1_LVT)		0.04	0.11 f
ctl_u/U67/Y (AND3X1_LVT)		0.03	0.15 f
ctl_u/U44/Y (AND2X1_LVT)		0.04	0.19 f
ctl_u/U18/Y (AND2X1_LVT)		0.04	0.23 f
ctl_u/PEready[6] (control)		0.00	0.23 f
<pre>comp_u/PEready[6] (Comparator)</pre>		0.00	0.23 f
comp_u/U23/Y (N	OR3X0_LVT)	0.03	0.26 r
comp_u/U25/Y (N	AND4X0_LVT)	0.02	0.28 f
comp_u/U3/Y (IN	VX1_LVT)	0.02	0.30 r
comp_u/U61/Y (A	0222X1_LVT)	0.05	0.36 r
comp u/U70/Y (OR3X1 LVT)		0.03	0.38 r
comp_u/U69/Y (A0221X1_LVT)		0.04	0.42 r
comp u/U122/Y (OR3X1 LVT)		0.03	0.45 r
comp u/U121/Y (A0222X1 LVT)		0.04	0.50 r
comp u/U130/Y (A021X1 LVT)		0.03	0.53 r
comp_u/U129/Y (OA22X1_LVT)		0.03	0.55 r
comp_u/U139/Y (AND2X1_LVT)		0.02	0.57 r
comp_u/U138/Y (OAI222X1_LVT)		0.04	0.61 f
comp_u/U136/Y (OA221X1_LVT)		0.02	0.63 f
comp_u/U47/Y (A0221X1_LVT)		0.02	0.65 f
comp_u/U45/Y (OA221X1_LVT)		0.02	0.67 f
comp_u/U44/Y (A021X1_LVT)		0.02	0.69 f
comp u/U141/Y (A022X1 LVT)		0.02	0.71 f
comp u/U140/Y (NAND2X0 LVT)		0.02	0.73 r
comp u/U38/Y (INVX1 LVT)		0.04	0.77 f
comp_u/U58/Y (A	0221X1_LVT)	0.03	0.80 f
comp_u/BestDist	reg[0]/D (DFFX1_HVT)	0.00	0.80 f
data arrival ti			0.80
<pre>clock ideal_clk</pre>	(rise edge)	3.85	3.85
clock network delay (ideal)		0.00	3.85
<pre>comp_u/BestDist_reg[0]/CLK (DFFX1_HVT)</pre>		0.00	3.85 r
library setup time		-0.02	3.82
data required time			3.82
data required t	ime		3.82
data arrival ti	me		-0.80
slack (MET)			3.02