Data Sheet

S6E63D6

Preliminary

240 RGB X 320 Dot 1-Chip Driver IC with LTPS Interface
for 262,144 Color AMOLED Display Panel

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System LSI Division
Device Solution Network
SAMSUNG ELECTRONICS CO., LTD.

(http://www.samsung.com/Products/Semiconductor/DisplayDriverIC)

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INTRODUCTION

The S6E63D6 is a single chip solution for Gate-IC-less AMOLED panel. Source driver with built-in memory, gate-IC-less level shifter and power circuits are integrated on this LSI. It can display to the maximum of 240-RGB x 320-dot graphics on 260k-color AMOLED panel. Moreover, the chip supports LTPS panel.

The S6E63D6 supports Qualcomm's high-speed serial interface, MDDI (Mobile Display Digital Interface) type I, which is an implementation of client device Video Electronics Standards Association (VESA) standard.
The MDDI is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link.

The S6E63D6 also supports 18-/16-/9-/8-bit high-speed bus interface to enable efficient data transfer to the GRAM.

There is an external interface. In case of display data, the S6E63D6 offers a flexible 18-/16-/6-bits bus of RGB interface for transferring the 260k colors display data.

The motion picture area can be designated in GRAM by window function. The specified window area can be updated selectively so that motion picture can be displayed simultaneously independent of still picture area.

The LSI operates at low voltage and has internal GRAMs to store 240-RGB x 320-dot 260k-color image data. Additionally, it has an internal booster that generates the OLED driving voltage and the voltage follower circuit for OLED driver.

The S6E63D6 is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities such as digital cellular phones supporting a web browser, bi-directional pagers, PMP, MP3P and small PDAs.

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FEATURES

Overalls

- 240-RGBx320-dot AM-OLED display controller/driver IC for 262,144 colors
- Gate IC less
- 240 channel source driver with time shared driving function

Various color-display control functions

- 262,144 colors can be displayed at the same time with RGB separated gamma adjust.
- 262,144 / 65,536/ 8 colors can be displayed.
- Vertical scroll display function in line units

Various interfaces

- 18-/16-/9-/8-bit high-speed parallel bus interface (80- and 68- system)
- Serial peripheral interface (SPI)
- 18-/16-/6-bit RGB interface
- MDDI (Mobile Display Digital Interface) support

Internal ram capacity: 240 x 18 x 320 = 1,382,400 bits

Writing to a window-ram address area by using a window-address function

Efficiently panel driving signals

- SOUT[1:240] : V0~V63 grayscale
- FLM, SFTCLK, SFTCLKB, SCLK1, SCLK2, CLA, CLB, CLC, BICTL_L, BICTL_R, EX_FLM, EX_CLK, EX_CLKB, ESR : VGL to VGH level

Low-power operation supports:

- Power-save mode: standby mode
- Partial display mode in any position

Internal oscillation circuit and external hardware reset

Internal power supply circuit

Operating voltage

- Apply voltage
  - I/O power-supply VDD3 to VSS = 1.65 to 3.3V
  - Analog power-supply VCI to VSS = 2.5 to 3.3V

- Generated voltage
  - VGH = 4.6 to 6.6V (gate circuit power supply)
  - VGL = -7.8 to -5.0V (gate circuit power supply)
  - VINT = - 4.0 to -1.0V (OLED pixel initialization first power supply)
  - Source output range = 0.96 to 4.2V

Released package type

- S6E63D6 is released COG type package format only.

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BLOCK DIAGRAM

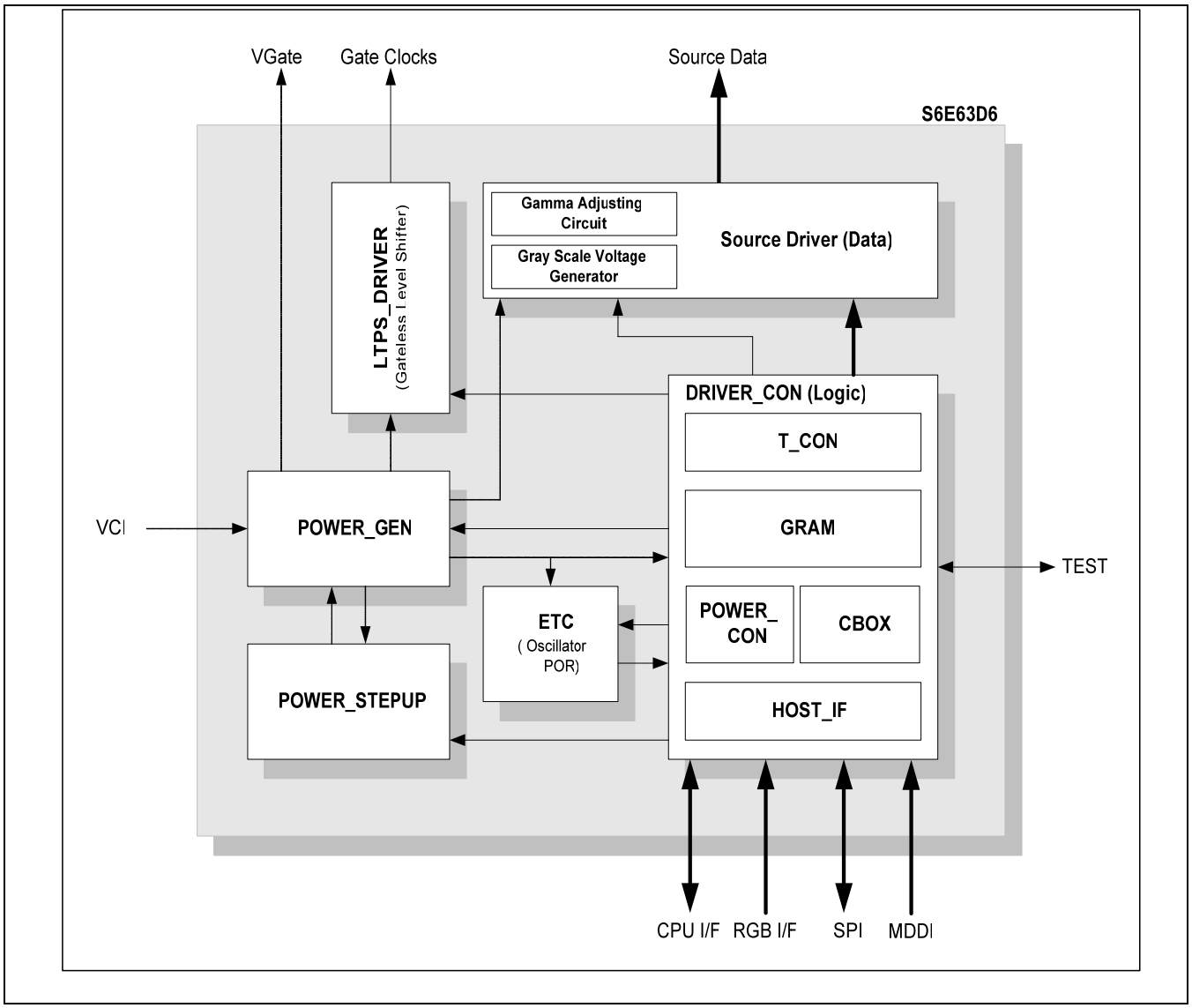

Figure1: S6E63D6 Block Diagram

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PAD CONFIGURATION

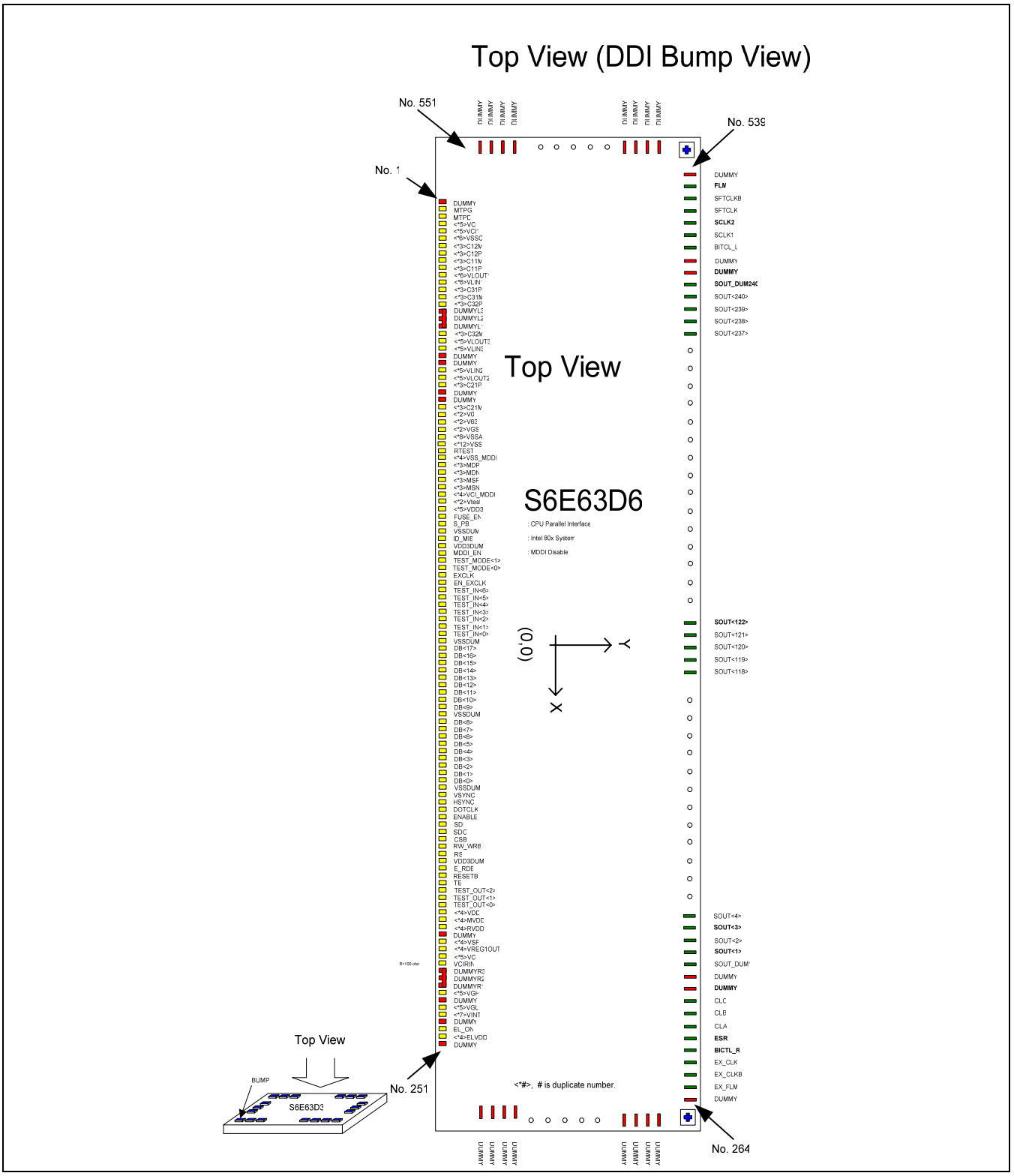

Figure2: Pad Configuration

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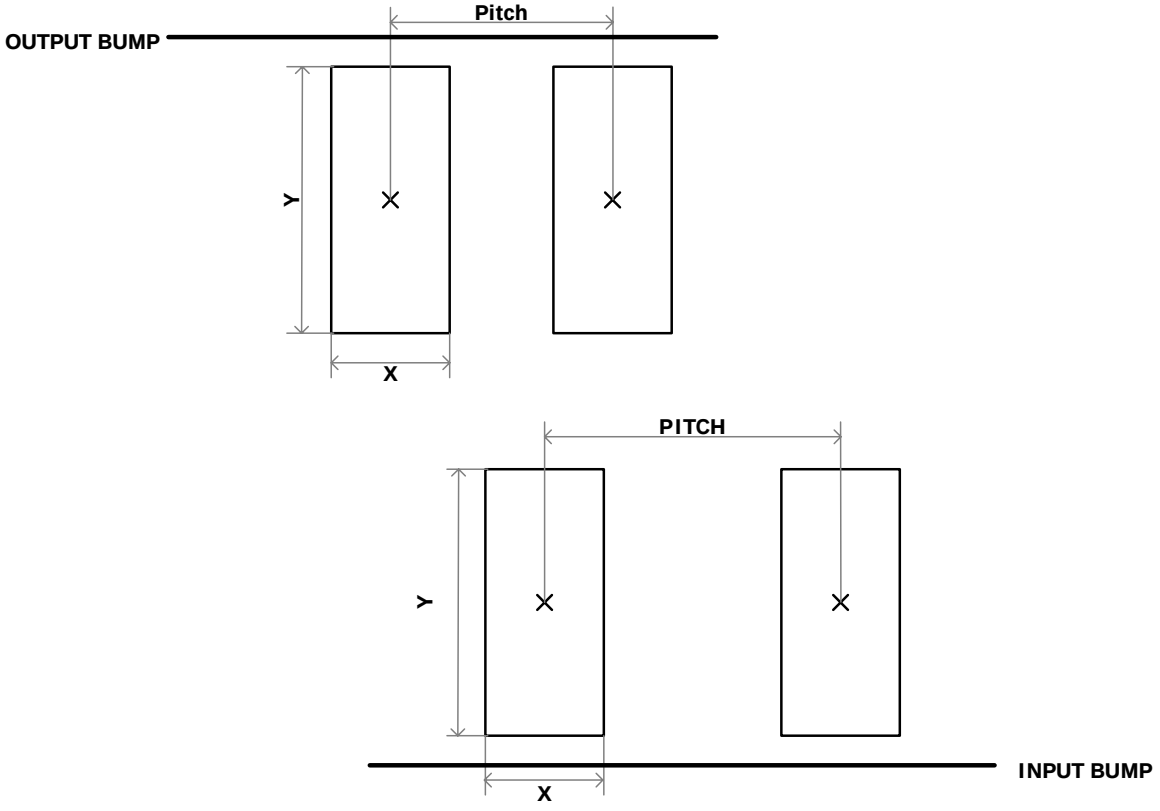
Table1: S6E63D6 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size (With scribe lane; 80um)	-	15,580	1,330	um
Chip thickness	-	300		
Bump pitch	Input pad	60		
	Output pad	54		
Pad size	Input pad (1-251)	30	91	
	Output pad (264-539)	36	91	
	Output pad (252-263, 540-551)	91	36	
Bump Height	All PADs	15 ± 3		



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ALIGN KEY CONFIGURATION AND COORDINATE

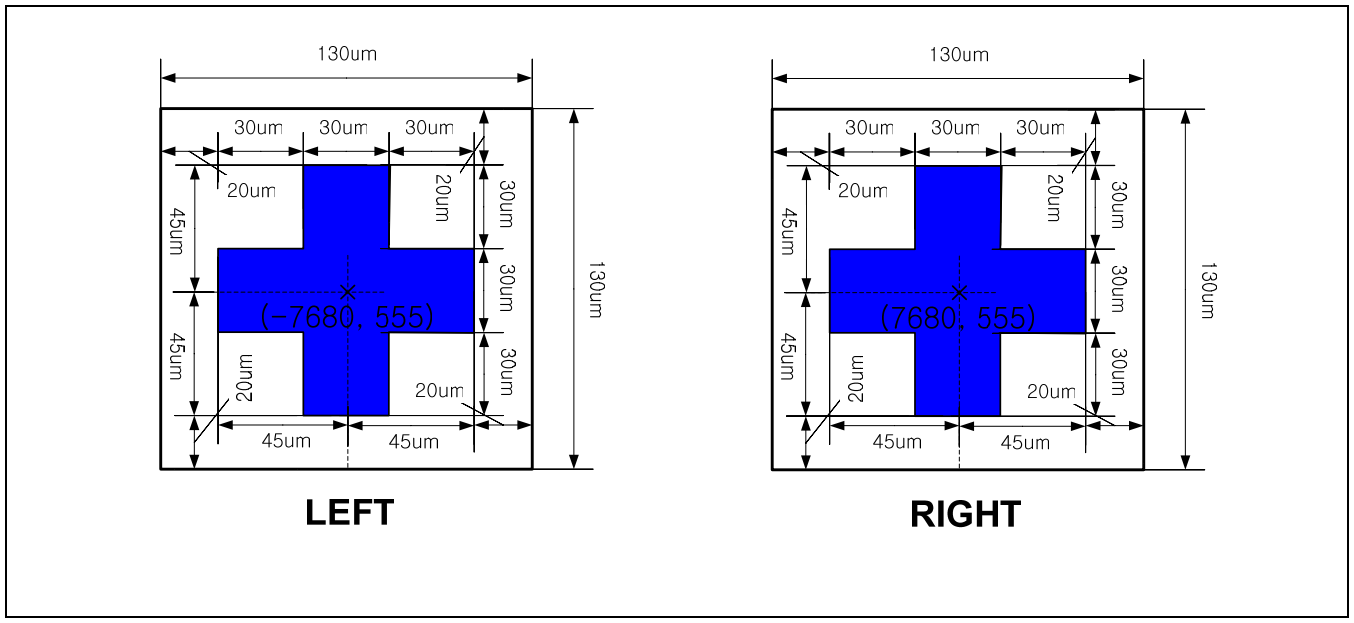

Figure3: COG Align Key

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PAD CENTER COORDINATES

Table2: Pad Center Coordinates

[Unit: um]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-7500.0	-572.5	51	C32P	-4500.0	-572.5	101	VSSA	-1500.0	-572.5
2	MTPG	-7440.0	-572.5	52	C32P	-4440.0	-572.5	102	VSSA	-1440.0	-572.5
3	MTPD	-7380.0	-572.5	53	DUMMYL3	-4380.0	-572.5	103	VSS	-1380.0	-572.5
4	VCI	-7320.0	-572.5	54	DUMMYL2	-4320.0	-572.5	104	VSS	-1320.0	-572.5
5	VCI	-7260.0	-572.5	55	DUMMYL1	-4260.0	-572.5	105	VSS	-1260.0	-572.5
6	VCI	-7200.0	-572.5	56	C32M	-4200.0	-572.5	106	VSS	-1200.0	-572.5
7	VCI	-7140.0	-572.5	57	C32M	-4140.0	-572.5	107	VSS	-1140.0	-572.5
8	VCI	-7080.0	-572.5	58	C32M	-4080.0	-572.5	108	VSS	-1080.0	-572.5
9	VCI1	-7020.0	-572.5	59	VLOUT3	-4020.0	-572.5	109	VSS	-1020.0	-572.5
10	VCI1	-6960.0	-572.5	60	VLOUT3	-3960.0	-572.5	110	VSS	-960.0	-572.5
11	VCI1	-6900.0	-572.5	61	VLOUT3	-3900.0	-572.5	111	VSS	-900.0	-572.5
12	VCI1	-6840.0	-572.5	62	VLOUT3	-3840.0	-572.5	112	VSS	-840.0	-572.5
13	VCI1	-6780.0	-572.5	63	VLOUT3	-3780.0	-572.5	113	VSS	-780.0	-572.5
14	VSSC	-6720.0	-572.5	64	VLIN3	-3720.0	-572.5	114	VSS	-720.0	-572.5
15	VSSC	-6660.0	-572.5	65	VLIN3	-3660.0	-572.5	115	RTEST	-660.0	-572.5
16	VSSC	-6600.0	-572.5	66	VLIN3	-3600.0	-572.5	116	VSS_MDDI	-600.0	-572.5
17	VSSC	-6540.0	-572.5	67	VLIN3	-3540.0	-572.5	117	VSS_MDDI	-540.0	-572.5
18	VSSC	-6480.0	-572.5	68	VLIN3	-3480.0	-572.5	118	VSS_MDDI	-480.0	-572.5
19	VSSC	-6420.0	-572.5	69	DUMMY	-3420.0	-572.5	119	VSS_MDDI	-420.0	-572.5
20	C12M	-6360.0	-572.5	70	DUMMY	-3360.0	-572.5	120	MDP	-360.0	-572.5
21	C12M	-6300.0	-572.5	71	VLIN2	-3300.0	-572.5	121	MDP	-300.0	-572.5
22	C12M	-6240.0	-572.5	72	VLIN2	-3240.0	-572.5	122	MDP	-240.0	-572.5
23	C12P	-6180.0	-572.5	73	VLIN2	-3180.0	-572.5	123	MDN	-180.0	-572.5
24	C12P	-6120.0	-572.5	74	VLIN2	-3120.0	-572.5	124	MDN	-120.0	-572.5
25	C12P	-6060.0	-572.5	75	VLIN2	-3060.0	-572.5	125	MDN	-60.0	-572.5
26	C11M	-6000.0	-572.5	76	VLOUT2	-3000.0	-572.5	126	MSP	0.0	-572.5
27	C11M	-5940.0	-572.5	77	VLOUT2	-2940.0	-572.5	127	MSP	60.0	-572.5
28	C11M	-5880.0	-572.5	78	VLOUT2	-2880.0	-572.5	128	MSP	120.0	-572.5
29	C11P	-5820.0	-572.5	79	VLOUT2	-2820.0	-572.5	129	MSN	180.0	-572.5
30	C11P	-5760.0	-572.5	80	VLOUT2	-2760.0	-572.5	130	MSN	240.0	-572.5
31	C11P	-5700.0	-572.5	81	C21P	-2700.0	-572.5	131	MSN	300.0	-572.5
32	VLOUT1	-5640.0	-572.5	82	C21P	-2640.0	-572.5	132	VCI_MDDI	360.0	-572.5
33	VLOUT1	-5580.0	-572.5	83	C21P	-2580.0	-572.5	133	VCI_MDDI	420.0	-572.5
34	VLOUT1	-5520.0	-572.5	84	DUMMY	-2520.0	-572.5	134	VCI_MDDI	480.0	-572.5
35	VLOUT1	-5460.0	-572.5	85	DUMMY	-2460.0	-572.5	135	VCI_MDDI	540.0	-572.5
36	VLOUT1	-5400.0	-572.5	86	C21M	-2400.0	-572.5	136	Vtest	600.0	-572.5
37	VLOUT1	-5340.0	-572.5	87	C21M	-2340.0	-572.5	137	Vtest	660.0	-572.5
38	VLIN1	-5280.0	-572.5	88	C21M	-2280.0	-572.5	138	VDD3	720.0	-572.5
39	VLIN1	-5220.0	-572.5	89	V0	-2220.0	-572.5	139	VDD3	780.0	-572.5
40	VLIN1	-5160.0	-572.5	90	V0	-2160.0	-572.5	140	VDD3	840.0	-572.5
41	VLIN1	-5100.0	-572.5	91	V63	-2100.0	-572.5	141	VDD3	900.0	-572.5
42	VLIN1	-5040.0	-572.5	92	V63	-2040.0	-572.5	142	VDD3	960.0	-572.5
43	VLIN1	-4980.0	-572.5	93	VGS	-1980.0	-572.5	143	FUSE_EN	1020.0	-572.5
44	C31P	-4920.0	-572.5	94	VGS	-1920.0	-572.5	144	S_PB	1080.0	-572.5
45	C31P	-4860.0	-572.5	95	VSSA	-1860.0	-572.5	145	VSSDUM	1140.0	-572.5
46	C31P	-4800.0	-572.5	96	VSSA	-1800.0	-572.5	146	ID_MIB	1200.0	-572.5
47	C31M	-4740.0	-572.5	97	VSSA	-1740.0	-572.5	147	VDD3DUM	1260.0	-572.5
48	C31M	-4680.0	-572.5	98	VSSA	-1680.0	-572.5	148	MDDI_EN	1320.0	-572.5
49	C31M	-4620.0	-572.5	99	VSSA	-1620.0	-572.5	149	TEST_MODE[1]	1380.0	-572.5
50	C32P	-4560.0	-572.5	100	VSSA	-1560.0	-572.5	150	TEST_MODE[0]	1440.0	-572.5

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Table3: Pad Center Coordinates (continued)

[Unit: um]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	EXCLK	1500.0	-572.5	201	MVDD	4500.0	-572.5	251	DUMMY	7500.0	-572.5
152	EN_EXCLK	1560.0	-572.5	202	MVDD	4560.0	-572.5	252	DUMMY	7697.5	-296.0
153	TEST_IN[6]	1620.0	-572.5	203	MVDD	4620.0	-572.5	253	DUMMY	7697.5	-242.0
154	TEST_IN[5]	1680.0	-572.5	204	MVDD	4680.0	-572.5	254	DUMMY	7697.5	-188.0
155	TEST_IN[4]	1740.0	-572.5	205	RVDD	4740.0	-572.5	255	DUMMY	7697.5	-134.0
156	TEST_IN[3]	1800.0	-572.5	206	RVDD	4800.0	-572.5	256	DUMMY	7697.5	-80.0
157	TEST_IN[2]	1860.0	-572.5	207	RVDD	4860.0	-572.5	257	DUMMY	7697.5	-26.0
158	TEST_IN[1]	1920.0	-572.5	208	RVDD	4920.0	-572.5	258	DUMMY	7697.5	28.0
159	TEST_IN[0]	1980.0	-572.5	209	DUMMY	4980.0	-572.5	259	DUMMY	7697.5	82.0
160	VSSDUM	2040.0	-572.5	210	VSP	5040.0	-572.5	260	DUMMY	7697.5	136.0
161	DB17	2100.0	-572.5	211	VSP	5100.0	-572.5	261	DUMMY	7697.5	190.0
162	DB16	2160.0	-572.5	212	VSP	5160.0	-572.5	262	DUMMY	7697.5	244.0
163	DB15	2220.0	-572.5	213	VSP	5220.0	-572.5	263	DUMMY	7697.5	298.0
164	DB14	2280.0	-572.5	214	VREG1OUT	5280.0	-572.5	264	DUMMY	7425.0	572.5
165	DB13	2340.0	-572.5	215	VREG1OUT	5340.0	-572.5	265	EX_FLM	7371.0	572.5
166	DB12	2400.0	-572.5	216	VREG1OUT	5400.0	-572.5	266	EX_FLM	7317.0	572.5
167	DB11	2460.0	-572.5	217	VREG1OUT	5460.0	-572.5	267	EX_CLKB	7263.0	572.5
168	DB10	2520.0	-572.5	218	VCI	5520.0	-572.5	268	EX_CLKB	7209.0	572.5
169	DB9	2580.0	-572.5	219	VCI	5580.0	-572.5	269	EX_CLK	7155.0	572.5
170	VSSDUM	2640.0	-572.5	220	VCI	5640.0	-572.5	270	EX_CLK	7101.0	572.5
171	DB8	2700.0	-572.5	221	VCI	5700.0	-572.5	271	BICTL_R	7047.0	572.5
172	DB7	2760.0	-572.5	222	VCI	5760.0	-572.5	272	BICTL_R	6993.0	572.5
173	DB6	2820.0	-572.5	223	VCIRIN	5820.0	-572.5	273	ESR	6939.0	572.5
174	DB5	2880.0	-572.5	224	DUMMYR3	5880.0	-572.5	274	ESR	6885.0	572.5
175	DB4	2940.0	-572.5	225	DUMMYR2	5940.0	-572.5	275	CLA	6831.0	572.5
176	DB3	3000.0	-572.5	226	DUMMYR1	6000.0	-572.5	276	CLA	6777.0	572.5
177	DB2	3060.0	-572.5	227	VGH	6060.0	-572.5	277	CLB	6723.0	572.5
178	DB1	3120.0	-572.5	228	VGH	6120.0	-572.5	278	CLB	6669.0	572.5
179	DB0	3180.0	-572.5	229	VGH	6180.0	-572.5	279	CLC	6615.0	572.5
180	VSSDUM	3240.0	-572.5	230	VGH	6240.0	-572.5	280	CLC	6561.0	572.5
181	VSYNC	3300.0	-572.5	231	VGH	6300.0	-572.5	281	DUMMY	6507.0	572.5
182	HSYNC	3360.0	-572.5	232	DUMMY	6360.0	-572.5	282	DUMMY	6453.0	572.5
183	DOTCLK	3420.0	-572.5	233	VGL	6420.0	-572.5	283	SOUT_DUM1	6399.0	572.5
184	ENABLE	3480.0	-572.5	234	VGL	6480.0	-572.5	284	SOUT[1]	6345.0	572.5
185	SDI	3540.0	-572.5	235	VGL	6540.0	-572.5	285	SOUT[2]	6291.0	572.5
186	SDO	3600.0	-572.5	236	VGL	6600.0	-572.5	286	SOUT[3]	6237.0	572.5
187	CSB	3660.0	-572.5	237	VGL	6660.0	-572.5	287	SOUT[4]	6183.0	572.5
188	RW_WRB	3720.0	-572.5	238	VINT	6720.0	-572.5	288	SOUT[5]	6129.0	572.5
189	RS	3780.0	-572.5	239	VINT	6780.0	-572.5	289	SOUT[6]	6075.0	572.5
190	VDD3DUM	3840.0	-572.5	240	VINT	6840.0	-572.5	290	SOUT[7]	6021.0	572.5
191	E_RDB	3900.0	-572.5	241	VINT	6900.0	-572.5	291	SOUT[8]	5967.0	572.5
192	RESETB	3960.0	-572.5	242	VINT	6960.0	-572.5	292	SOUT[9]	5913.0	572.5
193	TE	4020.0	-572.5	243	VINT	7020.0	-572.5	293	SOUT[10]	5859.0	572.5
194	TEST_OUT[2]	4080.0	-572.5	244	VINT	7080.0	-572.5	294	SOUT[11]	5805.0	572.5
195	TEST_OUT[1]	4140.0	-572.5	245	DUMMY	7140.0	-572.5	295	SOUT[12]	5751.0	572.5
196	TEST_OUT[0]	4200.0	-572.5	246	EL_ON	7200.0	-572.5	296	SOUT[13]	5697.0	572.5
197	VDD	4260.0	-572.5	247	ELVDD	7260.0	-572.5	297	SOUT[14]	5643.0	572.5
198	VDD	4320.0	-572.5	248	ELVDD	7320.0	-572.5	298	SOUT[15]	5589.0	572.5
199	VDD	4380.0	-572.5	249	ELVDD	7380.0	-572.5	299	SOUT[16]	5535.0	572.5
200	VDD	4440.0	-572.5	250	ELVDD	7440.0	-572.5	300	SOUT[17]	5481.0	572.5

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Table4: Pad Center Coordinates (continued)

[Unit: um]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SOUT[18]	5427.0	572.5	351	SOUT[68]	2727.0	572.5	401	SOUT[118]	27.0	572.5
302	SOUT[19]	5373.0	572.5	352	SOUT[69]	2673.0	572.5	402	SOUT[119]	-27.0	572.5
303	SOUT[20]	5319.0	572.5	353	SOUT[70]	2619.0	572.5	403	SOUT[120]	-81.0	572.5
304	SOUT[21]	5265.0	572.5	354	SOUT[71]	2565.0	572.5	404	SOUT[121]	-135.0	572.5
305	SOUT[22]	5211.0	572.5	355	SOUT[72]	2511.0	572.5	405	SOUT[122]	-189.0	572.5
306	SOUT[23]	5157.0	572.5	356	SOUT[73]	2457.0	572.5	406	SOUT[123]	-243.0	572.5
307	SOUT[24]	5103.0	572.5	357	SOUT[74]	2403.0	572.5	407	SOUT[124]	-297.0	572.5
308	SOUT[25]	5049.0	572.5	358	SOUT[75]	2349.0	572.5	408	SOUT[125]	-351.0	572.5
309	SOUT[26]	4995.0	572.5	359	SOUT[76]	2295.0	572.5	409	SOUT[126]	-405.0	572.5
310	SOUT[27]	4941.0	572.5	360	SOUT[77]	2241.0	572.5	410	SOUT[127]	-459.0	572.5
311	SOUT[28]	4887.0	572.5	361	SOUT[78]	2187.0	572.5	411	SOUT[128]	-513.0	572.5
312	SOUT[29]	4833.0	572.5	362	SOUT[79]	2133.0	572.5	412	SOUT[129]	-567.0	572.5
313	SOUT[30]	4779.0	572.5	363	SOUT[80]	2079.0	572.5	413	SOUT[130]	-621.0	572.5
314	SOUT[31]	4725.0	572.5	364	SOUT[81]	2025.0	572.5	414	SOUT[131]	-675.0	572.5
315	SOUT[32]	4671.0	572.5	365	SOUT[82]	1971.0	572.5	415	SOUT[132]	-729.0	572.5
316	SOUT[33]	4617.0	572.5	366	SOUT[83]	1917.0	572.5	416	SOUT[133]	-783.0	572.5
317	SOUT[34]	4563.0	572.5	367	SOUT[84]	1863.0	572.5	417	SOUT[134]	-837.0	572.5
318	SOUT[35]	4509.0	572.5	368	SOUT[85]	1809.0	572.5	418	SOUT[135]	-891.0	572.5
319	SOUT[36]	4455.0	572.5	369	SOUT[86]	1755.0	572.5	419	SOUT[136]	-945.0	572.5
320	SOUT[37]	4401.0	572.5	370	SOUT[87]	1701.0	572.5	420	SOUT[137]	-999.0	572.5
321	SOUT[38]	4347.0	572.5	371	SOUT[88]	1647.0	572.5	421	SOUT[138]	-1053.0	572.5
322	SOUT[39]	4293.0	572.5	372	SOUT[89]	1593.0	572.5	422	SOUT[139]	-1107.0	572.5
323	SOUT[40]	4239.0	572.5	373	SOUT[90]	1539.0	572.5	423	SOUT[140]	-1161.0	572.5
324	SOUT[41]	4185.0	572.5	374	SOUT[91]	1485.0	572.5	424	SOUT[141]	-1215.0	572.5
325	SOUT[42]	4131.0	572.5	375	SOUT[92]	1431.0	572.5	425	SOUT[142]	-1269.0	572.5
326	SOUT[43]	4077.0	572.5	376	SOUT[93]	1377.0	572.5	426	SOUT[143]	-1323.0	572.5
327	SOUT[44]	4023.0	572.5	377	SOUT[94]	1323.0	572.5	427	SOUT[144]	-1377.0	572.5
328	SOUT[45]	3969.0	572.5	378	SOUT[95]	1269.0	572.5	428	SOUT[145]	-1431.0	572.5
329	SOUT[46]	3915.0	572.5	379	SOUT[96]	1215.0	572.5	429	SOUT[146]	-1485.0	572.5
330	SOUT[47]	3861.0	572.5	380	SOUT[97]	1161.0	572.5	430	SOUT[147]	-1539.0	572.5
331	SOUT[48]	3807.0	572.5	381	SOUT[98]	1107.0	572.5	431	SOUT[148]	-1593.0	572.5
332	SOUT[49]	3753.0	572.5	382	SOUT[99]	1053.0	572.5	432	SOUT[149]	-1647.0	572.5
333	SOUT[50]	3699.0	572.5	383	SOUT[100]	999.0	572.5	433	SOUT[150]	-1701.0	572.5
334	SOUT[51]	3645.0	572.5	384	SOUT[101]	945.0	572.5	434	SOUT[151]	-1755.0	572.5
335	SOUT[52]	3591.0	572.5	385	SOUT[102]	891.0	572.5	435	SOUT[152]	-1809.0	572.5
336	SOUT[53]	3537.0	572.5	386	SOUT[103]	837.0	572.5	436	SOUT[153]	-1863.0	572.5
337	SOUT[54]	3483.0	572.5	387	SOUT[104]	783.0	572.5	437	SOUT[154]	-1917.0	572.5
338	SOUT[55]	3429.0	572.5	388	SOUT[105]	729.0	572.5	438	SOUT[155]	-1971.0	572.5
339	SOUT[56]	3375.0	572.5	389	SOUT[106]	675.0	572.5	439	SOUT[156]	-2025.0	572.5
340	SOUT[57]	3321.0	572.5	390	SOUT[107]	621.0	572.5	440	SOUT[157]	-2079.0	572.5
341	SOUT[58]	3267.0	572.5	391	SOUT[108]	567.0	572.5	441	SOUT[158]	-2133.0	572.5
342	SOUT[59]	3213.0	572.5	392	SOUT[109]	513.0	572.5	442	SOUT[159]	-2187.0	572.5
343	SOUT[60]	3159.0	572.5	393	SOUT[110]	459.0	572.5	443	SOUT[160]	-2241.0	572.5
344	SOUT[61]	3105.0	572.5	394	SOUT[111]	405.0	572.5	444	SOUT[161]	-2295.0	572.5
345	SOUT[62]	3051.0	572.5	395	SOUT[112]	351.0	572.5	445	SOUT[162]	-2349.0	572.5
346	SOUT[63]	2997.0	572.5	396	SOUT[113]	297.0	572.5	446	SOUT[163]	-2403.0	572.5
347	SOUT[64]	2943.0	572.5	397	SOUT[114]	243.0	572.5	447	SOUT[164]	-2457.0	572.5
348	SOUT[65]	2889.0	572.5	398	SOUT[115]	189.0	572.5	448	SOUT[165]	-2511.0	572.5
349	SOUT[66]	2835.0	572.5	399	SOUT[116]	135.0	572.5	449	SOUT[166]	-2565.0	572.5
350	SOUT[67]	2781.0	572.5	400	SOUT[117]	81.0	572.5	450	SOUT[167]	-2619.0	572.5

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Table5: Pad Center Coordinates (continued)

[Unit: um]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	SOUT[168]	-2673.0	572.5	501	SOUT[218]	-5373.0	572.5	551	DUMMY	-7697.5	-296.0
452	SOUT[169]	-2727.0	572.5	502	SOUT[219]	-5427.0	572.5				
453	SOUT[170]	-2781.0	572.5	503	SOUT[220]	-5481.0	572.5				
454	SOUT[171]	-2835.0	572.5	504	SOUT[221]	-5535.0	572.5				
455	SOUT[172]	-2889.0	572.5	505	SOUT[222]	-5589.0	572.5				
456	SOUT[173]	-2943.0	572.5	506	SOUT[223]	-5643.0	572.5				
457	SOUT[174]	-2997.0	572.5	507	SOUT[224]	-5697.0	572.5				
458	SOUT[175]	-3051.0	572.5	508	SOUT[225]	-5751.0	572.5				
459	SOUT[176]	-3105.0	572.5	509	SOUT[226]	-5805.0	572.5				
460	SOUT[177]	-3159.0	572.5	510	SOUT[227]	-5859.0	572.5				
461	SOUT[178]	-3213.0	572.5	511	SOUT[228]	-5913.0	572.5				
462	SOUT[179]	-3267.0	572.5	512	SOUT[229]	-5967.0	572.5				
463	SOUT[180]	-3321.0	572.5	513	SOUT[230]	-6021.0	572.5				
464	SOUT[181]	-3375.0	572.5	514	SOUT[231]	-6075.0	572.5				
465	SOUT[182]	-3429.0	572.5	515	SOUT[232]	-6129.0	572.5				
466	SOUT[183]	-3483.0	572.5	516	SOUT[233]	-6183.0	572.5				
467	SOUT[184]	-3537.0	572.5	517	SOUT[234]	-6237.0	572.5				
468	SOUT[185]	-3591.0	572.5	518	SOUT[235]	-6291.0	572.5				
469	SOUT[186]	-3645.0	572.5	519	SOUT[236]	-6345.0	572.5				
470	SOUT[187]	-3699.0	572.5	520	SOUT[237]	-6399.0	572.5				
471	SOUT[188]	-3753.0	572.5	521	SOUT[238]	-6453.0	572.5				
472	SOUT[189]	-3807.0	572.5	522	SOUT[239]	-6507.0	572.5				
473	SOUT[190]	-3861.0	572.5	523	SOUT[240]	-6561.0	572.5				
474	SOUT[191]	-3915.0	572.5	524	SOUT_DUM240	-6615.0	572.5				
475	SOUT[192]	-3969.0	572.5	525	DUMMY	-6669.0	572.5				
476	SOUT[193]	-4023.0	572.5	526	DUMMY	-6723.0	572.5				
477	SOUT[194]	-4077.0	572.5	527	BICTI_L	-6777.0	572.5				
478	SOUT[195]	-4131.0	572.5	528	BICTI_L	-6831.0	572.5				
479	SOUT[196]	-4185.0	572.5	529	SCLK1	-6885.0	572.5				
480	SOUT[197]	-4239.0	572.5	530	SCLK1	-6939.0	572.5				
481	SOUT[198]	-4293.0	572.5	531	SCLK2	-6993.0	572.5				
482	SOUT[199]	-4347.0	572.5	532	SCLK2	-7047.0	572.5				
483	SOUT[200]	-4401.0	572.5	533	SFTCLK	-7101.0	572.5				
484	SOUT[201]	-4455.0	572.5	534	SFTCLK	-7155.0	572.5				
485	SOUT[202]	-4509.0	572.5	535	SFTCLKB	-7209.0	572.5				
486	SOUT[203]	-4563.0	572.5	536	SFTCLKB	-7263.0	572.5				
487	SOUT[204]	-4617.0	572.5	537	FLM	-7317.0	572.5				
488	SOUT[205]	-4671.0	572.5	538	FLM	-7371.0	572.5				
489	SOUT[206]	-4725.0	572.5	539	DUMMY	-7425.0	572.5				
490	SOUT[207]	-4779.0	572.5	540	DUMMY	-7697.5	298.0				
491	SOUT[208]	-4833.0	572.5	541	DUMMY	-7697.5	244.0				
492	SOUT[209]	-4887.0	572.5	542	DUMMY	-7697.5	190.0				
493	SOUT[210]	-4941.0	572.5	543	DUMMY	-7697.5	136.0				
494	SOUT[211]	-4995.0	572.5	544	DUMMY	-7697.5	82.0				
495	SOUT[212]	-5049.0	572.5	545	DUMMY	-7697.5	28.0				
496	SOUT[213]	-5103.0	572.5	546	DUMMY	-7697.5	-26.0				
497	SOUT[214]	-5157.0	572.5	547	DUMMY	-7697.5	-80.0				
498	SOUT[215]	-5211.0	572.5	548	DUMMY	-7697.5	-134.0				
499	SOUT[216]	-5265.0	572.5	549	DUMMY	-7697.5	-188.0				
500	SOUT[217]	-5319.0	572.5	550	DUMMY	-7697.5	-242.0				

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PIN DESCRIPTION

POWER SUPPLY PINS

Table6: Power supply pin description

Symbol	I/O	Description
VDD	Power	Power supply for internal logic and internal RAM. Internally, voltage regulator output is connected to this pin. Connect a capacitor for stabilization. Don't apply any external power to this pin.
MVDD	Power	Internal power for RAM. Connect this pin to VDD externally.
RVDD	Power	Regulated logic power voltage (1.5V)
VDD3	Power	I/O power supply. (1.65V ~ 3.3V)
VCI	Power	Power supply for analog circuits. (VCI : 2.5 ~ 3.3V) An internal reference power supply for VCI1 amp.
VCI_MDDI	Power	Analog power supply (VCI_MDDI : 2.5 ~ 3.3V)
VSS VSSA VSSC	Ground	System ground (0V).
VSS_MDDI	Power	System ground level for I/O
VGS	I	A reference level for the grayscale voltage generation circuit. Connect this pin to an external resistor when a source driver is used to adjust grayscale levels for each panel.
VCI1	I/O	A reference voltage for 1st booster.
VCIRIN	I	A reference voltage input pin for power block when using an external VCIR generation mode.
VLIN1 / VLOUT1	I/O	Input pin for applying VLOUT1 voltage level / 1st booster output pin. Recommend to connect VLIN1 to VLOUT1.
VLIN2 / VLOUT2	I/O	Input pin for applying VLOUT2 voltage level / 2nd booster output pin. Recommend to connect VLIN2 to VLOUT2.
VLIN3 / VLOUT3	I/O	Input pin for applying VLOUT3 voltage level / 3rd booster output pin. Recommend to connect VLIN3 to VLOUT3.
C11P,C11M C12P,C12M	I/O	External capacitor connection pins used for the 1'st booster circuit.
C21P,C21M	I/O	External capacitor connection pins used for the 2nd booster circuit.

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Table7: Power supply pin description(Continued)

Symbol	I/O	Description
C31P,C31M C32P,C32M	I/O	External capacitor connection pins used for the 3rd booster circuit.
VREG1OUT	I/O	A reference level for the grayscale voltage with the amplitude between VLOUT1 and GND.
VGH	O	The positive voltage used in the gate driver.
VGL	O	The negative voltage used in the gate driver.
VINT	O	A voltage for initializing an OLED panel.
VSP	O	Power supply for the external photo sensor. If not use, this pin must be open.
ELVDD	I	Power supply for the generation of VSP. If not use, this pin must be fixed to VSS level.
MTPG	I	A voltage for the MTP programming (Initialization, Erasing, and Programming). If not use, this pin must be open.
MTPD	I	A voltage for the MTP programming (Initialization, Erasing, and Programming). If not use, this pin must be open.
Vex	I	Must be fixed to VSS level.

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SYSTEM / RGB INTERFACE PINS

Table8: System interface pin description

<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>S_PB</td><td>I</td><td colspan="3">Selects the CPU interface mode
“Low” = Parallel Interface, “High” = Serial Interface</td></tr>
<tr><td>MDDI_EN</td><td>I</td><td colspan="3">Selects the MDDI interface
“Low” = MDDI Disable, “High” = MDDI Enable</td></tr>
<tr><td>ID_MIB</td><td>I</td><td colspan="3">Selects the CPU type
“Low” = Intel 80x-system, “High” = Motorola 68x-system
If S-PB = “High”, the pin is used as ID setting bit for a device code.</td></tr>
<tr><td>CSB</td><td>I</td><td colspan="3">Chip select signal input pin.
Low: S6E63D6 is selected and can be accessed
High: S6E63D6 is not selected and cannot be accessed</td></tr>
<tr><td>RS</td><td>I</td><td colspan="3">Register select pin.
Low: Index/status, High: Instruction parameter, GRAM data
Must be fixed at VDD3 level when not used.</td></tr>
<tr><td rowspan="4">RW_WRB/
SCL</td><td rowspan="4">I</td><td>Pin function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>RW</td><td>68-system</td><td>Read/Write operation selection pin.
Low: Write, High: Read</td></tr>
<tr><td>WRB</td><td>80-system</td><td>Write strobe signal. (Input pin)
Data is fetched at the rising edge.</td></tr>
<tr><td>SCL</td><td>Serial Peripheral Interface (SPI)</td><td>The synchronous clock signal.
(Input pin)</td></tr>
<tr><td rowspan="4">E_RDB</td><td rowspan="4">I</td><td>Pin function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>E</td><td>68-system</td><td>Read/Write operation enable pin.</td></tr>
<tr><td>RDB</td><td>80-system</td><td>Read strobe signal. (Input pin)
Read out data at the low level.</td></tr>
<tr><td colspan="3">When SPI mode is selected, fix this pin at VDD3 level.</td></tr>
<tr><td>SDI</td><td>I</td><td colspan="3">For a serial peripheral interface (SPI), input data is fetched at the rising edge of the SCL signal. Fix SDI pin at VSS level if the pin is not used.</td></tr>
<tr><td>SDO</td><td>O</td><td colspan="3">For a serial peripheral interface (SPI), serves as the serial data output pin (SDO). Successive bits are output at the falling edge of the SCL signal.</td></tr>
<tr><td>RESETB</td><td>I</td><td colspan="3">Reset pin Initializes the IC when low. Should be reset after power-on.</td></tr>
<tr><td>DB17-DB0</td><td>I/O</td><td colspan="3">Bi-directional data bus.
When CPU I/F,
18-bit interface : DB 17-0
16-bit interface : DB 17-10, DB 8-1
9-bit interface : DB 8-0
8-bit interface : DB 8-1
When RGB I/F,
18-bit interface : DB 17-0
16-bit interface : DB 17-10, DB 8-1
6-bit interface : DB 8-3
Fix unused pin to the VSS level.</td></tr>
</table>

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Table9: System interface pin description (Continued)

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable signal pin for RGB interface.
EPL=”0”: Only in case of ENABLE=”Low”, the IC can be access via RGB interface.
EPL=”1”: Only in case of ENABLE=”High”, the IC can be access via RGB interface
<table>
<tr><th>EPL</th><th>ENABLE</th><th>GRAM write</th><th>GRAM address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Updated</td></tr>
</table>
Fix ENABLE pin at VSS level if the pin is not used.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Frame-synchronizing signal.
VSPL= “0”: Low active, VSPL=”1”: High active
Fix this pin at VSS level if the pin is not used.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Line-synchronizing signal.
HSPL=”0”: Low active, HSPL=”1”: High active
Fix this pin at VSS level if the pin is not used.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>Input pin for clock signal of external interface: dot clock.
DPL=”0”: Display data is fetched at DOTCLK’s rising edge
DPL=”1”: Display data is fetched at DOTCLK’s falling edge
Fix this pin at VSS level if the pin is not used.</td></tr>
</table>

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Tabel10: MDDI pin description

Symbol	I/O	Description
MDP	I/O	Positive MDDI data input/output. If MDDI is not used, this pad should be floating.
MDN	I/O	Negative MDDI data input/output. If MDDI is not used, this pad should be floating.
MSP	I	Positive MDDI strobe input. If MDDI is not used, this pad should be floating.
MSN	I	Negative MDDI strobe input. If MDDI is not used, this pad should be floating.
GPIO[9:0] (DB[17:8])	I/O	General purpose input/output If GPIO is not used in MDDI mode, this pin should be fixed at VSS level.
S_CSB (DB[7])	O	Chip select for Sub Panel Driver IC Low: Sub Panel Driver IC is selected and can be accessed. High: Sub Panel Driver IC is not selected and can not be accessed. If sub panel is not used in MDDI mode, this pin should be floating
S_RS (DB[6])	O	Register select for Sub Panel Driver IC Low : Index/status, High : Control Must be fixed at VSS level, when this signal is not used. If sub panel is not used in MDDI mode, this pin should be floating
S_WRB (DB[5])	O	Write Strobe signal for Sub Panel Driver IC Only 80-system 18/16 bit mode is enabled, so Data is fetched at the rising edge. If sub panel is not used in MDDI mode, this pin should be floating
S_DB[8-0] (DB[4:0], TE, TEST_OUT[2:0])	O	For Sub Panel, this pin can be used to transfer DB[8:0] data to Sub Panel Driver IC. If sub panel is not used in MDDI mode, this pin should be floating.
HSYNC VSYNC ENABLE DOTCLK	I	In MDDI mode, Fixed at VSS level.
RW_WRB E_RDB RS	I	In MDDI mode, Fixed at VDD3 level.
CSB	I	In MDDI mode, Fixed at VDD3 level.

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DISPLAY PINS

Table11: Display pin description

Symbol	I/O	Description
SOUT[1:240]	O	Source driver output pins. The direction of them is determined by the value of SS register.
FLM	O	Start pulse of vertical line shift.
SFTCLK, SFTCLKB	O	Clock for gate driver shift.
SCLK1, SCLK2	O	LTPS signals
CLA, CLB, CLC	O	LTPS signals
BICTL_L	O	LTPS signal
BICTL_R	O	LTPS signal
EX_FLM	O	Don't use this pin. IC maker's test pins.
EX_CLK, EX_CLKB	O	Don't use this pin. IC maker's test pins.
ESR	O	Shift register enable signal
EL_ON	O	The external ELVDD regulator enable pin

MISCELLANEOUS PINS

Table12: Oscillator and internal power regulator pin description

Symbol	I/O	Description
DUMMYR[3:1] DUMMYL[3:1]	-	Contact resistance measurement pin. In normal operation, leave this pin open
DUMMY	-	Dummy pins don't care. Leave these pins open.
V0/V63	O	Gamma voltage monitoring pin.
VDD3DUM	O	This pin is connected to VDD3 line internally. Use for to connect neighbor-setting pins.
VSSDUM	O	This pin is connected to VSS line internally. Use for to connect neighbor-setting pins.
FUSE_EN	I	Don't use this pin. IC maker's test pins. This pin must be tied to VDD3.
RTEST	I	Don't use this pin. IC maker's test pins. This pin must be tied to VSS.
EN_EXCLK	I	Don't use this pin. IC maker's test pins. Fix this pin at VSS level if the pin is not used.
EXCLK	I	Don't use this pin. IC maker's test pins. Fix this pin at VSS level if the pin is not used.
TEST_MODE[1:0]	I	Don't use this pin. IC maker's test pins. Fix this pin at VSS level if the pin is not used.
TEST_IN[6:0]	I	Don't use this pin. IC maker's test pins. Fix this pin at VSS level if the pin is not used.
TE	O	Tearing effect output pin. In normal operation, leave this pin open.
TEST_OUT[2:0]	O	Output pins used only for test purpose at vendor-side. In normal operation, leave this pin open.

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FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

The S6E63D6 has ten high-speed system interfaces: an 80-system 18-/16-/9-/8-bit bus, a 68-system 18-/16-/9-/8-bit and two type serial interface (SPI: Serial Peripheral Interface).
The S6E63D6 has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information for control register and GRAM. The WDR temporarily stores data to be written into control register and GRAM. The RDR temporarily stores data read from GRAM. Data written into the GRAM from CPU is initially written to the WDR and then written to the GRAM automatically. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are valid. Execution time for instruction, except oscillation start, is 0-clock cycle so that instructions can be written in succession.

Table13: Register Selection (18-/16-/9-/8- Parallel Interface)

SYSTEM	RW_WRB	E_RDB	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM through RDR
80	0	1	0	Write index to IR
	1	0	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	0	1	Read from GRAM through RDR

Table14: CSB signal (GRAM update control)

CSB	Operation
0	Data is written to GRAM, GRAM address is updated
1	Data is not written to GRAM, GRAM address is not updated

Table15: Register Selection (Serial Peripheral Interface)

R/W bit	RS bit	Operation
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM through RDR

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HIGH SPEED SERIAL INTERFACE (MDDI)

This interface will be introduced, see the section “Description of MDDI Interface”

SUB PANEL CONTROL

Sub panel control block will be introduced, see the section “Description of Sub Panel Control”

EXTERNAL INTERFACE (RGB-I/F)

The S6E63D6 incorporates RGB interface as external interface for motion picture display.
When the RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display. The RGB data for display (DB17-0) are written according to enable signal (ENABLE) in synchronization with VSYNC, HSYNC, and DOTCLK signal. This allows flicker-free updating of the screen. See the section on the EXTERNAL DISPLAY INTERFACE.

ADDRESS COUNTER (AC)

The address counter (AC) assigns address to GRAM. When an address-set-instruction is written to the IR, the address information is sent from IR to AC. After writing to the GRAM, the address value of AC is automatically increased/ decreased by 1 according to ID1-0 bit of control register. After reading data from GRAM, the AC is updated automatically.

GRAPHICS RAM (GRAM)

The graphics RAM (GRAM) has 18-bits/pixel and stores the bit-pattern data for 240-RGB x 320-dot display.

TIMING GENERATOR

The Panel Interface Controller generates timing signals for LTPS drive. Also it generates control signals for the operation of internal circuits such as source driver and GRAM. The GRAM read operations done by this Timing Generator and GRAM write operations done through system interface are performed independently to avoid the interference between them.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates OLED driving voltage that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting registers. 262,144 possible colors can be displayed at the same time by this LSI. Gamma is set for R,G, and B individually.

OSCILLATION CIRCUIT (OSC)

The S6E63D6 can provide R-C oscillation simply through the internal oscillation-resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the internal register. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the OSCILLATION CIRCUIT section.

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SOURCE DRIVER CIRCUIT

The source driving circuit of S6E63D6 consists of a 240 source drivers (SOUT[1] to SOUT[240]). Image data is latched when 240-pixel data has arrived. The latched data then enables the source drivers to generate drive waveform outputs.
The SS register can change the shift direction of 240 source driver output data for the device-mount configuration.

LTPS PANEL INTERFACE CIRCUIT

LTPS panel interface circuit does level–shift operation and outputs to control LTPS panel.

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GRAM ADDRESS MAP

The image data stored in GRAM corresponds to pixel data on display as shown below:

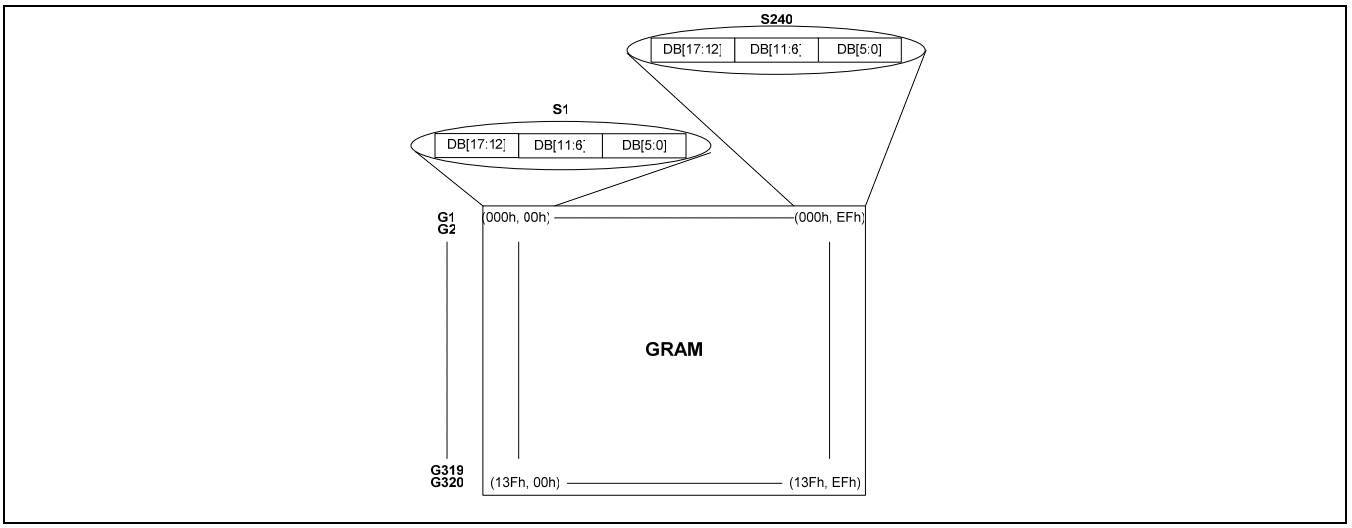

Figure4: GRAM address (SS="0")

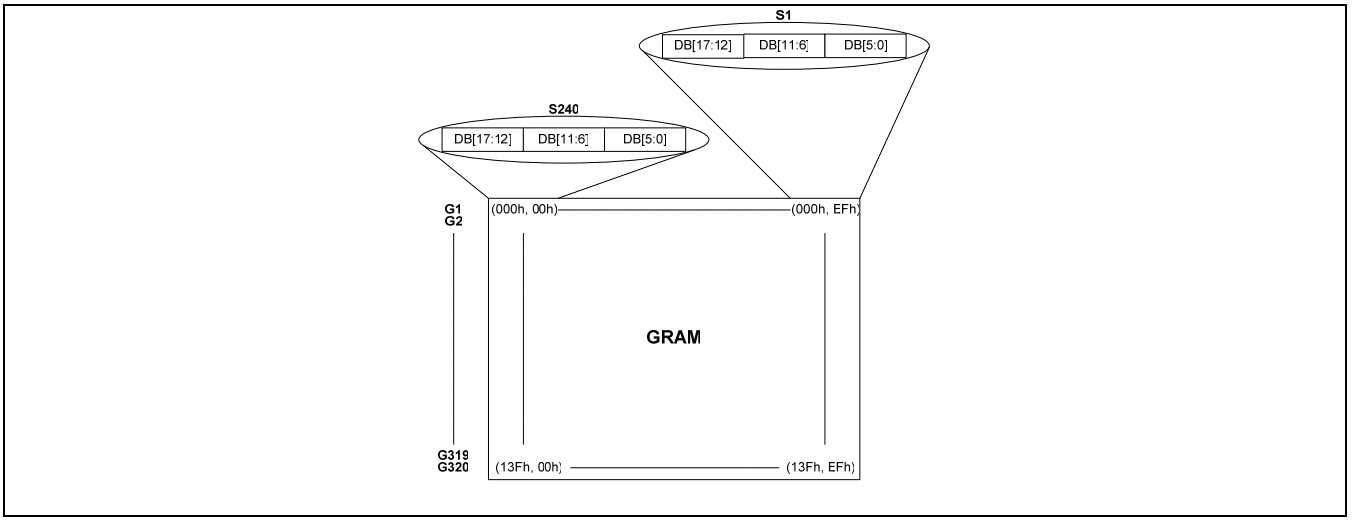

Figure5: GRAM address (SS="1")

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INSTRUCTIONS

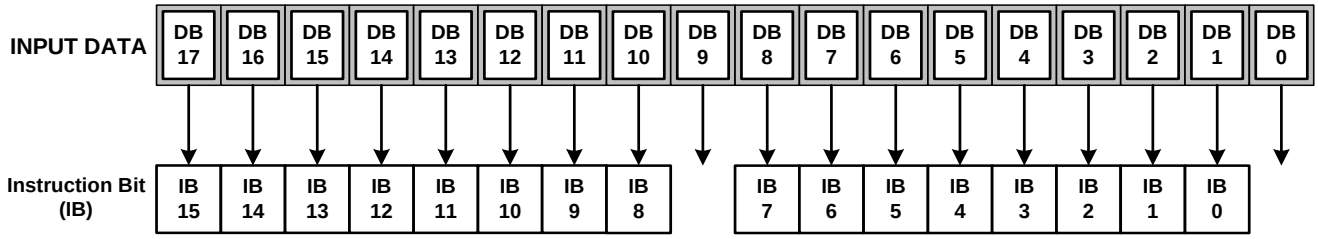
The S6E63D6 uses the 18-bit bus architecture. Before the internal operation of the S6E63D6 starts, control information is stored temporarily in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the S6E63D6 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17 to DB0), make up the S6E63D6 instructions.
There are seven categories of instructions that:

- Specify the index
- Control the display
- Control power management
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the LTPS driver and power supply IC

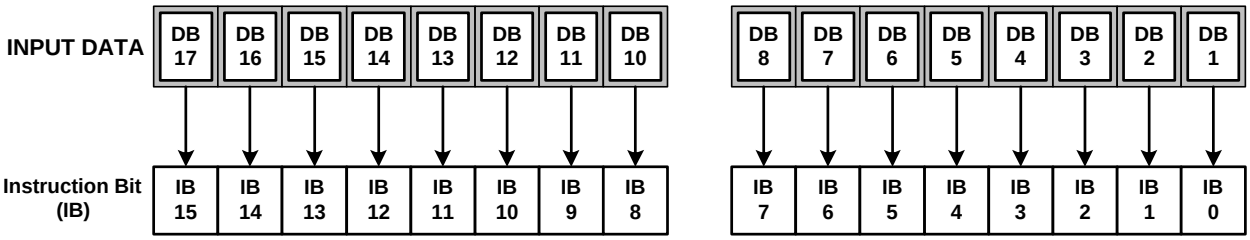
Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. As instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment differs from interface-setup (18-/16-/9-/8-/SPI), so instructions should be fetched according to the data format shown below:

68/80-system 18-bit Interface



68/80-system 16-bit Interface/SPI(Serial Peripheral Interface)



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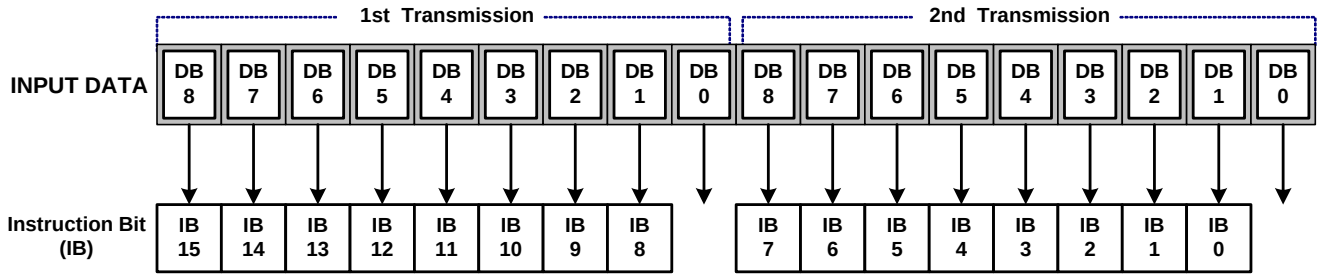
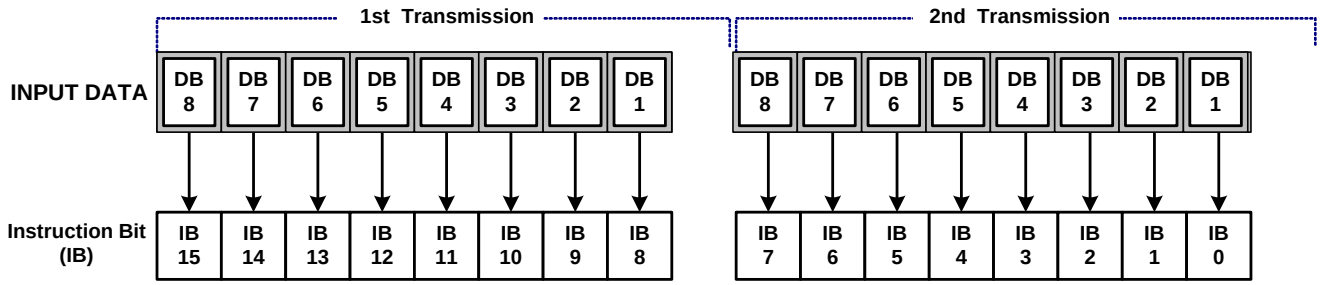
68/80-system 9-bit Interface



68/80-system 8-bit Interface



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INSTRUCTION TABLE

Table16: Instruction Table

Index	Reg. No	R/W	RS		IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
I/F Control	IR	W	0	Set index register value	X	X	X	X	X	X	X	X	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	SR	R	0	Status Read	X	X	X	X	X	X	X	L8	L7	L6	L5	L4	L3	L2	L1	L0
	R0h	W	0	No Operation	No operation															
Display Control	R01h	W	1	Display Duty control	FP3	FP2	FP1	FP0	BP3	BP2	BP1	BP0	X	X	NL5	NL4	NL3	NL2	NL1	NL0
	R02h	W	1	RGB Interface Control	X	X	X	X	X	X	X	RM	DM	X	RIM1	RIM0	VSPL	HSPL	EPL	DPL
	R03h	W	1	Entry Mode	CLS	MDT1	MDT0	BGR	X	X	X	SS	X	X	I/D1	I/D0	X	X	X	AM
	R04h	W	1	Clock Control	X	X	X	X	X	X	X	X	X	X	DCR1	DCR0	X	X	X	X
	R05h	W	1	Display Control1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DISP_ON
	R06h	W	1	Display Control2	X	X	X	X	X	X	X	X	X	X	X	CL	X	X	TEMON	REV
	R07h	W	1	Panel IF Control1	X	X	X	CLWEA4	CLWEA3	CLWEA2	CLWEA1	CLWEA0	X	X	X	X	X	X	X	X
	R08h	W	1	Panel IF Control2	X	X	X	CLWEB4	CLWEB3	CLWEB2	CLWEB1	CLWEB0	X	X	X	CLWEC4	CLWEC3	CLWEC2	CLWEC1	CLWeC0
	R09h	W	1	Panel IF Control3	SCTE3	SCTE2	SCTE1	SCTE0	SCWE3	SCWE2	SCWE1	SCWE0	X	SHE2	SHE1	SHE0	X	CLTE2	CLTE1	CLTE0
	R0Ah	W	1	Panel IF Control4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GTCON1	GTCON0
Device Read	R0Fh	R	0	**Device code read**	1	1	0	0	0	0	1	1	1	1	0	1	0	0	1	1
Power Control	R10h	W	1	Stand By	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	STB
	R12h	W	1	Power Gen1	X	X	X	X	X	X	X	X	X	X	X	X	VC3	VC2	VC1	VC0
	R13h	W	1	Power Gen2	X	X	VINT3	VINT2	VINT1	VINT0	X	VGH3	VGH2	VGH1	VGH0	X	VGL3	VGL2	VGL1	VGL0
	R14h	W	1	Power Step Up Control1	X	DC22	DC21	DC0		DC12	DC11	DC10	X	X	X	X	X	X	BT1	BT0
	R18h	W	1	Oscillator Control	X	X	X	X	X	X	X	X	X	X	RADJ5	RADJ4	RADJ3	RADJ2	RADJ1	RADJ0
	R1Ah	W	1	Source Driver Control	X	X	X	X	X	X	X	X	X	X	GAMMA_TEST	SDUM_ON	X	SAP2	SAP1	SAP0
GRAM Access	R20h	W	1	**GRAM address set** AD16-0: Set GRAM	X	X	X	X	X	X	X	X	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
	R21h	W	1		X	X	X	X	X	X	X	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
	R22h	W	1	GRAM Write	**WD17-0 : Pin assignment varies according to the interface method**															
		R	1	GRAM Read	**RD17-0 : Pin assignment varies according to the interface method**															

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Table17: Instruction Table(Continued)

Index	Reg. No	R/W	RS		IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
I/F Control	R23h	W	0	I/F Select	Select 18/16-Bit Data Bus Interface															
	R24h	W	0		Select 9/8-Bit Data Bus Interface															
Position Control	R30h	W	1	Vertical Scroll Control	X	X	X	X	X	X	X	SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
	R31h	W	1		X	X	X	X	X	X	X	SEA8	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0
	R32h	W	1	Vertical Scroll Control 2	X	X	X	X	X	X	X	SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
	R33h	W	1	Partial Screen Driving Position	X	X	X	X	X	X	X	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	R34h	W	1		X	X	X	X	X	X	X	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	R35h	W	1	Vertical RAM Address Position	X	X	X	X	X	X	X	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	R36h	W	1		X	X	X	X	X	X	X	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
	R37h	W	1	Horizontal RAM Address Position	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
MDDI I/F	38h	W	1	Client initiated wake-up	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VWAKE_EN
	39h	W	1	MDDI Link wake-up start position	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	X	WKF3	WKF2	WKF1	WKF0	X	X
	3Ah	W	1	Sub panel control	X	X	X	X	X	X	X	X	SUB_SEL7	SUB_SEL6	SUB_SEL5	SUB_SEL4	SUB_SEL3	SUB_SEL2	SUB_SEL1	SUB_SEL0
	3Bh	W	1		X	X	X	X	X	X	X	X	SUB_WR7	SUB_WR6	SUB_WR5	SUB_WR4	SUB_WR3	SUB_WR2	SUB_WR1	SUB_WR0
	3C	W	1		X	X	X	X	X	X	X	X	FCV_EN	X	X	X	MPU_MODE	STN_EN	SUB_IM1	SUB_IM0

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Table19: Instruction Table(Continued)

Index	Reg. No	R/W	RS		IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0
MTP Control	R60h	W	1	Test Key	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1
	R61h	W	1	MTP Selection	X	X	X	X	X	X	X	MTP_WRB	X	X	X	MTP_SEL	X	X	X	MTP_ERB
	R62h	W	1	MTP Register Setting R	X	R21_DK2	R21_DK1	R21_DK0	R21_BT2	R21_BT1	R21_BT0	X	R63_DK3	R63_DK2	R63_DK1	R63_DK0	R63_BT3	R63_BT2	R63_BT1	R63_BT0
	R63h	W	1	MTP Register Setting G	X	G21_DK2	G21_DK1	G21_DK0	G21_BT2	G21_BT1	G21_BT0	X	G63_DK3	G63_DK2	G63_DK1	G63_DK0	G63_BT3	G63_BT2	G63_BT1	G63_BT0
	R64h	W	1	MTP Register Setting B	X	B21_DK2	B21_DK1	B21_DK0	B21_BT2	B21_BT1	B21_BT0	X	B63_DK3	B63_DK2	B63_DK1	B63_DK0	B63_BT3	B63_BT2	B63_BT1	B63_BT0
	R65h	W	1	MTP Register Offset	X	X	X	X	X	X	X	X	X	X	X	X	X	E_OST2	E_OST1	E_OST_0
GPIO Control	R66h	W	1	**GPIO value**	X	X	X	X	X	X	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
	R67h	W	1	**in/output control**	X	X	X	X	X	X	GPIO_CON9	GPIO_CON8	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0
	R68h	W	1	**GPIO Clear**	X	X	X	X	X	X	GPCLR9	GPCLR8	GPCLR7	GPCLR6	GPCLR5	GPCLR4	GPCLR3	GPCLR2	GPCLR1	GPCLR0
	R69h	W	1	**GPIO interrupt enable**	X	X	X	X	X	X	GPIO_EN9	GPIO_EN8	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
	R6Ah	W	1	**GPIO polarity selection**	X	X	X	X	X	X	GPPOL9	GPPOL8	GPPOL7	GPPOL6	GPPOL5	GPPOL4	GPPOL3	GPPOL2	GPPOL1	GPPOL0
Gamma Control	R70h	W	1	Gamma Top Bottom Control R	X	X	CR56	CR55	CR54	CR53	CR52	CR51	CR50	X	X	X	CR03	CR02	CR01	CR00
	R71h	W	1	Gamma Top Bottom Control G	X	X	CG56	CG55	CG54	CG53	CG52	CG51	CG50	X	X	X	CG03	CG02	CG01	CG00
	R72h	W	1	Gamma Top Bottom Control B	X	X	CB56	CB55	CB54	CB53	CB52	CB51	CB50	X	X	X	CB03	CB02	CB01	CB00
	R73h	W	1	Gamma Control R 1,2	X	X	CR15	CR14	CR13	CR12	CR11	CR10	X	X	CR25	CR24	CR23	CR22	CR21	CR20
	R74h	W	1	Gamma Control R 3,4	X	X	CR35	CR34	CR33	CR32	CR31	CR30	X	X	CR45	CR44	CR43	CR42	CR41	CR40
	R75h	W	1	Gamma Control G 1,2	X	X	CG15	CG14	CG13	CG12	CG11	CG10	X	X	CG25	CG24	CG23	CG22	CG21	CG20
	R76h	W	1	Gamma Control G 3,4	X	X	CG35	CG34	CG33	CG32	CG31	CG30	X	X	CG45	CG44	CG43	CG44	CG41	CG40
	R77h	W	1	Gamma Control B 1,2	X	X	CB15	CB14	CB13	CB12	CB11	CB10	X	X	CB25	CB24	CB23	CB22	CB21	CB20
	R78h	W	1	Gamma Control B 3,4	X	X	CB35	CB34	CB33	CB32	CB31	CB30	X	X	CB45	CB44	CB43	CB42	CB41	CB40
	R80h	W	1	Gamma Select	X	X	X	X	X	X	X	X	X	X	X	X	GS_SEL3	GS_SEL2	GS_SEL1	GS_SEL0

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Instruction Descriptions

Index

The index instruction specifies indexes. It sets the register number in the range of 0000000b to 1111111b in binary form. However, do not access index registers and instruction bits that are not allocated in this document.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	X	X	X	X	X	X	X	X	X	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction reads out the internal status of the IC.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

L8–0: Indicate the position of horizontal line currently being driven.

No Operation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	No Operation															

This command does not have any effect on the display module. However it can be used to terminate Memory Write and Read in 22h command.

DISPLAY DUTY CONTROL (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP3	FP2	FP1	FP0	BP3	BP2	BP1	BP0	X	X	NL5	NL4	NL3	NL2	NL1	NL0

*01h Initial Value = 1000_1000_XX10_1000

FP / BP

Sets the period of Blank Area, which is placed at the beginning and the end of a frame. FP[3:0] is for a Front Porch and BP[3:0] is for a Back Porch. When Front Porch and Back Porch are set, the settings should meet the following conditions.

BP+FP ≤ TBD lines
FP ≥ TBD lines
BP ≥ TBD lines

When S6E63D6 operates in External Clock Operation mode, the Back Porch (BP) will start on the falling edge of the VSYNC signal and display operation begins just after the Back Porch period. The Front Porch (FP) will start when data of the number of lines specified by the NL has been displayed. During the period between the completion of the Front Porch and the next VSYNC signal, the display will remain blank.

Table20: Blank Period Control with FP and BP

FP[3:0] (BP[3:0])	Number of Raster Periods In Front (Back) Porch
0000	SETTING DISABLE
0001	SETTING DISABLE
0010	2
0011	3
0100	4
---	---
1000	8
---	---
1100	12
1101	13
1110	14
1111	SETTING DISABLE

NL

Specifies the number of lines driving OLED drive. The number of lines for the OLED drive can be adjusted for every eight lines. The selected value should be equal to or larger than the size of the panel to be driven. GRAM address mapping is not affected by the value of the drive duty ratio.

Table21: NL and Drive Duty

NL[5:0]	Display Size	Drive Line
00_0000 ~ 01_0011	SETTING DISABLE	
01_0100	240 X 160	160
01_0101	240 X168	168
01_0110	240X176	176
01_0111	240X184	184
---	---	---
10_0111	240 X 312	312
10_1000	240 X 320	320
10_1001 ~ 11_1111	SETTING DISABLE	

[NOTE] A back porch period and a front porch period will be inserted as a blank period before and after driving all LTPS lines.

RGB INTERFACE CONTROL (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	RM	DM	X	RIM 1	RIM 0	VSP L	HSP L	EPL	DPL

*02h Initial Value = XXXX_XXX0_0X00_0000

RM

Specifies the interface for GRAM accesse as shown below. This register and DM register can be set independently.

DM

Specifies the display operation mode. The interface can be set based on the bit of DM. In Internal Clock Opeartion mode the source clock for display operation comes from internal oscillator while in External Clock Opeartion mode it comes from RGB interface(DOTCLK, VSYNC, HSYNC).

Table22: RM, DM, GRAM Access Interface and Display Operation Mode

RM	DM	GRAM Access Interface	Display operation mode
0	0	System interface	Internal clock operation
1	1	RGB interface	External clock operation

[NOTE] [RM, DM]= 01, [RM, DM]=10 setting disable.

RIM

Specifies RGB interface mode when the RGB interface is used. This register is valid when RM is set to “1”. DM and this register should be set before proper display operation is performed through the RGB interface.

Table23: RIM and RGB Interface Mode

RIM[1:0]	RGB Interface mode
00	18-bit RGB interface (one transfer per pixel)
01	16-bit RGB interface (one transfer per pixel)
10	6-bit RGB interface (three transfers per pixel)
11	SETTING DISABLE

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You should notice that some display functions, which will be described later, cannot be used according to the display mode shown below.

Table24: Display Functions and Display Modes

Function	External Clock Operation Mode	Internal Clock Operation Mode
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Rotation	Cannot be used	Can be used
Mirroring	Cannot be used	Can be used
Window Function	Cannot be used	Can be used

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Table25: Display State and Interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still Pictures	Internal Clock	System interface (RM=0)	Internal clock (DM=0)
Motion Pictures	RGB interface	RGB interface (RM=1)	RGB interface (DM=1)

[NOTE] 1) The instruction register can only be set through the system interface(SPI).
2) The RGB interface mode should not be set during operation.
For the transition flow for each operation mode, see the External Display Interface section.

Internal Clock Mode

All display operation is controlled by signals generated by the internal clock in internal clock mode.
All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB Interface Mode

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (HSYNC), and dot clock (DOTCLK) in RGB interface mode. These signals should be supplied during display operation in this mode.

The display data is transferred to the internal RAM via DB17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the motion picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The periods of the front (FP), back (BP) porch, and the display are automatically generated in the S6E63D6 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC).

VSPL

Determines the active polarity of VSYNC.

Table26: VSPL and VSYNC

VSPL	VSYNC	Description
0 (1)	0 (1)	Valid (Valid)
0 (1)	1 (0)	Invalid (Invalid)

HSPL

Determines the active polarity of HSYNC.

Table27: HSPL and VSYNC

HSPL	HSYNC	Description
0 (1)	0 (1)	Valid (Valid)
0 (1)	1 (0)	Invalid (Invalid)

EPL

Determines the active polarity of ENABLE for using RGB interface.

Table28: EPL, ENABLE and RAM access

EPL	ENABLE	RAM Write	RAM Address
0 (1)	0 (1)	Valid (Valid)	Updated (Updated)
0 (1)	1 (0)	Invalid (Invalid)	Hold (Hold)

DPL

Determines the active polarity of DOTCLK.

Table29: HSPL and VSYNC

DPL	DOTCLK	Description
0 (1)	↑ (↓)	Valid (Valid)
0 (1)	↓ (↑)	Invalid (Invalid)

ENTRY MODE (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	CLS	MDT 1	MDT 0	BGR	X	X	X	SS	X	X	I/D1	I/D0	X	X	X	AM

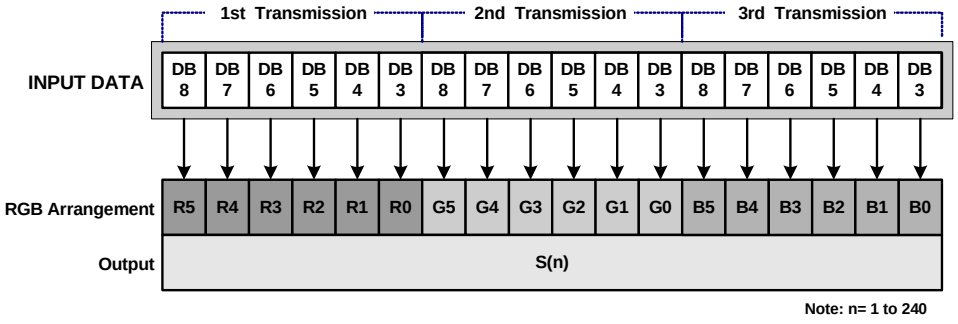
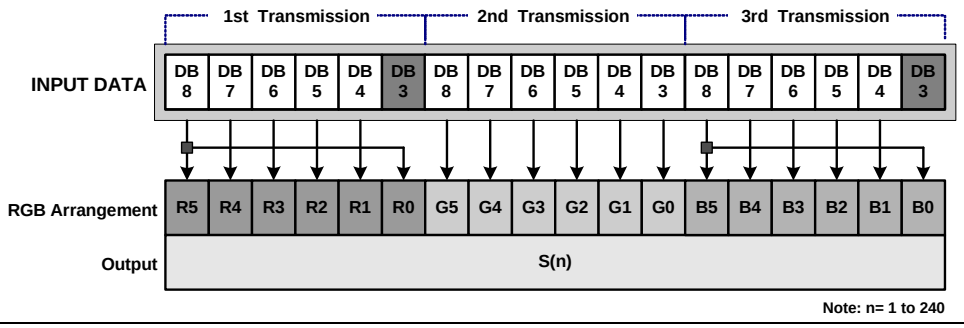
*03h Initial Value = 0000_XXX0_XX11_XXX0

CLS: This bit is used to define the color and interface bus format, When MDT0-1 = 00
CLS = 0 : 65K-color mode through 8-bit(Index address 24h) or 16-bit bus(Index address 23h)
CLS = 1 : 262K-color mode through 9-bit(Index address 24h) or 18-bit bus(Index address 23h)

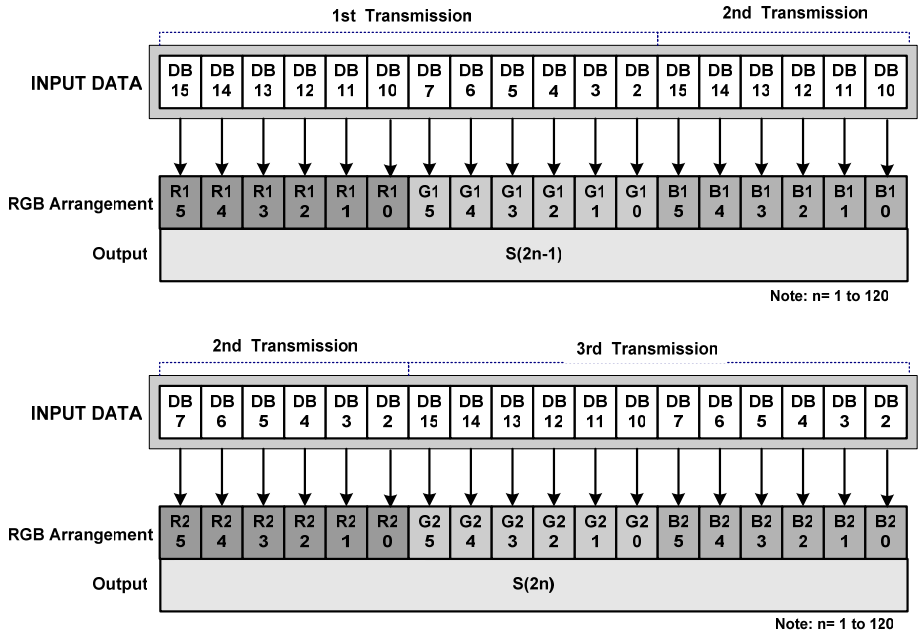
MDT1: This bit is active on the 80-system of 8-bit bus, and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 80-system of 16-bit bus, and the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set in the 8-bit or16-bit mode, set MDT1 bit to be “0”.

MDT0: When 8-bit or16-bit 80 interface mode and MDT1 bit =1, MDT0 defines color depth for the IC.
8-bit (80-system), MDT0 = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)
8-bit (80-system), MDT0 = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

16-bit (80-system), MDT0 = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)
16-bit (80-system), MDT0 = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

<table>
<tr><th>Interface Mode</th><th>MDT1</th><th>MDT0</th><th>Write data to GRAM</th></tr>
<tr><td>*</td><td>0</td><td>0</td><td>Default value. Multiple Data Transfer(MDT1-0) function is not available. Data Transfer is controlled by interface mode. (Depends on S_PB, ID_MIB pins, CLS register and Index address 23h or 24h)</td></tr>
<tr><td rowspan="3">80/68 system 8-bit</td><td>0</td><td>1</td><td>Multiple Data Transfer(MDT1-0) function is not available.</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td> 
</td></tr>
<tr><td>1</td><td> 
</td></tr>
</table>

Preliminary

<table>
<tr><th>Interface Mode</th><th>MDT1</th><th>MDT0</th><th>Data Assignment</th></tr>
<tr><td rowspan="3">80/68 system 16-bit</td><td rowspan="2">0</td><td>1</td><td> 
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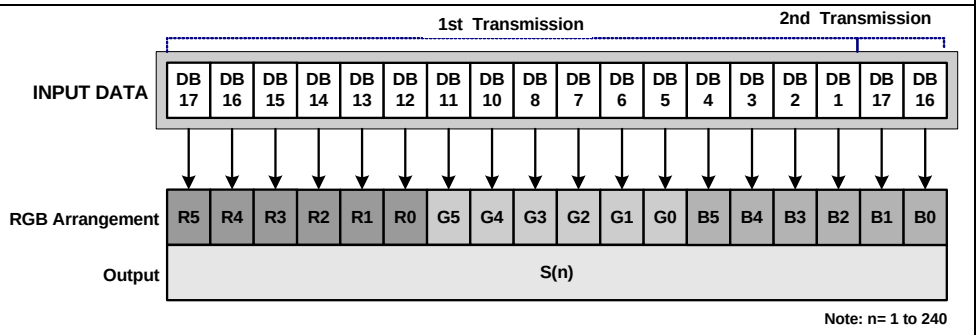
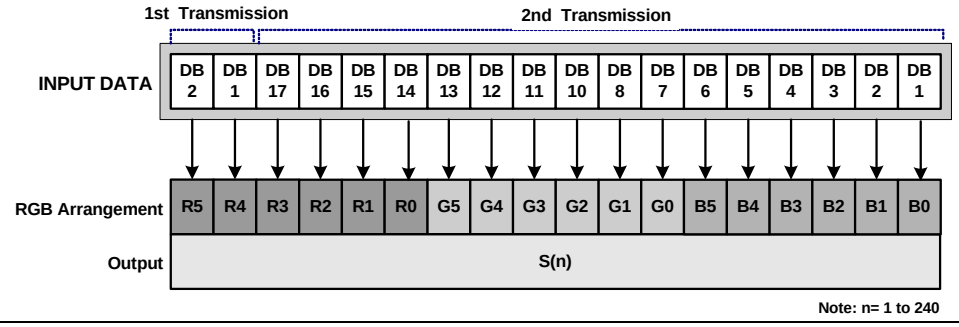
<tr><td>1</td><td>0</td><td> 
</td></tr>
<tr><td>1</td><td>1</td><td> 
</td></tr>
</table>

Preliminary

BGR: About writing 18-bit data to GRAM, it is changed <R><G><B> into <B><G><R>.

- BGR = 0 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {R, G, B}. Actually the analog value that corresponds to DB[17:12] is output firstly at source output
- BGR = 1 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {B, G, R}. Actually the analog value that corresponds to DB[5:0] is output firstly at source output.

SS

Selects the direction of the source driver channel in pixel unit.
When user changes the value of SS, memory should be updated to apply the change.

Table30: Source Output Direction Control with SS (SS = "1")

	S240	S239	S238		S3	S2	S1
G1	"00000"H	"00001"H	"00002"H	•••••••••	"000ED"H	"000EE"H	"000EF"H
G2	"00100"H	"00101"H	"00102"H	•••••••••	"001ED"H	"001EE"H	"001EF"H
G3	"00200"H	"00201"H	"00202"H	•••••••••	"002ED"H	"002EE"H	"002EF"H
G4	"00300"H	"00301"H	"00302"H	•••••••••	"003ED"H	"003EE"H	"003EF"H
G5	"00400"H	"00401"H	"00402"H	•••••••••	"004ED"H	"004EE"H	"004EF"H
G6	"00500"H	"00501"H	"00502"H	•••••••••	"005ED"H	"005EE"H	"005EF"H
G7	"00600"H	"00601"H	"00602"H	•••••••••	"006ED"H	"006EE"H	"006EF"H
G8	"00700"H	"00701"H	"00702"H	•••••••••	"007ED"H	"007EE"H	"007EF"H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
G313	"13800"H	"13801"H	"13802"H	•••••••••	"138ED"H	"138EE"H	"138EF"H
G314	"13900"H	"13901"H	"13902"H	•••••••••	"139ED"H	"139EE"H	"139EF"H
G315	"13A00"H	"13A01"H	"13A02"H	•••••••••	"13AED"H	"13AEE"H	"13AEF"H
G316	"13B00"H	"13B01"H	"13B02"H	•••••••••	"13BED"H	"13BEE"H	"13BEF"H
G317	"13C00"H	"13C01"H	"13C02"H	•••••••••	"13CED"H	"13CEE"H	"13CEF"H
G318	"13D00"H	"13D01"H	"13D02"H	•••••••••	"13DED"H	"13DEE"H	"13DEF"H
G319	"13E00"H	"13E01"H	"13E02"H	•••••••••	"13EED"H	"13EEE"H	"13EEF"H
G320	"13F00"H	"13F01"H	"13F02"H	•••••••••	"13FED"H	"13FEE"H	"13FEF"H

[NOTE] For the case of SS = "0", refer to "GRAM ADDRESS MAP" presented earlier. You should notice that the order of source output is reversed.

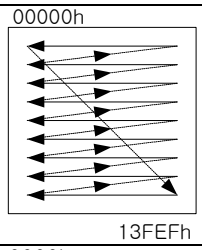
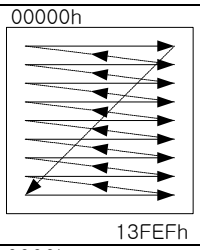
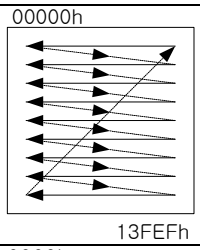
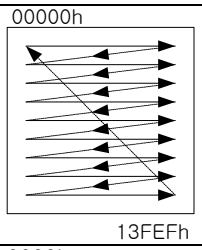
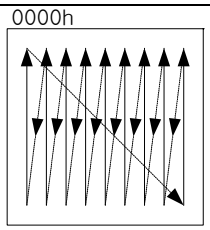
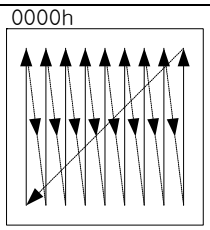
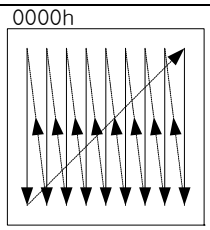
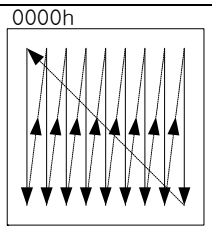
ID

When ID[1], ID[0] = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM.
When ID[1], ID[0] = 0, the AC is automatically decreased by 1 after the data is written to the GRAM.
The increment/decrement setting of the address counter using ID[1:0] is done independently for the horizontal address and vertical address.

AM

Sets the automatic update method of the AC after the data is written to GRAM. When AM = “0”, the data is continuously written in horizontally. When AM = “1”, the data is continuously written vertically. When window addresses are specified, the GRAM in the window range can be written to according to the ID[1:0] and AM.

Table31: Address Direction Setting

	ID[1:0] = “00” H: decrement V: decrement	ID[1:0] = “01” H: increment V: decrement	ID[1:0] = “10” H: decrement V: increment	ID[1:0] = “11” H: increment V: increment
AM=”0” Horizontal Update				
AM=”1” Vertical Update				

[NOTE] When window addresses have been set, the GRAM can only be written within the window.

When AM or ID is set, the start address should be written accordingly prior to memory write.

Preliminary

CLOCK CONTROL (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	x	x	x	x	x	x	x	x	x	DCR 1	DCR 0	x	x	x	x

*04h Initial Value = XXXX_XXXX_XX00_XXXX

DCR

Sets the division ratio of step –up clock, DCCLK, in External Clock Operation mode. In this case, DOTCLK must be input periodically and continuously.

Table32: DCR and Division Ratio of DCCLK

DCR[1:0]	Division ratio of DCCLK
00	DOTCLK / 4
01	DOTCLK / 8
10	DOTCLK / 16
11	DOTCLK / 32

DISPLAY CONTROL – 1 (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	x	X	X	X	DISP_ON

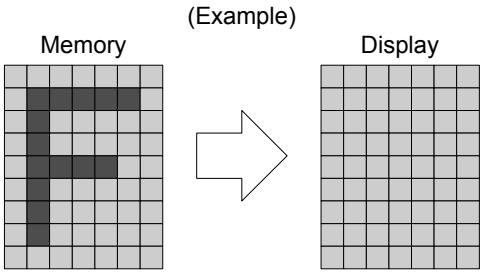
*05h Initial Value = XXXX_XXXX_XXXX_XXX0

DISP_ON

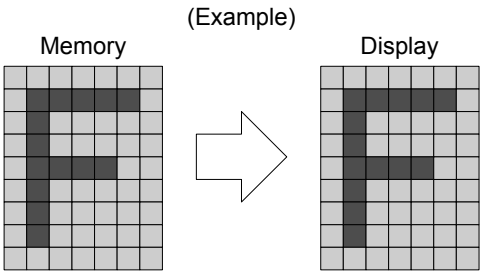
Output from the Frame Memory is enabled.

This register makes No Change of contents of frame memory

DISP_ON = 0 (Display is black image),



DISP_ON = 1,



For more information, see the Instruction Set Up Sequence.

Preliminary

DISPLAY CONTROL – 2 (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	CL	X	X	TEM ON	REV

*06h Initial Value = XXXX_XXXX_XXX0_XX00

CL

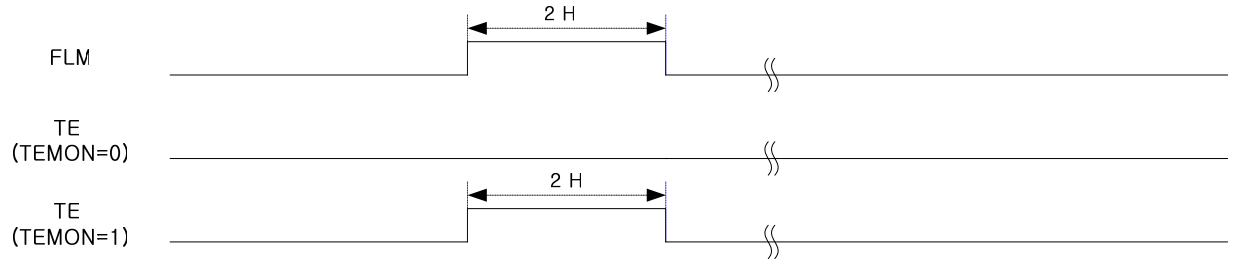
Sets color depth of display.

Table33: Color Control by CL

CL	Description
0	262,144 / 65,536 colors [NOTE]
1	8 colors

[NOTE] It depend on interface mode(18bit or 16bit).

TEMON :
TEMON = 0, Disable the TE output signal from the FLM signal line for preventing Tearing Effect.
TEMON = 1, Enable the TE output signal from the FLM signal line for preventing Tearing Effect.



REV

Displays all characters and graphics display sections with reversal when REV = 1. The grayscale level can be reversed.

Table34: REV and Source Output Level in Normal Display Area

REV	GRAM Data	Source Output Level in Displayed Area
0	6'b000000 ~ 6'b111111	V0 (High Voltage) ~ V63(Low Voltage)
1	6'b000000 ~ 6'b111111	V63 (Low Voltage) ~ V0 (High Voltage)

Preliminary

PANEL INTERFACE CONTROL – 1 (R07h)

PANEL INTERFACE CONTROL – 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	CLWEA4	CLWEA3	CLWEA2	CLWEA1	CLWEA0	X	X	X	X	X	X	X	X

*07h Initial Value = XXX0_1100_XXXX_XXXX

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	CLWEB4	CLWEB3	CLWEB2	CLWEB1	CLWEB0	X	X	X	CLWEC4	CLWEC3	CLWEC2	CLWEC1	CLWEC0

*08h Initial Value = XXX0_1100_XXX0_1100

CLWEA, CLWEB, CLWEC

Specifies the interval time of CLA, CLB, CLC respectively.

Table35: CLWEx and the intervals

CLWEx[4:0]	Description
0_0000	SETTING DISABLE
0_0001	0.5 HCLK
0_0010	1 HCLK
---	---
0_1100	6 HCLK
---	---
1_1110	15 HCLK
1_1111	15.5 HCLK

[NOTE] For the information of HCLK, refer to “FRAME FREQUENCY CACULATION”

PANEL INTERFACE CONTROL – 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCTE3	SCTE2	SCTE1	SCTE0	SCWE3	SCWE2	SCWE1	SCWE0	X	SHE2	SHE1	SHE0	X	CLTE2	CLTE1	CLTE0

*09h Initial Value = 1000_0101_X001_X010

SCTE

Specifies the rising position of SCLK1, SCLK2

Table36: SCTE and the rising position of SCLK1, SCLK2

SCTE[3:0]	Description
0000	16.5 HCLKs
0001	17 HCLKs
0010	17.5 HCLKs
---	----
1000	20.5 HCLKs
---	----
1110	23.5 HCLKs
1111	24 HCLKs

SCWE

Specifies the width of SCLK1, SCLK2

Table37: SCWE and the width of SCLK1, SCLK2

SCWE[3:0]	Description
0000	8 HCLKs
0001	8.5 HCLKs
0010	9 HCLKs
---	---
0101	10.5 HCLKs
---	---
1110	15 HCLKs
1111	15.5 HCLKs

SHE

Specifies the latency of CLB and CLC.

Table38: SHE and the latency of CLB and CLC

SHE[2:0]	Description
000	SETTING DISABLE
001	0.5 HCLK
010	1 HCLK
---	---
110	3 HCLK
111	3.5 HCLK

CLTE

Specifies the falling position of CLA.

Table39: CLTE and the falling position of CLA

CLTE[2:0]	Description
000	SETTING DISABLE
001	0.5 HCLK
010	1 HCLK
011	1.5 HCLKs
---	---
110	3 HCLKs
111	3.5 HCLKs

PANEL INTERFACE CONTROL – 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	GTC ON1	GTC ON0

*0Ah Initial Value = XXXX_XXXX_XXXX_XX00

GTCON

Specifies the panel interface signals.

Table40: GTCON and the panel interface signals

Output Pin	Output Signal			
	GTCON[1:0]=00	GTCON[1:0]=01	GTCON[1:0]=10	GTCON[1:0]=11
BICTL_L	VGH	VGL	VGH	VGL
BICTL_R	VGH	VGL	VGH	VGL
FLM	FLM	FLM	FLM	FLM
SFTCLK	SFTCLK	SFTCLK	VGL	VGL
SFTCLKB	SFTCLKB	SFTCLKB	VGH	VGH
SCLK1	SCLK1	SCLK2	SCLK1	SCLK2
SCLK2	SCLK2	SCLK1	SCLK2	SCLK1
EX_FLM	EX_FLM	EX_FLM	EX_FLM	EX_FLM
EX_CLK	EX_CLK	EX_CLKB	VGL	VGL
EX_CLKB	EX_CLKB	EX_CLK	VGH	VGH
ESR	ESR	ESR	ESR	ESR
CLA	CLA	CLA	CLA	CLA
CLB	CLB	CLB	CLB	CLB
CLC	CLC	CLC	CLC	CLC

STAND BY (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	STB

*10h Initial Value = XXXX_XXXX_XXXX_XXX1

STB

When STB = “1”, S6E63D6 enters Standby mode, where display operation completely stops including the internal R-C oscillation. Furthermore, no external clock pulses are supplied. For details, see the “STANDBY SEQENCE” described later.
Only the following instructions can be executed during the standby mode.

– Standby mode cancel ; STB = “0”

POWER GEN1 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	x	x	x	x	x	x	x	x	x	X	x	VC3	VC2	VC1	VC0

*12h Initial Value = XXXX_XXXX_XXXX_1000

V reference voltage of VLOUT1, VLOUT2 and VLOUT3.

VC[3:0]	VCI1 [Without Load]
0000	2.10 V
0001	2.15 V
0010	2.20 V
0011	2.25 V
0100	2.30 V
0101	2.35 V
0110	2.40 V
0111	2.45 V
1000	2.50 V
1001	2.55 V
1010	2.60 V
1011	2.65 V
1100	2.70 V
1101	2.75 V
1110	Setting Disable
1111	Setting Disable

[NOTE] Set VCI1 in the range of VCI > VCI1 + 0.3V

POWER GEN2 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	VINT3	VINT2	VINT1	VINT0	X	VGH3	VGH2	VGH1	VGH0	X	VGL3	VGL2	VGL1	VGL0

*13h Initial Value = XX01_01X0_011X_1010

VINT3[3:0] set VINT (control voltage of OLED Panel). It can be amplified -2.0 to -0.5 times of VCIR.

VINT[3:0]	VINT value
0000	-1.0 V
0001	-1.2 V
0010	-1.4 V
0011	-1.6 V
0100	-1.8 V
0101	-2.0 V
0110	-2.2 V
0111	-2.4 V
1000	-2.6 V
1001	-2.8 V
1010	-3.0 V
1011	-3.2 V
1100	-3.4 V
1101	-3.6 V
1110	-3.8 V
1111	-4.0 V

[NOTE] Set VINIT in the range of V VINT > VLOUT3 + 1.0V

VGH[3:0] set VGH (High Voltage Level for Gate).

VGH[3:0]	VGH value
0000	4.6 V
0001	4.8 V
0010	5.0 V
0011	5.2 V
0100	5.4 V
0101	5.6 V
0110	5.8 V
0111	6.0 V

1000	6.2 V
1001	6.4 V
1010	6.6 V
1011	Setting disable
1100	Setting disable
1101	Setting disable
1110	Setting disable
1111	Setting disable

[NOTE] Set VGH in the range of VGH < VLOUT2-1.0V

VGL[3:0] bits set VGL (Low Voltage Level for Gate).

VGL[3:0]	VGL Value
0000	-5.0 V
0001	-5.2 V
0010	-5.4 V
0011	-5.6 V
0100	-5.8 V
0101	-6.0 V
0110	-6.2 V
0111	-6.4 V
1000	-6.6 V
1001	-6.8 V
1010	-7.0 V
1011	-7.2 V
1100	-7.4 V
1101	-7.6 V
1110	-7.8 V
1111	Setting disable

[NOTE] Set VGL in the range of VGL > VLOUT3 + 1.0V

POWER STEP UP CONTROL 1 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	DC2 2	DC2 1	DC2 0	X	DC1 2	DC1 1	DC1 0	X	X	X	X	X	X	BT1	BT0

*14h Initial Value = X100_X010_XXXX_XX00

DC2[2:0] is the operating frequency in the step-up circuit 2 is selected.
DC1[2:0] is the operating frequency in the step-up circuit 1 is selected.

DC2[2:0]	Step-up Cycle in Step-up Circuit 2		DC1[2:0]	Step-up Cycle in Step-up Circuit 1	
	DM=0	DM=1		DM=0	DM=1
000	OSC_CK/16	DCCLK/16	000	OSC_CK/16	DCCLK/16
001	OSC_CK/24	DCCLK/24	001	OSC_CK/24	DCCLK/24
010	OSC_CK/32	DCCLK/32	010	OSC_CK/32	DCCLK/32
011	OSC_CK/48	DCCLK/48	011	OSC_CK/48	DCCLK/48
100	OSC_CK/64	DCCLK/64	100	OSC_CK/64	DCCLK/64
101	OSC_CK/96	DCCLK/96	101	OSC_CK/96	DCCLK/96
110	OSC_CK/128	DCCLK/128	110	OSC_CK/128	DCCLK/128
111	OSC_CK/256	DCCLK/256	111	OSC_CK/256	DCCLK/256

[NOTE] DM is Display Method. DCCLK is for External I/F. See instruction R02h, R04h.

BT[1:0] switch the output factor of step-up. Adjust scale factor of the step-up circuit by the voltage used.

BT[1:0]	VLOUT1	VLOUT2	VLOUT3
00	VCI1 x 2	VCI1 x 4	-(VCI1 x 4)
01	VCI1 x 2	VCI1 x 4	-(VCI1 x 3)
10	VCI1 x 2	VCI1 x 3	-(VCI1 x 4)
11	VCI1 x 2	VCI1 x 3	-(VCI1 x 3)

START OSCILLATION (R18h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	RADJ5	RADJ4	RADJ3	RADJ2	RADJ1	RADJ0

*18h Initial Value = XXXX_XXXX_XX01_1111

Select the oscillation frequency of internal oscillator.

RADJ[5:0]	Oscillation Speed	RADJ[5:0]	Oscillation Speed
000000	x 0.543(Min.)	010101	x 0.782
000001	x 0.551	010110	x 0.800
000010	x 0.560	010111	x 0.818
000011	x 0.568	011000	x 0.835
000100	x 0.578	011001	x 0.855
000101	x 0.586	011010	x 0.877
000110	x 0.596	011011	x 0.899
000111	x 0.606	011100	x 0.921
001000	x 0.615	011101	x 0.946
001001	x 0.626	011110	x 0.972
001010	x 0.637	011111	x 1.000
001011	x 0.647	100000	x 1.037
001100	x 0.660	100001	x 1.067
001101	x 0.671	100010	x 1.101
001110	x 0.685	100011	x 1.135
001111	x 0.697	100100	x 1.172
010000	x 0.707	100101	x 1.212
010001	x 0.721	100110	x 1.256
010010	x 0.736	100111	x 1.302
010011	x 0.751	101000	X1.352(Max.)
010100	x 0.766	101001 ~ 111111	Setting disable

SOURCE DRIVER CONTROL (R1Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	GAMMA_TEST	SDUM_ON	X	SAP2	SAP1	SAP0

*1Ah Initial Value = XXXX _XXXX_XX00_X101

When GAMMA_TEST='1', V0/V63 pins are shorted to each gamma voltage V0/V63 and gamma voltage V0/V63 can be monitored or be forced by external voltage level.

GAMMA_TEST	V0 / V63
0	Hi-z
1	V0 / V63

When SDUM_ON='1', SOUT_DUM1 and SOUT_DUM240 pins are shorted to SOUT[1], SOUT[240] output and can be monitored.

SDUM_ON	SOUT_DUM1 / SOUT_DUM240
0	Hi-z
1	SOUT[1] / SOUT[240]

Adjust the slew-rate of the operational amplifier of the source driver. If higher SAP[2:0] is set, OLED panel having higher resolution of higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But, these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP[2:0]="000", operational amplifiers are turned off, so current consumption can be reduced

SAP[2:0]	Slew-Rate of Operational Amplifier	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier stops.	
001	Slow	Small
010	Slow or medium	Small or medium
011	Medium	Medium
100	Medium or small fast	Medium or small large
101	Small fast	Small large
110	Fast	large
111	Big fast	Big large

GRAM ADDRESS SET (R20h)

GRAM ADDRESS SET (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

*20h Initial Value = XXXX _XXXX_0000_0000

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

*21h Initial Value = XXXX _XXX0_0000_0000

AD

You can write initial GRAM address into internal Address Counter (AC). When GRAM data is transferred through System Interface or RGB Interface, the AC is automatically updated according to AM and ID. This allows consecutive write without re-setting address in AC. But when GRAM data is read, the AC is not automatically updated.
GRAM address setting is not allowed in Standby mode. Ensure that the address is set within the specified window area.
When RGB interface is used (RM=”1”) to access GRAM, AD[16:0] will be set in the address counter at the falling edge of the VSYNC signal. And when one uses System Interface to access GRAM (RM = “0”), AD[16:0] will be set upon the execution of an instruction.

Table41: GRAM Address Range

AD[16:0]	GRAM setting
“00000h” to “00AFh”	Bitmap data for G1
“00100h” to “01AFh”	Bitmap data for G2
“00200h” to “02AFh”	Bitmap data for G3
“00300h” to “03AFh”	Bitmap data for G4
⋮	⋮
“13C00h” to “13CEFh”	Bitmap data for G317
“13D00h” to “13DEFh”	Bitmap data for G318
“13E00h” to “13EEFh”	Bitmap data for G319
“13F00h” to “13FEFh”	Bitmap data for G320

WRITE DATA TO GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data (WD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)															
W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
		When RGB-interface															

WD17-0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to I/D bit settings. The GRAM cannot be accessed in standby mode. When 16- or 8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

When data is written to RAM used by RGB interface via the system interface, please make sure that write data conflicts do not occur.

When the 18-bit RGB interface is in use, 18-bit data is written to RAM via DB17-0 and 262,144-colors are available. When the 16-bit RGB interface is in use, the MSB is written to its LSB and 65,536-colors are available.

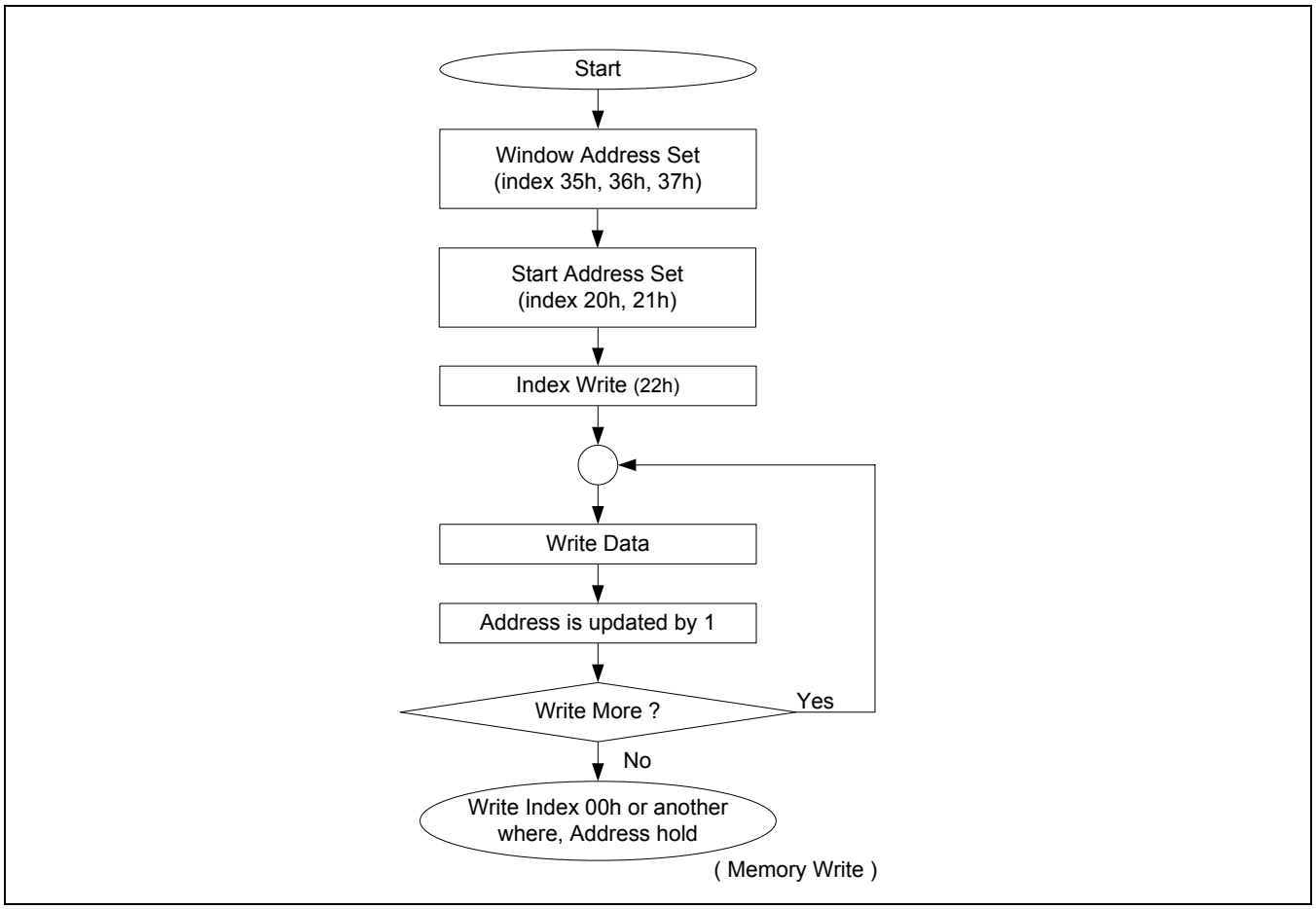


Figure6: Memory Data Write Sequence

READ DATA FROM GRAM (R22h)

R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RAM Read data (RD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)																	

RD17–0: Read 18-bit data from the GRAM. When the data is read to the CPU, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

In case of 16-/8-bit interface, the LSB of <R><B> color data will not be read.
This function is not available in RGB interface mode.

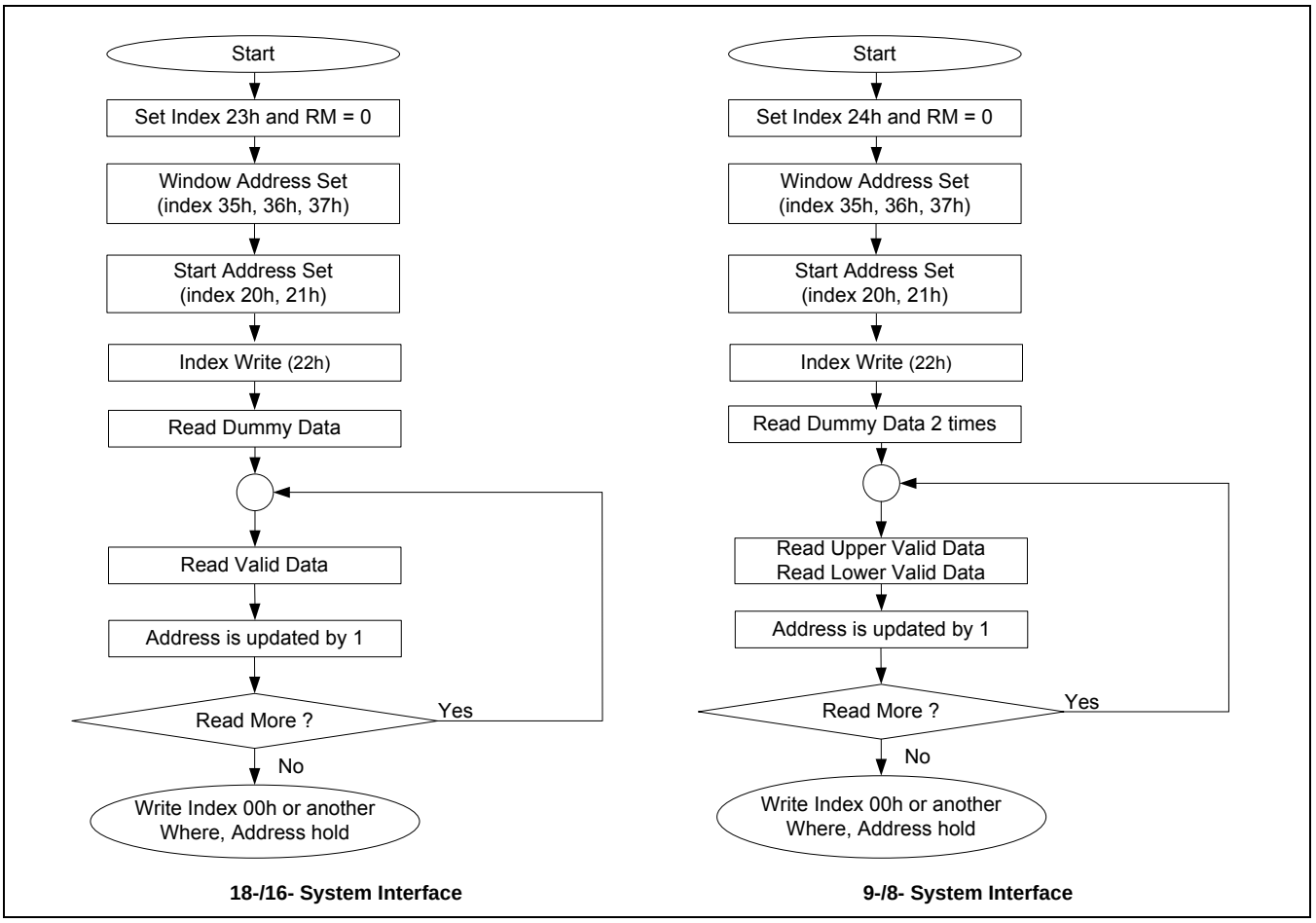


Figure7: Memory Data Read Sequence

SELECT DATA BUS 1 (R23h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	Select 18-/16-bit Data Bus Interface															

SELECT DATA BUS 2 (R24h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	Select 9-/8-bit Data Bus Interface															

We can select system interface mode by pins and instruction as following.

Table42: System Interface mode

Pins			Registers				
MDDI_EN	S_PB	ID_MIB	Index Address	Command (CLS)	Command MDT[1]	Command MDT[0]	Description
0	0 (Parallel)	0 (80 mode)	default & 24h (9/8bit)	0 (80 8bit)	0	x	80-system 8-bit 65k bus interface
					1	0	80-system 8-bit 260k bus interface
						1	80-system 8-bit 65k bus interface
				1(80 9bit)	x	X	80-system 9-bit 260k bus interface
			Index 23 h (18/16bit)	0 (80 16bit)	0	0	80-system 16-bit 65k bus interface
						1	80-system 16-bit 260k bus interface
					1	X	80-system 16-bit 260k bus interface
				1(80 18bit)	x	X	80-system 18-bit 260k bus interface
		1 (68 mode)	default & 24h (9/8bit)	0 (68 8bit)	0	X	68-system 8-bit 65k bus interface
					1	0	68-system 8-bit 260k bus interface
						1	68-system 8-bit 65k bus interface
				1 (68 9bit)	x	X	68-system 9-bit 260k bus interface
			Index 23 h (18/16bit)	0 (68 16bit)	0	0	68-system 16-bit 65k bus interface
						1	68-system 16-bit 260k bus interface
					1	x	68-system 16-bit 260k bus interface
				1 (68 18bit)	x	x	68-system 18-bit 260k bus interface
	1 (Serial)	ID	x	x	x	x	Serial peripheral interface (SPI)
1	x	x	x	x	x	x	

[NOTE] For details, see the ENTRY MODE (Instruction R03h).

VERTICAL SCROLL CONTROL 1 (R30h, R31h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SSA 8	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0
W	1	X	X	X	X	X	X	X	SEA 8	SEA 7	SEA 6	SEA 5	SEA 4	SEA 3	SEA 2	SEA 1	SEA 0

*30h Initial Value = XXXX_XXX0_0000_0000
*31h Initial Value = XXXX_XXX1_0011_1111

SSA8-0: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	Scroll Start Address
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

SEA8-0: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA8	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0	Scroll End Address
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

[NOTE] Don't set any higher raster-row than 319 ("13F"H)
Set SS18-10 ≦ SSA8-0, if set out of range, SSA8-0 = SS18-10.
Set SE18-10 ≧ SEA8-0, if set out of range, SEA8-0 = SE18-10

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VERTICAL SCROLL CONTROL 2 (R32h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SST 8	SST 7	SST 6	SST 5	SST 4	SST 3	SST 2	SST 1	SST 0

*32h Initial Value = XXXX_XXX0_0000_0000

SST8-0: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any raster-row from the 1st to 320th can be scrolled for the number of the raster-row. After 319th raster-row is displayed, the display restarts from the first raster-row. When SST8-0 = 00000000, Vertical Scroll Function is disabled.

SST8	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Step
0	0	0	0	0	0	0	0	0	Scroll Disabled
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	0	1	1	3 raster-row
0	0	0	0	0	0	1	0	0	4 raster-row
0	0	0	0	0	0	1	0	1	5 raster-row
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	0	316 raster-row
1	0	0	1	1	1	1	0	1	317 raster-row
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

[NOTE] Don't set any higher raster-row than 319 ("13F"H)
Set SS18-10 < SSA8-0 + SST8-0 ≦ SEA8-0 ≦ SE18-10, if set out of range, Scroll function is disabled

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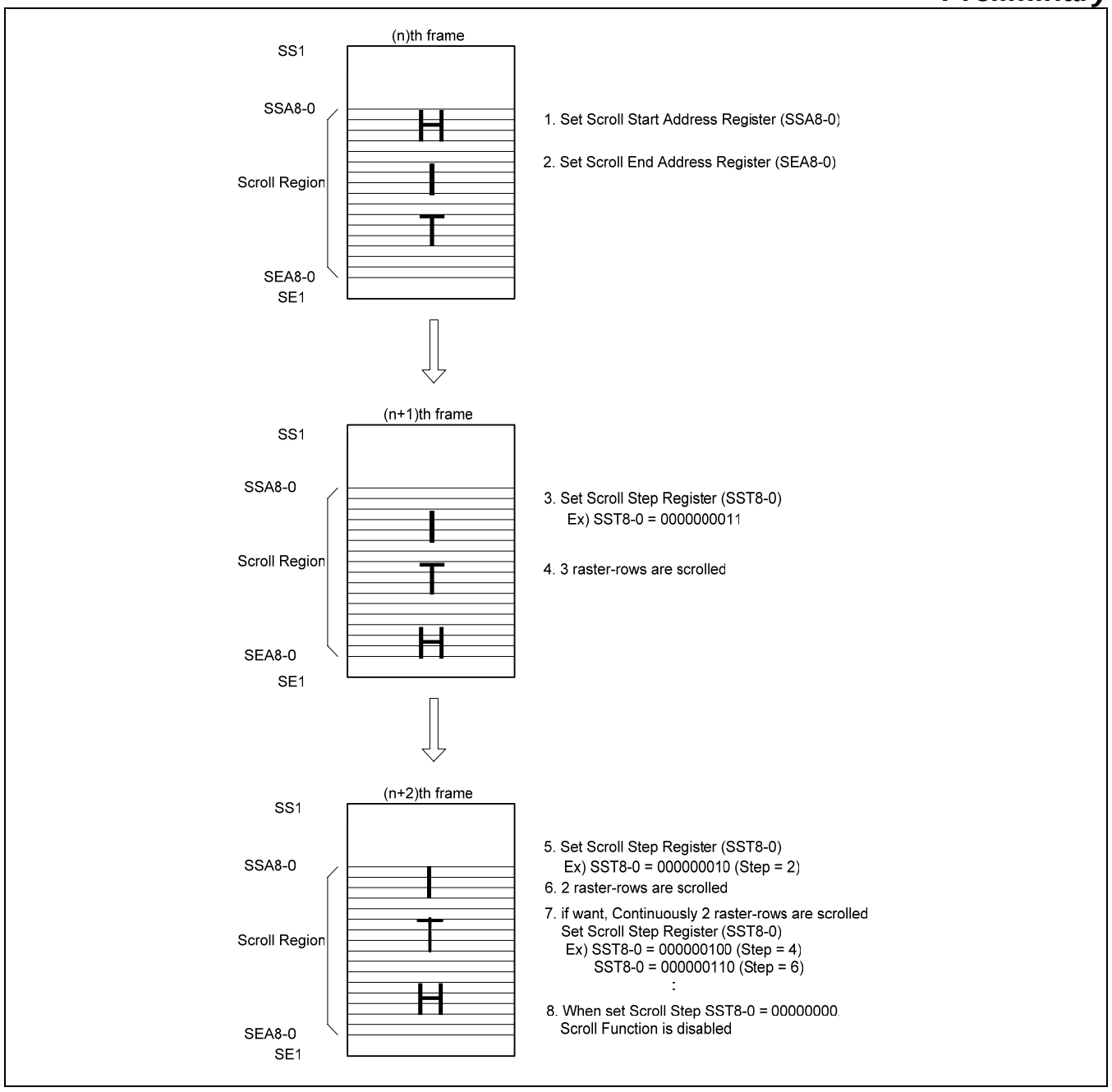

Figure8: Vertical Scroll Display

PARTIAL SCREEN DRIVING POSITION (R33h, R34h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	X	X	X	X	X	X	X	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10

*33h Initial Value = XXXX_XXX0_0000_0000
*34h Initial Value = XXXX_XXX1_0011_1111

SS18–10: Specify the drive starting position for the first screen in a line unit. The OLED driving starts from the 'set value +1' gate driver.

SE18–10: Specify the driving end position for the screen in a line unit. The OLED driving is performed to the 'set value + 1' gate driver. For instance, when SS18–10 = 019h and SE18–10 = 029h are set, the OLED driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS18–10 ≤ SE18–10 ≤13Fh.

[NOTE] DO NOT set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.
Ex) SS18-0=007h and SE18-0=010h are performed from G8 to G17.

The S6E63D6 can select and drive partial screens at any position with the screen-driving position registers (R33h, R34h). Any partial screens required for display are selectively driven and reducing OLED-driving voltage and power consumption.

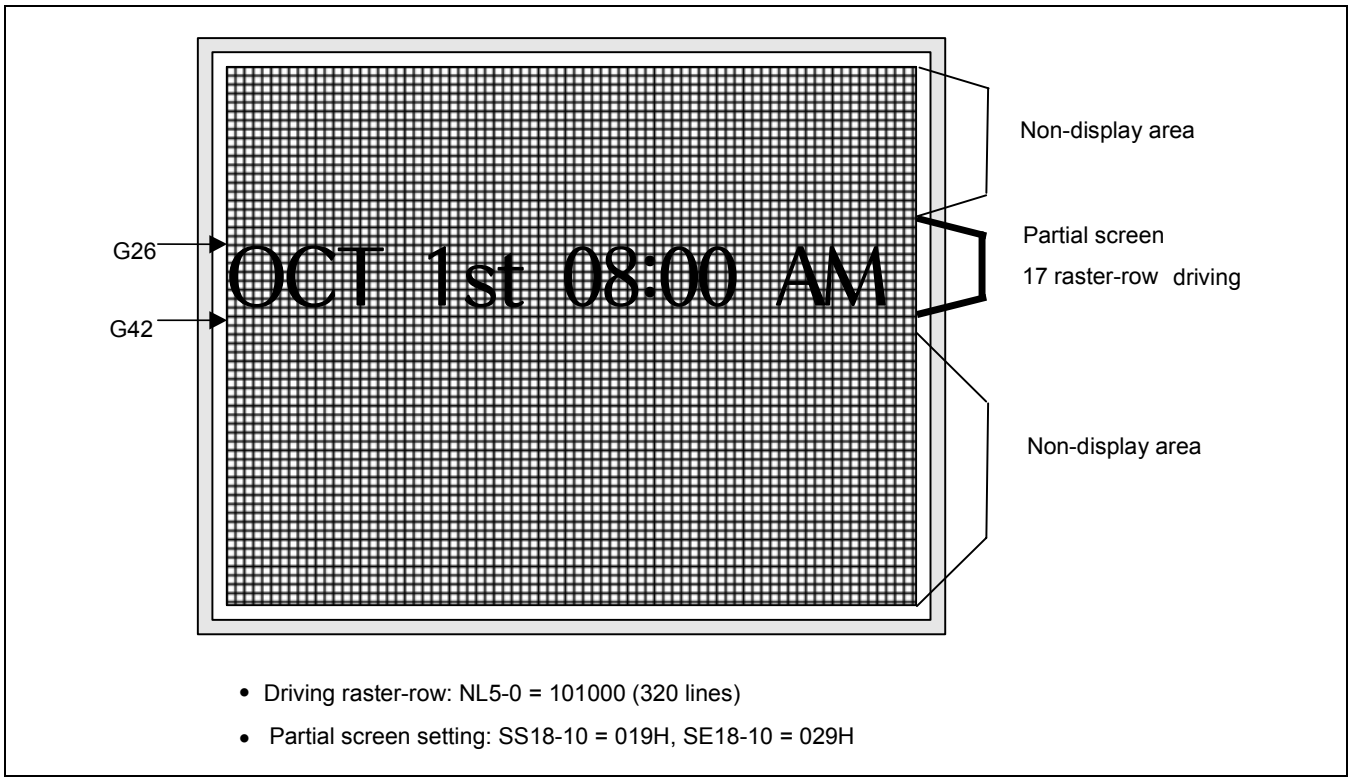

Figure9: Driving On Partial Screen

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RESTRICTION ON PARTIAL DISPLAY AREA SETTING

The following restrictions must be satisfied when setting the start line (SS18 to 10) and end line (SE18 to 10) of the partial screen driving position register (R33h, R34h) for the S6E63D6. Note that incorrect display may occur if the restrictions are not satisfied.

Table43: Restrictions on the partial Screen Driving Position Register Setting

Register setting	Display operation
(SE18 to 10) – (SS18 to 10) = NL*8	Full screen display Normally displays (SS18 to 10) to (SE18 to 10)
(SE18 to 10) – (SS18 to 10) < NL*8	Partial display Normally displays (SS18 to 10) to (SE18 to 10) Black display for all other times (RAM data is not related at all)
(SE18 to 10) – (SS18 to 10) > NL*8	Setting disabled

[NOTE] 000h ≤ SS18 to 10 ≤ SE18 to 10 ≤ 13Fh

VERTICAL RAM ADDRESS POSITION (R35h,R36h)

HORIZONTAL RAM ADDRESS POSITION (R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	VSA 8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
W	1	X	X	X	X	X	X	X	VEA 8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0
W	1	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0

*35h Initial Value = XXXX_XXX0_0000_0000
*36h Initial Value = XXXX_XXX1_0011_1111
*37h Initial Value = 0000_0000_1110_1111

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VSA8-0 to the address specified by VEA8-0. Note that an address must be set before RAM is written.

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HSA7-0 to the address specified by HEA 7-0. Note that an address must be set before RAM is written..

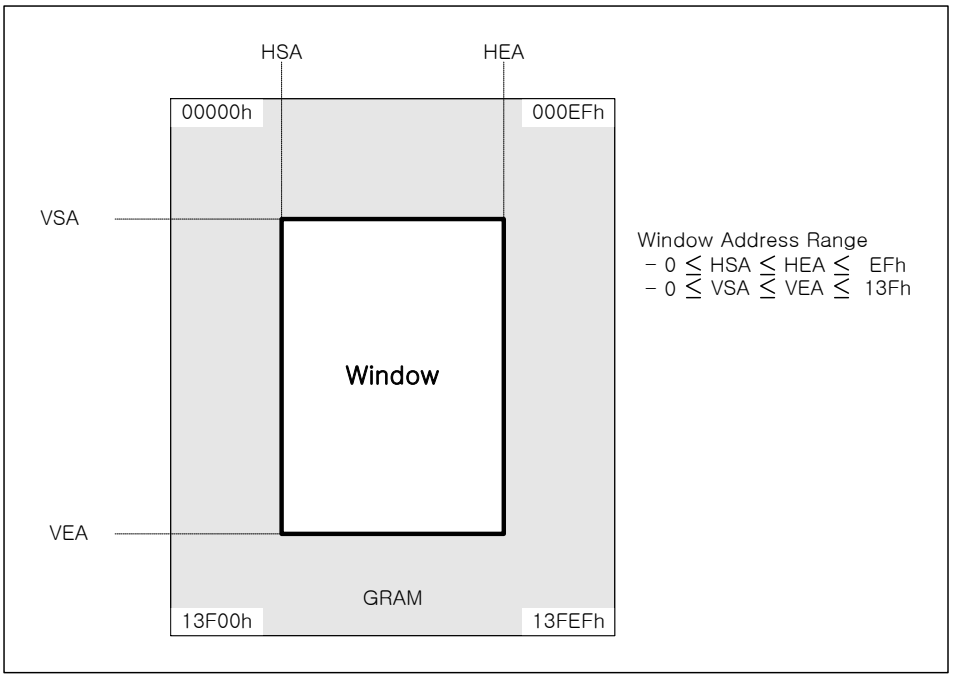

Figure10: Window Address Function

[NOTE] Ensure that the Window addresses are within the GRAM address space.

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CLIENT INITIATED WAKE-UP (R38h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VWAKE_EN

*38h Initial Value = XXXX_XXXX_XXXX_XXX0

VWAKE_EN : When VWAKE_EN is 1, client initiated wake-up is enabled. But parameter data IB[15:1] must be "0000h", otherwise, client initiated wake-up is disabled.

MDDI LINK WAKE-UP START POSITION (R39h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	X	WKF3	WKF2	WKF1	WKF0	X	X

*39h Initial Value = 0000_0000_0X00_00XX

WKF3-0 : When client initiated wake-up is used at MDDI, the frame position that data is updated is set by the value of WKF 3-0. The range of WKF is from '0000' to '1111'.
If WKF is '0000', data is updated at the first frame, and if "1111" data update starts after 16th frame.

WKL8-0 : When client initiated wakeup is used at MDDI, data is updated at the line the value of WKL7-0 in the frame that is set by WKF3-0. The range of WKL is from '000h' to '1FFh'.
If WKL is '000h', data is updated at the first line, and if WKL is '0FFh', data update starts at the 256th line.

Setting of WFK and WKL is needed for client-initiated link wake-up.
For example, WKF is "0010" and WKL is "0001", data is updated at second line of third frame.

SUB PANEL CONTROL 1 (R3Ah / R3Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	SUB_SEL							
W	1	X	X	X	X	X	X	X	X	SUB_WR							

*3Ah Initial Value = XXXX_XXXX_0111_1010
*3Bh Initial Value = XXXX_XXXX_0010_0010

SUB_SEL : SUB_SEL is the index of main/sub panel selection. Initial value of SUB_SEL is '7Ah'.
In MDDI mode, If written register address is '7Ah' (initial state: SUB_SEL is '7Ah') and register data is '0001h', then main panel is selected, and if that is "0000h", then sub panel is selected.
Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_WR : SUB_WR is the index of sub panel data write. Initial value of SUB_WR is '22h'.
When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 22h), index for GRAM access is automatically transferred before GRAM data transfer.
When sub panel driver IC uses other address, 22h address have to be changed. Then user can change SUB_WR value from 22h to other value.

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SUB PANEL CONTROL 2 (R3Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	FCV_EN	X	X	X	MPU_MODE	STN_EN	SUB_IM1	SUB_IM0

*3Ch Initial Value = XXXX_XXXX_0XXX_0000

SUB_IM1-0: set the sub-panel interface

SUB_IM1	SUB_IM0	Interface
0	0	18bit
0	1	9bit
1	0	16bit
1	1	8bit

STN_EN: set the panel property.
STN_EN = “1”: STN panel.
STN_EN = “0”: TFT panel**.**

MPU_MODE: set the MPU interfaces
MPU_MODE = “1”: 68 mode
MPU_MODE = “0”: 80 mode

FCV_EN : data format conversion enable signal
FCV_EN = “1”: 16 bit data format conversion (not used)
FCV_EN = “0”: current 16bit data format

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TEST KEY COMMAND (R60h)

MTP CONTROL (R61h)

MTP REGISTER SETTING (R62h, R63h, R64h, R65h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	0	0	0	0	1	1	1	1
W	1	X	X	X	X	X	X	X	MTP_ WRB	X	X	X	MTP_ SEL	X	X	X	MTP_ ERB
W	1	X	R21_DK2	R21_DK1	R21_DK0	R21_BT2	R21_BT1	R21_BT0	X	R63_DK3	R63_DK2	R63_DK1	R63_DK0	R63_BT3	R63_BT2	R63_BT1	R63_BT0
W	1	X	G21_DK2	G21_DK1	G21_DK0	G21_BT2	G21_BT1	G21_BT0	X	G63_DK3	G63_DK2	G63_DK1	G63_DK0	G63_BT3	G63_BT2	G63_BT1	G63_BT0
W	1	X	B21_DK2	B21_DK1	B21_DK0	B21_BT2	B21_BT1	B21_BT0	X	B63_DK3	B63_DK2	B63_DK1	B63_DK0	B63_BT3	B63_BT2	B63_BT1	B63_BT0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	E_OST2	E_OST1	E_OST_0

*Initial Value MTP_WRB: 1'b1, MTP_SEL: 1'b1, MTP_ERB: 1'b1
R21_DK[2:0]: 3'd0, R21_BT[2:0]: 3'd0, R63_DK[3:0]: 4'd0, R63_BT[3:0]: 4'd0
G21_DK[2:0]: 3'd0, G21_BT[2:0]: 3'd0, G63_DK[3:0]: 4'd0, G63_BT[3:0]: 4'd0
B21_DK[2:0]: 3'd0, B21_BT[2:0]: 3'd0, B63_DK[3:0]: 4'd0, B63_BT[3:0]: 4'd0
E_OST[2:0]:3'd0

Test Key Command : Protection command. When Test Key Command =8Ch, MTP_WRB and MTP_ERB are valid

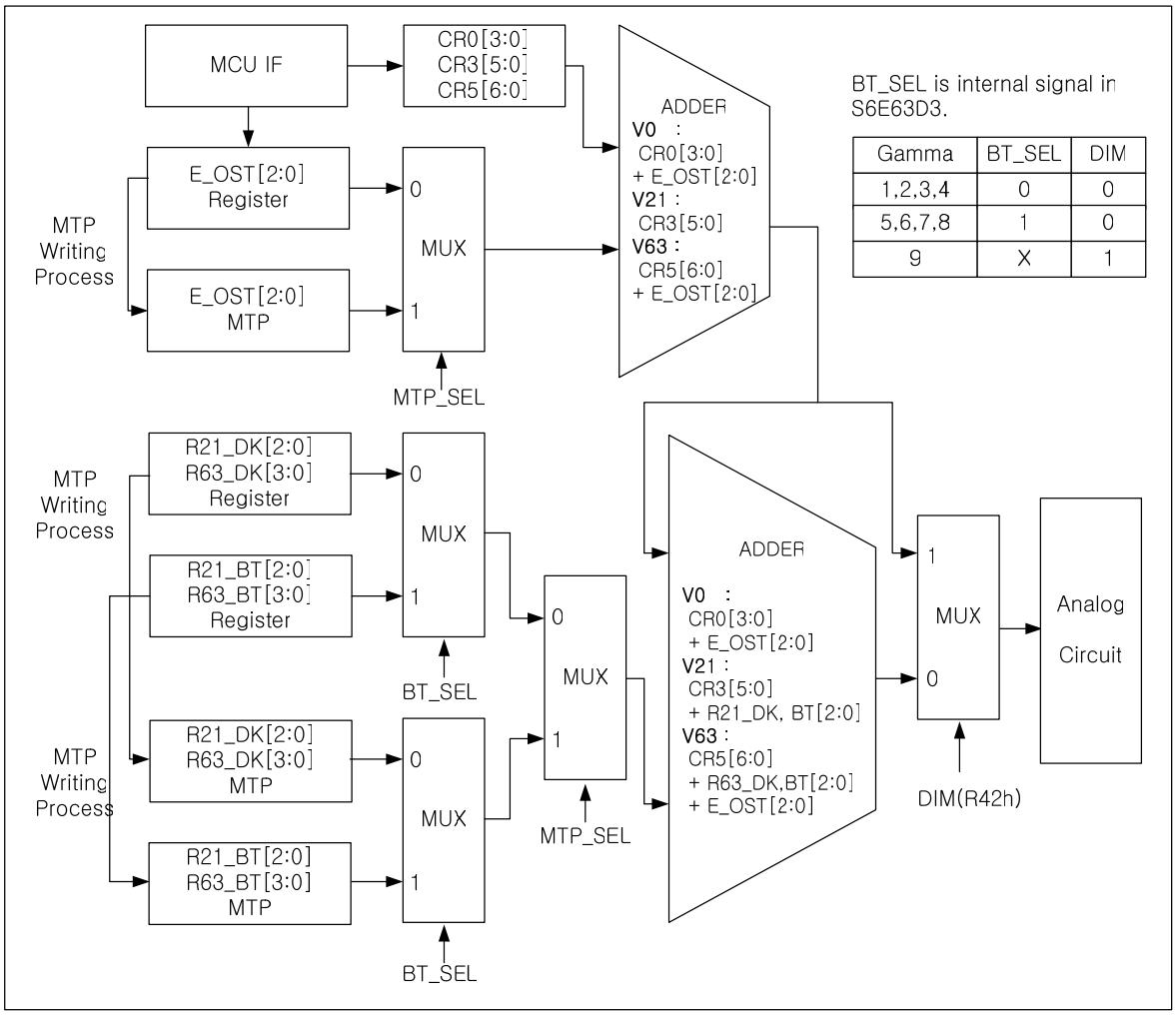
MTP_WRB: MTP Write enable signal. If you want to write data to MTP cell, set MTP_WRB = 0
MTP_SEL: Selects MTP value or register value added to CR5[6:0], CG5[6:0], CB5[6:0], CR3[5:0], CG3[5:0], and CB3[5:0]
MTP_ERB**:** Enable for MTP initial or erase. When MTP_ERB = 0, MTP initialization or erase is enabled.

R21_DK[3:0], R21_BT[[3:0]: V21(Red) offset compensation value.
G21_DK[3:0], G21_BT[[3:0]: V21(Green) offset compensation value.
B21_DK[3:0], B21_BT[[3:0]: V21(Blue) offset compensation value.

R63_DK[4:0], R63_BT[[4:0]: V63(Red) offset compensation value.
G63_DK[4:0], G63_BT[[4:0]: V63(Green) offset compensation value.
B63_DK[4:0], B63_BT[[4:0]: V63(Blue) offset compensation value.

E_OST[2:0]: ELVDD offset compensation value

Preliminary



Preliminary

R(G,B)_21[2:0]	complement offset value	R(G,B)_63[3:0]	complement offset value	E_OST[2:0]	complement offset value
011	+3	0111	+7	011	+3
010	+2	0110	+6	010	+2
001	+1	0101	+5	001	+1
000	0	0100	+4	000	0
111	-1	0011	+3	111	-1
110	-2	0010	+2	110	-2
101	-3	0001	+1	101	-3
100	-4	0000	0	100	-4
		1111	-1		
		1110	-2		
		1101	-3		
		1100	-4		
		1011	-5		
		1010	-6		
		1001	-7		
		1000	-8		

Preliminary

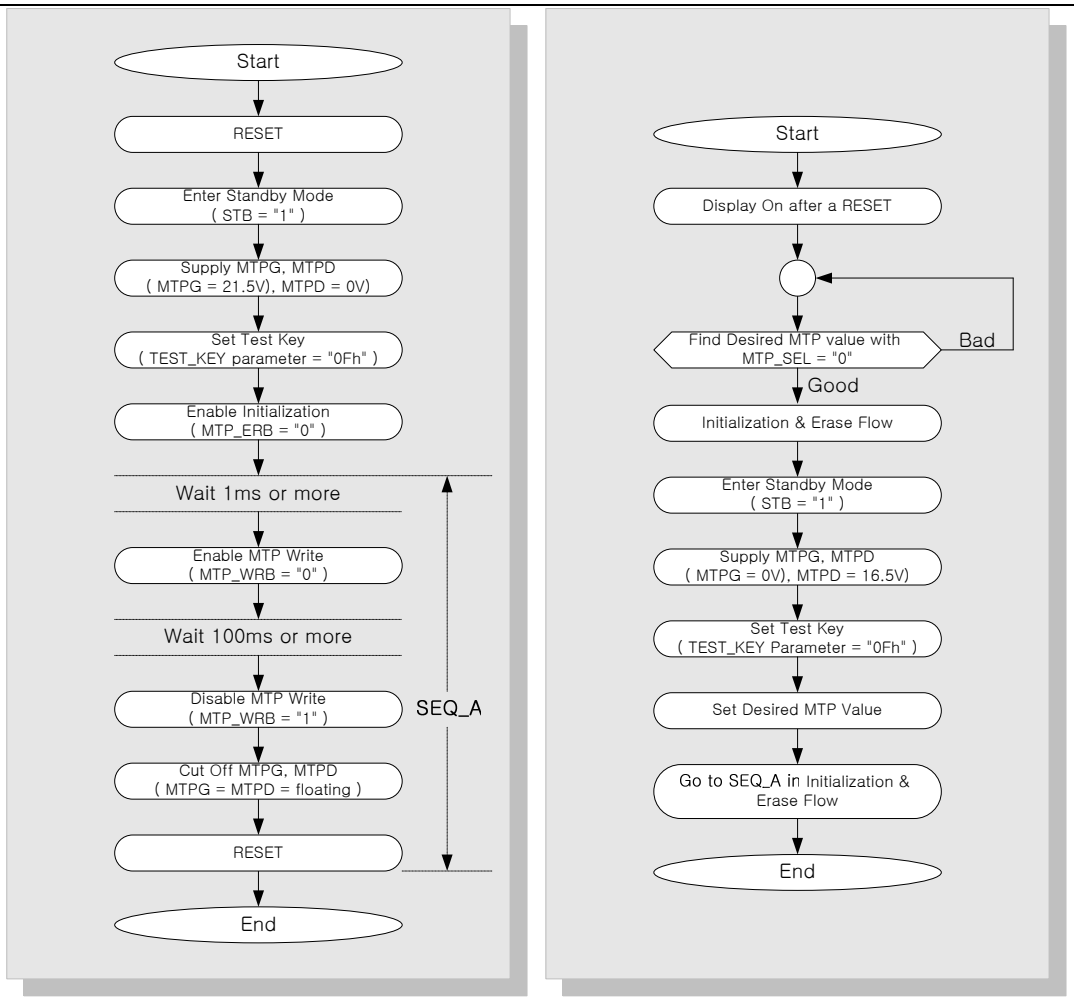


Figure16: MTP Initialization, Erase and program

Preliminary

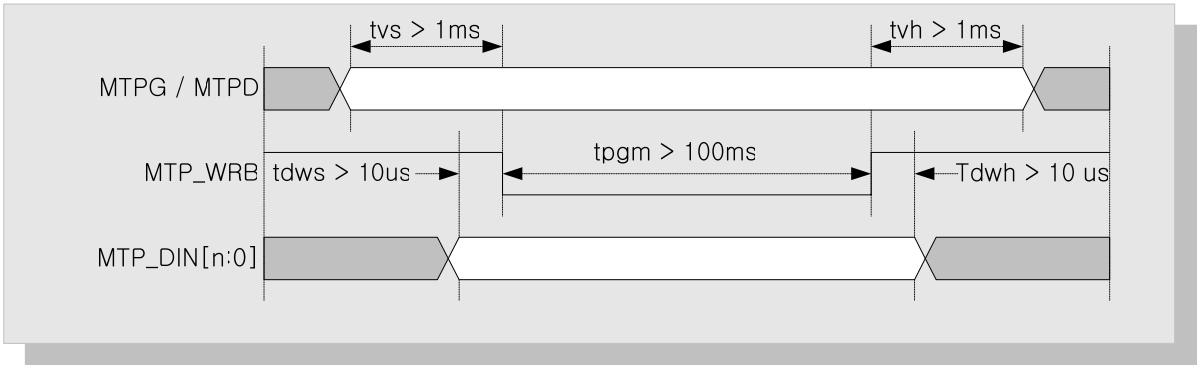


Figure17: Timing of MTP Program

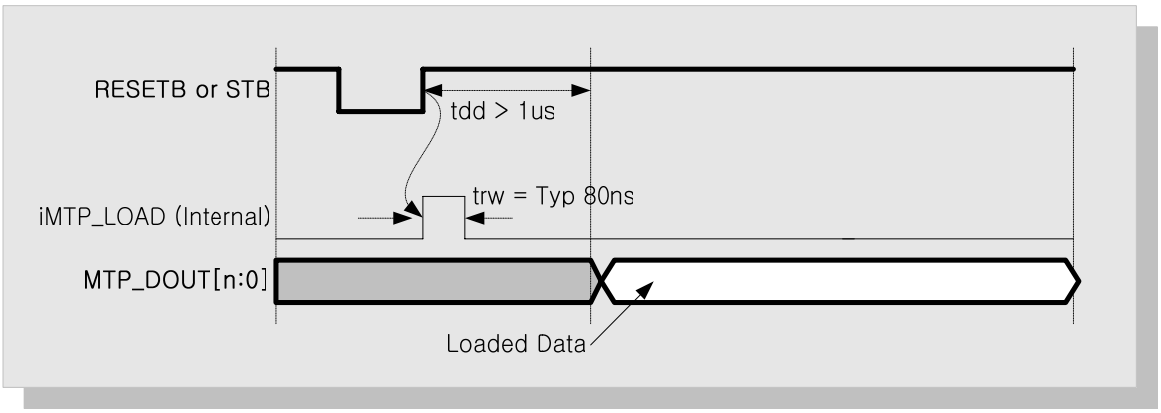


Figure18: Timing of MTP Load

Preliminary

GPIO CONTROL (R66h/R67h/R68h/R69h/R6Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
W	1	X	X	X	X	X	X	GPIO_CON9	GPIO_CON8	GPIO_CON7	GPIO_CON6	GPIO_CON5	GPIO_CON4	GPIO_CON3	GPIO_CON2	GPIO_CON1	GPIO_CON0
W	1	X	X	X	X	X	X	GPCLR9	GPCLR8	GPCLR7	GPCLR6	GPCLR5	GPCLR4	GPCLR3	GPCLR2	GPCLR1	GPCLR0
W	1	X	X	X	X	X	X	GPIO_EN9	GPIO_EN8	GPIO_EN7	GPIO_EN6	GPIO_EN5	GPIO_EN4	GPIO_EN3	GPIO_EN2	GPIO_EN1	GPIO_EN0
W	1	X	X	X	X	X	X	GPPOL9	GPPOL8	GPPOL7	GPPOL6	GPPOL5	GPPOL4	GPPOL3	GPPOL2	GPPOL1	GPPOL0

*66h Initial Value = XXXX_XX00_0000_0000
*67h Initial Value = XXXX_XX00_0000_0000
*68h Initial Value = XXXX_XX00_0000_0000
*69h Initial Value = XXXX_XX00_0000_0000
*6Ah Initial Value = XXXX_XX11_1111_1111

GPIO: GPIO value. When GPIO is input mode, GPIO value is set to the register.
GPIO_CON: Control of GPIO, When GPIO_CON is “0”, then GPIO is input mode, and when “1”, then GPIO is output mode
GPCLR: After client is wakeup, GPIO
GPIO_EN: When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.
GPPOL: If the bit is set to “1”, GPIO interrupt happens at rising edge of GPIN, If set to “0”, it happens at falling edge.

For more information about these registers, refer to GPIO CONTROL section

GAMMA CONTROL (R70h to R78h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	CR56	CR55	CR54	CR53	CR52	CR51	CR50	X	X	X	CR03	CR02	CR01	CR00
W	1	X	X	CG56	CG55	CG54	CG53	CG52	CG51	CG50	X	X	X	CG03	CG02	CG01	CG00
W	1	X	X	CB56	CB55	CB54	CB53	CB52	CB51	CB50	X	X	X	CB03	CB02	CB01	CB00
W	1	X	X	CR15	CR14	CR13	CR12	CR11	CR10	X	X	CR25	CR24	CR23	CR22	CR21	CR20
W	1	X	X	CR35	CR34	CR33	CR32	CR31	CR30	X	X	CR45	CR44	CR43	CR42	CR41	CR40
W	1	X	X	CG15	CG14	CG13	CG12	CG11	CG10	X	X	CG25	CG24	CG23	CG22	CG21	CG20
W	1	X	X	CG35	CG34	CG33	CG32	CG31	CG30	X	X	CG45	CG44	CG43	CG44	CG41	CG40
W	1	X	X	CB15	CB14	CB13	CB12	CB11	CB10	X	X	CB25	CB24	CB23	CB22	CB21	CB20
W	1	X	X	CB35	CB34	CB33	CB32	CB31	CB30	X	X	CB45	CB44	CB43	CB42	CB41	CB40

These registers set the one of the 9 gamma sets according to GS_SEL[3:0]

CR5[6:0]: The amplitude adjust register
CR4[4:0]: The amplitude adjust register
CR3[4:0]: The amplitude adjust register
CR2[4:0]: The amplitude adjust register
CR1[4:0]: The amplitude adjust register
CR0[3:0]: The amplitude adjust register
CG5[6:0]: The amplitude adjust register
CG4[4:0]: The amplitude adjust register
CG3[4:0]: The amplitude adjust register
CG2[4:0]: The amplitude adjust register
CG1[4:0]: The amplitude adjust register
CG0[3:0]: The amplitude adjust register
CB5[6:0]: The amplitude adjust register
CB4[4:0]: The amplitude adjust register
CB3[4:0]: The amplitude adjust register
CB2[4:0]: The amplitude adjust register
CB1[4:0]: The amplitude adjust register
CB0[3:0]: The amplitude adjust register

For details, see the GAMMA ADJUSTMENT FUNCTION.

GAMMA SELECT (R80h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	GS_SEL3	GS_SEL2	GS_SEL1	GS_SEL0

*80h Initial Value = XXXX_XXXX_XXXX_0100

Selects the gamma set controlled by 70H ~ 78H

Preliminary

RESET FUNCTION

The S6E63D6 is initialized internally by RESET input. The reset input should be held 'L' for at least 10us. Do not access the GRAM nor initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

INSTRUCTION SET INITIALIZATION

1. Display duty control (R01h) : FP3_0=1000, BP3_0=1000, NL5_0=10_1000
2. RGB interface control (R02h) : RM=0, DM=0, RIM1_0=00, VSPL=0, HSPL=0, EPL=0, DPL=0
3. Entry mode (R03h) : CLS=0, MDT1_0=00, BGR=0, SS=0, ID1_0=11, AM=0
4. Clock control (R04h) : DCR1_0=00
5. Display control 1 (R05h) : DISP_ON=0
6. Display control 2 (R06h) : CL=0, TEMON=0, REV=0
7. Panel interface control 1 (R07h) : CLWEA4_0=0_1100
8. Panel interface control 2 (R08h) : CLWEB4_0=0_1100, CLWEC4_0=0_1100
9. Panel interface control 3 (R09h) : SCTE3_0=1000, SCWE3_0=0101, SHE2_0=001, CLTE2_0=010
10. Panel interface control 4 (R0Ah) : GTCON1_0=00
11. Stand by (R10h) : STB=1
12. Power gen 1 (R12h) : VC3_0=1000
13. Power gen 2 (R13h) : VINT3_0=0101, VGH3_0=0011, VGL3_0=1010
14. Power step up control 1 (R14h) : DC22_0=100, DC12_0=010, BT1_0=00
15. Start oscillation (R18h) : RADJ5_0=01_1111
16. Source driver control (R1Ah) : GAMMA_TEST=0, SDUM_ON=0, SAP2_0=101
17. GRAM address set (R20h) : AD7_0=0000_0000
18. GRAM address set (R21h) : AD16_8=0_0000_0000
19. Vertical scroll control 1 (R30h, R31h) : SSA8_0=0_0000_0000, SEA8_0=1_0011_1111
20. Vertical scroll control 2 (R32h) : SST8_0=0_0000_0000
21. Partial screen driving position (R33h, R34h) : SS18_0=0_0000_0000, SE18_0=1_0011_1111
22. Vertical RAM address position (R35h, R36h) : VSA8_0=0_0000_0000, VEA8_0=1_0011_1111
23. Horizontal RAM address position (R37h) : HAS7_0=0000_0000, HEA7_0=1110_1111
24. Client initiated wake up (R38h) : VWAKE_EN=0
25. MDDI link wake up start position (R39h) : WKL8_0=0_0000_0000, WKF3_0=0000
26. Sub panel control 1(R3Ah, R3Bh) : SUB_SEL7_0=0111_1010, SUB_WR7_0=0010_0010
27. Sub panel control 2 (R3Ch) : FCV_EN=0, MPU_MODE=0, STN_EN=0, SUB_IM1_0=00
28. MTP control (R61h) : MTP_WRB=1, MTP_SEL=1, MTP_ERB=1
29. MTP register setting 1 (R62h) : R21_DK2_0=000, R21_BT2_0=000, R63_DK3_0=0000, R63_BT3_0=0000
30. MTP register setting 2 (R63h) : G21_DK2_0=000, G21_BT2_0=000, G63_DK3_0=0000, G63_BT3_0=0000
31. MTP register setting 3 (R64h) : B21_DK2_0=000, B21_BT2_0=000, B63_DK3_0=0000, B63_BT3_0=0000
32. MTP register setting 4 (R65h) : E_OST2_0=000
33. GPIO control (R66h, R67h, R68h. R69h, R6Ah) : GPIO9_0=00_0000_0000, GPIO_CON9_0=00_0000_0000
    GPCLR9_0=00_0000_0000, GPIO_EN9_0=00_0000_0000, GPPOL9_0=11_1111_1111

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POWER SUPPLY

PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.

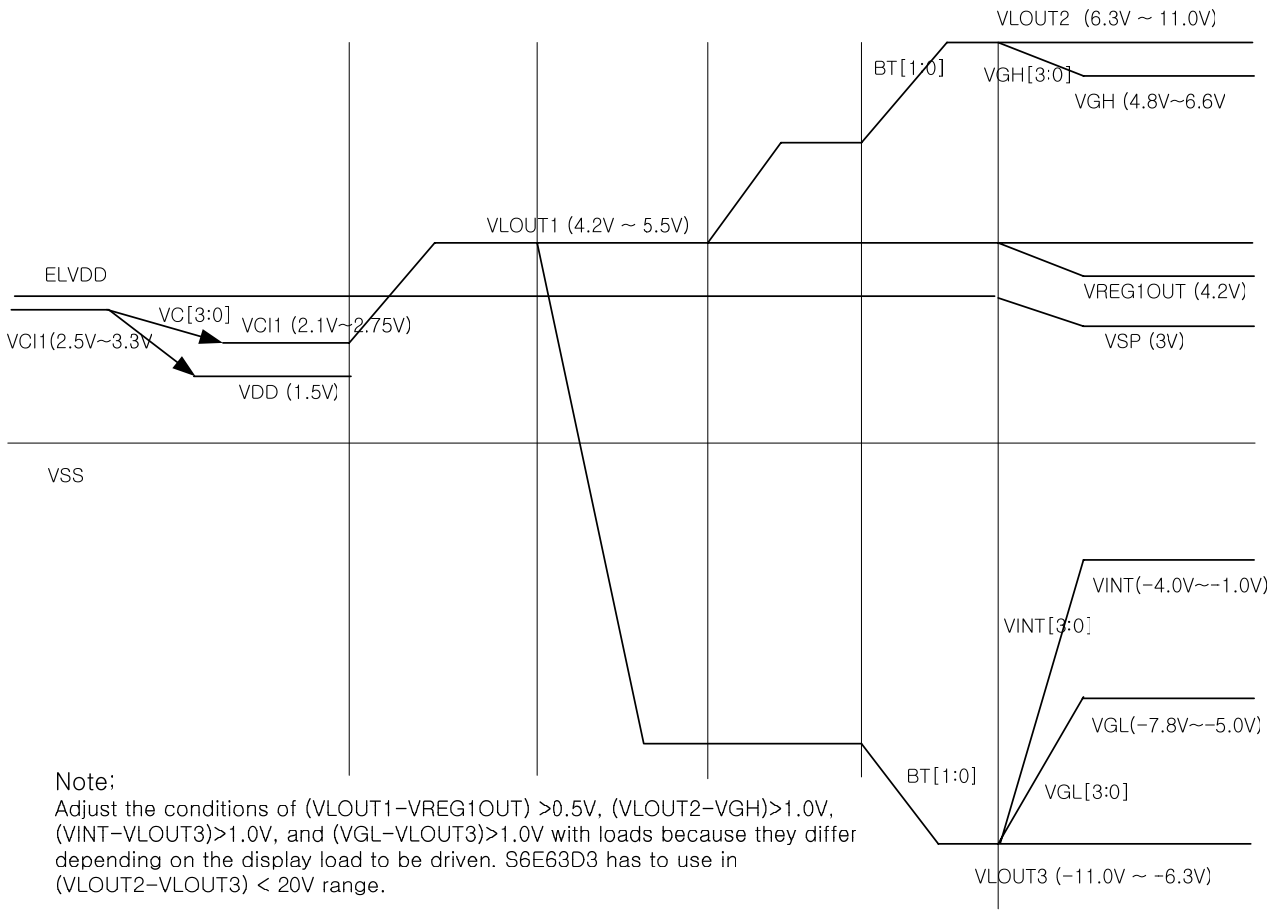

Figure19: Pattern Diagram for Voltage Setting

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VOLTAGE REGULATION FUNCTION

The S6E63D6 has the internal voltage regulator. By the use of this function, unexpected damages on internal logic circuit can be avoided. Furthermore, power consumption can also be obtained. Detailed function description and application configuration is described in the following diagram.

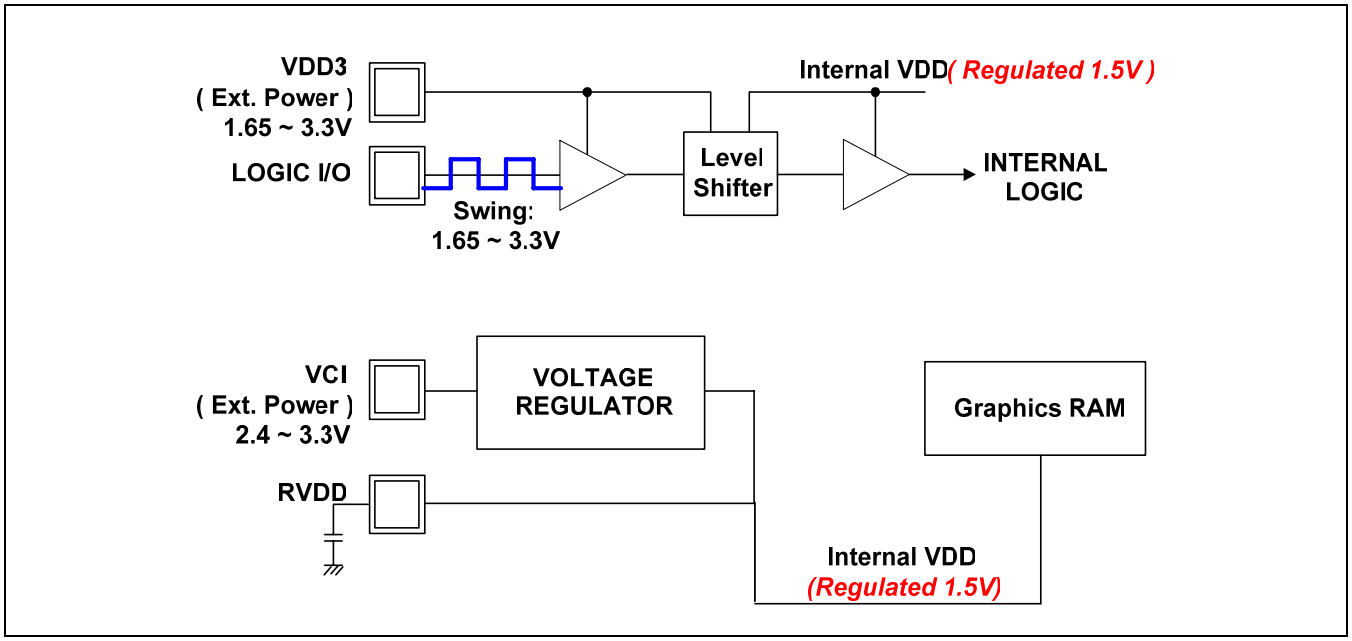

Figure20: Voltage Regulation Function

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INTERFACE SPECIFICATION

The S6E63D6 incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display motion pictures. Selecting these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The external display interface includes RGB interface. This allows flicker-free screen update.
When RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The display data (DB17-0) is written according to the values of the data enable signal (ENABLE) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. In addition, using the window address function enables rewriting only to the internal RAM area to display motion pictures. Using this function also enables simultaneously display of the motion picture area and the RAM data that was written.

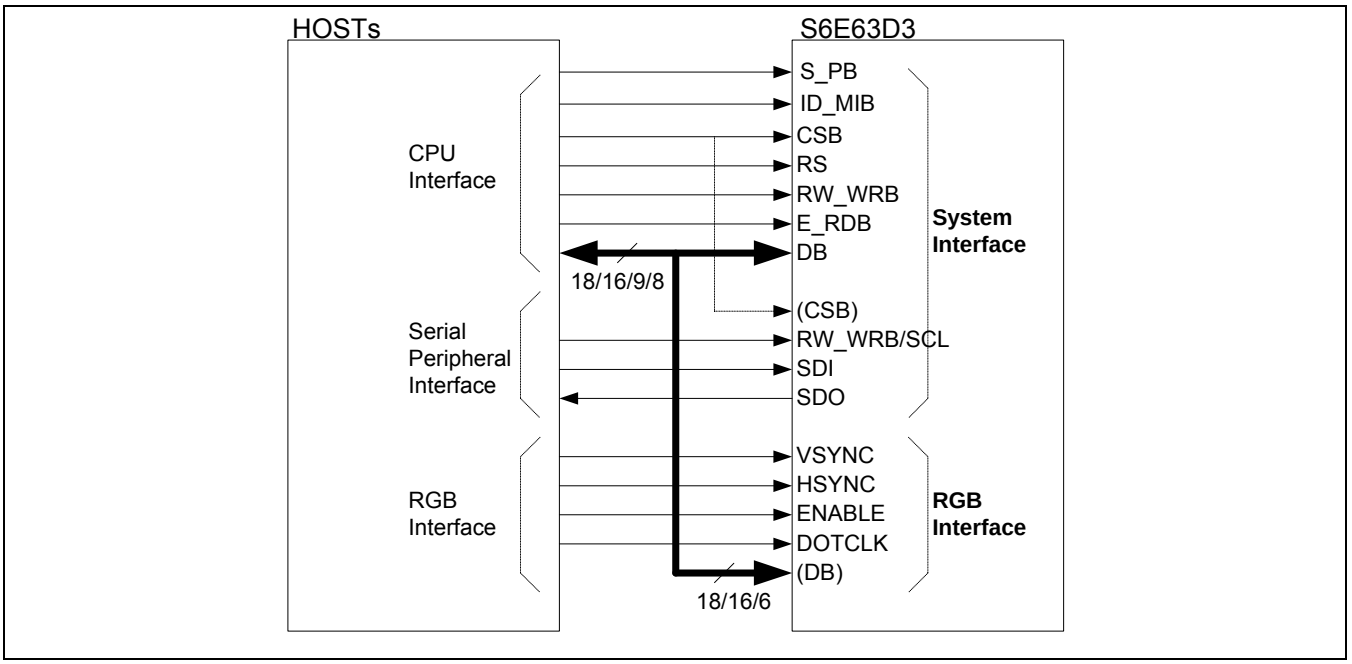

Figure21: System Interface and RGB Interface

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SYSTEM INTERFACE

S6E63D6 is enabling to set instruction and access to RAM by selecting S_PB, ID_MIB pins and Instruction in the system interface mode.

Table44: System Interface mode

Pins			Registers				
MDDI_EN	S_PB	ID_MIB	Index Address	Command (CLS)	Command MDT[1]	Command MDT[0]	Description
0	0 (Parallel)	0 (80 mode)	default & 24h (9/8bit)	0 (80 8bit)	0	x	80-system 8-bit 65k bus interface
					1	0	80-system 8-bit 260k bus interface
						1	80-system 8-bit 65k bus interface
				1(80 9bit)	x	X	80-system 9-bit 260k bus interface
			Index 23 h (18/16bit)	0 (80 16bit)	0	0	80-system 16-bit 65k bus interface
						1	80-system 16-bit 260k bus interface
					1	X	80-system 16-bit 260k bus interface
				1(80 18bit)	x	X	80-system 18-bit 260k bus interface
		1 (68 mode)	default & 24h (9/8bit)	0 (68 8bit)	0	X	68-system 8-bit 65k bus interface
					1	0	68-system 8-bit 260k bus interface
						1	68-system 8-bit 65k bus interface
				1 (68 9bit)	x	X	68-system 9-bit 260k bus interface
			Index 23 h (18/16bit)	0 (68 16bit)	0	0	68-system 16-bit 65k bus interface
						1	68-system 16-bit 260k bus interface
					1	x	68-system 16-bit 260k bus interface
				1 (68 18bit)	x	x	68-system 18-bit 260k bus interface
	1 (Serial)	ID	x	x	x	x	Serial peripheral interface (SPI)
1	x	x	x	x	x	x	

[NOTE] For details, see the ENTRY MODE (Instruction R03h).

We can select system interface mode by pins and instruction, don't care 8-/16-bit bus system after power on.

1. In case of 8/9-bit bus system.

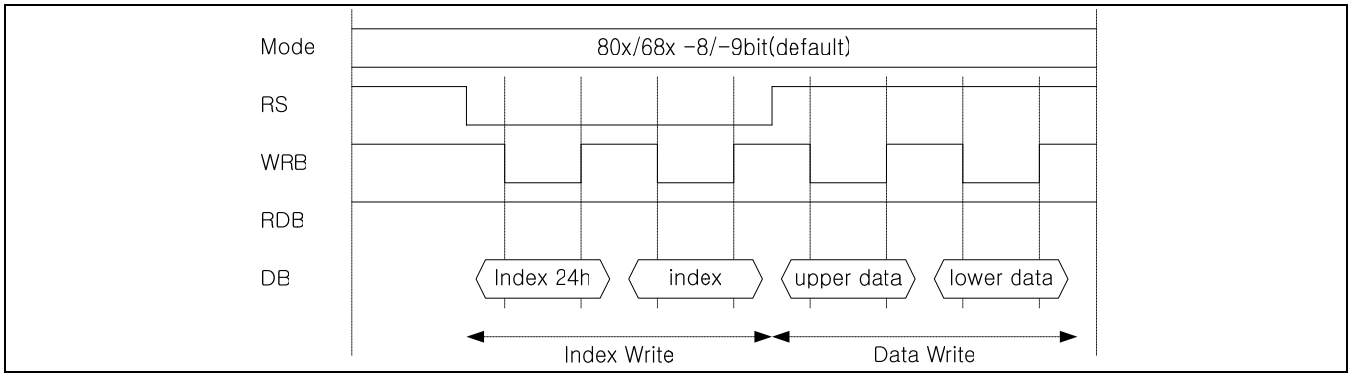

Figure21: 8/9-bit bus system

2. In case of 18/16-bit bus system

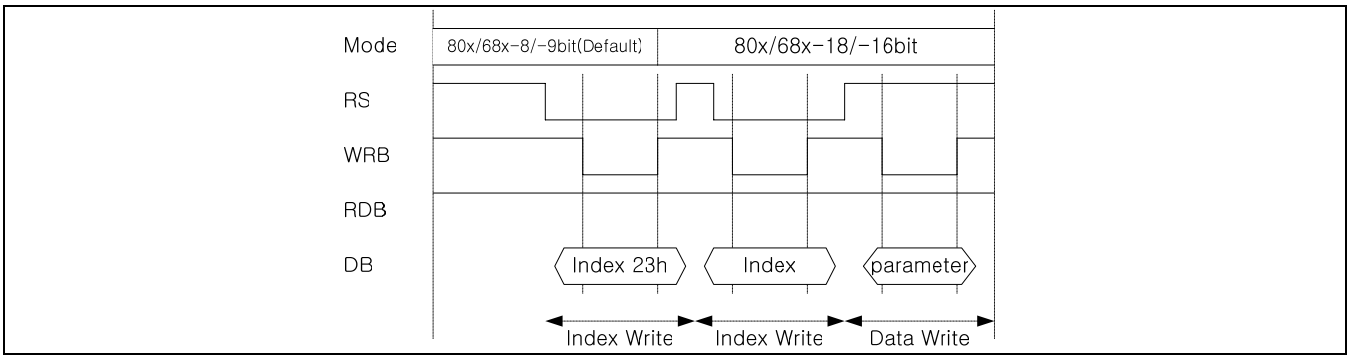

Figure22: 18/16-bit bus system

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68-SYSTEM 18-BIT BUS INTERFACE

Bit Assignment

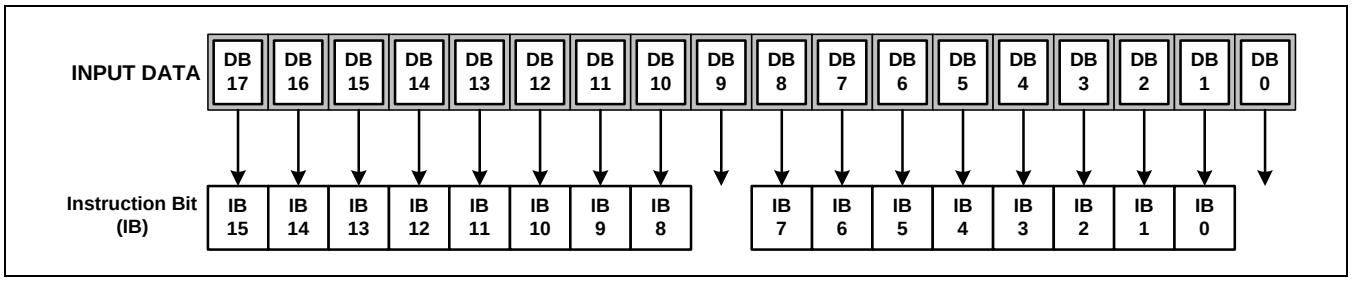

Figure23: Instruction Format For 18-Bit Interface

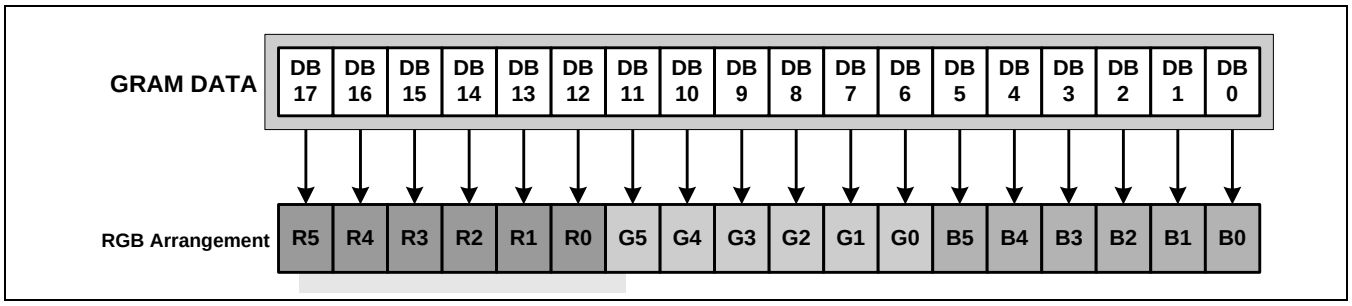

Figure24: RAM Data Write Format For 18-Bit Interface

Timing Diagram

There are 4 timing conditions for 68-system 18-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

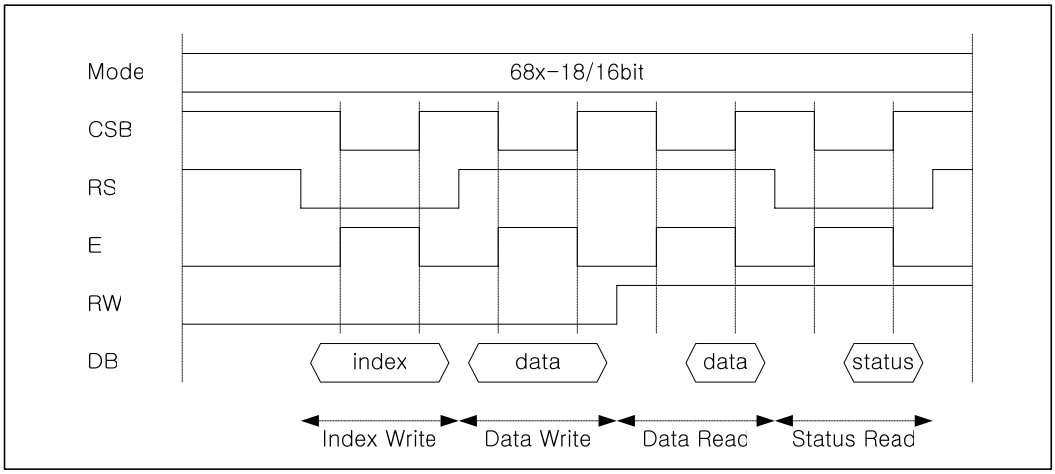

Figure25: Timing Diagram of 68-System 18-Bit bus interface

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68-SYSTEM 16-BIT BUS INTERFACE

Bit Assignment

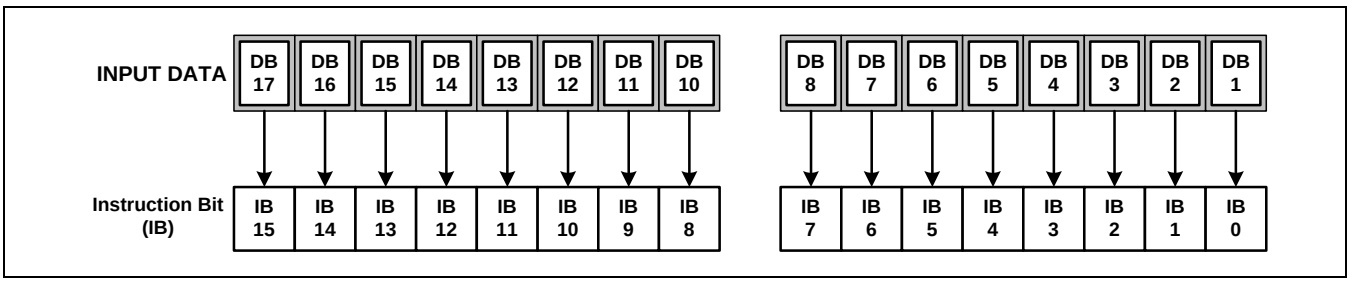

Figure26: Instruction Format For 16-Bit Interface

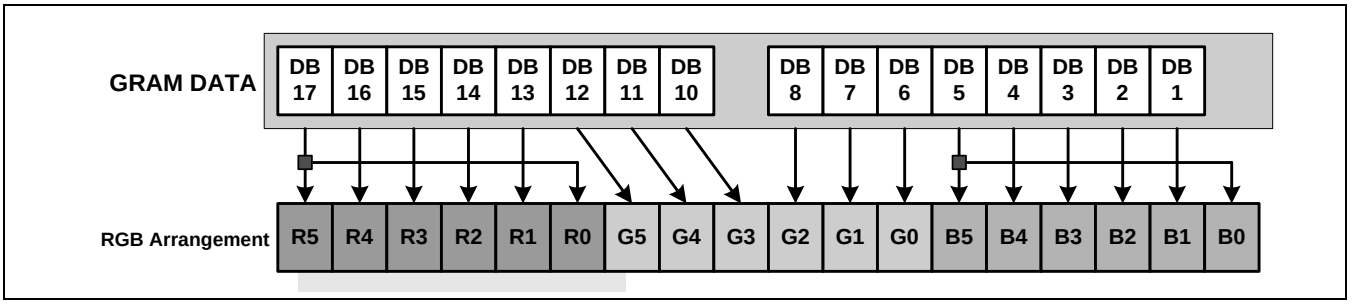

Figure27: RAM Data Write Format For 16-Bit Interface

Timing Diagram

There are 4 timing conditions for 68-system 16-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

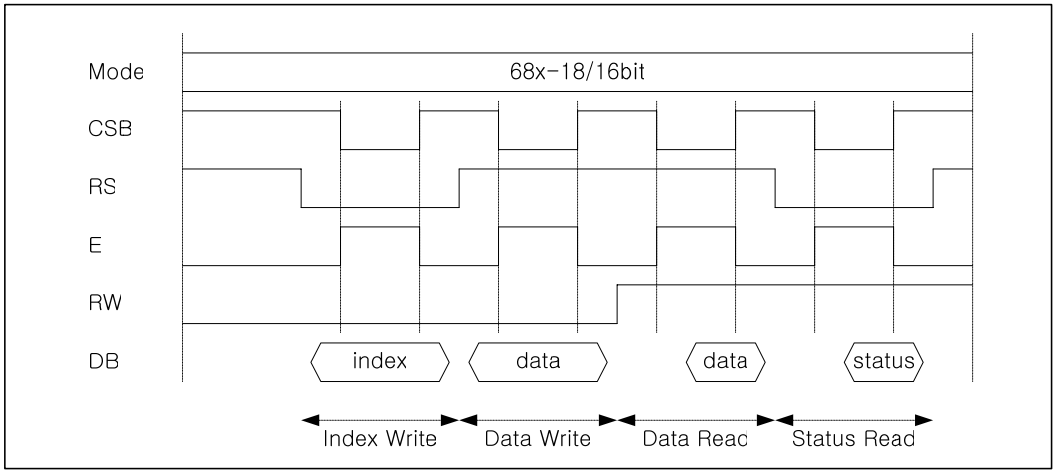

Figure28: Timing Diagram of 68-System 16-Bit bus interface

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68-SYSTEM 9-BIT BUS INTERFACE

Bit Assignment

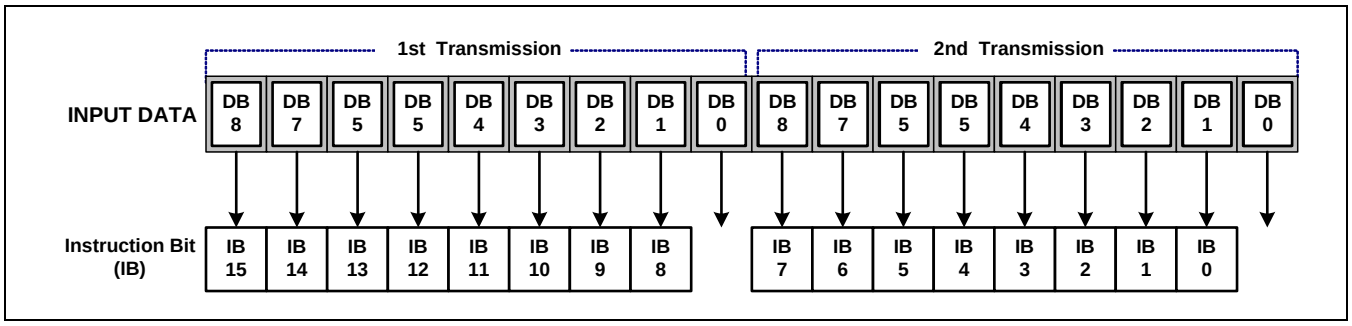

Figure29: Instruction Format For 9-Bit Interface

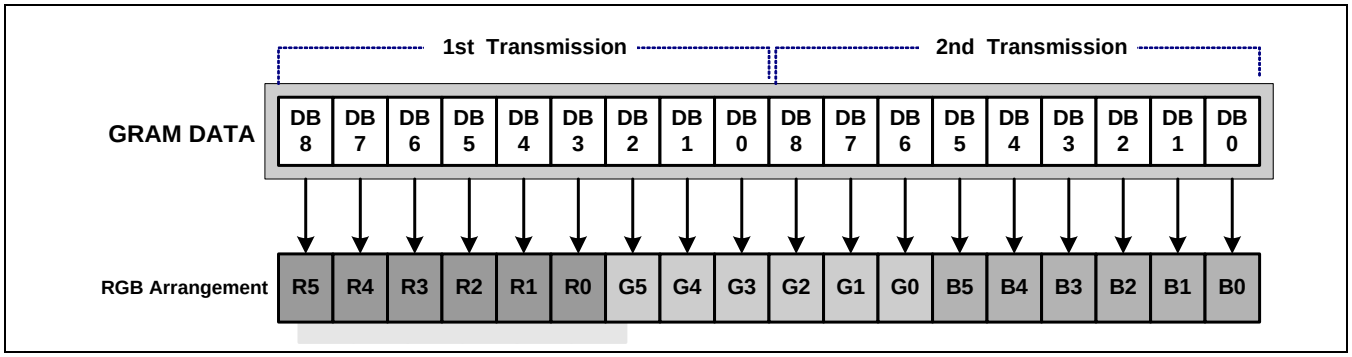

Figure30: RAM Data Write Format For 9-Bit Interface

Timing Diagram

There are 4 timing conditions for 68-system 9-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word. Note that the upper byte must also be written when the index register is written.

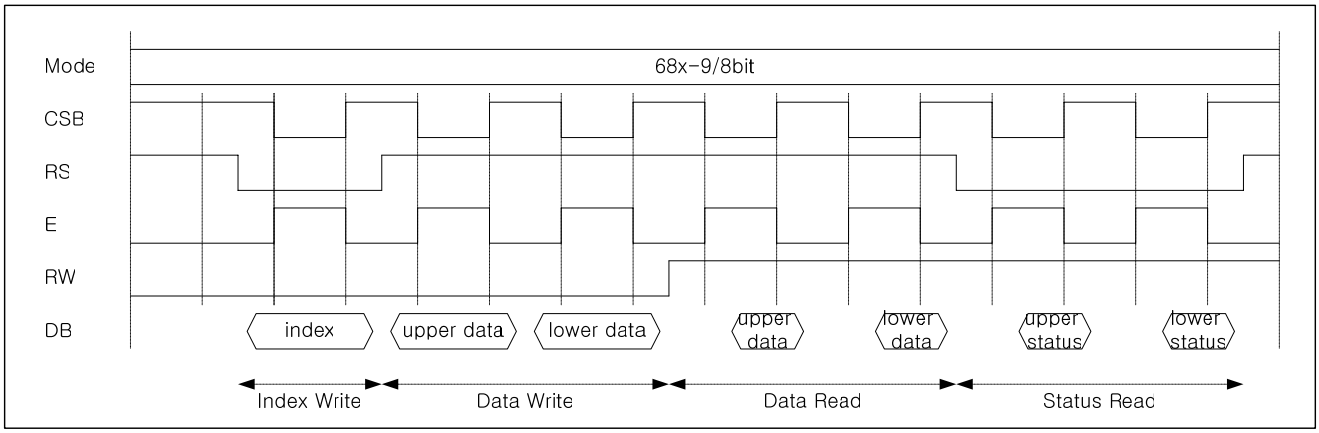

Figure31: Timing Diagram of 68-System 9-Bit bus interface

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68-SYSTEM 8-BIT BUS INTERFACE

Bit Assignment

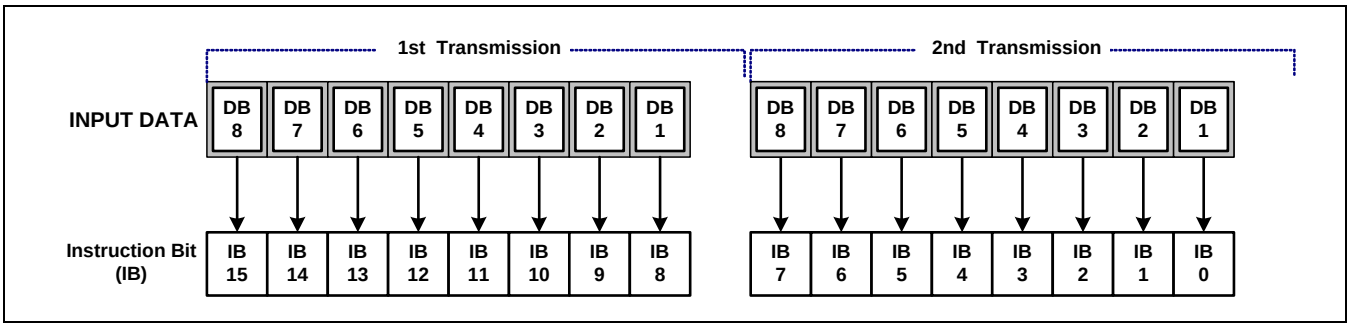

Figure32: Instruction Format For 8-Bit Interface

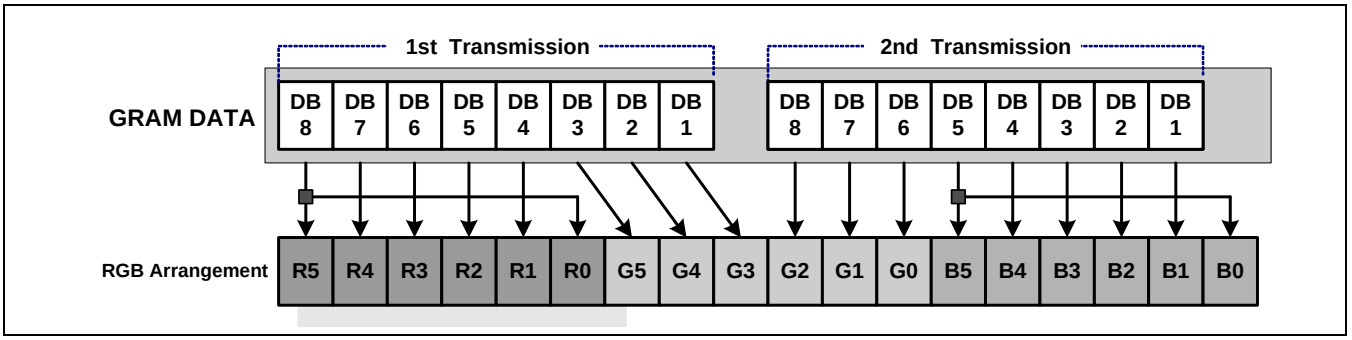

Figure33: RAM Data Write Format For 8-Bit Interface

Timing Diagram

There are 4 timing conditions for 68-system 8-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word. Note that the upper byte must also be written when the index register is written.

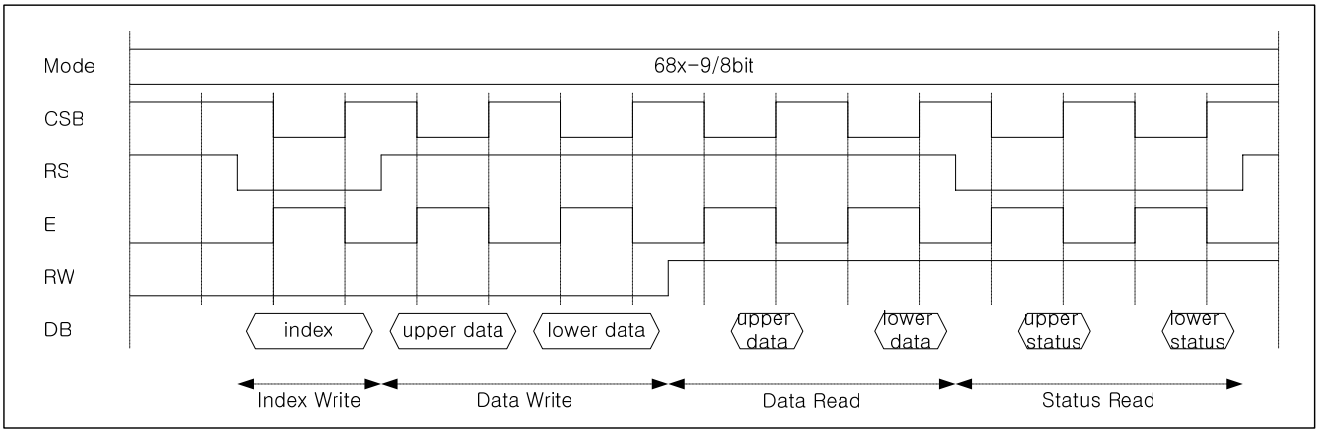

Figure34: Timing Diagram of 68-System 8-Bit bus interface

Preliminary

80-SYSTEM 18-BIT BUS INTERFACE

Bit Assignment

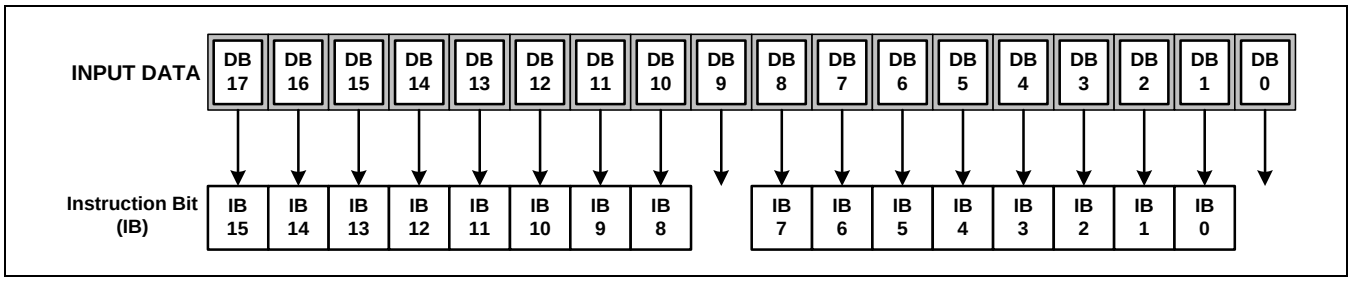

Figure35: Instruction Format For 18-Bit Interface

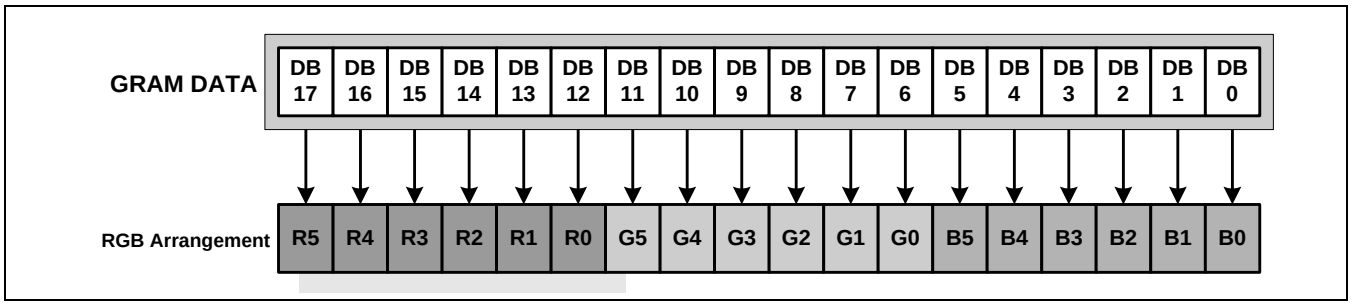

Figure36: RAM Data Write Format For 18-Bit Interface

Timing Diagram

There are 4 timing conditions for 80-system 18-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

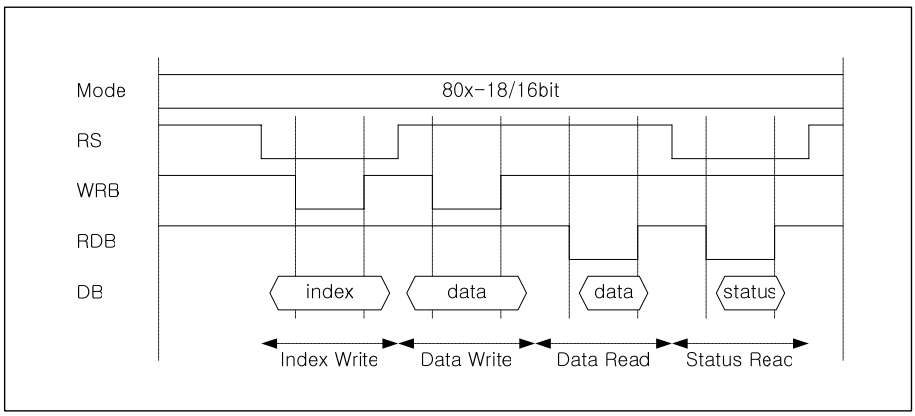

Figure37: Timing Diagram of 80-System 18-Bit bus interface

Preliminary

80-SYSTEM 16-BIT BUS INTERFACE

Bit Assignment

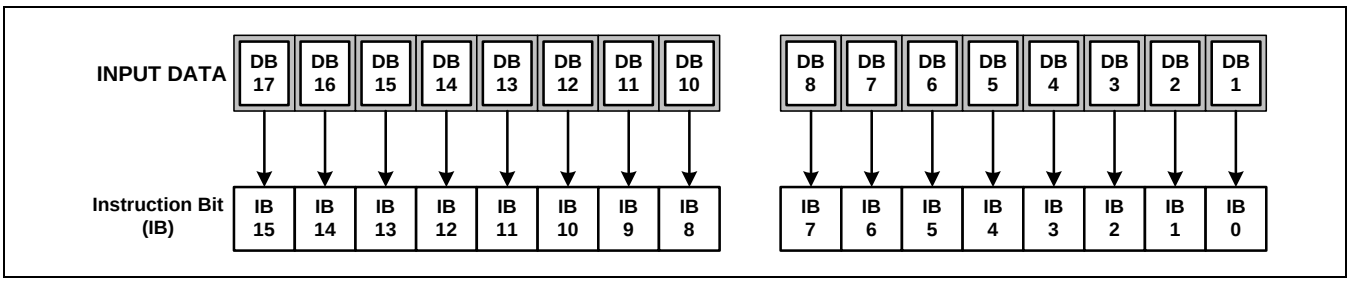

Figure38: Instruction Format For 16-Bit Interface

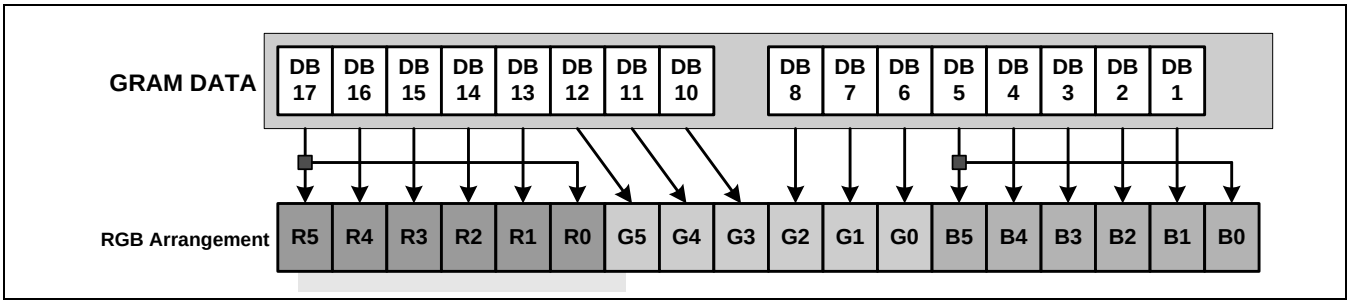

Figure39: RAM Data Write Format For 16-Bit Interface

Timing Diagram

There are 4 timing conditions for 80-system 16-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

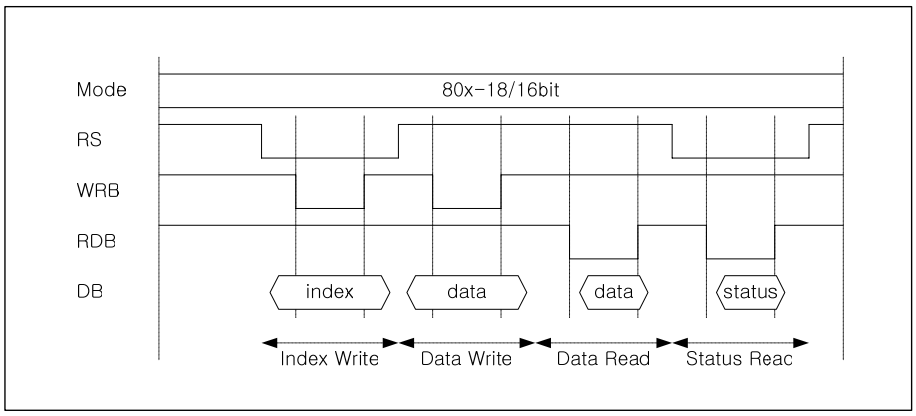

Figure40: Timing Diagram of 80-System 16-Bit bus interface

Preliminary

80-SYSTEM 9-BIT BUS INTERFACE

Bit Assignment

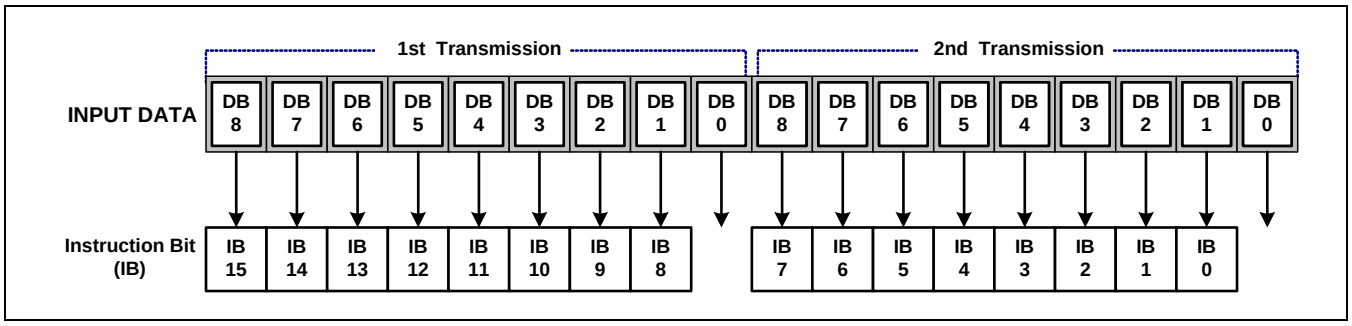

Figure41: Instruction Format For 9-Bit Interface

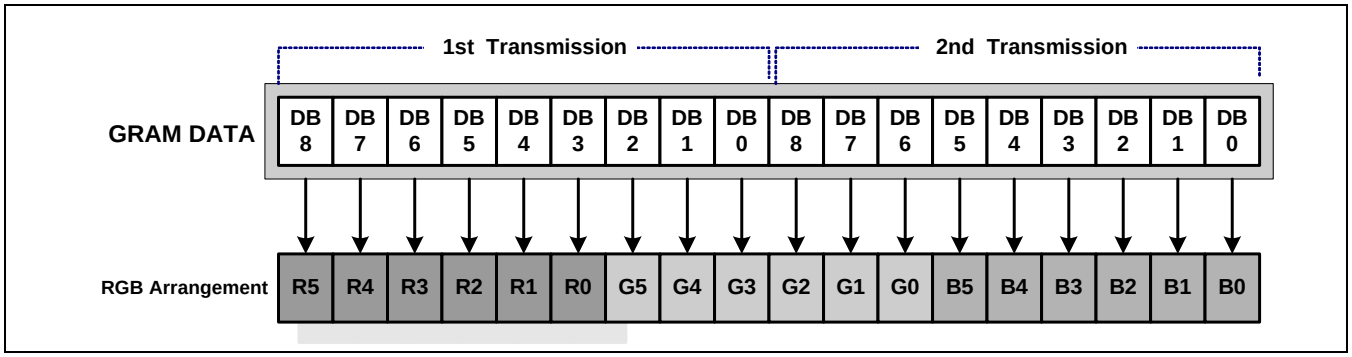

Figure42: RAM Data Write Format For 9-Bit Interface

Timing Diagram

There are 4 timing conditions for 80-system 9-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word. Note that the upper byte must also be written when the index register is written.

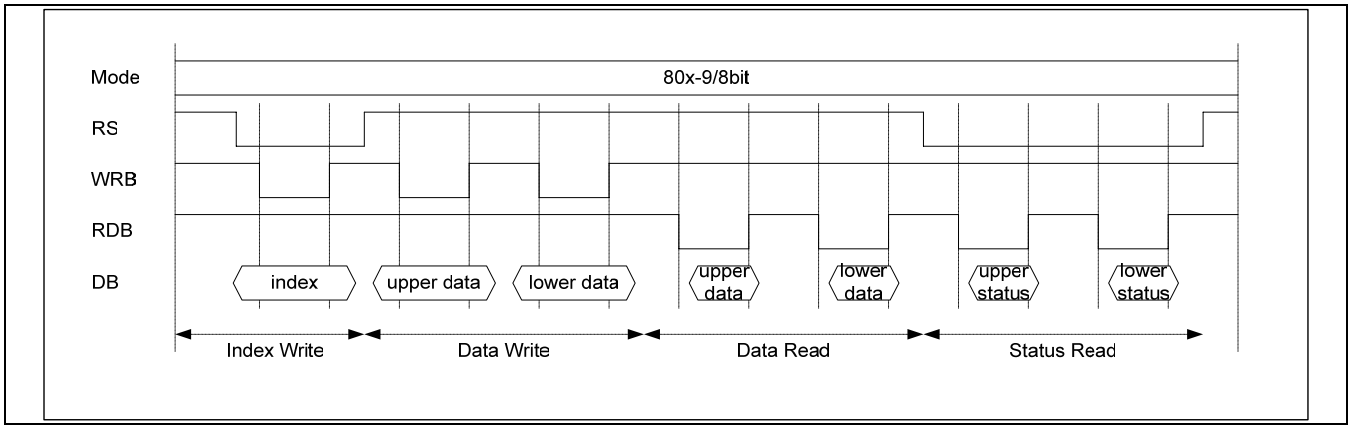

Figure43: Timing Diagram of 80-System 9-Bit bus interface

Preliminary

80-SYSTEM 8-BIT BUS INTERFACE

Bit Assignment

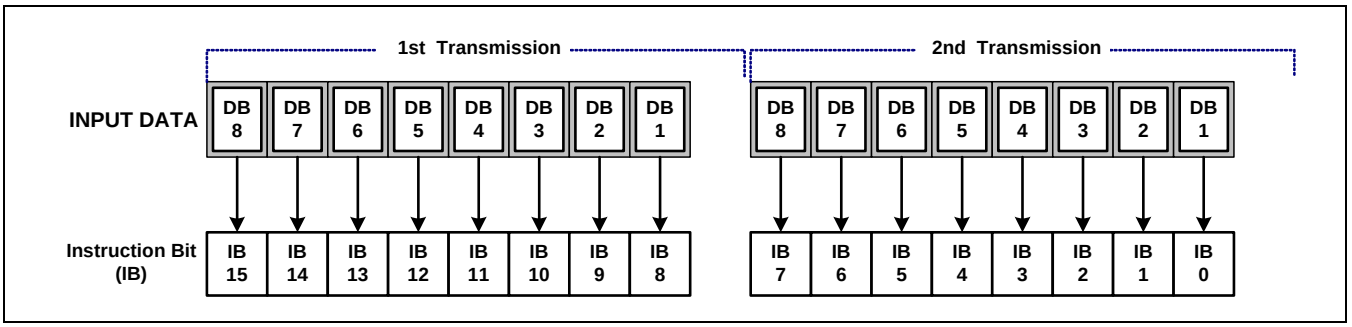

Figure44: Instruction Format For 8-Bit Interface

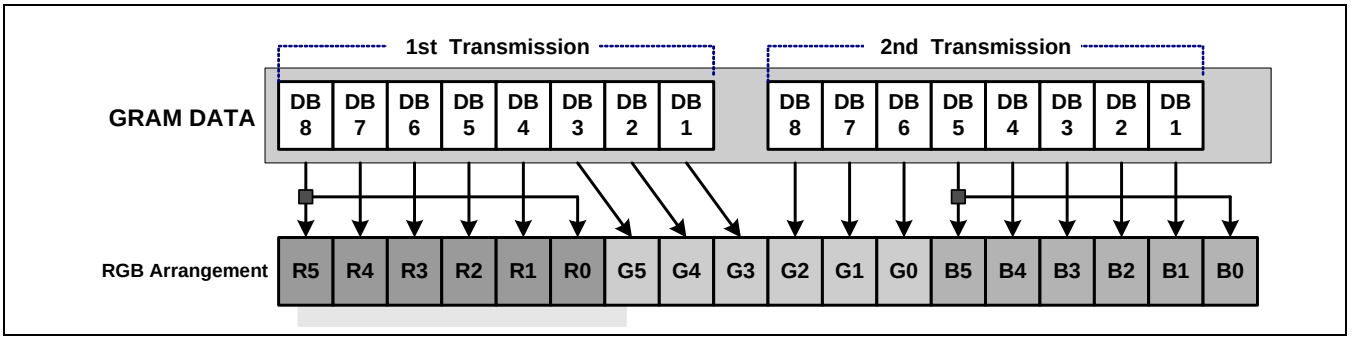

Figure45: RAM Data Write Format For 8-Bit Interface

Timing Diagram

There are 4 timing conditions for 80-system 8-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word. Note that the upper byte must also be written when the index register is written.

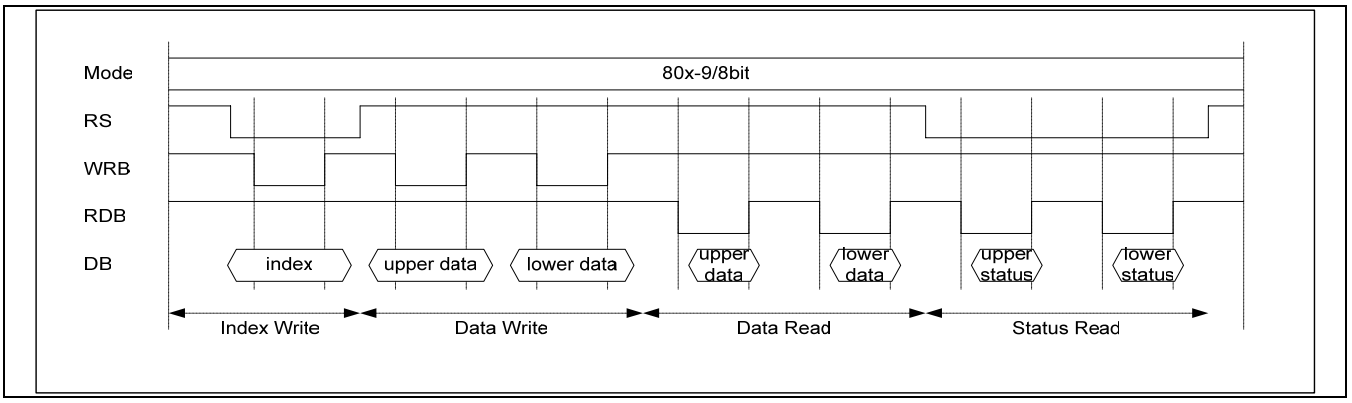

Figure46: Timing Diagram of 80-System 8-Bit bus interface

Preliminary

68-/80-SYSTEM 8-/9-BIT INTERFACE SYNCHRONIZATION FUNCTION

The S6E63D6 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-/9-bit data transfer in the 8-/9-bit bus interface. Noise causing transfer mismatch between the upper and lower bits can be corrected by a reset triggered by writing a “22h” instruction. The next transfer starts from the upper bits. Executing synchronization function periodically can recover any runaway in the display system.

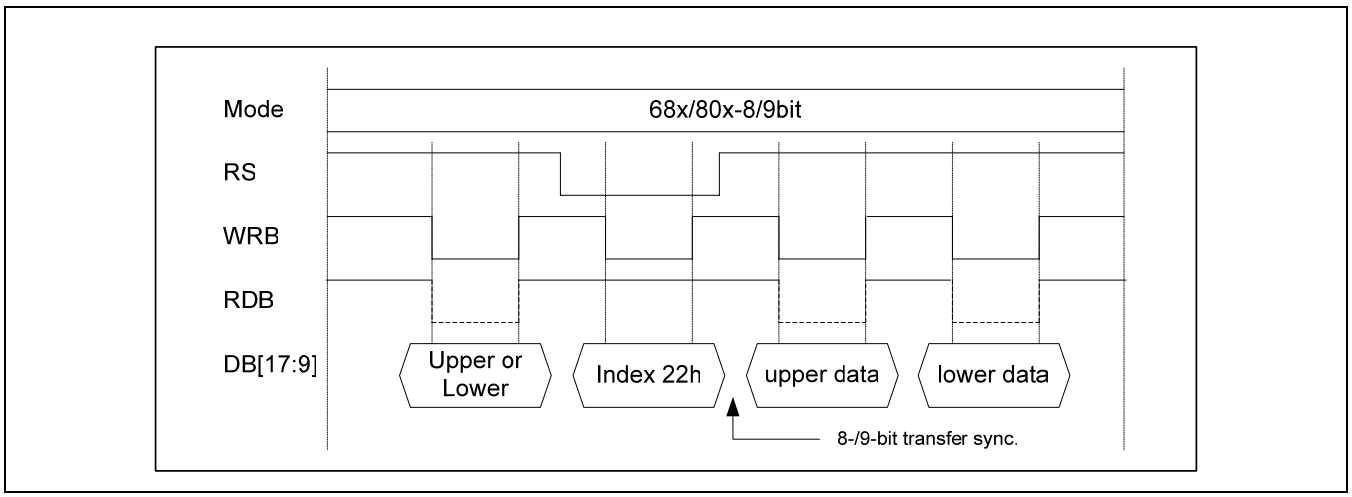

Figure47: 8-/9-bit Interface Transfer Synchronization

Preliminary

SERIAL PERIPHERAL INTERFACE

Setting the S_PB pin to the VDD3 level allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-0 pins are used only data bus of RGB Interface.

The S6E63D6 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

The S6E63D6 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the S6E63D6. When selected, the S6E63D6 receives the subsequent data string. The least significant bit (LSB) of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single S6E63D6 because the seventh bit of the start byte is used as a register select bit (RS). That is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write operation is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the S6E63D6 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All S6E63D6 instructions are 16 bits. Two bytes are received with the MSB first (DB17 to DB0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The S6E63D6 starts to read correct RAM data from the fifth byte.

Table45: Start Byte Format

Transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

NOTE: ID bit is selected by the ID_MIB pin.

Table46: RS and R/W Bit Function

RS	R/W	Function
0	0	Set index register
0	1	Read status

Bit Assignment

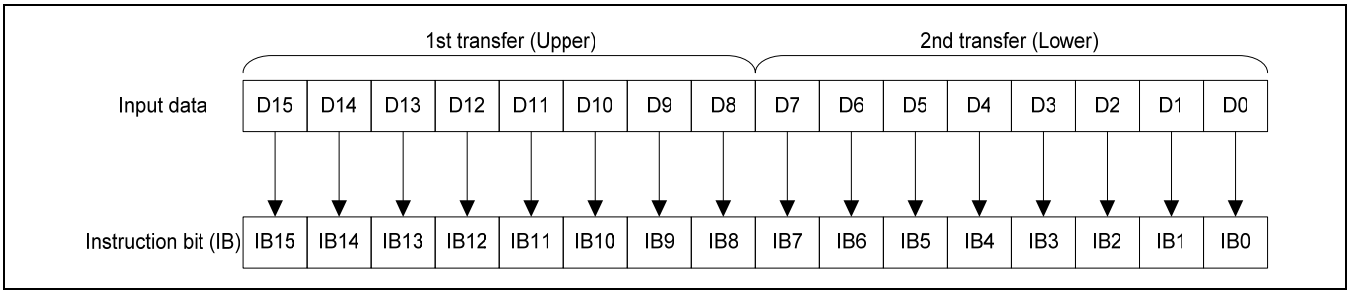

Figure48: Bit Assignment of Instructions on SPI

Preliminary

Timing Diagram

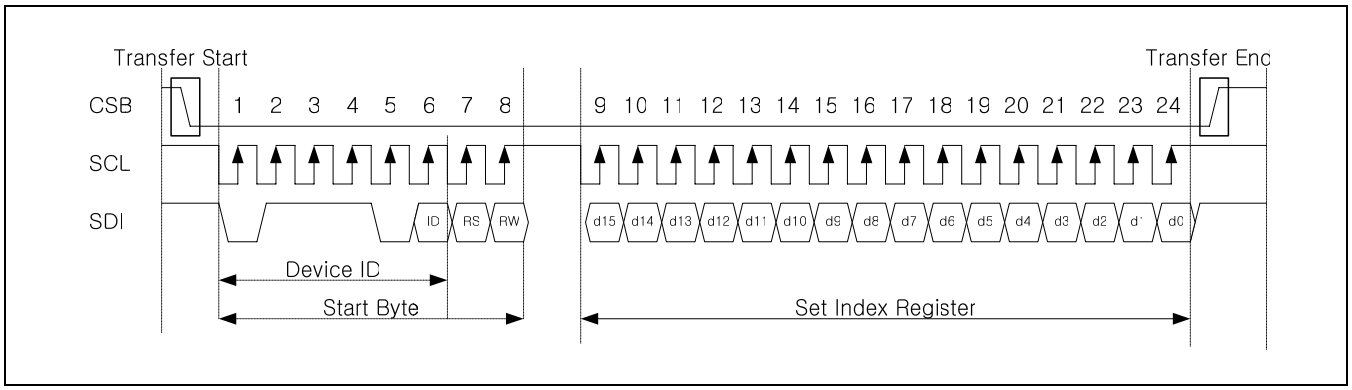

Figure49: Basic Timing Diagram of Register Data Transfer through SPI

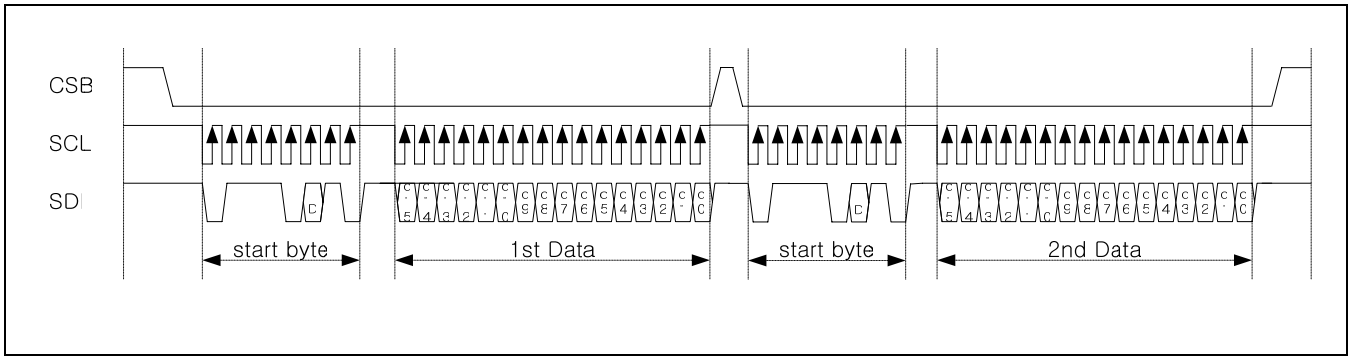

Figure50: Timing Diagram of Consecutive Register Data-Write through SPI

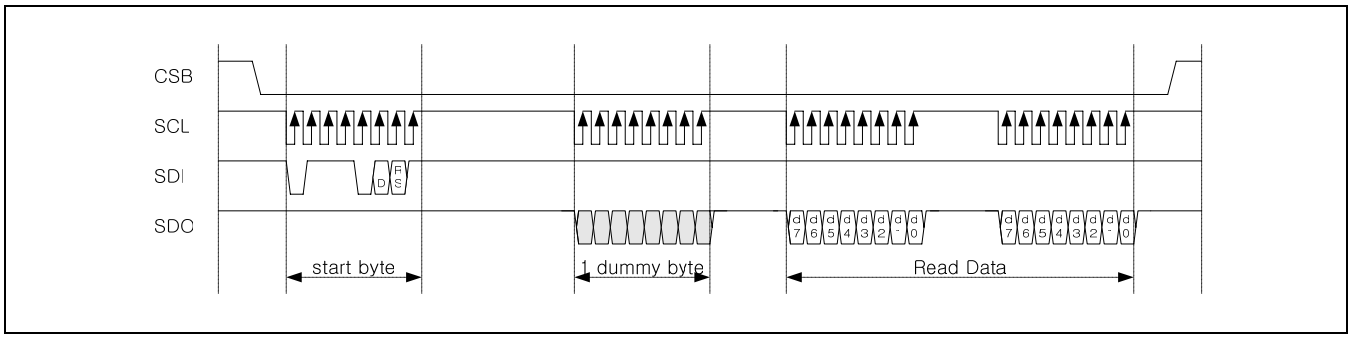

Figure51: Timing Diagram of Register Read through SPI

Preliminary

INDEX AND PARAMETER RECOGNITION

If more parameter command is being sent, exceed parameters are ignored.

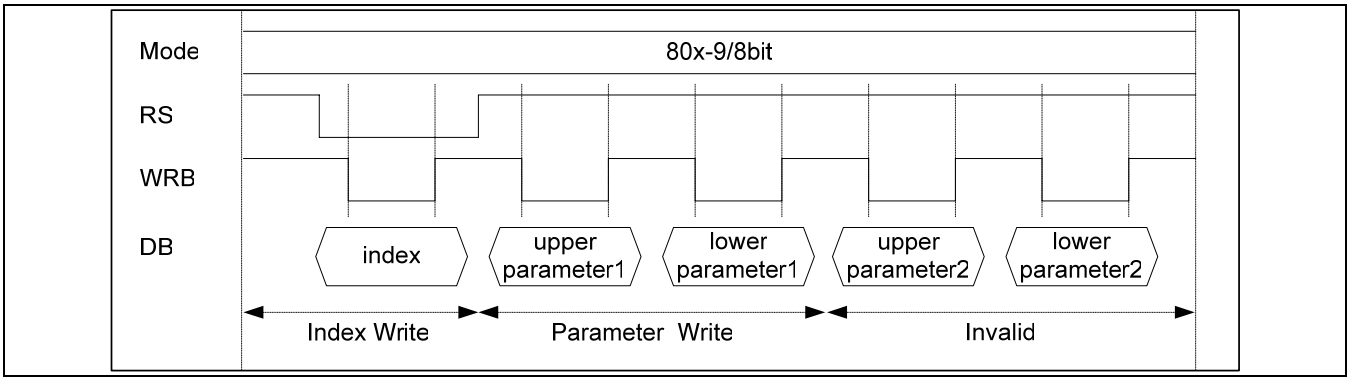

Figure52: Index and parameter recognition with 8-/9-bit interface

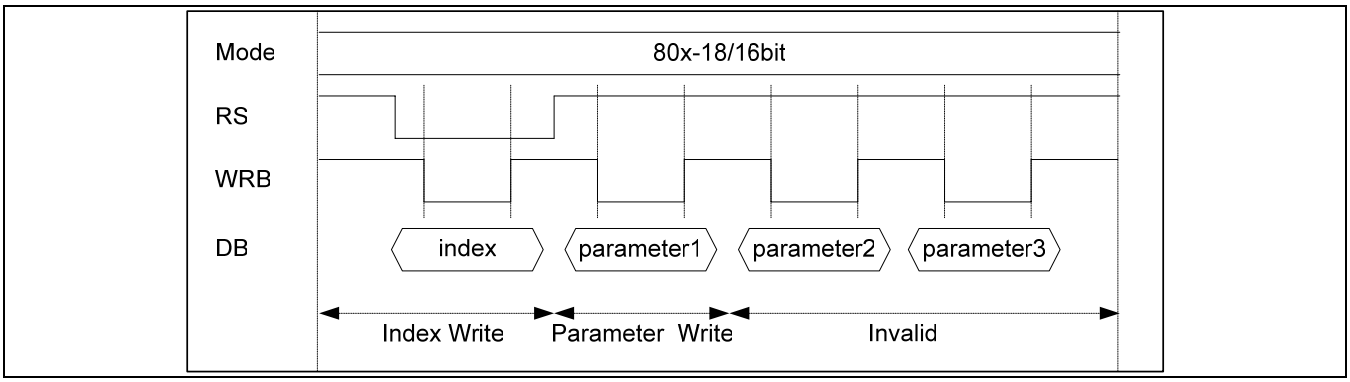

Figure53: Index and parameter recognition with 18-/16-bit interface

Preliminary

EXTERNAL DISPLAY INTERFACE

The following interfaces are available as external display interface. It is determined by bit setting of RIM1-0. RAM accesses can be performed via the RGB interface.

Table47: RIM Bits

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17 to 0
0	1	16-bit RGB interface	DB17 to10, 8 to 1
1	0	6-bit RGB interface	DB8 to3
1	1	Setting disabled	

ENABLE SIGNAL

The relationship between EPL and ENABLE signals is shown below. When ENABLE is not active, the address is not updates. When ENABLE is active, the address is updated.

Table48: Relationship between EPL and ENABLE

EPL	ENABLE	RAM WRITE	RAM ADDRESS
0	0	Valid	Updated
0	1	Invalid	Hold
1	0	Invalid	Hold
1	1	Valid	Update

Preliminary

18-Bit RGB interface

Bit Assignment

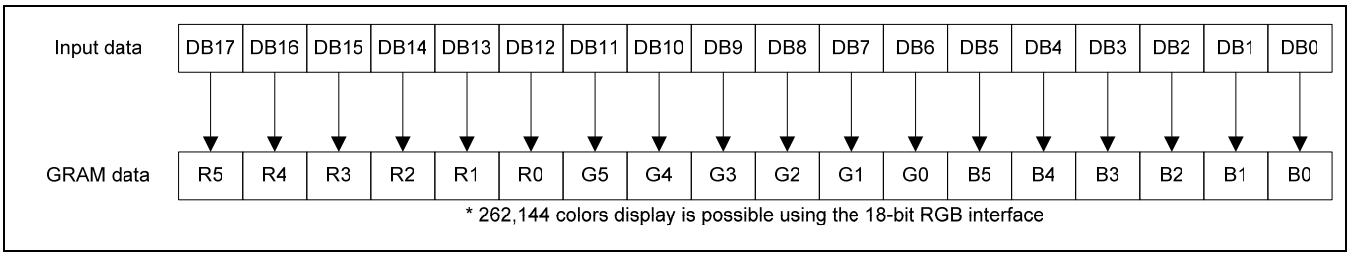

Figure54: Bit Assignment of GRAM Data on 18bit RGB Interface

16-Bit RGB interface

Bit Assignment

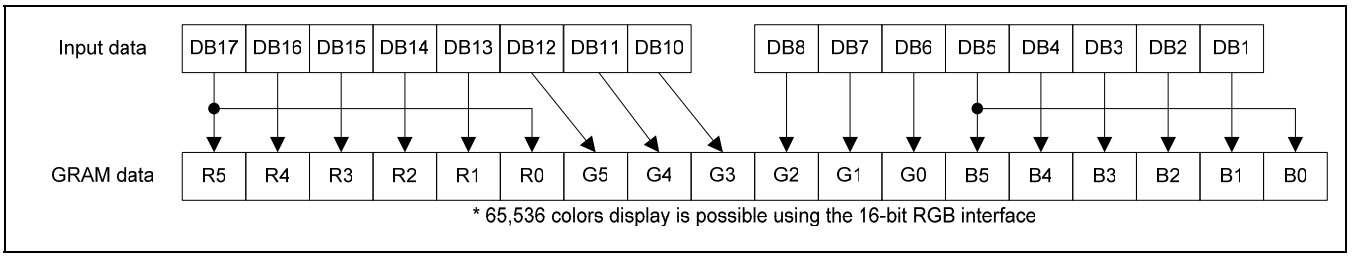

Figure55: Bit Assignment of GRAM Data on 16bit RGB Interface

Timing Diagram

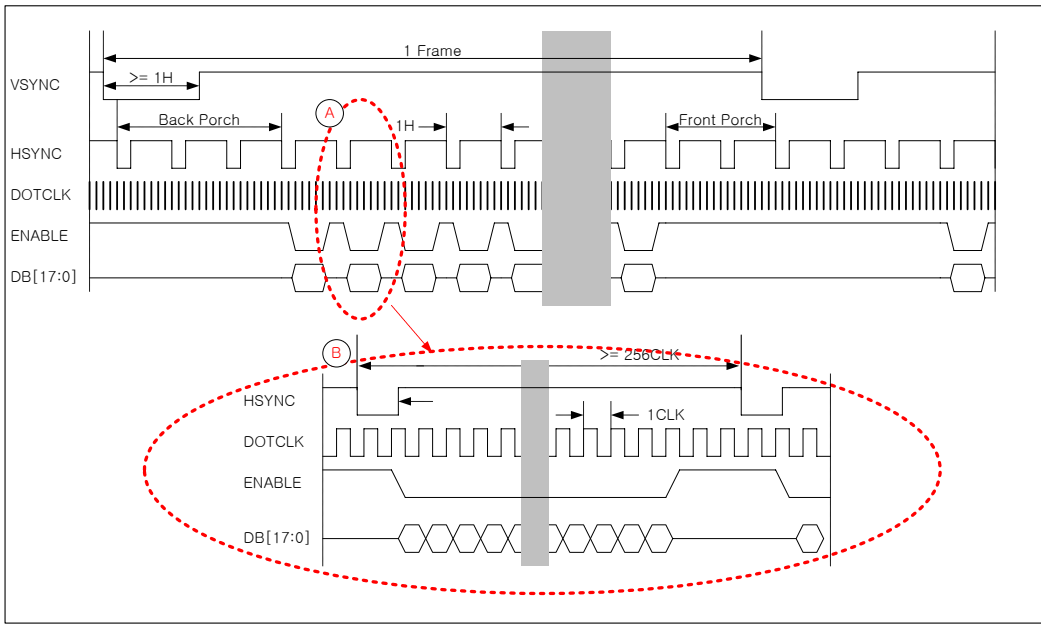

Figure56: Timing Diagram of 18/16bit RGB Interface

[NOTE] 1. 1 HSYNC Period must be >= 256 DOTCLK

Preliminary

6-Bit RGB interface

In order to transfer data on 6bit RGB Interface there should be three transfers.

Bit Assignment

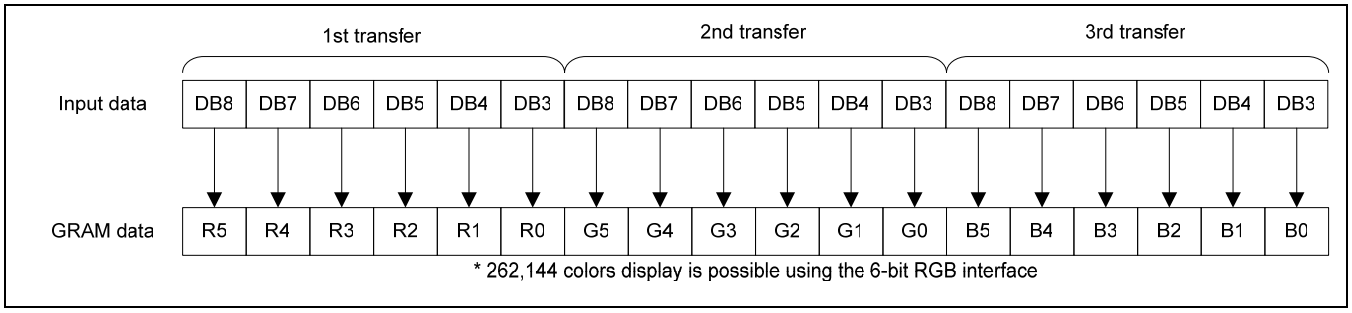

Figure57: Bit Assignment of GRAM Data on 6bit RGB Interface

Timing Diagram

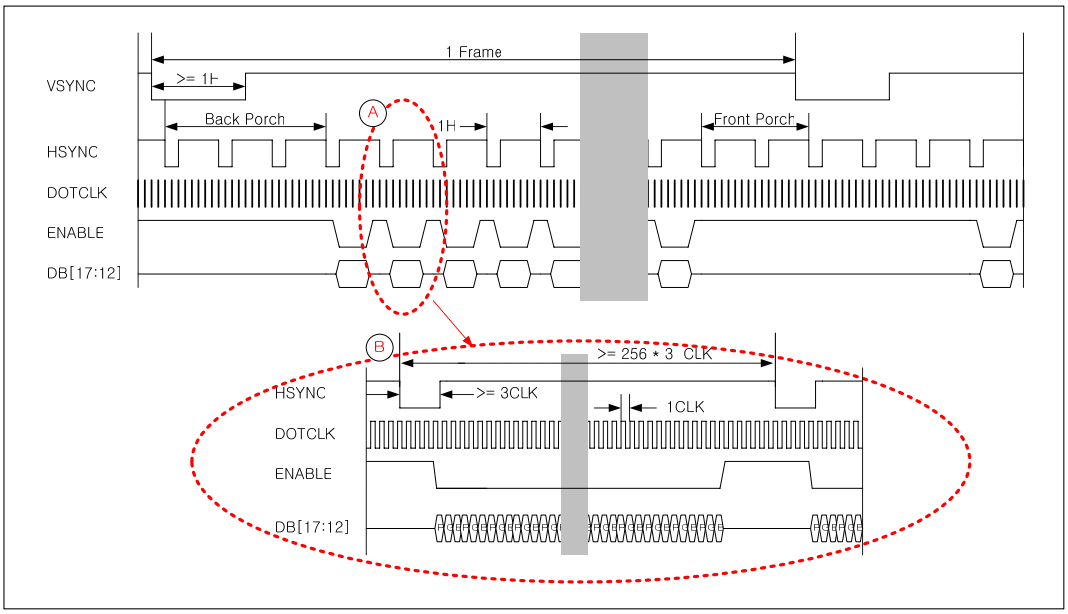

Figure58: Timing Diagram of 6bit RGB Interface

[NOTE]

1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.
   VSYNC, HSYNC, ENABLE, DOTCLK, and DB[8:3] should be transferred in units of three clocks.
2. 1 HSYNC Period must be >= 256 * 3 DOTCLK

Transfer Synchronization

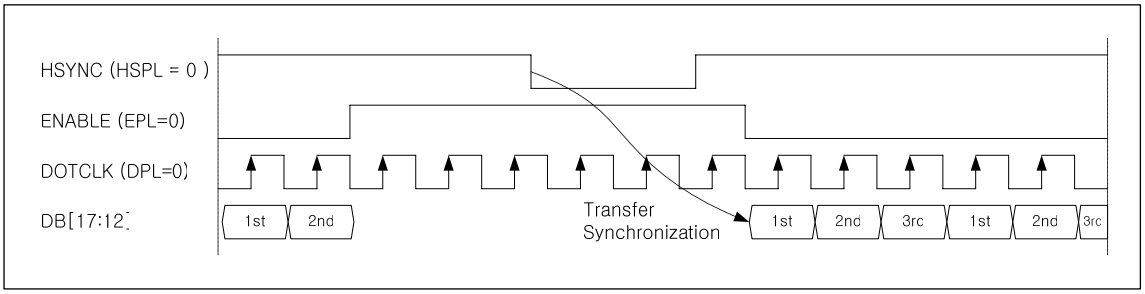

Figure59: Transfer Synchronization Function in 6-bit RGB Interface mode

[NOTE] The figure shows Transfer Synchronization function for 6bit RGB Interface. S6E63D6 has a transfer counter to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of HSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every new transfer restarts with HSYNC signal. In this method, when data is consecutively transferred in such a way as displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation.

[NOTE] The internal display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

Time chart for RGB interface is shown below. (In case of EPL = 0)

Preliminary

INTERFACE SWAPPING FOR MEMORY ACCESS

DISPLAY MODES AND GRAM ACCESS CONTROL

Display mode and RAM Access is controlled as shown below. For each display status, display mode control and RAM Access control are combined properly.

Table49: DISPLAY MODE & RAM ACCESS CONTROL

Display Status	GRAM Access (RM)	Display Mode (DM)
Internal Clock Operation (Still Picture Display)	System Interface (RM = 0)	Internal Clock Operation (DM = 0)
RGB I/F (Displaying Motion Picture)	RGB Interface (RM = 1)	External Clock Operation (DM = 1)
MDDI interface (Displaying motion Pictures)	System interface (RM=0)	MDDI interface (D=0)

[NOTE 1] Only system interface can set Instruction register.
[NOTE 2] When the RGB Interface is being operated do not change the RGB Interface mode (RIM).

Internal Clock Operation mode with System Interface

Every operation in Internal Clock Operation mode is done in synchronization with the internal clock which is generated by internal OSC. The signals input through RGB interface are all meaningless. Access to internal GRAM is done via system interface.

External Clock Operation mode with RGB Interface

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation. Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

Preliminary

USAGE ON EXTERNAL DISPLAY INTERFACE

1. When external display interface is in use, the following functions are not available.

Table50: External Display Interface and Internal Display Operation

Function	External Display Interface	Internal Display Operation
Partial Display	Not Available	Available
Scroll Function	Not Available	Available
Rotation	Not Available	Available
Mirroring	Not Available	Available
Window Function	Not Available	Available

2. VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB interface.

3. RGB data are transferred for three clock cycles in 6-bit RGB interface. Data transferred, therefore, should be transferred in units of RGB.

4. Interface signals, VSYNC, HSYNC, DOTCLK, ENABLE and DB17-0 should be set in units of RGB (pixels) to match RGB transfer.

5. Transitions between internal operation mode and external display interface should follow the mode transition sequence shown below.

6. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

Preliminary

MDDI (MOBILE DISPLAY DIGITAL INTERFACE)

INTRODUCTION OF MDDI

The S6E63D6 supports MDDI. The MDDI is a differential & serial interface with high speed. Both command and image data transfer can be achieved with MDDI.
MDDI host & client are linked with Data and STB line. Through Data line, command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.
Through STB line, strobe signal is transferred. When the link is in “FORWARD direction”, data is transferred from host to client; in “REVERSE direction”, client transfer reverse data to MDDI host.

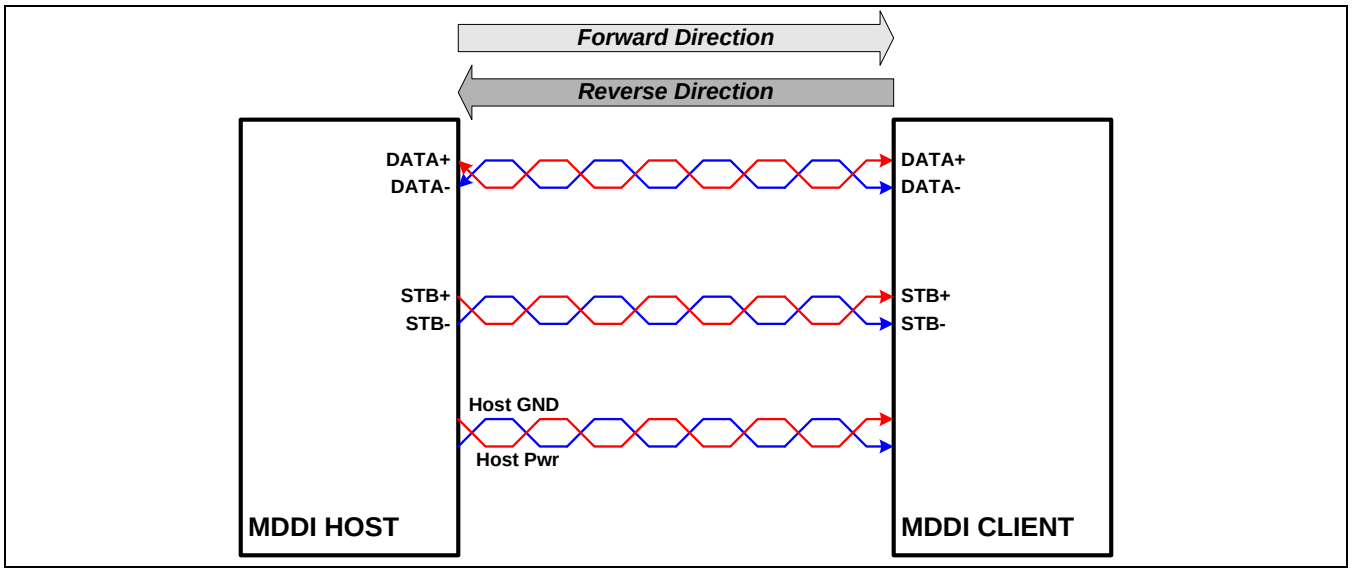

Figure60: Physical connection of MDDI host and client

DATA-STB ENCODING

Data is encoded using a DATA-STB method. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure below illustrates how the data sequence “1110001011” is transmitted using DATA-STB encoding.

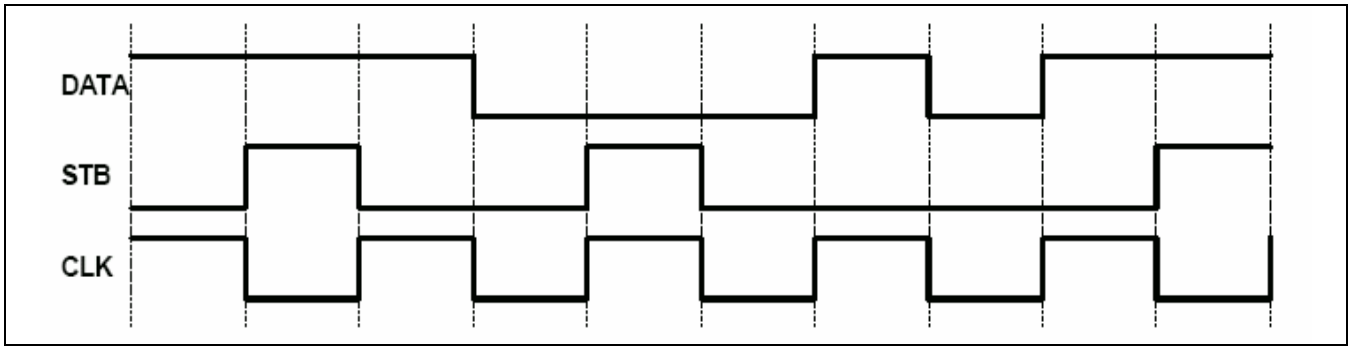

Figure61: Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

Preliminary

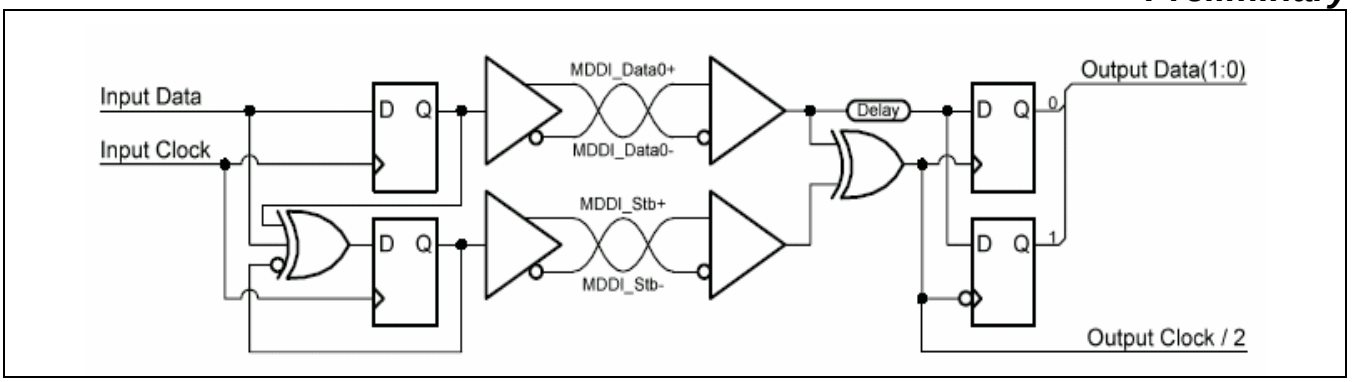

Figure62: Data / STB Generation & Recovery circuit

MDDI DATA / STB

The Data (MDP/MDN) and STB(MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

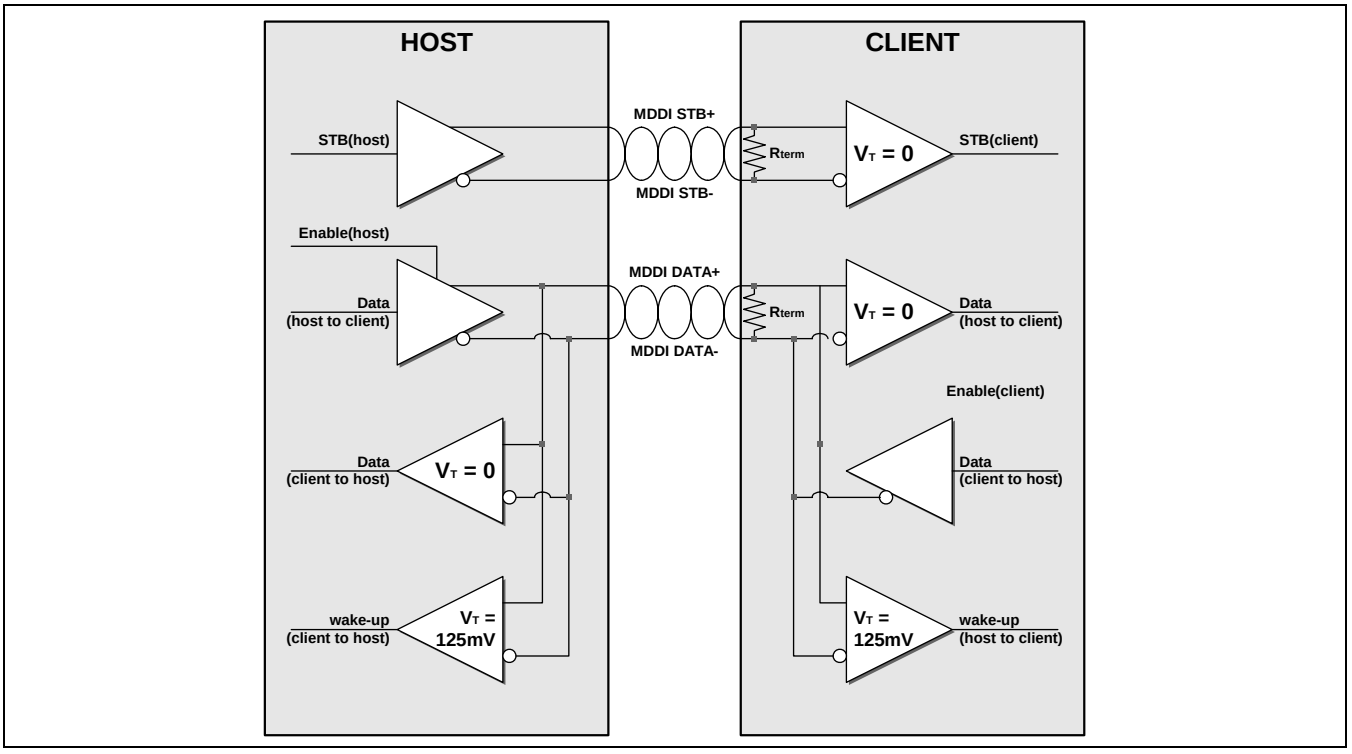

Figure63: Differential connection between host and client

Preliminary

HIBERNATION / WAKE-UP

S6E63D6 support hibernation mode for reducing interface power consumption.
The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption.

In hibernation mode, hi-speed transceivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

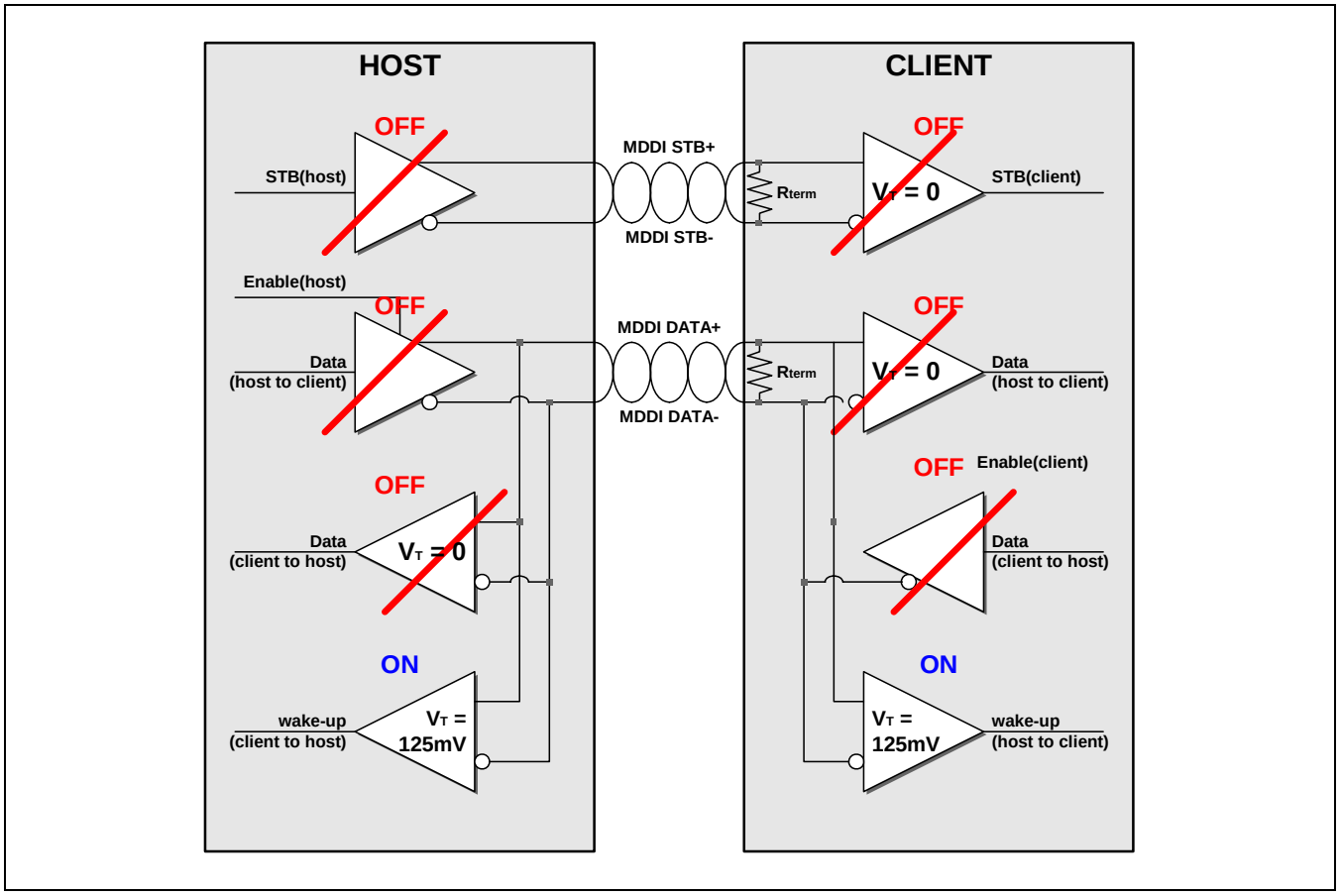

Figure64: MDDI Transceiver / Receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detect using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Both the client and the host can wake up the link, so 2-types of wake-up are supported in S6E63D6: Host-initiated link wakeup and Client-initiated link wakeup.

Preliminary

MDDI LINK WAKE-UP PROCEDURE

Rules for Entering the Hibernation State :

- The host sends 64 MDDI_Stb cycles after the CRC of the Link Shutdown Packet. Also after this CRC the host shall drive MDDI_Data0 to a logic-zero level and disable the MDDI_Data0 output of the host in the range of after the rising edge of the 16th to before the rising edge of the 48th MDDI_Stb cycles (including output disable propagation delays).

- The host shall finish sending the 64 MDDI_Stb cycles after the CRC of the Link Shutdown packet before it initiates the wake-up sequence.

- The client shall wait until after the rigins edge of the 48th MDDI_Stb cycle after the CRC of the Link Shutdown Packet or later before it drives MDDI_Data0 to a logic-one level to attempt to wake-up the host.

- The client shall place its high-speed receivers for MDDI_Data0 and MDDI_Stb into hibernation any time after the rising edge of the 48th MDDI_Stb cycle after the CRC of the Link Shutdown Packet. It is recommended that the client place its high-speed MDDI_Data0 and MDDI_Stb receivers into hibernation before the rising edge of the 64th MDDI_Stb cycle after the CRC of the Link Shutdown Packet.

Rules for Wake-up from the Hibernation State :

- When the client needs service from the host it generates a request pulse by driving MDDI_Data0 to a logic-one level for 70 to 1000 μ sec while MDDI_Stb is inactive and keeps MDDI_Data0 driven to a logic-one level for 70 MDDI_Stb cycles(range of 60 to 80) after MDDI_Stb becomes active. Then the client disables the MDDI_Data0 driver by placing it into a high-impedance state.

- If MDDI_Stb is active during hibernation(which is unlikely, but allowed per the spec) then the client may only drive MDDI_Data0 to a logic one level for 70 MDDI_Stb cycles (range of 60 to 80). This action causes the host to restart data traffic on the forward link and to poll the client for its status.

- The host shall detect the presence of the request pulse from the client (using the low-power differential receiver with a +125mV offset) and begin the startup sequence by first driving MDDI_Stb to a logic-zero level and MDDI_Data0 to a logic-high level for at least 200nsec, and then while toggling MDDI_Stb it shall continue to drive MDDI_Data0 to a logic-one level for 150 MDDI_Stb cycles (range of 140 to 160) and to logic-zero for 50 MDDI_Stb cycles. The client shall not send a service request pulse if it detects MDDI_Data0 at a logic-one level for more than 80 MDDI_Stb cycles. After the client has detected MDDI_Data0 at a logic-one level for 60 to80 MDDI_Stb cycles it shall begin to search for the interval where drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles then the host starts sending packets on the link. The first packet sent shall be a Sub-frame Header Packet. The client begins to look for the Sub-frame header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles of the 50 cycle interval.

- The host may initiate the wake-up by first enabling MDDI_Stb and simultaneously drive it to a logic-zero level. MDDI_Stb shall not be driven to a logic-one level until pulses are output as described below. After MDDI_Stb reaches a valid logic-zero level the host shall enable MDDI_Data0 and simultaneously drive it to a logic-one level. MDDI_Data0 shall not be driven to a logic-zero level during the wake-up process until the interval where it is

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driven to a logic-zero level for an interval of 50 MDDI_Stb pulses as described below. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level before driving pulses on MDDI_Stb. This timing relationship shall always occur while considering the worst-case output enable delays. This guarantees that the client has sufficient time to fully enable its MDDI_Stb receiver after being woken up by a logic-one level on MDDI_Data0 that was driven by the host.

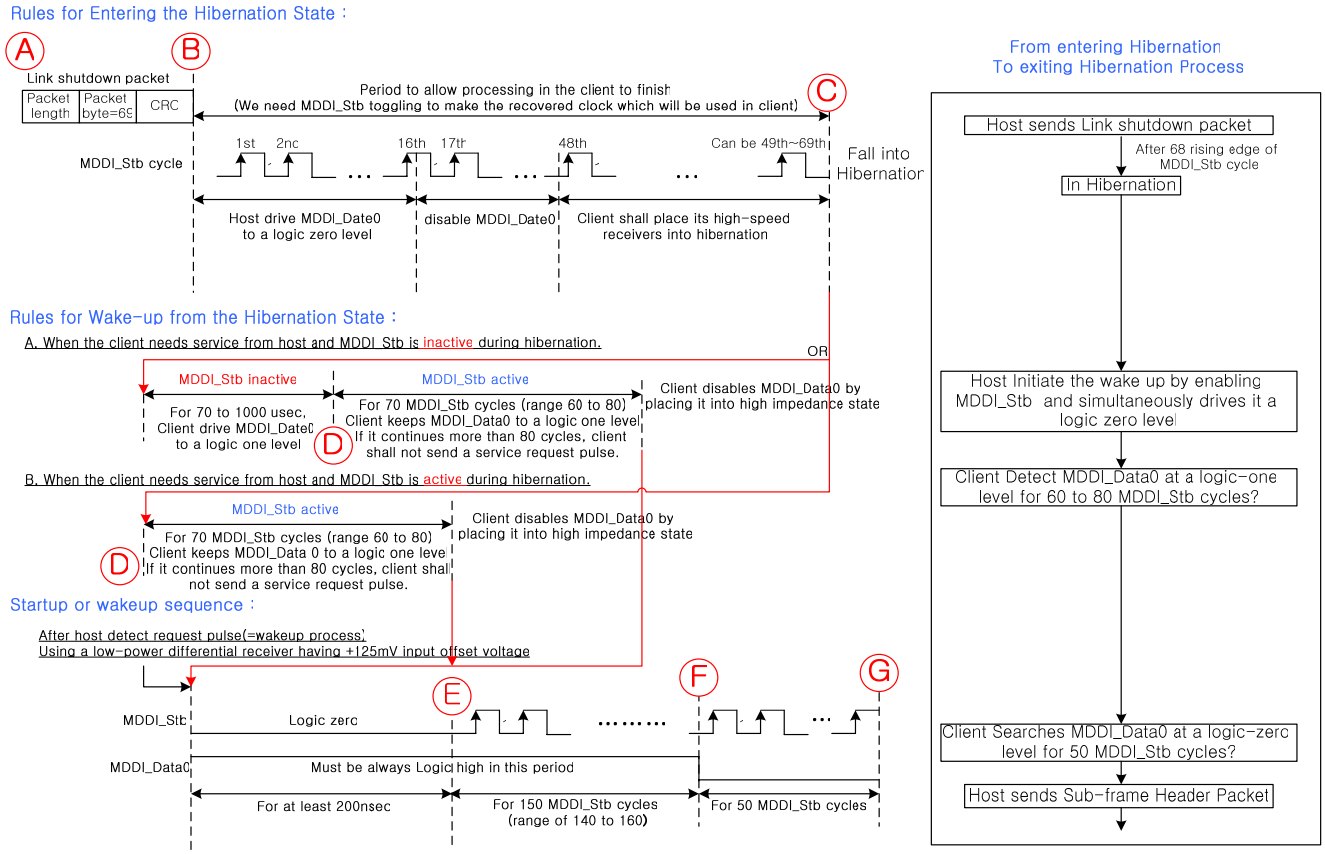

Figure65: Process from entering Hibernation To exiting Hibernation

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1) Host-initiated Link Wake-up Procedure

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

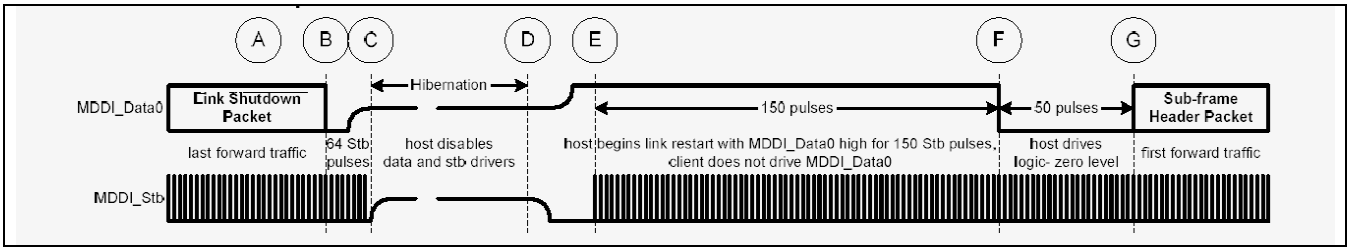

Figure66: Host-initiated link wakeup sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device.
Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.
The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level.
The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet.
Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

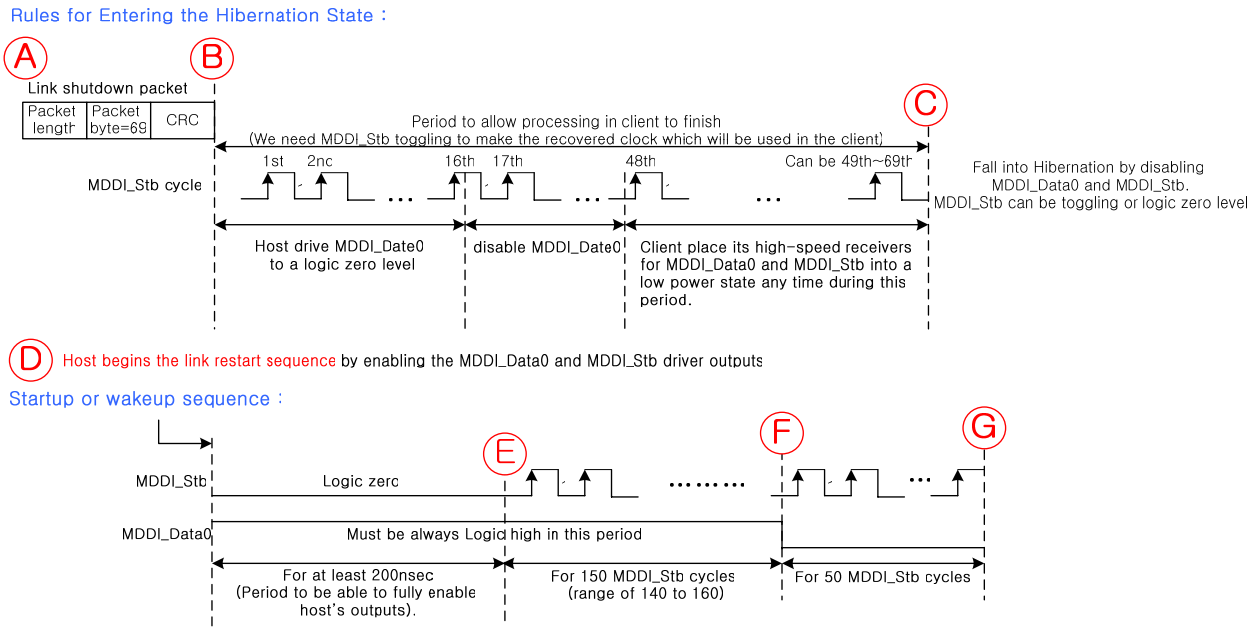

Figure67: Host-initiated link wakeup sequence

2) Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

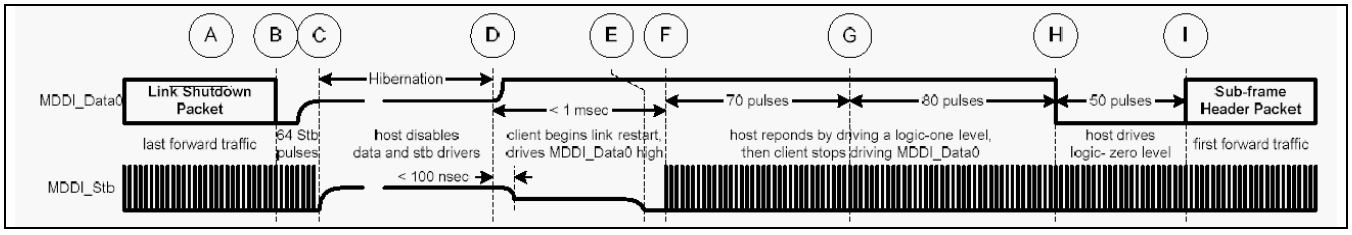

Figure68: Client-initiated link wake-up sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device.
Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an

offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver.
The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client.
After that, the client enables its MDDI_Data0 driver while driving MDDI_Data0 to a logic-one level. It is allowed for MDDI_Data0 and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs.
The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb.
This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data0 at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data0. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

G. The client continues to drive MDDI_Data0 to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data0 driver at point G. The host continues to drive MDDI_Data0 to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data0 to logic-zero level.

H. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

I. After asserting MDDI_Data0 to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet.
The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

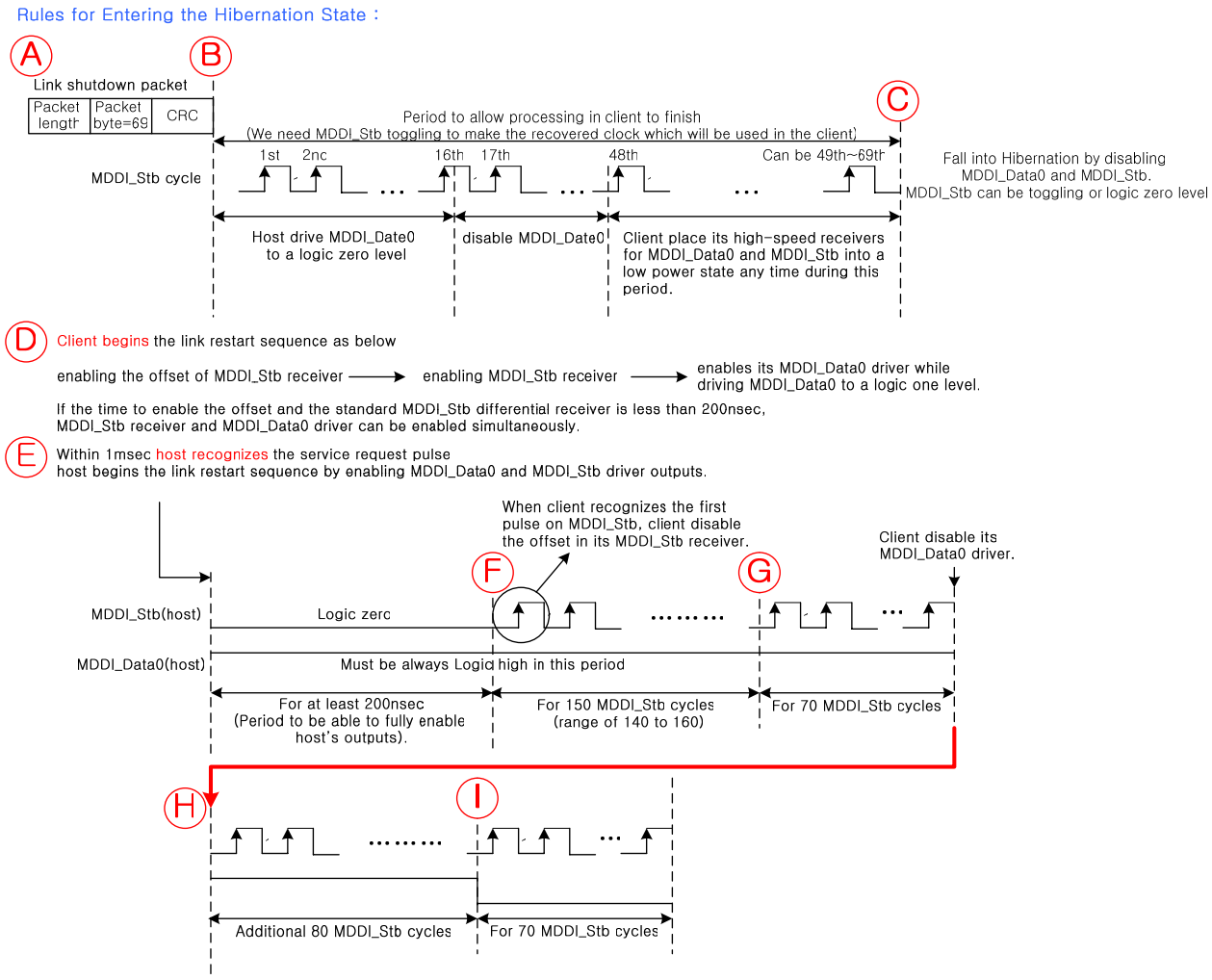

Figure69: Client-initiated link wake-up sequence

S6E63D6 supports 2-types of client-initiated link wake-up: VSYNC based Link Wake-up & GPIO based Link Wake-up. As client-initiated wake-up action is executed in hibernation state only, register setting for each wake-up have to be set before link shut-down.

VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (50h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6E63D6.
Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

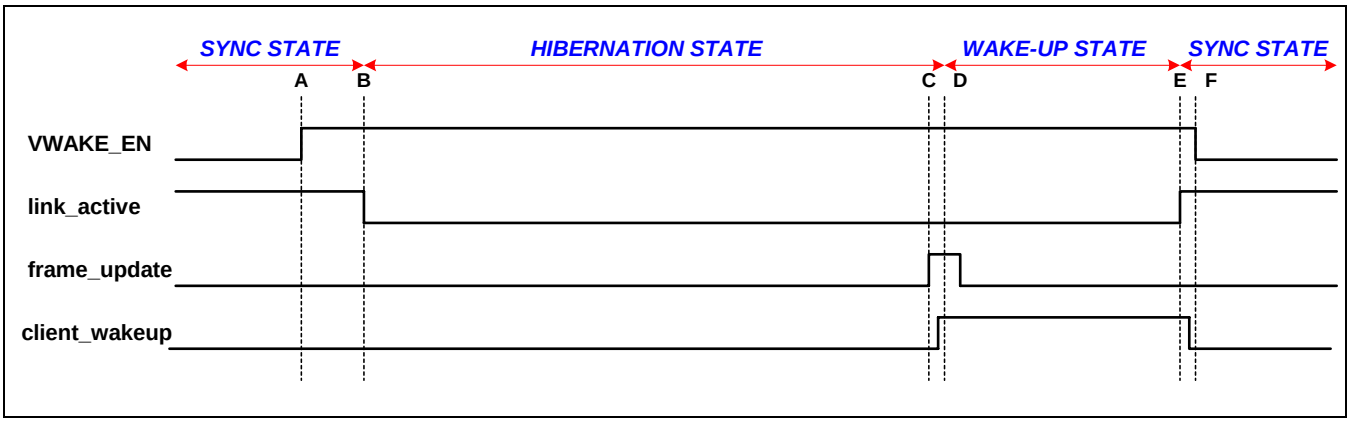

Figure70: VSYNC based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6E63D6.

C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up point can be set using WKF and WKL (51h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

E. link_active goes high after the host brings the link out of hibernation.

F. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

GPIO Based Link Wake-up

In VSYNC-based link wake-up, wake-up enable register setting prior to link shut-down. GPIO based Link wake-up is enabled by interrupt from outside of the IC. For GPIO based link wake-up, GPIO interrupt enable and GPIO PAD mode (to input mode) setting must be set. Once S6E63D6 receive interrupt, internal GPIO base link wake-up flag set to high, and the following procedure is similar to that of VSYNC based link wake-up.
The following figure shows detailed timing for GPIO based link wake-up.

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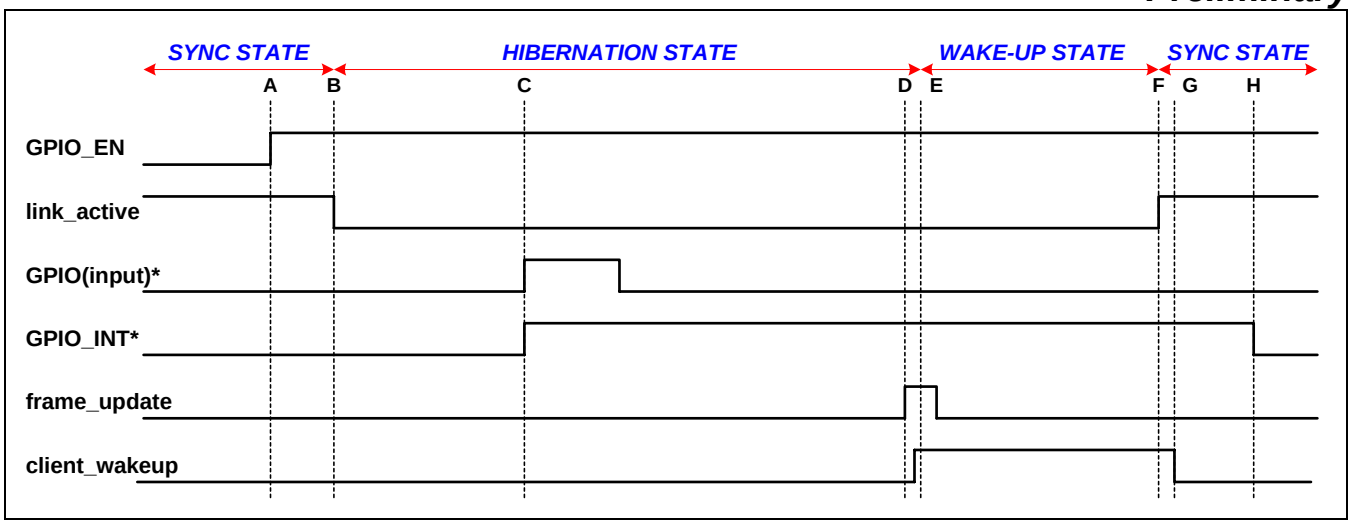

Figure71: GPIO based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

A. Host sets the GPIO interrupt enable register (69h: GPIO_EN) for a particular GPIO through register access packet.

B. Link goes into hibernation (and link_active)goes low) when the host has no more data to send to the IC.

C. GPIO input goes high, and the GPIO interrupt (GPIO_INT) is latched.

D. Frame_update signal goes high indicating that the display has wrapped around. Link wake-up point can be set using WKF and WKL (51h) registers.

E. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

F. Link_active goes high after the host brings the link out of hibernation.

G. After link wake-up, client_wakeup signal is reset to low.

H. MDDI host clears the interrupt by writing to the interrupt clear register with the bit set for that particular interrupt (GPCLR: 68h). Between point G and H the host will have read the GPIO_INT values to see what interrupts are active.

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GPIO CONTROL

S6E63D6 offers 10(maximum) GPIO that can be used as input or output independently.
Some application or device on the upper clamshell needs several control signals which are supplied by base band modem or application processor directly. If number of application on the upper clamshell increases, also control signals increase, causing the interface more costly.
In S6E63D6, GPIO can be the solution for that problem. User may control the 10 GPIOs as input or output by use of simple register setting. So additional connection between base band modem / AP (application processor) and components on upper clamshell are not needed.

The following table shows several set of register for GPIO.

Register	width	Description		Reset value
GPIO (66h)	[9:0]	Write	For GPIO output mode: output GPIO register(66h) value to GPIO PAD	10'h000
		Read	GPIO PAD status	
GPIO_CON (67h)	[9:0]	Write	GPIO PAD input/output mode control : (0 : input / 1 : output)	10'h000
		Read	GPIO_CON (67h) register value	
GPCLR (68h)	[9:0]	Write	For GPIO input mode: clear specified GPIO interrupt (set by GPIO PAD input).	10'h000
		Read	GPIO interrupt state (set by GPIO PAD input).	
GPIO_EN (69h)	[9:0]	Write	For GPIO input mode: enable specified GPIO interrupt	10'h000
		Read	GPIO_EN (69h) register value.	
GPPOL (6Ah)	[9:0]	Write	For GPIO input mode: GPIO interrupt polarity setting	10'h3FF
		Read	GPPOL (6Ah) register value.	

In GPIO output mode, the IC output GPIO (66h) register value to the defined PAD.
Set GPIO_CON register as output mode before use GPIO output.

10 different GPIO output can be controlled simultaneously using 1-register access packet (66h register access) so that minimum access time for each GPIO output will be 1-register access time.

GPIO input mode can only be used as client-initiated link wake-up.
For more information, refer to GPIO based link wake-up section.

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3) Host-initiated Wake-up from Hibernation with Connection from client

This is actually a host-initiated wake-up, but we have included the case where the client also wants to wake up the link with the latest possible request. The labeled events are :

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles(including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.
E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
F. At up to 70 MDDI_Stb cycles after point E the client has not yet recognized that the host is driving MDDI_Data0 to a logic-one level so the client also drives MDDI_Data0 to a logic-one level. This occurs because the client has a need to request service from the host and does not recognize that the host has already begun the link restart sequence.
G. The client ceases to drive MDDI_Data0, and places its driver into a high-impedance state by disabling its output. The host continues to drive MDDI_Data0 to a logic-one level for 80 additional MDDI_Stb cycles.
H. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.
I. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point I the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point I.

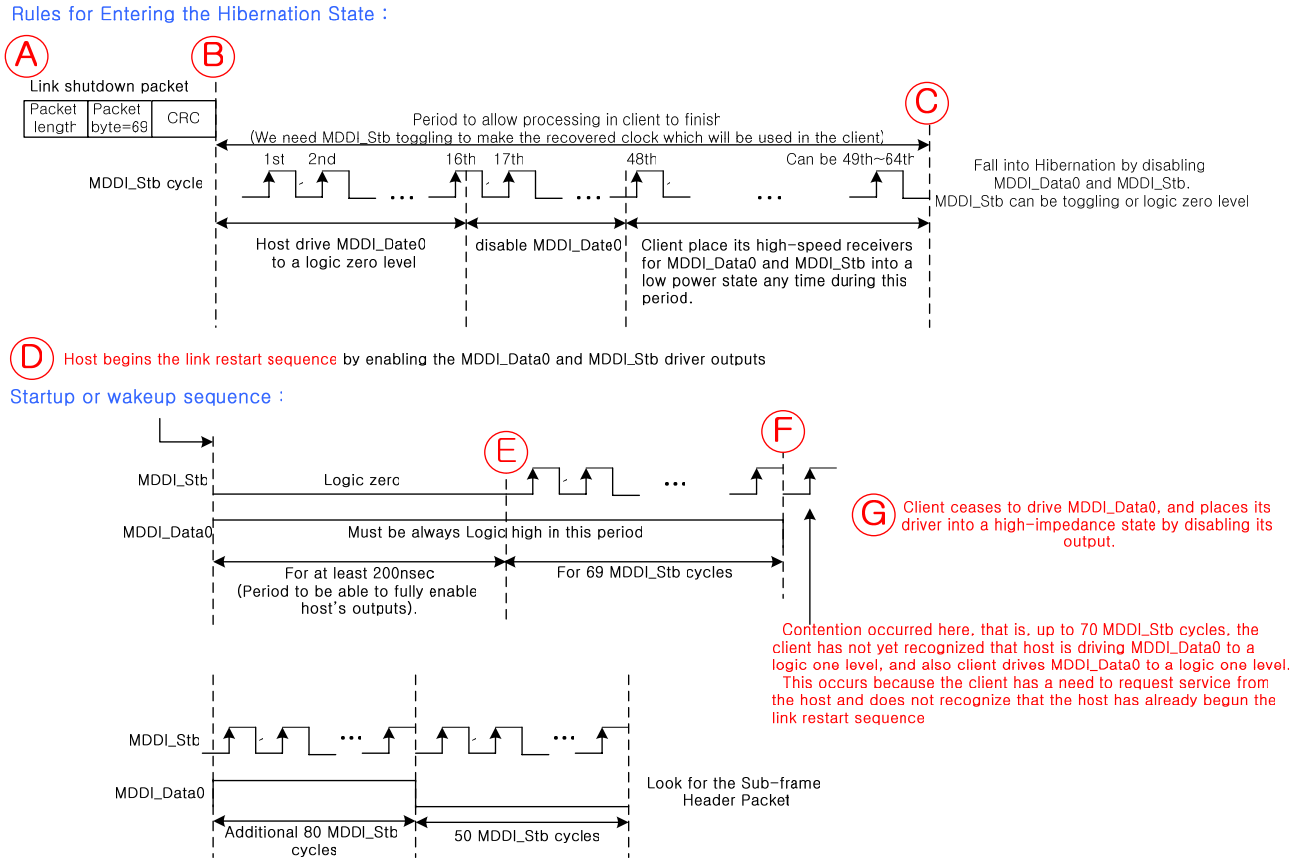

Figure72: Host-initiated Wake-up process from Hibernation with Connection from client

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MDDI PACKET

MDDI transfer data by packet format. MDDI host can make many packets and transfer them.
In S6E63D6, several packets format is supported. Most packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).
A number of packets, started by sub-frame header packet, construct 1 sub frame.

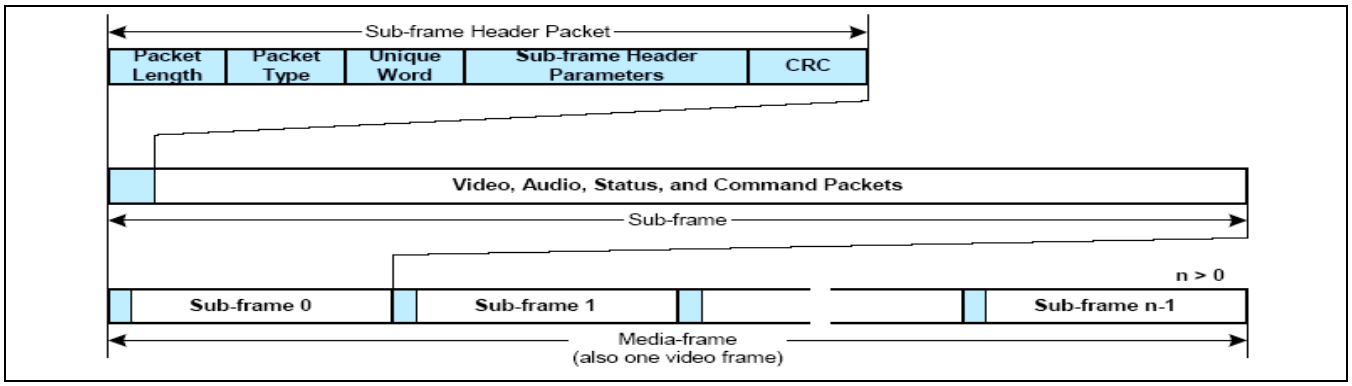

Figure73: MDDI packet structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.
The following table describes 9 types of packet which is supported in S6E63D6.

PACKET	FUNCTION	DIRECTION
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Clinet request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-frame header packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet
mddi frame count : specifies number of media frames
CRC : error check

Figure74: Sub-frame header packet structure

Register access packet

packet length	packet type = 146	bClient ID	Read/Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Register Access packet is 146(decimal))
bClient ID : set to all zero
Read/Write Info : to write register value, bits[15:14] = "00"
to read register value, bits[15:14] = "11"
bits[13:0] is all zero
Register Address : Register address is set written here.
Parameter CRC : To error check from packet length to register address
Register Data List : Paramter data is written here.
CRC : To error check register data list.

Figure75: Register access packet structure

Video Stream packet

packet length	packet type=16	bClientID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom edge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length – 26 bytes	2 bytes

packet length : packet length not including packatet length block
packet type : packet type(video stream packet is 16)
bClientID : reserved, set all 0
video data format descriptor : bits[15:13] = 010 : raw RGB format(fixed value)
bits[12] = 1 : Only packed type is available(fixed value)
bits[11:0] = 0110_0110_0110 : 18 bit pixel
bits[11:0] = 0101_0110_0101 : 16 bit pixel
pixel data attributes : bits[1:0] = 11 : displayed both eyes(fixed value)
bits[5] = 1 : X left edge .. Y start edge is not defined.(fixed value)
other bits are all zero.
X left edge : Not used in S6D0139, set all zero.
Y top edge : Not used in S6D0139, set all zero.
X right edge : Not used in S6D0139, set all zero.
Y bottom edge : Not used in S6D0139, set all zero.
X start : Not used in S6d0139, set all zero.
Y start : Not used in S6d0139, set all zero.
Pixel count : Write number of pixel.
Paramter CRC : To error check from packet length to pixel count.
pixel data : pixel data info. number of pixel data must not be over 65509.
pixel data CRC : To pixel data error check.

Figure76: Video stream packet structure

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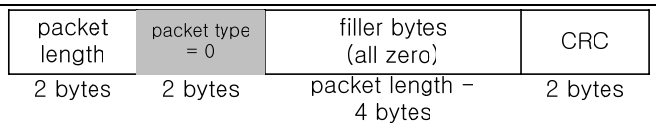
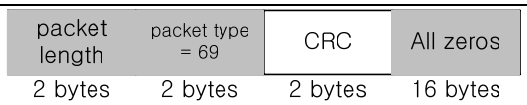
Filler packet



packet length : packet length not including packet length block
packet type : packet type(Filler packet is 0(decimal))
filler bytes : set to all zero(The size is under packet length availabe)
CRC : To error check

Figure77: Filler packet structure

Link shutdown packet



packet length : packet length not including packet length block
packet type : packet type(Link shutdown packet is 69(decimal))
CRC : To error check
All zeros : write all zero (size is 16 bytes, because MDDI for S6D0142 is type 1)

Figure78: Link shutdown packet structure

: fixed value

For More information about MDDI packet, please refer to VESA MDDI spec.

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MDDI OPERATING STATE

In MDDI, six operation modes are available. The following table describes six modes.

STATE	OSC	Step-up Circuit	Internal Logic status	MDDI I/O	Wake-up by
SLEEP	ON	Disabled	Display OFF MDDI Link hibernation	Hibernation driver ON	Host - Initiated
WAIT	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
Normal	ON	Enabled	Display ON MDDI Link in SYNC	standard driver ON	-
NAP	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
IDLE	ON	Enabled	Display ON MDDI Link hibernation	Hibernation driver ON	Host - Initiated Client - Initiated (Vsync, GPIO)
STOP	OFF	Disabled	Display OFF MDDI Link OFF	Driver All OFF	RESET

SLEEP: Initial status when external power is connected to the IC.
In this state, internal oscillator is operating, and MDDI link is in hibernation state.
As no command or signal is applied to the IC except RESET input, internal logic or step-up circuit is OFF.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic or step-up is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, step-up circuit, and internal logic circuit is ON. Register access or Video data transfer is available in NORMAL state.

IDLE: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal step-up & logic circuits are still operating. MDDI link wakeup will be accomplished when vsync wakeup register is set before hibernation or GPIO interrupt is set.

NAP: This state is set by register access. Step-up and Internal logic is OFF, but MDDI link is ON.
MDDI link have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by register access (R10h). In this state, MDDI link, internal oscillator, step-up, and logic circuit are all OFF. To release STOP state, input reset signal. After reset, status is SLEEP state.

Preliminary

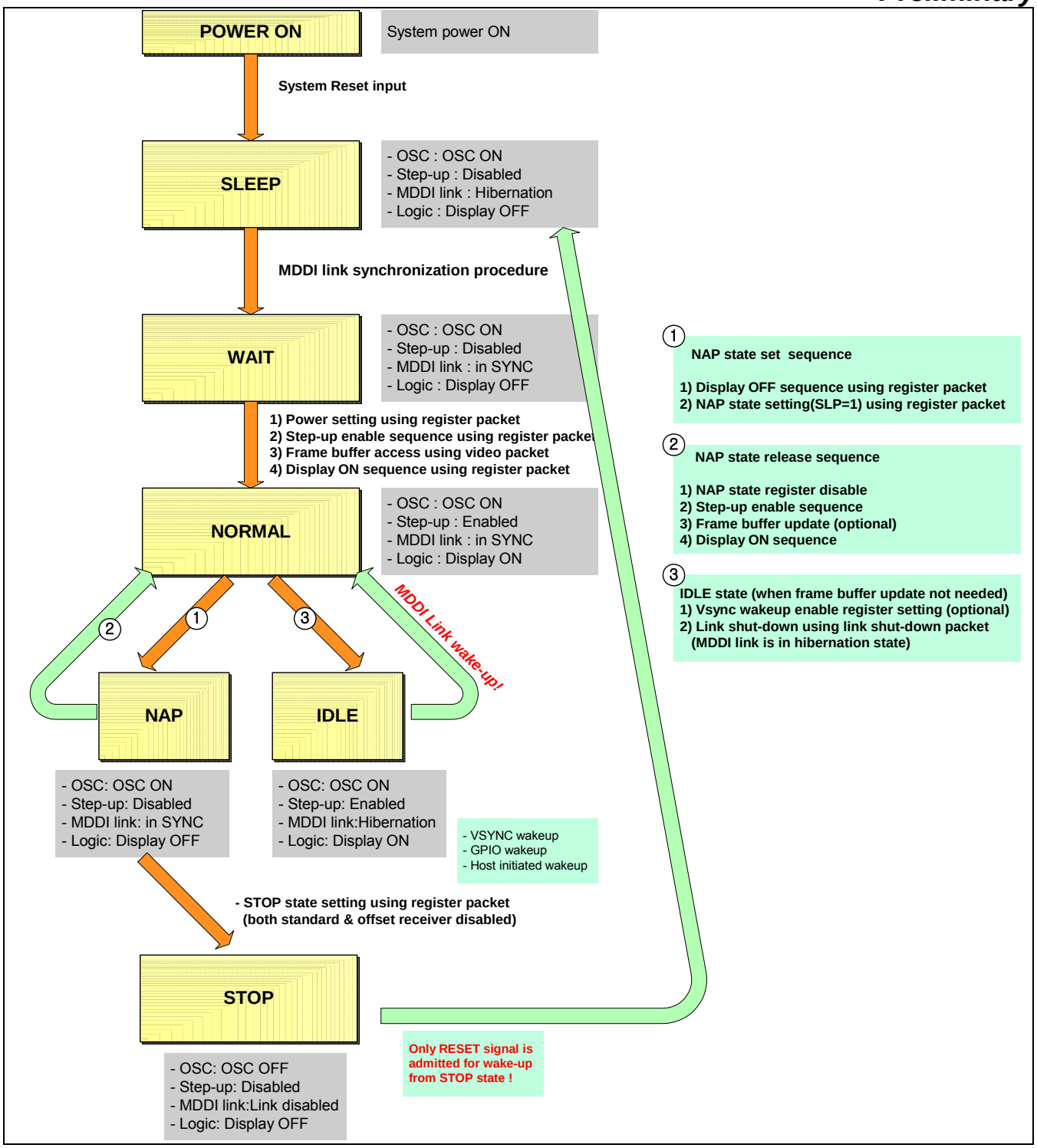


Figure79: Operating state in MDDI mode

Preliminary

TEARING-LESS DISPLAY

In S6E63D6, the matching between data write timing and written data display timing is important. If timing is mismatched, tearing effect can occur.
To avoid display tearing effect, two possible ways are suggested.
First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely (?) in this case.
Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update.
The following figures describe some examples to avoid display tearing phenomenon.

1. Display speed is faster than data write.

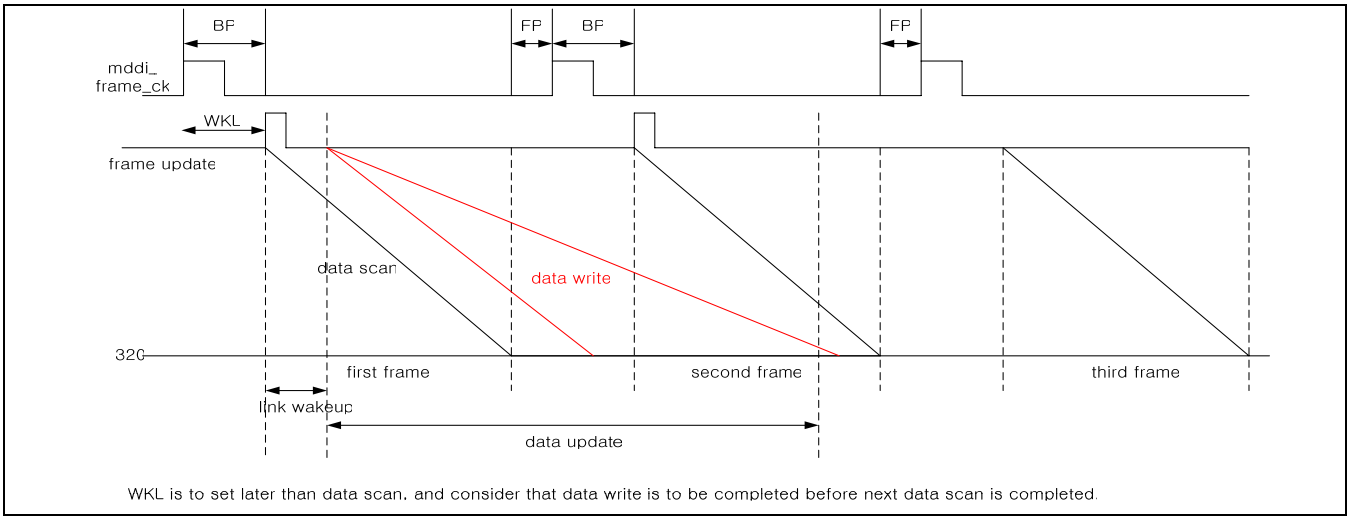


Figure80: Tearing-less display: display speed is faster than data write

2. Display speed is slower than data write.

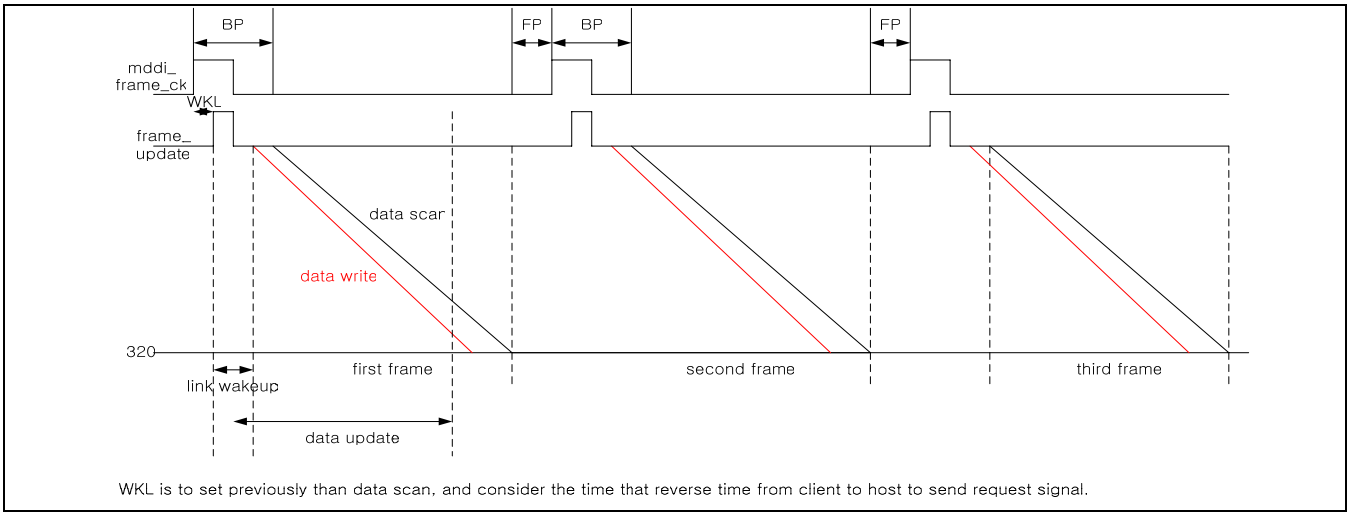


Figure81: Tearing-less display: data write speed is faster than display

Preliminary

SUB PANEL CONTROL

S6E63D6 support sub panel control function which controls sub panel driver IC using 80-mode protocol (CSB, RS, WRB & DB). When MDDI host (Base band modem) sends several packets to S6E63D6, if the packet is for sub panel, the IC converts the packet to 80-mode protocol & sends them to sub panel driver IC. So separated line for sub panel control are not needed. After all, S6E63D6 enables the sub panel driver IC which doesn't support MDDI to be applied to the system. S6E63D6 supports only 80-mode 18/16 bit format for sub panel control.

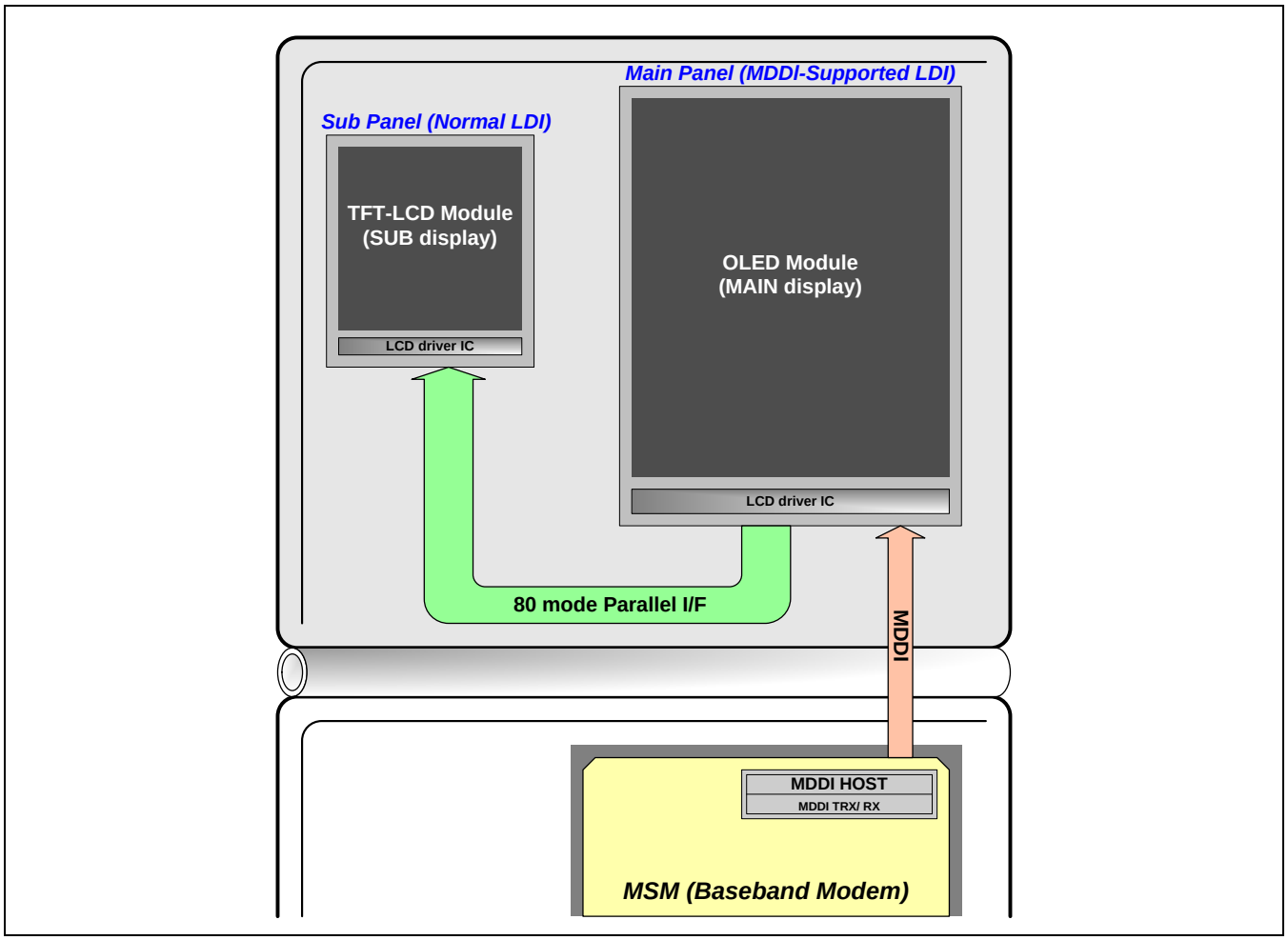


Figure82: Schematic diagram of sub panel control function

Preliminary

MAIN / SUB PANEL SELECTION

Using 7Ah register (7Ah address can be changed using SUB_SEL register), main / sub panel data path can be selected. When S6E63D6 receives register access packet (Initially 7Ah index) from MDDI host, it decodes the packet and checks the last bit of the register data field is '1' or '0'. If the last bit is '0', the following register access packet or video stream packet is transferred to the sub panel control signal generation block.

Sub panel selection address (Initially 7Ah) can be changed using SUB_SEL register. Do not change the SUB_SEL value to previously occupied address.

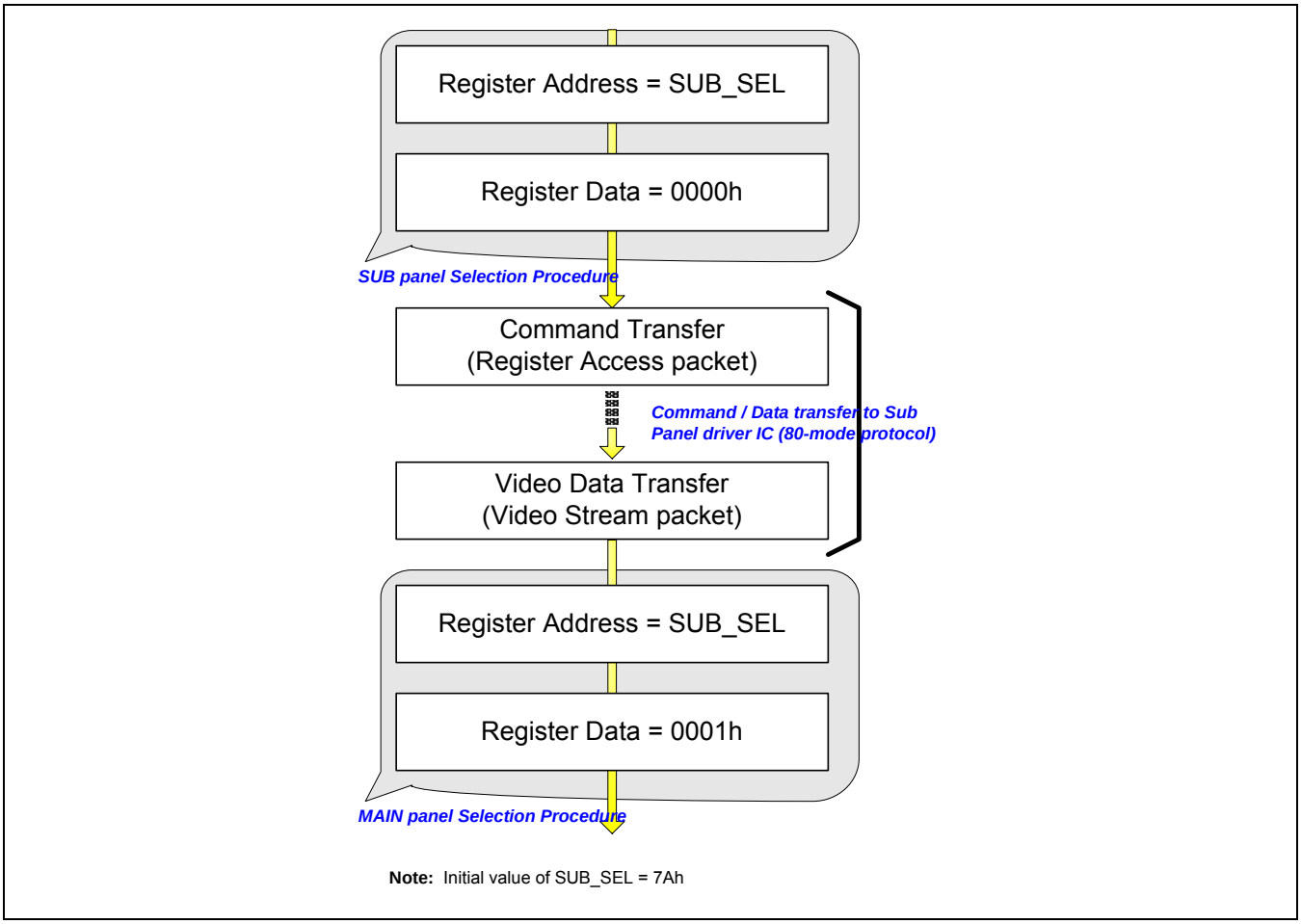


Figure83: Main / Sub panel selection procedure

When video data is transferred to the sub panel driver IC via S6E63D6, additional GRAM access command (normally 22h) is automatically generated in S6E63D6.

Preliminary

SUB PANEL CONTROL TIMING

1. TFT type sub panel timing

1.1 Register data transfer timing

If sub panel is selected, and sub panel type is TFT, register setting is executed like below figure.
Register data is transferred through S_DB[17:10] & S_DB[8:1] in 18/16 bit type. If 9/8 bit type is used, data is transferred thorough S_DB[17:10]. Refer to sub panel control(15h index) section.

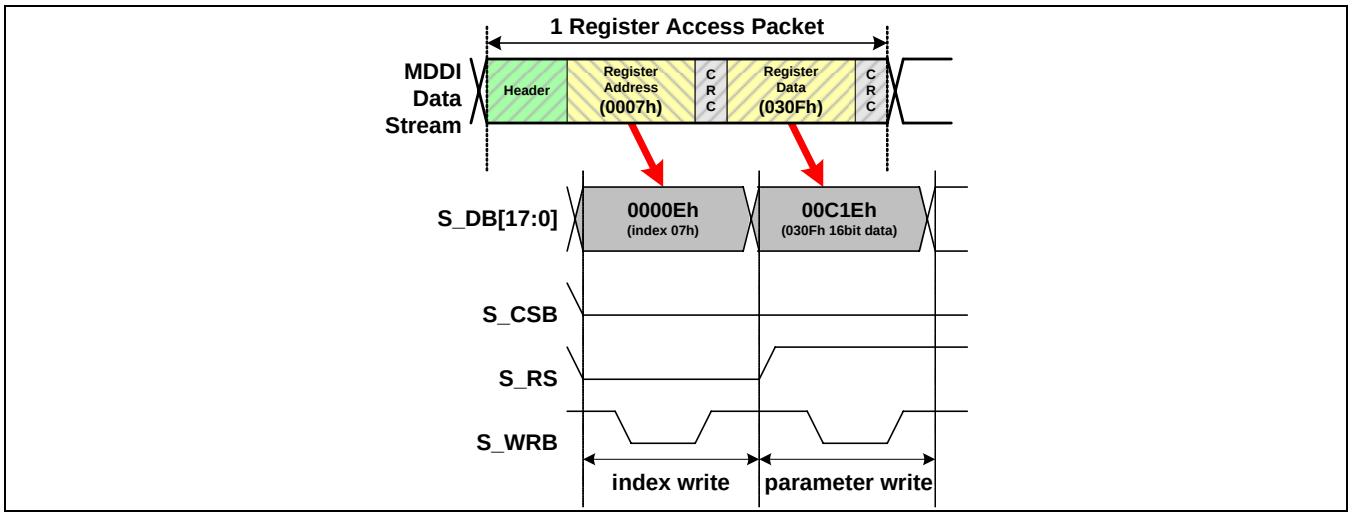


Figure84: 18/16 bit type register access data transfer

In 9/8 bit mode, S_DB[17:10] is used. In this mode, data is transferred at two times. First transfer is MSB 8bit and second transfer is LSB 8bit.

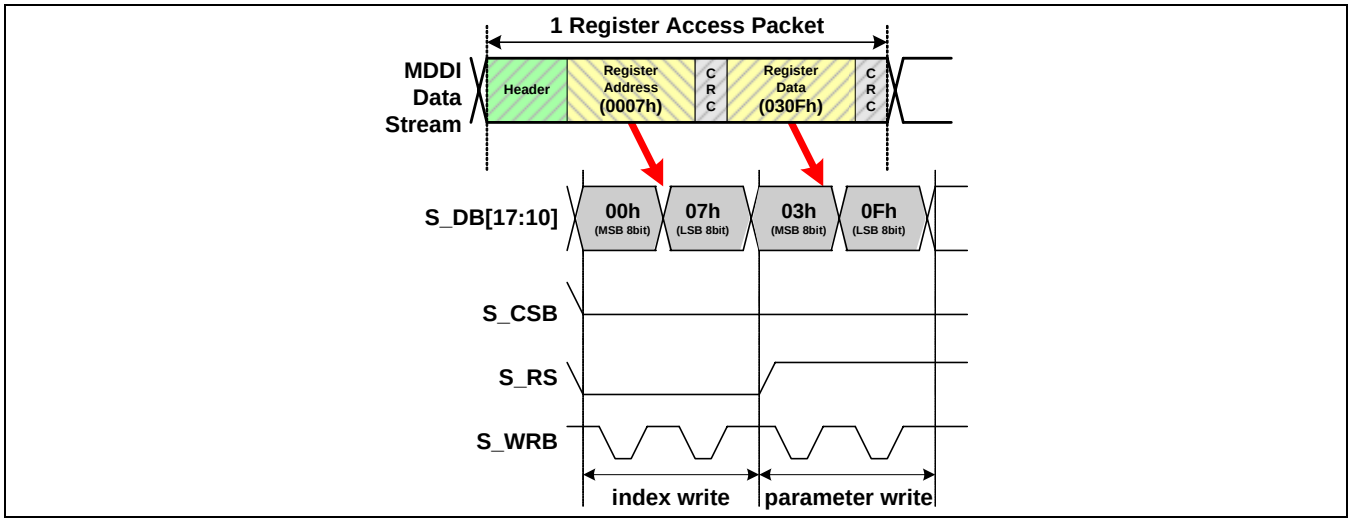


Figure85: 9/8 bit type register access data transfer

This figure shows register setting in 18/16 bit & 68 mode. In 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Because S6E63D6 only writes data to sub panel module.

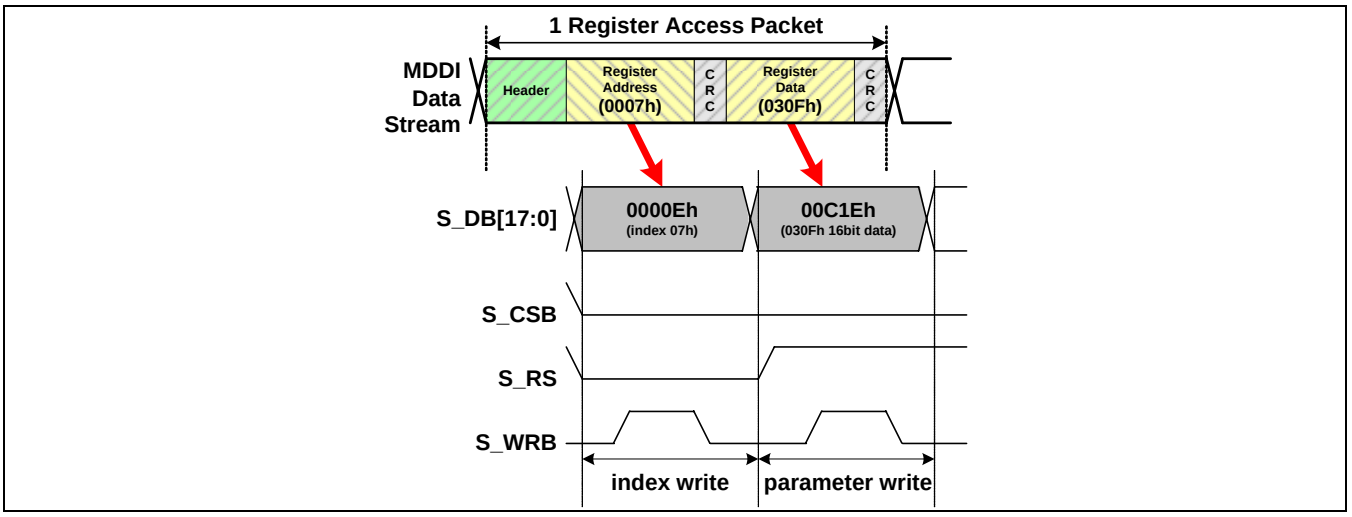


Figure86: 68 mode 18 bit register data transfer

1.2 Video data transfer timing

In TFT type sub panel, STN_EN register in 15h index is “0”, and if user wants to use 68-mode interface protocol, then MPU_MODE is set to “1”. 18/16/9/8 mode is selected as setting SUB_IM register. Refer to 15h index description.

This figure shows 80 mode 18 bit Video data transfer.

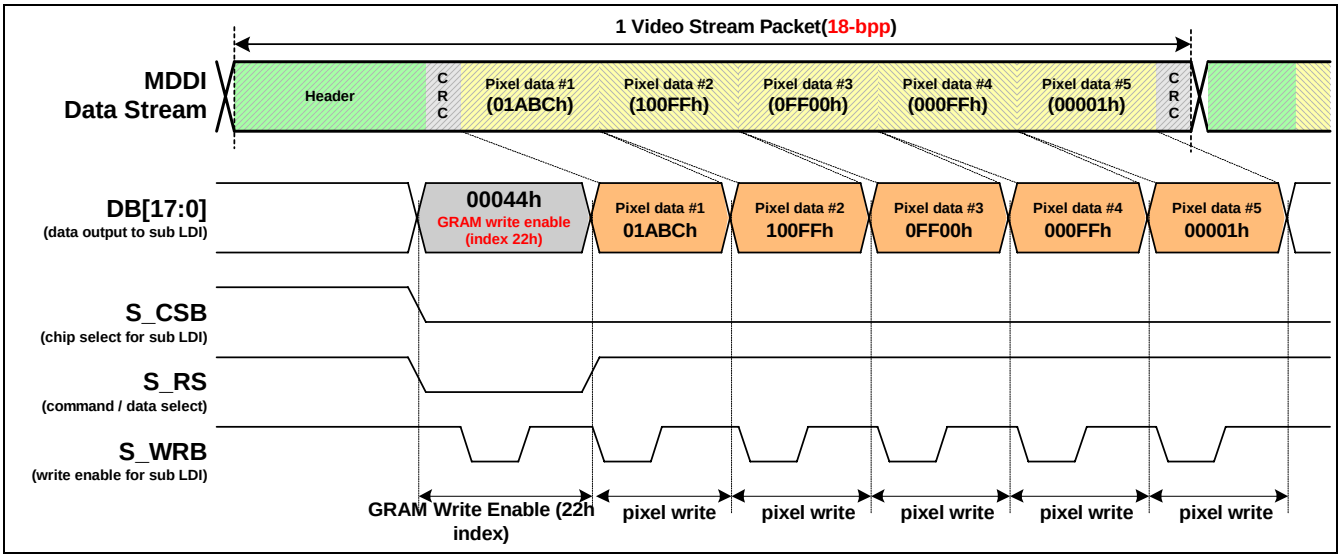


Figure87: 80 mode 18 bit video data transfer

Preliminary

This fugure shows 68 mode 18 bit. In 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Because S6E63D6 only writes data to sub panel module.

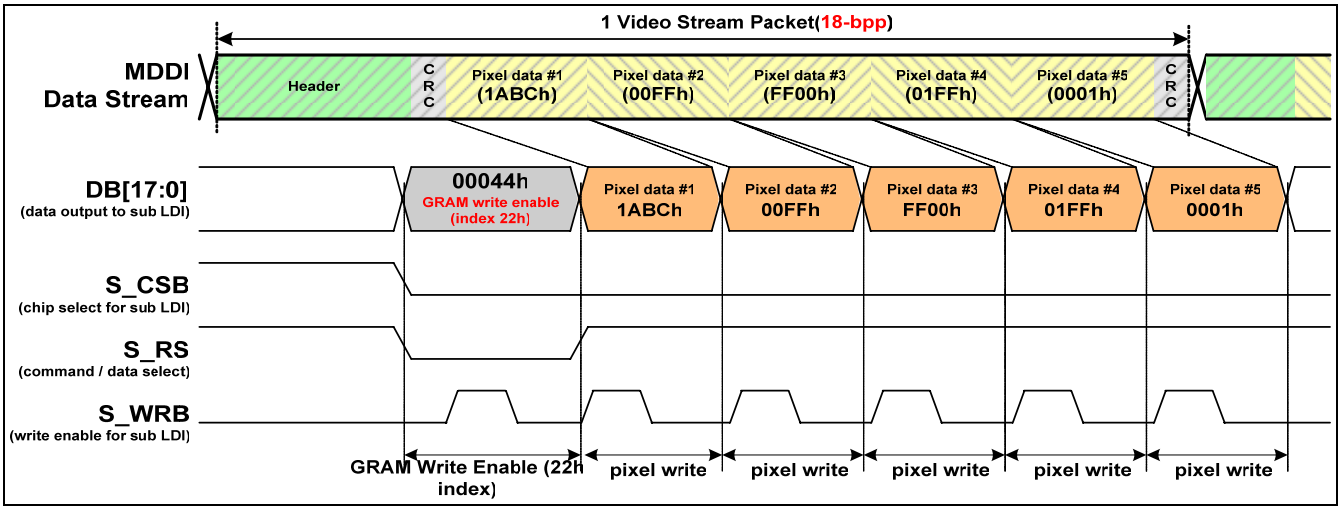


Figure88: 68 mode 18 bit video data transfer

This figure shows 80-mode 16 bit Video data transfer.

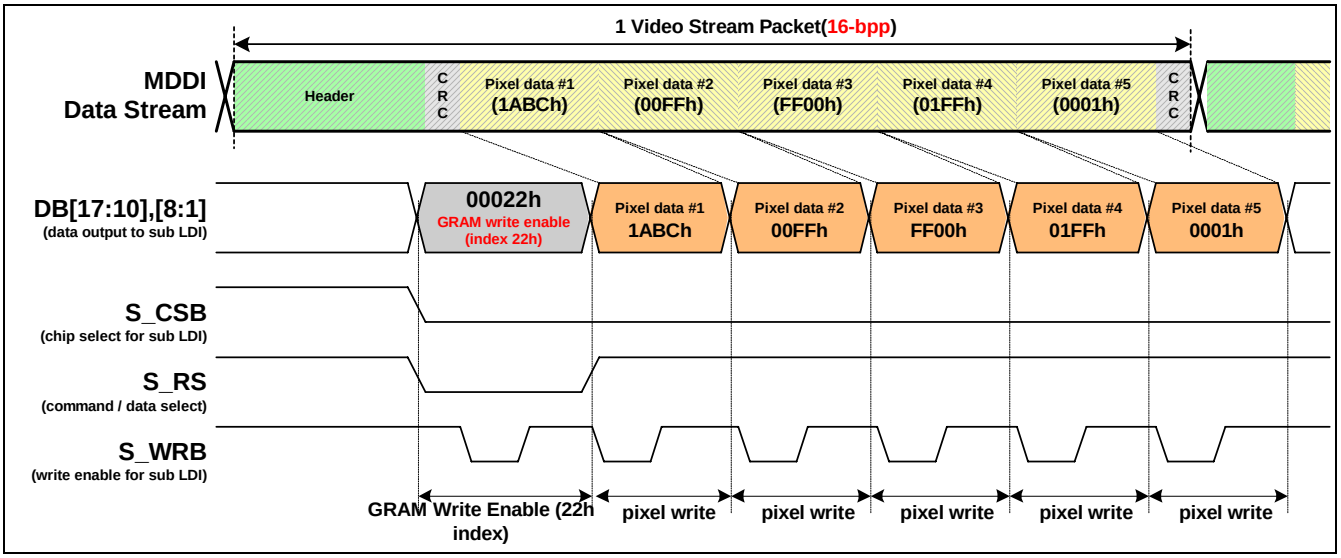


Figure89: 80 mode 16 bit video data transfer

This figure shows 80-mode 9 bit Video data transfer.

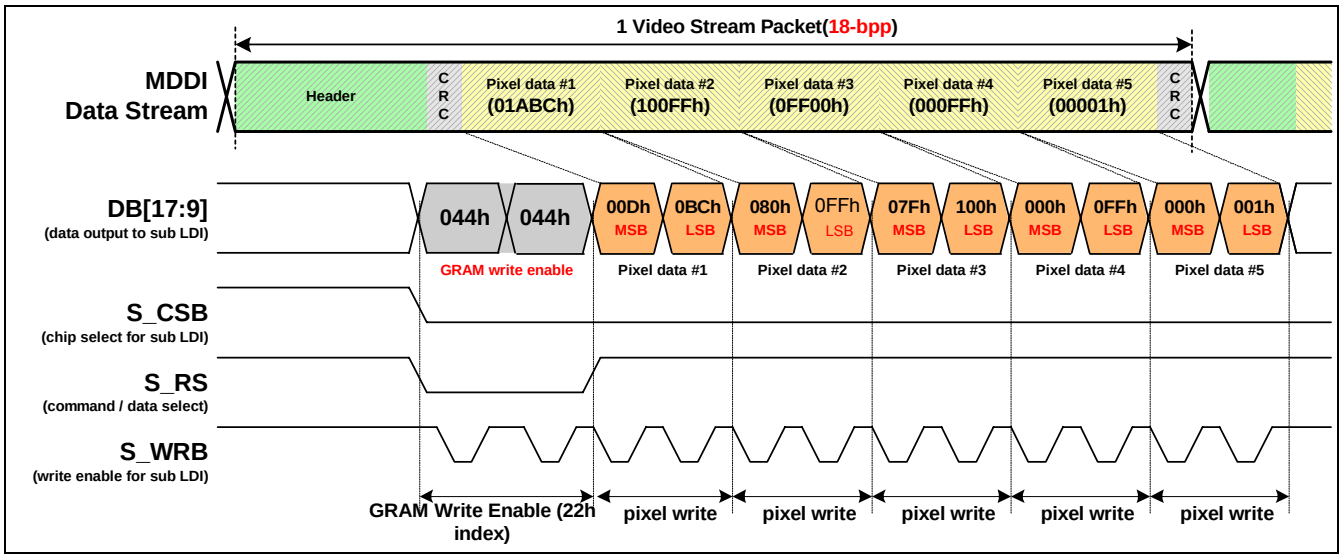


Figure90: 80 mode 9 bit video data transfer

This figure shows 80-mode 8 bit Video data transfer.

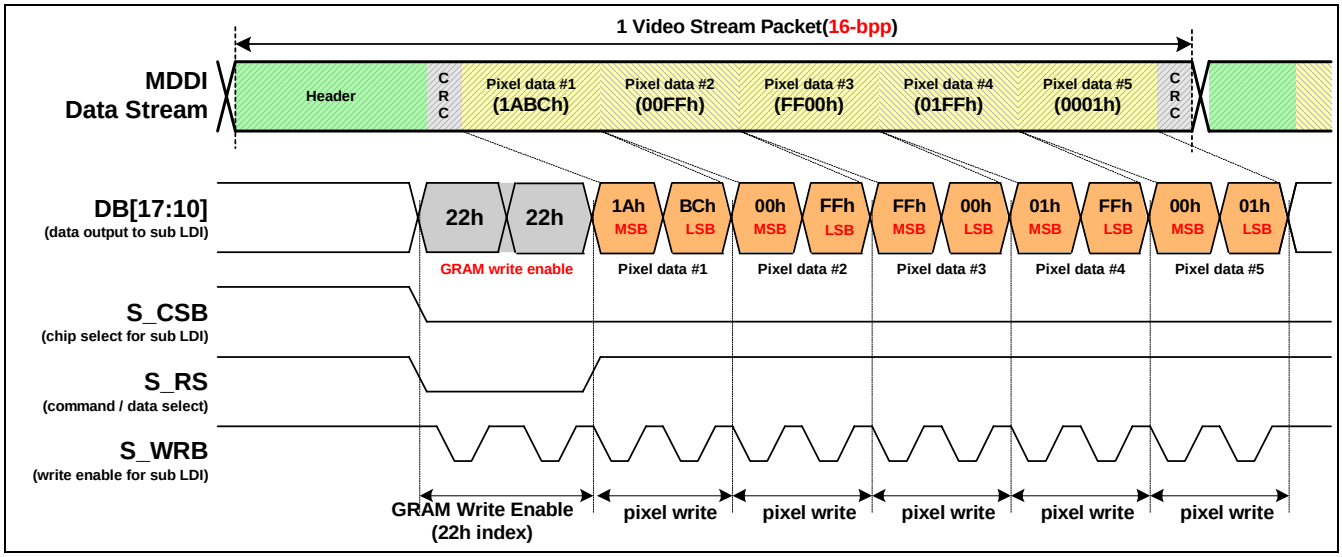


Figure91: 80 mode 8 bit video data transfer

2. STN type sub panel timing

2.1 Register data transfer timing

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter. Instruction type is only 8bit. To use STN type, STN_EN is set to “1”. In STN type, S6E63D6 controls S_RS pin using register address[0] in register access packet. Register address[0] is “0”, then S_RS is set to “0”, and register address[0] is “1”, S_RS is set to “1”. Refer to sub panel control(15h index) section.

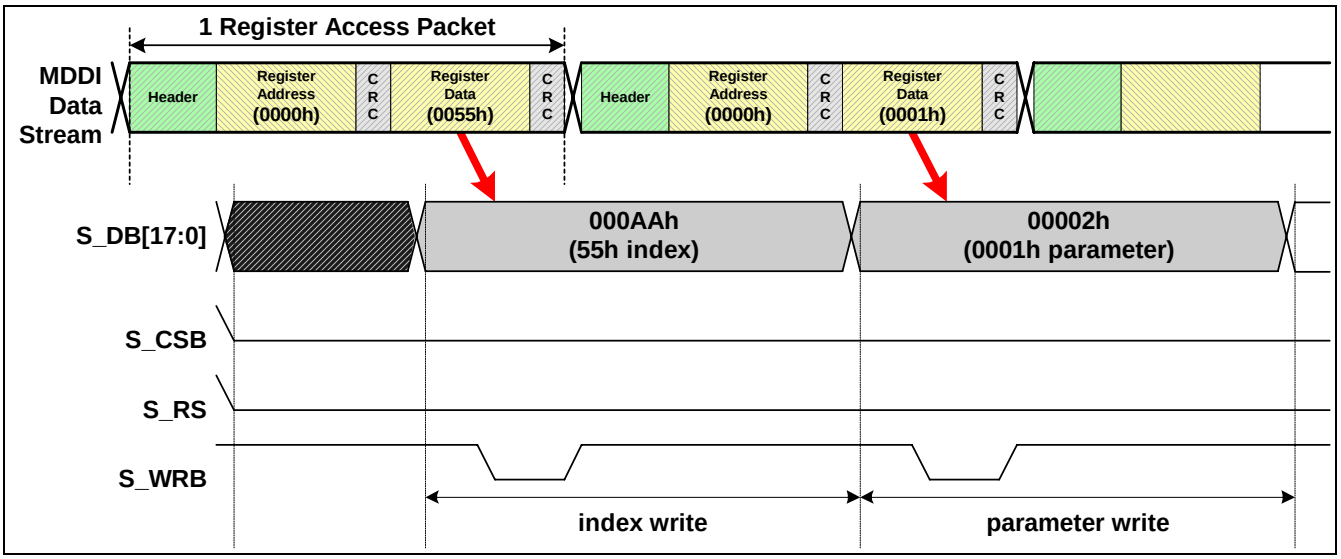


Figure92: 80 mode STN type convetional register instruction

This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is “1”. S_RS is controlled using register address[0] of register access packet.

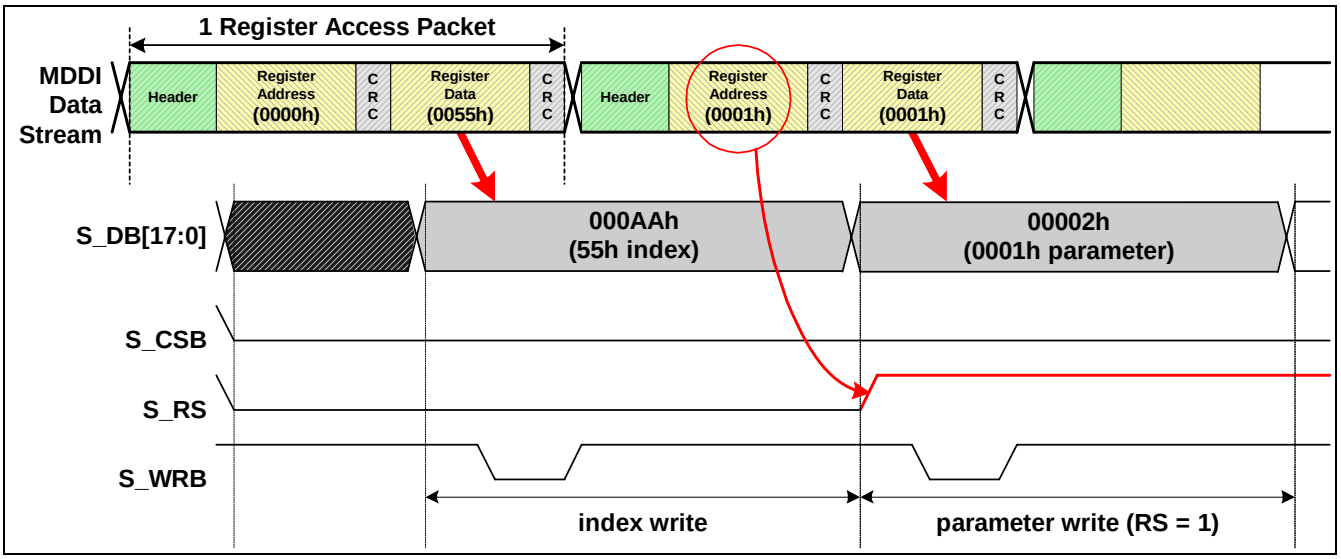


Figure93: 80 mode STN type included parameter

Preliminary

2.2 Video data transfer timing

In STN mode, video data start register (like 22H is TFT mode) does not need generally. But some STN type needs video data start register. If those type STN DDI is used, user has to set the register index.
This figure shows STN 16 bit mode video data transfer.

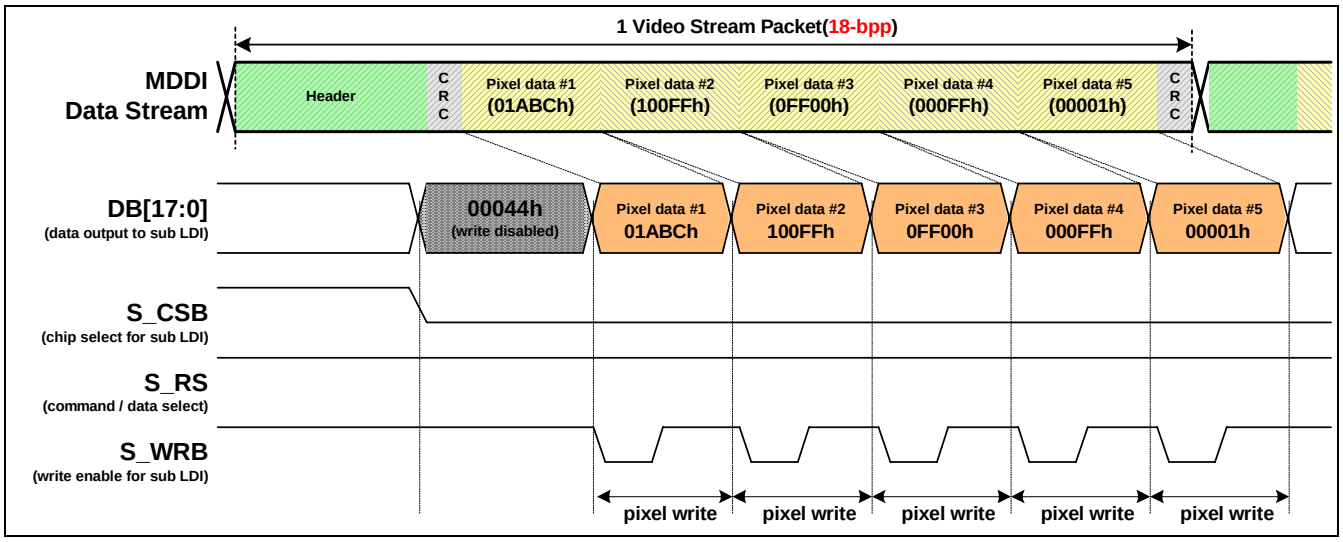


Figure94: 80 mode STN type 16 bit video data transfer

This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. Fist transfer is MSB 8bits, and second is LSB 8bits.

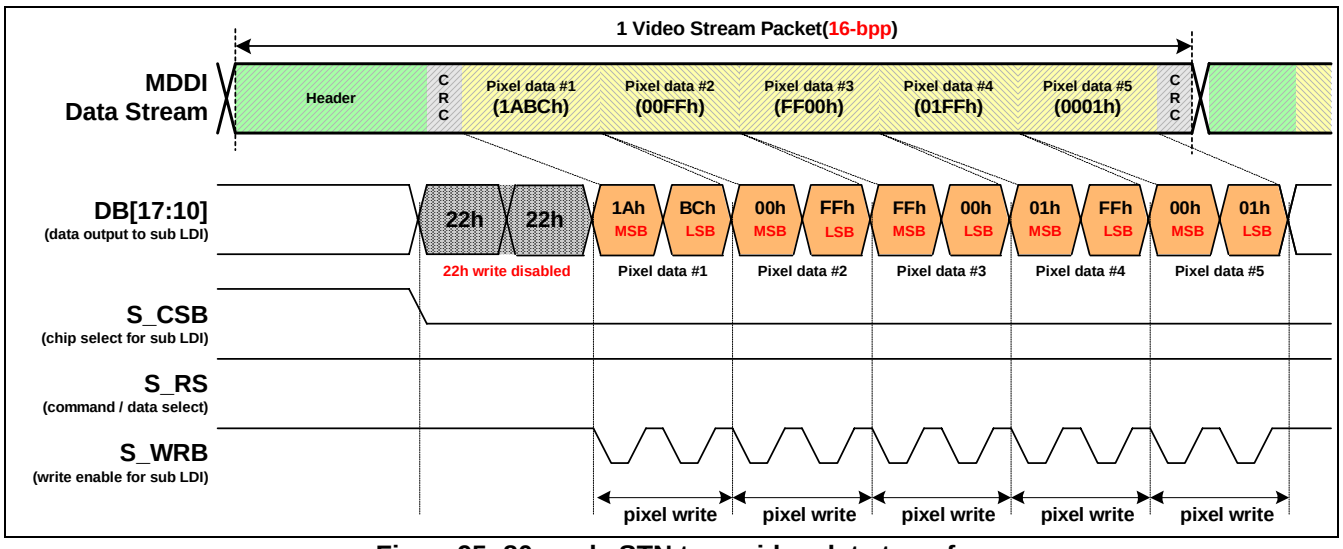
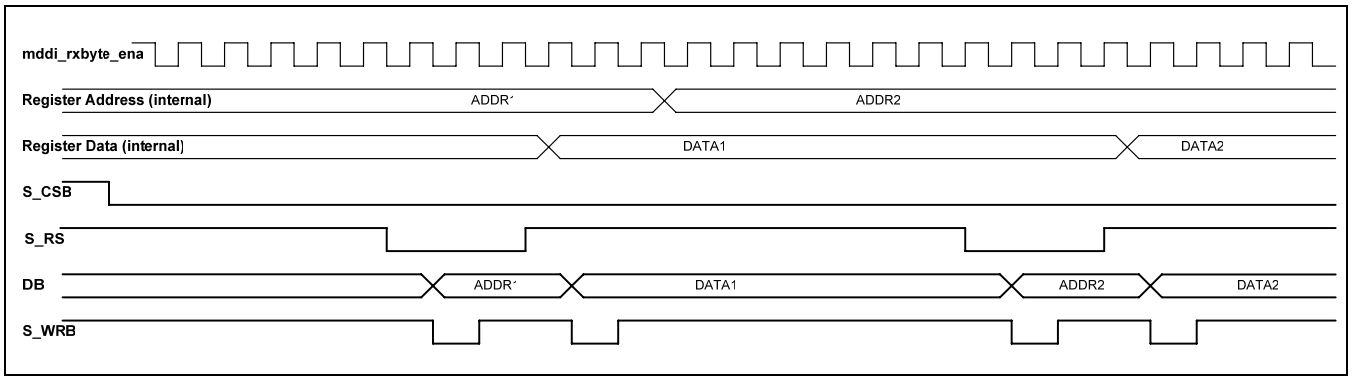


Figure95: 80 mode STN type video data transfer

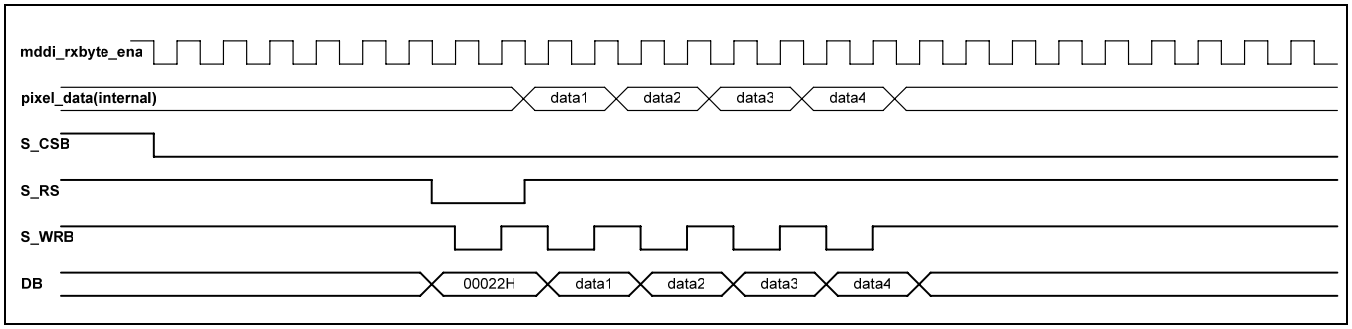
Preliminary

SUB PANEL CONTROL TIMING

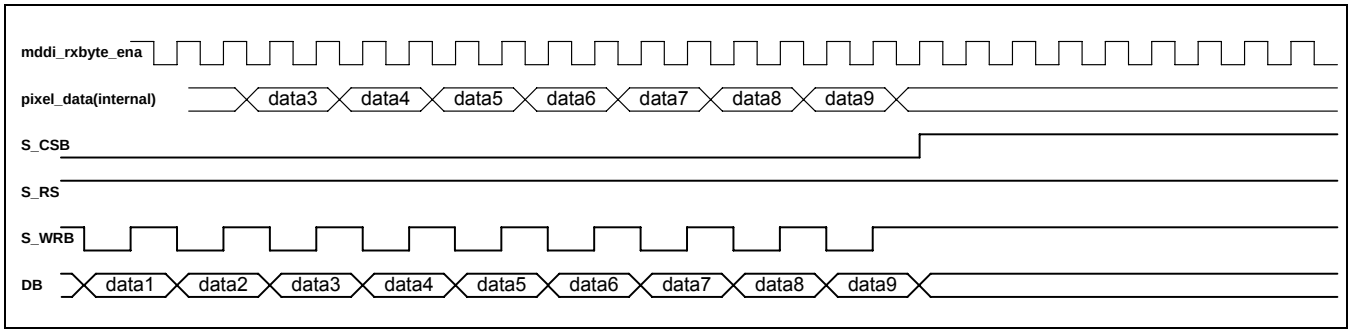
1. Index/parameter write for sub panel LDI



2. Image data write for sub panel LDI



3. Change data path from sub panel to main panel



Preliminary

AMOLED PANEL CONTROL INTERFACE

S6E63D6 outputs some timing signals (FLM, SFTCLK, SFTCLKB, SCLK1, SCLK2, CLA, CLB, CLC, BICTL_L, BICTL_R, EX_FLM, EX_CLK, EX_CLKB, ESR) for controlling an AMOLED panel with built-in gates. S6E63D6 has built-in level shifter for AMOLED panel. Output voltage level for high is VGH voltage, for low is VGL voltage.

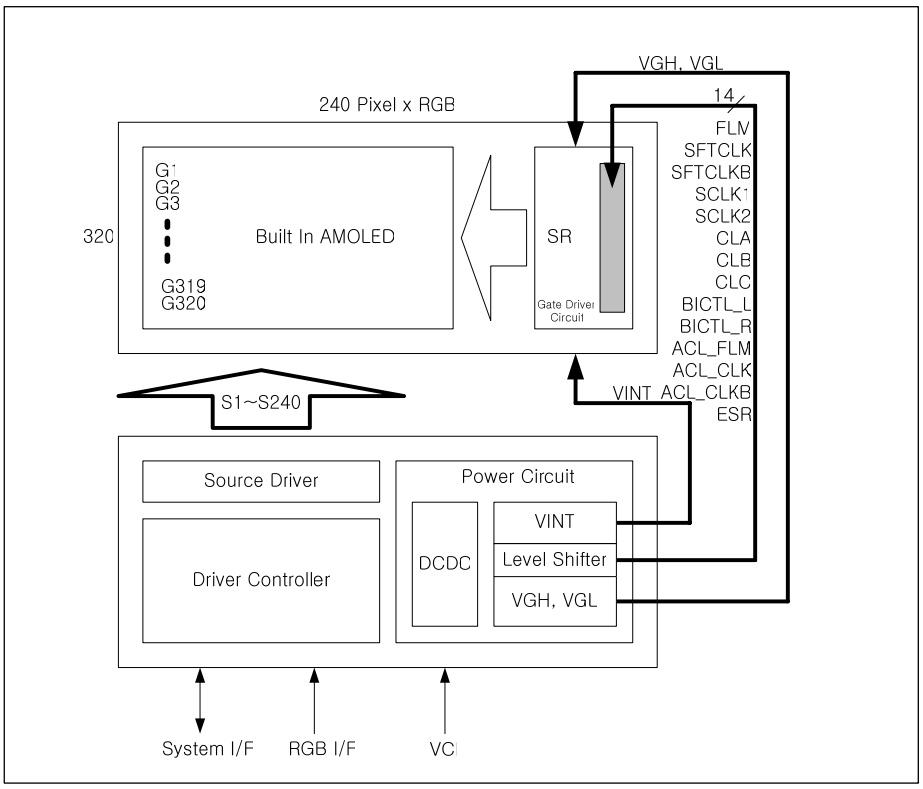


Figure96: An Exemplary Combination

Preliminary

PANEL INTERFACE TIMING

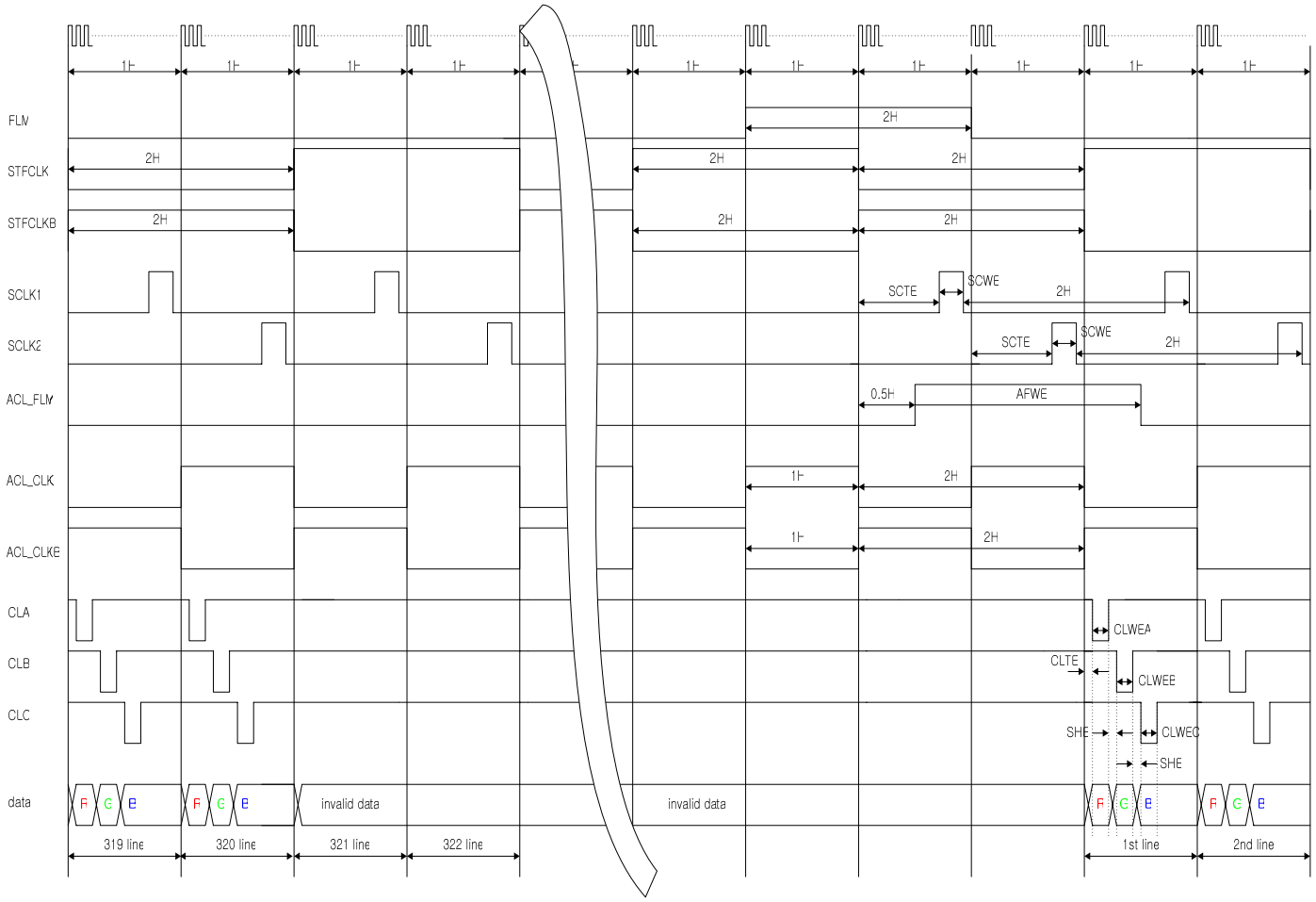


Figure97: Timing Diagram of Panel Interface Signals (GTCON=00)

Preliminary

In Internal Clock Operation mode, the panel interface signals are generated based on internally generated oscillator clock. But in External Clock Operation mode, those are generated based on RGB I/F Signals. The Figure below shows the relation between them for External Clock Operation mode.

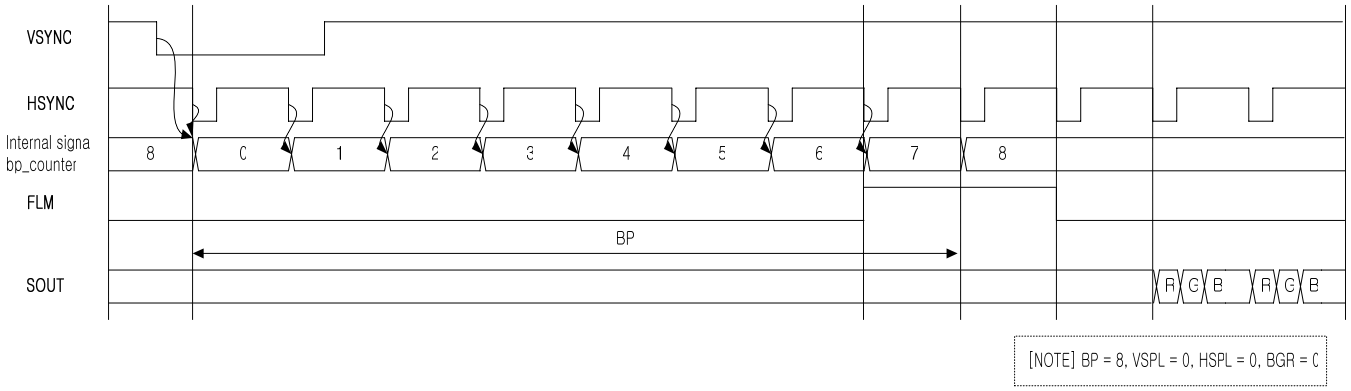


Figure98: VSYNC and Panel Interface Signals in External Clock Operation mode

Preliminary

R, G, B INDEPENDENT GAMMA ADJUSTMENT FUNCTION

S6E63D6 provides the gamma adjustment function to display 262,144 colors simultaneously.

The gamma adjustment is executed by the amplitude adjusting registers and curve adjusting registers.
Since, those control registers incorporate independent adjustment of the gamma function for R, G, B independently, it is highly possible that user determine the best appropriate configuration according to the trait of the display panel.

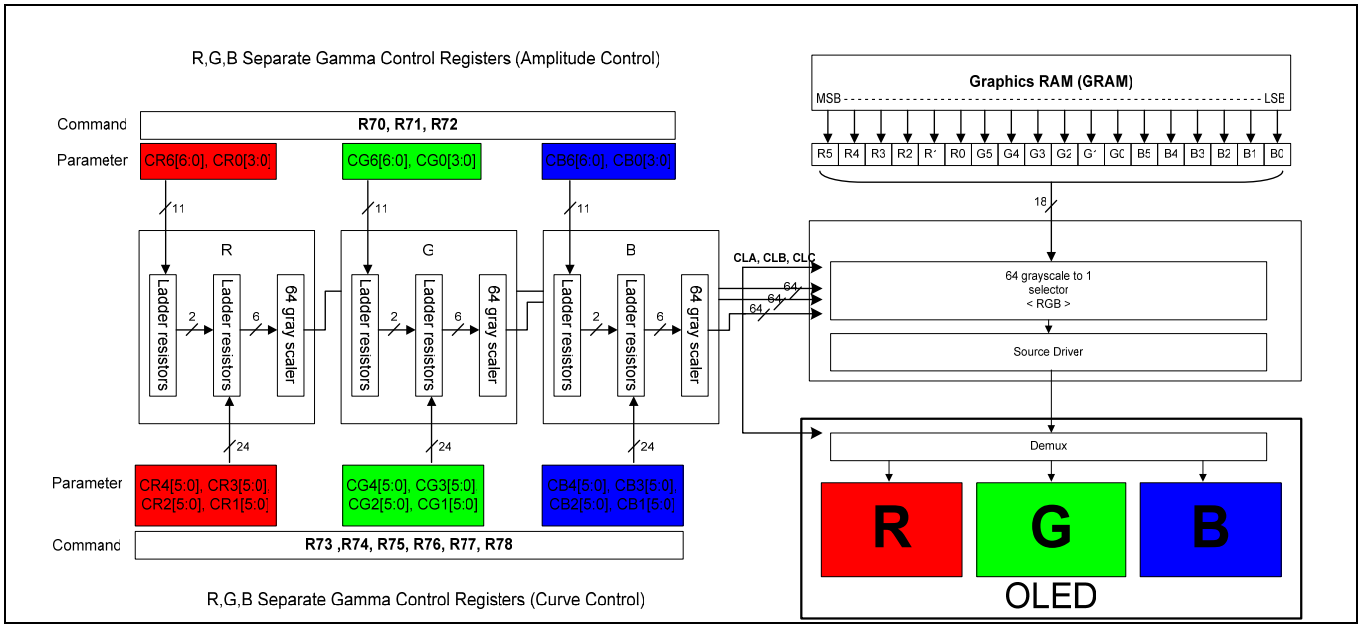


Figure99: Grayscale Control

Preliminary

STRUCTURE of GRAYSCALER

Grayscale level can be determined by registers that adjust both amplitude and curve. Also, the period of each level is split by the internal ladder resistor and generates level between V0 to V63.
Amplitude adjusting part determines upper (V0) and lower (V63) bound voltage and curve adjusting part determines each 4 point (V4, V10, V21, V42) voltages independently for flexible curve control.

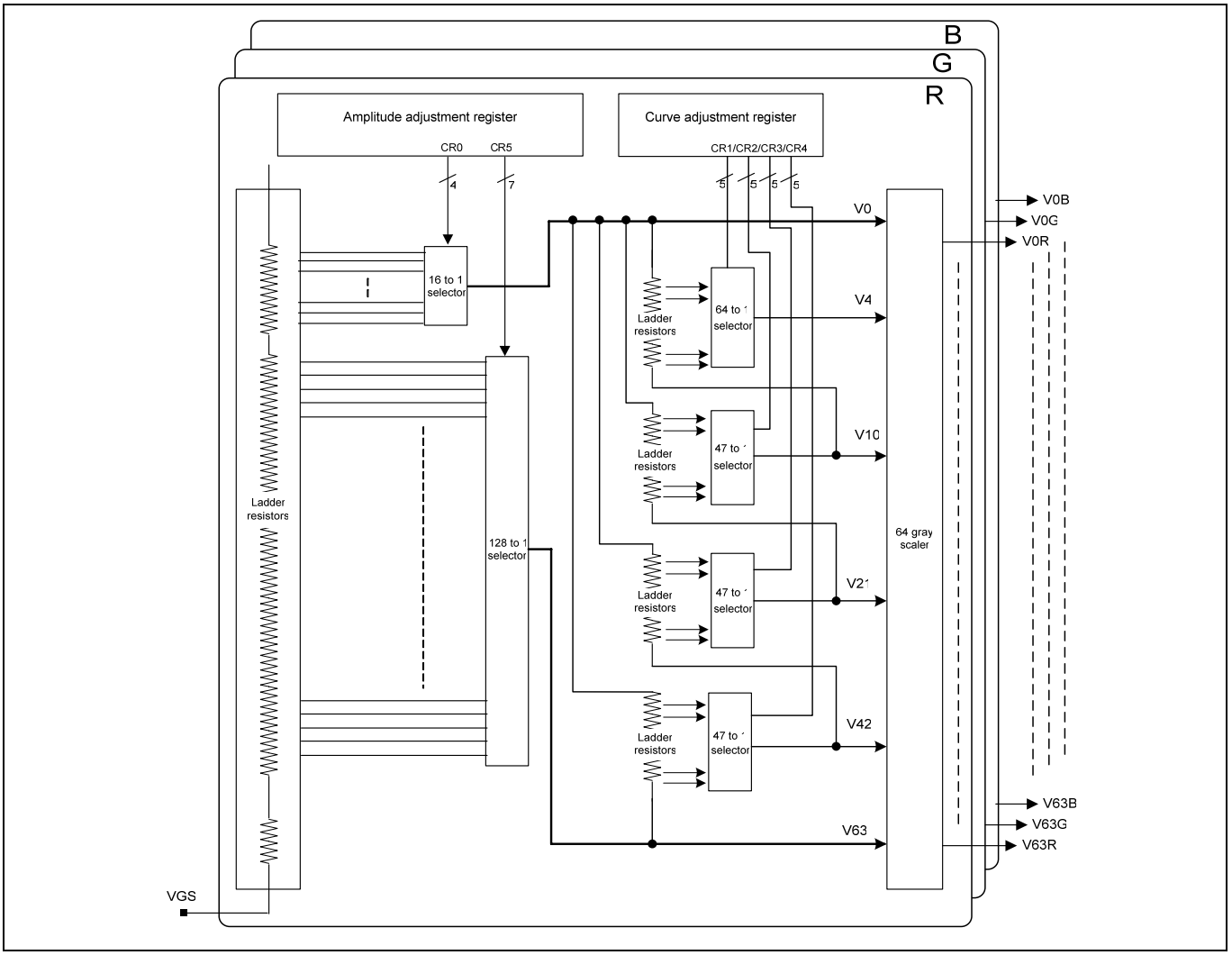


Figure100: Structure of gray scaler

SAMSUNG ELECTRONICS

Preliminary

R, G, B INDEPENDENT GAMMA ADJUSTMENT REGISTERS

These are registers to set up the grayscale voltage in accordance with the gamma specification of the AMOLED panel. The registers can set up both amplitude and curve character of grayscale voltage respectively with corresponding bits as the function of grayscale number. Each configuration can be made for R, G, B independently. There shows the operation of each register below.

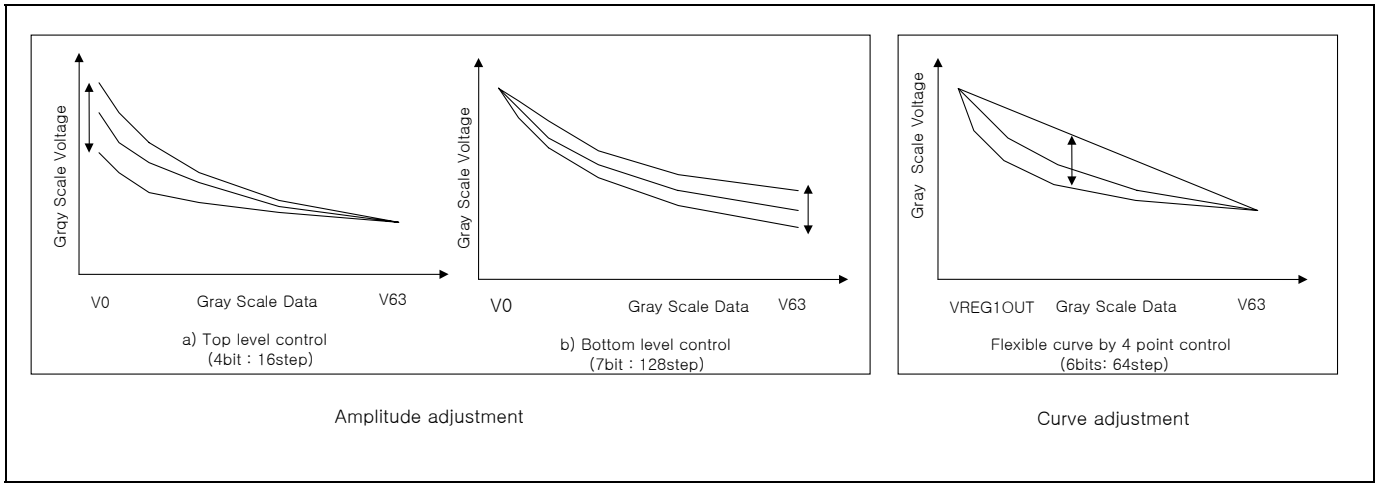


Figure101: The Operation of Adjusting Register

Preliminary

AMPLITUDE ADJUSTING REGISTERS

These are the registers for adjusting the amplitude of grayscale voltage. The registers for adjusting amplitude consists of two parts, one of which is for top level voltage (V0) and the other of which is for bottom level voltage (V63). CR0[3:0], CG0[3:0] and CB0[3:0] registers control the top level voltage. CR5[6:0], CG5[6:0] and CB5[6:0] registers control the bottom level voltage. V0 and V63 are selected in divided voltage from ladder resistor strings between VGS and VREG1OUT. Separate registers are prepared for R, G, B respectively.

Table52: Amplitude adjusting register

Register	for R	for G	for B	Content of configuration
R40H ~ R41H	CR0[3:0]	CG0[3:0]	CB0[3:0]	Grayscale voltage adjusting for top level voltage
	CR5[6:0]	CG5[6:0]	CB5[6:0]	Grayscale voltage adjusting for bottom level voltage

Table53: Relationship between amplitude adjusting register and V0

Register value CR0[3:0], CG0[3:], CB0[3:0]	Formula
0 0 0 0	VREG1OUT – VREG1OUT x (0 /105)
0 0 0 1	VREG1OUT – VREG1OUT x (1 / 105)
0 0 1 0	VREG1OUT – VREG1OUT x (2 / 105)
0 0 1 1	VREG1OUT – VREG1OUT x (3 / 105)
0 1 0 0	VREG1OUT – VREG1OUT x (4 / 105)
0 1 0 1	VREG1OUT – VREG1OUT x (5 / 105)
0 1 1 0	VREG1OUT – VREG1OUT x (6 / 105)
0 1 1 1	VREG1OUT – VREG1OUT x (7 / 105)
1 0 0 0	VREG1OUT – VREG1OUT x (8 / 105)
1 0 0 1	VREG1OUT – VREG1OUT x (9 / 105)
1 0 1 0	VREG1OUT – VREG1OUT x (10 / 105)
1 0 1 1	VREG1OUT – VREG1OUT x (11 / 105)
1 1 0 0	VREG1OUT – VREG1OUT x (12 / 105)
1 1 0 1	VREG1OUT – VREG1OUT x (13 / 105)
1 1 1 0	VREG1OUT – VREG1OUT x (14 / 105)
1 1 1 1	VREG1OUT – VREG1OUT x (15 / 105)

Preliminary

Table54: Relation between amplitude adjusting register and V63

Register value CR5[6:0] CG5[[6:0], CB5[6:0]	Formula
0 0 0 0 0 0 0	VREG1OUT – VREG1OUT x (35 / 210)
0 0 0 0 0 0 1	VREG1OUT – VREG1OUT x (36 / 210)
0 0 0 0 0 1 0	VREG1OUT – VREG1OUT x (37 / 210)
0 0 0 0 0 1 1	VREG1OUT – VREG1OUT x (38 / 210)
0 0 0 0 1 0 0	VREG1OUT – VREG1OUT x (39 / 210)
0 0 0 0 1 0 1	VREG1OUT – VREG1OUT x (40 / 210)
0 0 0 0 1 1 0	VREG1OUT – VREG1OUT x (41 / 210)
0 0 0 0 1 1 1	VREG1OUT – VREG1OUT x (42 / 210)
0 0 0 1 0 0 0	VREG1OUT – VREG1OUT x (43 / 210)
. . .	. . .
1 1 1 0 0 0 0	VREG1OUT – VREG1OUT x (147 / 210)
1 1 1 0 0 0 1	VREG1OUT – VREG1OUT x (148 / 210)
1 1 1 0 0 1 0	VREG1OUT – VREG1OUT x (149 / 210)
1 1 1 0 0 1 1	VREG1OUT – VREG1OUT x (150 / 210)
1 1 1 0 1 0 0	VREG1OUT – VREG1OUT x (151 / 210)
1 1 1 0 1 0 1	VREG1OUT – VREG1OUT x (152 / 210)
1 1 1 0 1 1 0	VREG1OUT – VREG1OUT x (153 / 210)
1 1 1 0 1 1 1	VREG1OUT – VREG1OUT x (154 / 210)
1 1 1 1 0 0 0	VREG1OUT – VREG1OUT x (155 / 210)
1 1 1 1 0 0 1	VREG1OUT – VREG1OUT x (156 / 210)
1 1 1 1 0 1 0	VREG1OUT – VREG1OUT x (157 / 210)
1 1 1 1 0 1 1	VREG1OUT – VREG1OUT x (158 / 210)
1 1 1 1 1 0 0	VREG1OUT – VREG1OUT x (159 / 210)
1 1 1 1 1 0 1	VREG1OUT – VREG1OUT x (160 / 210)
1 1 1 1 1 1 0	VREG1OUT – VREG1OUT x (161 / 210)
1 1 1 1 1 1 1	VREG1OUT – VREG1OUT x (162 / 210)

Preliminary

CURVE ADJUSTING REGISTERS

The curve adjusting registers are used for adjusting the characteristic curve of the grayscale voltage as the function of grayscale number. The registers also control R, G, B independently like the amplitude adjusting register. To accomplish the adjustment, these registers control the each 4 reference voltage by three 47 to 1 selector and a 64 to 1 selector. The 47 or 64 leveled reference voltage generated from the ladder resistor strings between V0 and V63. The registers for adjusting curve consist of 4 reference point – V4, V10, V21 and V42.

Table55: Gamma Curve Adjusting Register

Register	For R	for G	for B	Content of configuration
R43H ~ R46H	CR1[5:0]	CG1[5:0]	CB1[5:0]	Grayscale voltage adjusting for V4
	CR2[5:0]	CG2[5:0]	CB2[5:0]	Grayscale voltage adjusting for V10
	CR3[5:0]	CG3[5:0]	CB3[5:0]	Grayscale voltage adjusting for V21
	CR4[5:0]	CG4[5:0]	CB4[5:0]	Grayscale voltage adjusting for V42

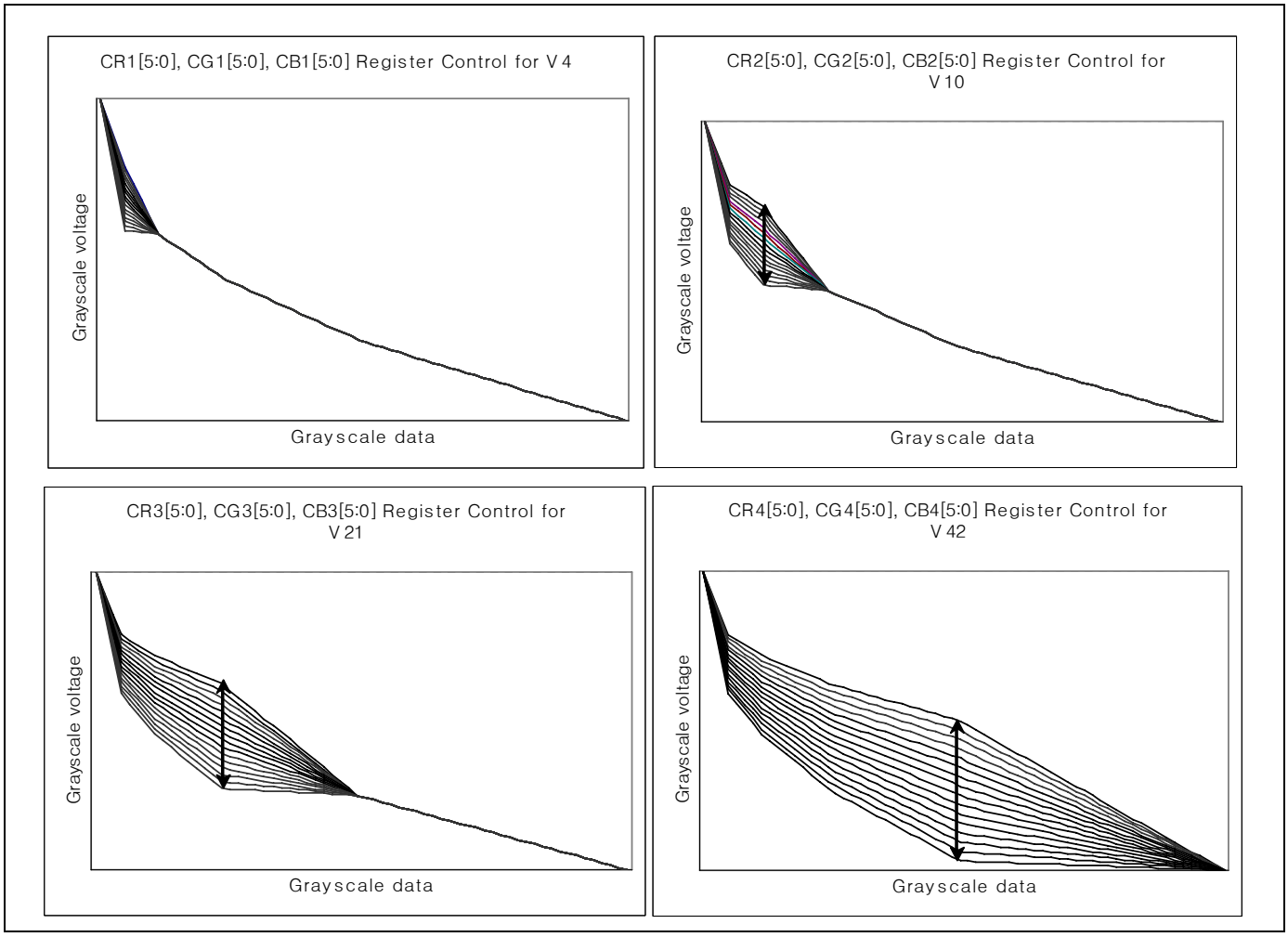


Figure102: Gamma curve adjustment

CURVE ADJUSTING BLOCK

Below appears the table indicating the relation between the value of these registers and voltage-dividing ratio.

Table56: Relationship between value of curve adjusting register and voltage-dividing ratio

Register value	Voltage dividing resistor value	Register value	Voltage dividing resistor value
CR1[5:0] CG1[5:0] CB1[5:0]	**V4 formula**	**CR2[5:0] CG2[5:0] CB2[5:0]**	**V10 formula**
000000	V0 - (V0 – V10) x 98/210	000000	V0 - (V0 – V21) x 193/300
000001	V0 - (V0 – V10) x 99/210	000001	V0 - (V0 – V21) x 194/300
000010	V0 - (V0 – V10) x 100/210	000010	V0 - (V0 – V21) x 195/300
000011	V0 - (V0 – V10) x 101/210	000011	V0 - (V0 – V21) x 196/300
000100	V0 - (V0 – V10) x 102/210	000100	V0 - (V0 – V21) x 197/300
. . .	. . .	. . .	. . .
111011	V0 - (V0 – V10) x 157/210	101010	V0 - (V0 – V21) x 235/300
111100	V0 - (V0 – V10) x 158/210	101011	V0 - (V0 – V21) x 236/300
111101	V0 - (V0 – V10) x 159/210	101100	V0 - (V0 – V21) x 237/300
111110	V0 - (V0 – V21) x 160/210	101101	V0 - (V0 – V21) x 238/300
111111	V0 - (V0 – V21) x 161/210	101110 ~ 111111	V0 - (V0 – V21) x 239/300
CR3[5:0] CG3[5:0] CB3[5:0]	**V21 formula**	**CR4[5:0] CG4[5:0] CB4[5:0]**	**V42 formula**
000000	V0 - (V0 – V42) x 85/150	000000	V0 - (V0 – V63) x 95/150
000001	V0 - (V0 – V42) x 86/150	000001	V0 - (V0 – V63) x 96/150
000010	V0 - (V0 – V42) x 87/150	000010	V0 - (V0 – V63) x 97/150
000011	V0 - (V0 – V42) x 88/150	000011	V0 - (V0 – V63) x 98/150
000100	V0 - (V0 – V42) x 89/150	000100	V0 - (V0 – V63) x 99/150
. . .	. . .	. . .	. . .
101010	V0 - (V0 – V42) x 127/150	101010	V0 - (V0 – V63) x 137/150
101011	V0 - (V0 – V42) x 128/150	101011	V0 - (V0 – V63) x 138/150
101100	V0 - (V0 – V42) x 129/150	101100	V0 - (V0 – V63) x 139/150
101101	V0 - (V0 – V42) x 130/150	101101	V0 - (V0 – V63) x 140/150
101110 ~ 111111	V0 - (V0 – V42) x 131/150	101110 ~ 111111	V0 - (V0 – V63) x 141/150

64 GRAY SCALE OUTPUT VOLTAGE

Below appears the table indicating the relation between the GRAM data value and output voltage value.

Table57: Grayscale Output Voltage Formula

Gray date	Output value	Gray data	Output value
0	**V0**	32	V42 + (V21 – V42) x 10/21
1	V4 + (V0 – V4) x 28/48	33	V42 + (V21 – V42) x 9/21
2	V4 + (V0 – V4) x 12/48	34	V42 + (V21 – V42) x 8/21
3	V4 + (V0 – V4) x 6/48	35	V42 + (V21 – V42) x 7/21
4	**V4**	36	V42 + (V21 – V42) x 6/21
5	V10 + (V4 – V10) x 20/25	37	V42 + (V21 – V42) x 5/21
6	V10 + (V4 – V10) x 15/25	38	V42 + (V21 – V42) x 4/21
7	V10 + (V4 – V10) x 10/25	39	V42 + (V21 – V42) x 3/21
8	V10 + (V4 – V10) x 7/25	40	V42 + (V21 – V42) x 2/21
9	V10 + (V4 – V10) x 3/25	41	V42 + (V21 – V42) x 1/21
10	**V10**	42	**V42**
11	V21 + (V10 – V21) x 21/24	43	V63 + (V42 – V63) x 20/21
12	V21 + (V10 – V21) x 19/24	44	V63 + (V42 – V63) x 19/21
13	V21 + (V10 – V21) x 17/24	45	V63 + (V42 – V63) x 18/21
14	V21 + (V10 – V21) x 14/24	46	V63 + (V42 – V63) x 17/21
15	V21 + (V10 – V21) x 12/24	47	V63 + (V42 – V63) x 16/21
16	V21 + (V10 – V21) x 10/24	48	V63 + (V42 – V63) x 15/21
17	V21 + (V10 – V21) x 8/24	49	V63 + (V42 – V63) x 14/21
18	V21 + (V10 – V21) x 6/24	50	V63 + (V42 – V63) x 13/21
19	V21 + (V10 – V21) x 4/24	51	V63 + (V42 – V63) x 12/21
20	V21 + (V10 – V21) x 2/24	52	V63 + (V42 – V63) x 11/21
21	**V21**	53	V63 + (V42 – V63) x 10/21
22	V42 + (V21 – V42) x 20/21	54	V63 + (V42 – V63) x 9/21
23	V42 + (V21 – V42) x 19/21	55	V63 + (V42 – V63) x 8/21
24	V42 + (V21 – V42) x 18/21	56	V63 + (V42 – V63) x 7/21
25	V42 + (V21 – V42) x 17/21	57	V63 + (V42 – V63) x 6/21
26	V42 + (V21 – V42) x 16/21	58	V63 + (V42 – V63) x 5/21
27	V42 + (V21 – V42) x 15/21	59	V63 + (V42 – V63) x 4/21
28	V42 + (V21 – V42) x 14/21	60	V63 + (V42 – V63) x 3/21
29	V42 + (V21 – V42) x 13/21	61	V63 + (V42 – V63) x 2/21
30	V42 + (V21 – V42) x 12/21	62	V63 + (V42 – V63) x 1/21
31	V42 + (V21 – V42) x 11/21	63	**V63**

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OUTPUT LEVEL AS THE FUNCTION OF GRAM DATA

Output level could be described as the function of GRAM DATA like below.

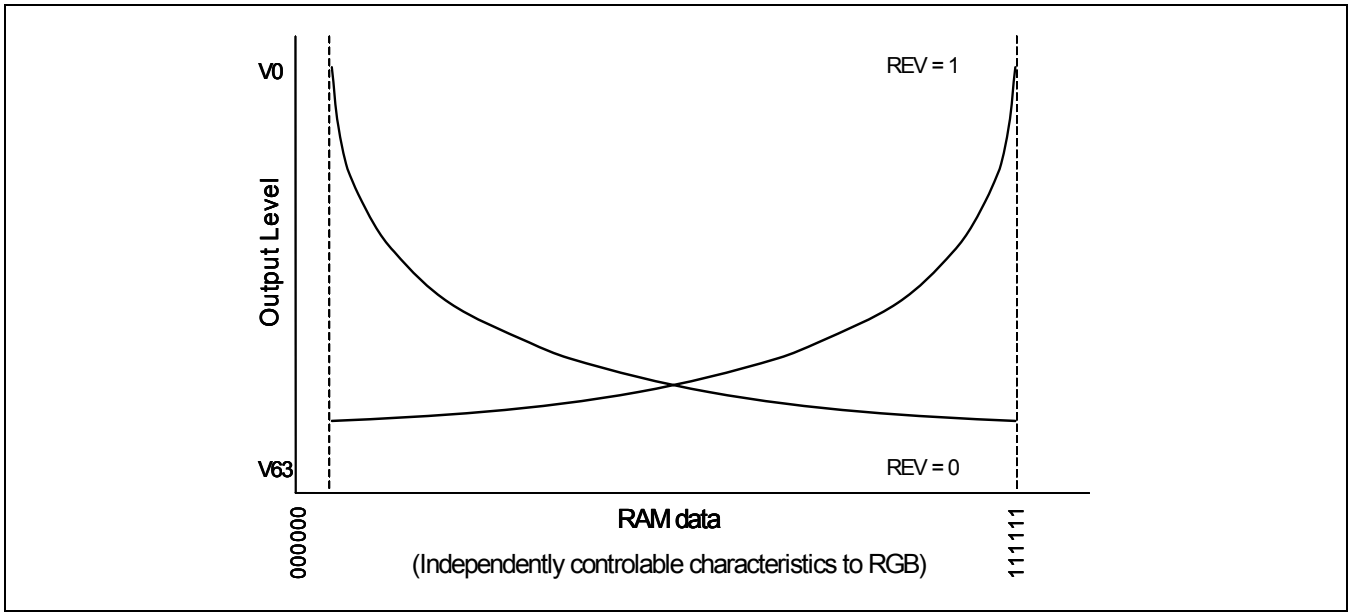

Figure103: Relationship between RAM Data and Output Voltage

Table58: GRAM Data and Grayscale Level

GRAM data	Grayscale		GRAM data	Grayscale		GRAM data	Grayscale		GRAM data	Grayscale	
RGB	REV=0	REV=1	RGB	REV=0	REV=1	RGB	REV=0	REV=1	RGB	REV=0	REV=1
000000	V0	V63	010000	V16	V47	100000	V32	V31	110000	V48	V15
000001	V1	V62	010001	V17	V46	100001	V33	V30	110001	V49	V14
000010	V2	V61	010010	V18	V45	100010	V34	V29	110010	V50	V13
000011	V3	V60	010011	V19	V44	100011	V35	V28	110011	V51	V12
000100	V4	V59	010100	V20	V43	100100	V36	V27	110100	V52	V11
000101	V5	V58	010101	V21	V42	100101	V37	V26	110101	V53	V10
000110	V6	V57	010110	V22	V41	100110	V38	V25	110110	V54	V9
000111	V7	V56	010111	V23	V40	100111	V39	V24	110111	V55	V8
001000	V8	V55	011000	V24	V39	101000	V40	V23	111000	V56	V7
001001	V9	V54	011001	V25	V38	101001	V41	V22	111001	V57	V6
001010	V10	V53	011010	V26	V37	101010	V42	V21	111010	V58	V5
001011	V11	V52	011011	V27	V36	101011	V43	V20	111011	V59	V4
001100	V12	V51	011100	V28	V35	101100	V44	V19	111100	V60	V3
001101	V13	V50	011101	V29	V34	101101	V45	V18	111101	V61	V2
001110	V14	V49	011110	V30	V33	101110	V46	V17	111110	V62	V1
001111	V15	V48	011111	V31	V32	101111	V47	V16	111111	V63	V0

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THE 8-COLOR DISPLAY MODE

The S6E63D6 incorporates 8-color display mode. The voltage levels to be used are VREG1OUT and V63 and all the other grayscale levels V0~V62are halt. So that it attempts to lower power consumption.
During the 8-color mode, the Gamma micro adjustment register, C1R~C4R, C1G~C4G and C1B~C4B are invalid. The level power supply (V0-V62) is in OFF condition during the 8-color mode in order to select VREG1OUT/V63.

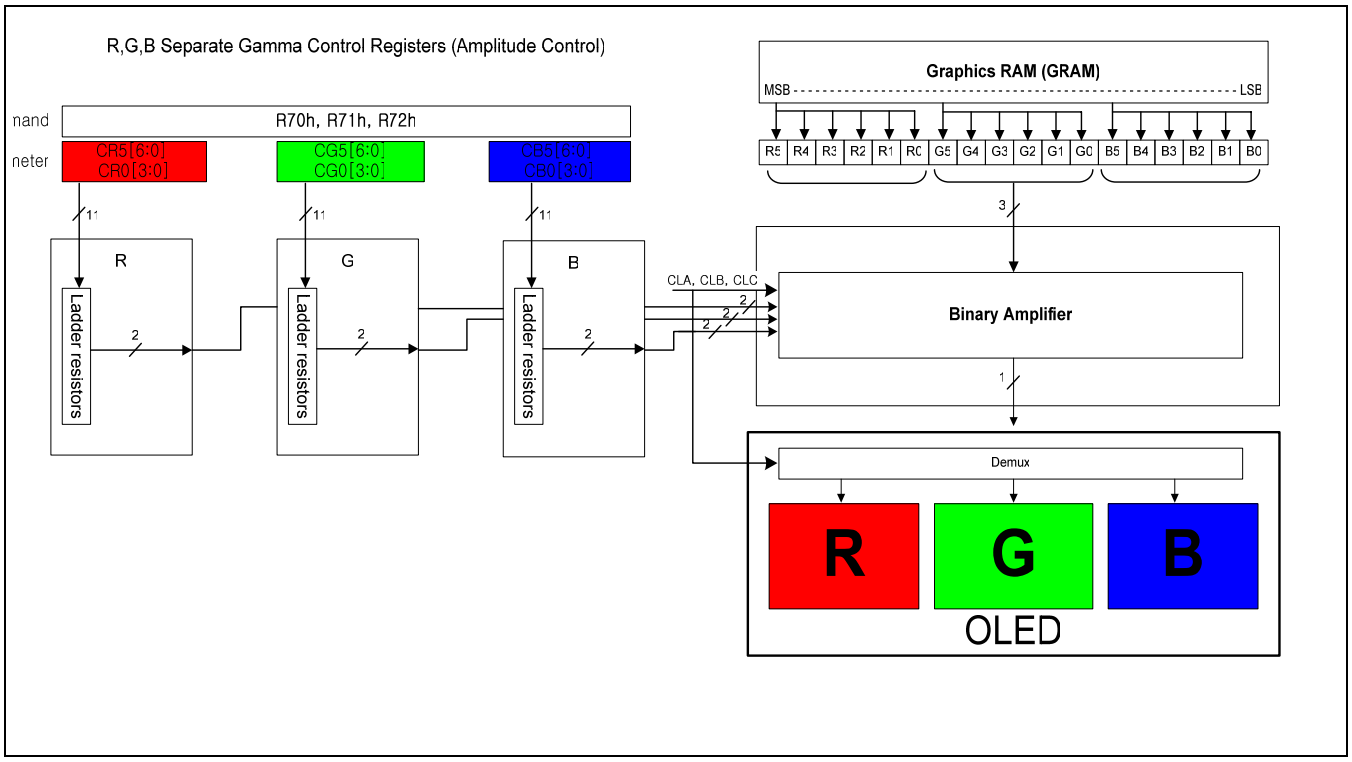

Figure104: 8-color display control

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SET UP FLOW OF STANDBY

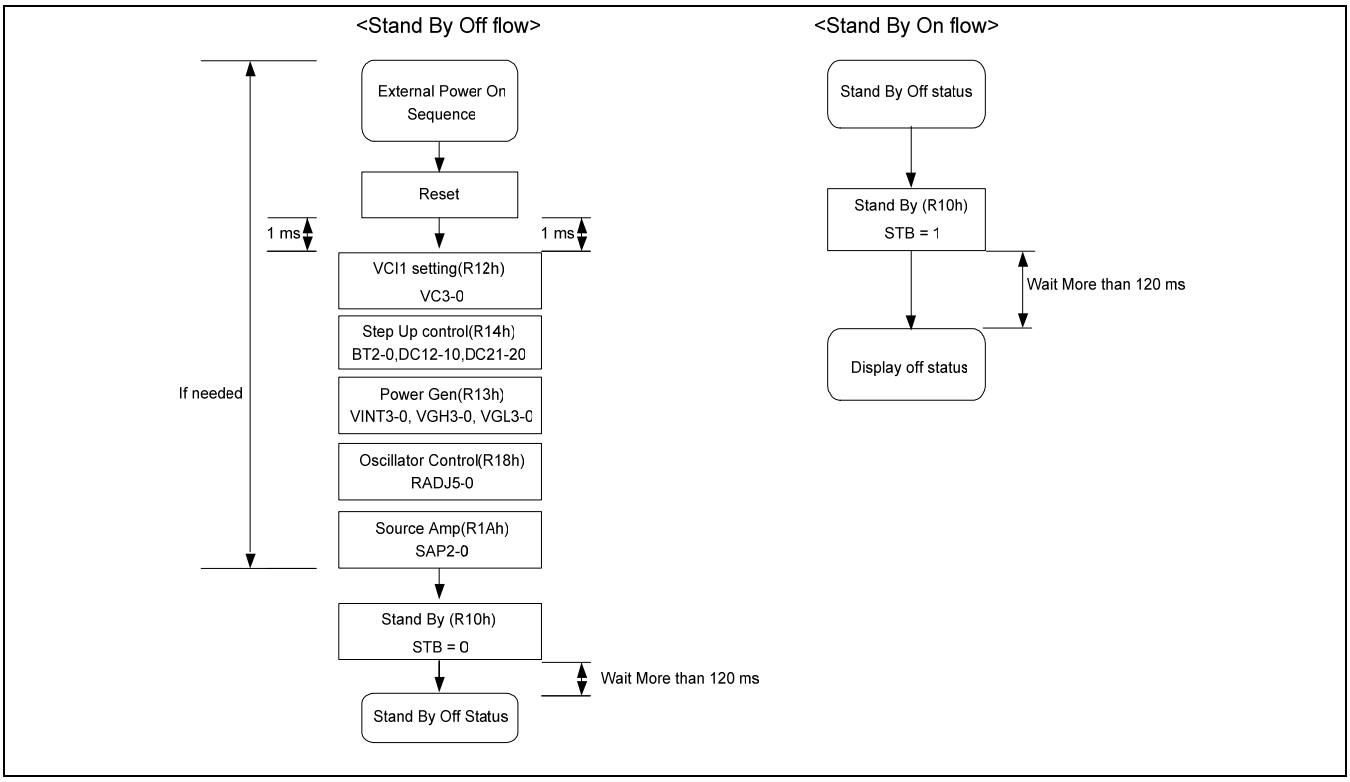

Figure105: Setup flow of STNADBY

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OSCILLATION CIRCUIT

The S6E63D6 can provide R-C oscillation. S6E63D6 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

FRAME FREQUENCY CALCULATION

The relation between the AMOLED driver duty and the frame frequency can be found by the following expression.

$$\text{Frame Frequency} = \frac{\text{fosc}}{64 \times (\text{Line Number} + \text{BP} + \text{FP})}$$

fosc : R-C Oscillation Frequency
Line Number : Number of lines specified by NL
FP : The number of lines for Front Porch (FP)
BP : The number of lines for Back Porch (BP)

Figure106: Formula for the Frame Frequency

EXAMPLE CALCULATION

Parameters	Description
Line Number	320
Frame Frequency	60
BP	8
FP	8
fosc	1,290,240 Hz

■ **Display Clock Frequency**

Table59: DISPLAY CLOCK FREQUENCY

	1 HCLK	1 Horizontal Period
Internal Clock Operation	Fosc / 2	32 HCLKs
External Clock Operation	Fdotclk / 8(RIM=00,01) Fdotclk/24(RIM = 10)	32 HCLKs

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APPLICATION CIRCUIT

The following figure indicates a typical application circuit for S6E63D6.

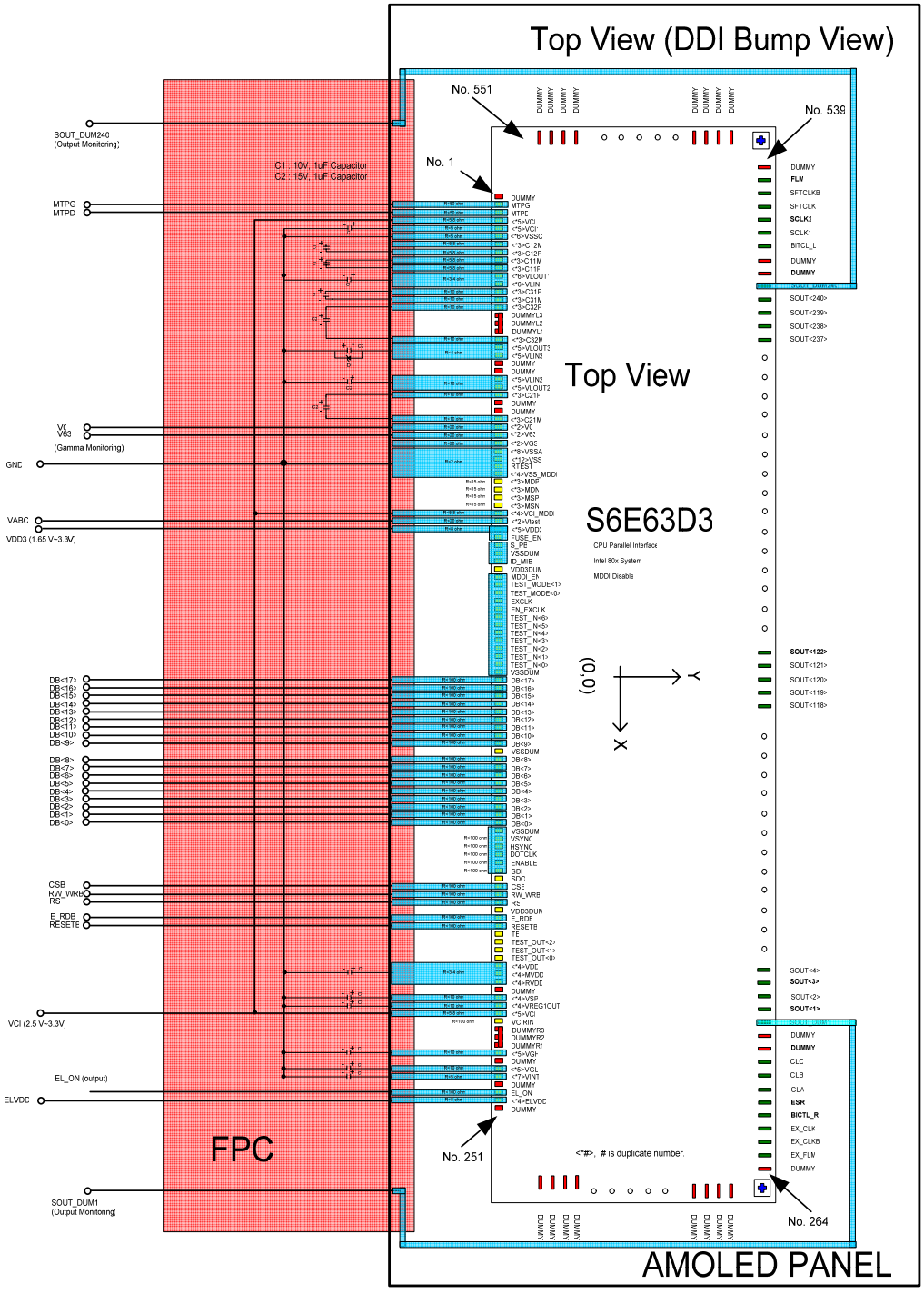

Figure107: S6E63D6 Application (80 System CPU Parallel Interface)

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table60: Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage	VDD3	-0.3 ~ 5.0	V
Supply voltage for step-up circuit	VCI	-0.3 ~ 5.0	V
Supply Voltage range	|VLIN2 – VLIN3|	20	V
Input Voltage range	Vin	-0.3 to VDD + 0.5	V

Notes:

1. Absolute maximum rating is the limit value. When the IC is exposed operating environment beyond this range, the IC do not assure operations and may be damaged permanently, not be able to be recovered.
2. Absolute maximum rating is guaranteed only when our company's package used.

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DC CHARACTERISTICS

Table61: DC Characteristics

(VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	4.6	-	6.6	V	
	VGL		-7.8	-	-5.0	V	
	VINT	-	-4.0	-	-1.0	V	
Photo Sensor Power	VSP	-	2.9	3.0	3.1	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	fosc	Frame frequency = 60Hz Display line = 320 line	1192.3	1324.8	1457.2	kHz	
1st step-up input voltage	VCI1	-	2.1	-	2.75	V	
1st step-up output voltage	VLOUT1	Without load	+4.2	-	+5.5	V	
1st step-up output efficiency	VLOUT1	$I_{\_VLOUT1\_LOAD}$ = 2.3mA	90	95	-	%	
2nd step-up output voltage	VLOUT2	Without load	+6.3	-	+11.0	V	
2nd step-up output efficiency	VLOUT2	$I_{\_VLOUT2\_LOAD}$ = 0.1mA	90	93	-	%	
3rd step-up output voltage	VLOUT3	Without load	-11.0	-	-6.3	V	
3rd step-up output efficiency	VLOUT3	$I_{\_VLOUT3\_LOAD}$ = 0.1mA	90	93	-	%	
Source Output voltage deviation (channel to channel)	-	-	-	±TBD	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	±TBD	-	mV	
Source driver output voltage range	Vso	-	0.96	-	4.2	V	
LTPS driver output voltage deviation	-	-	-	-	TBD	V	
Driving voltage	dVGH	voltage deviation	-	-	TBD	V	
	dVGL		-	-	TBD	V	
Current consumption during normal operation	I_{VDD3}	No load, Ta = 25 °C VCI=2.8V Frame(f)=60Hz	-	-	TBD	uA	-
	I_{VCI}		-	-	TBD	mA	-

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Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power Supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply Voltage	1.65	1.8	3.3	V	
Logic High level input voltage	V_{IH}		0.7*VDD3		VDD3	V	
Logic Low level input voltage	V_{IL}		0.0		0.3*VDD3	V	
Logic High level output voltage	V_{OH}	I_{OUT} = -1mA	0.8*VDD3		VDD3	V	
Logic Low level output voltage	V_{OL}	I_{OUT} = +1mA	0.0		0.2*VDD3	V	
Analog High level output voltage	EL_ON_{OH}	8uA	1.6			V	
Analog Low level output voltage	EL_ON_{OL}	8uA	0		0.4	V	

(VDD3 = 1.65~3.3V, VCI = 2.5~3.3V, Ta = 25℃)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
VREG1OUT		.	4.185	4.2	4.215	V	

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PANEL INTERFACE

GATE IC LESS LEVEL SHIFTER OUTPUT CHARACTERISTICS

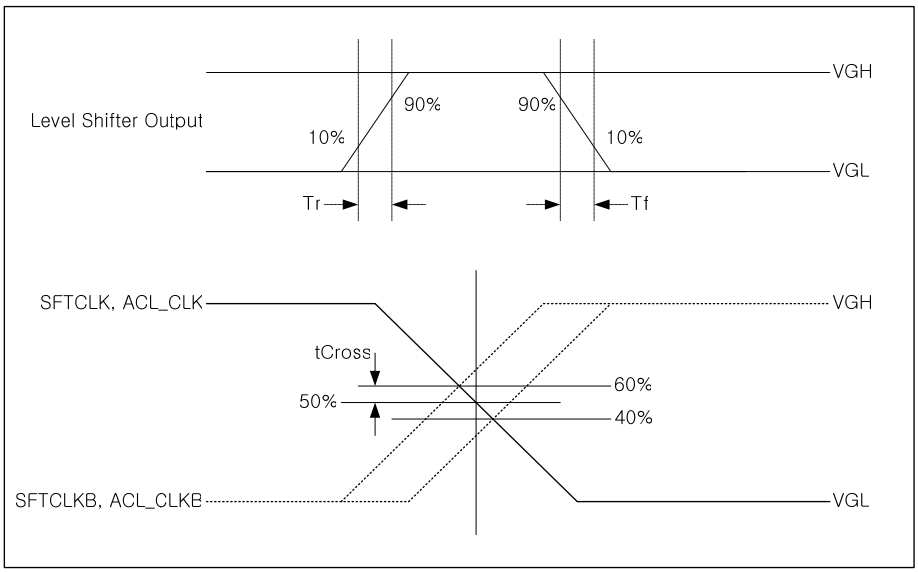

Figure108: AC Characteristics of Level Shifter Output

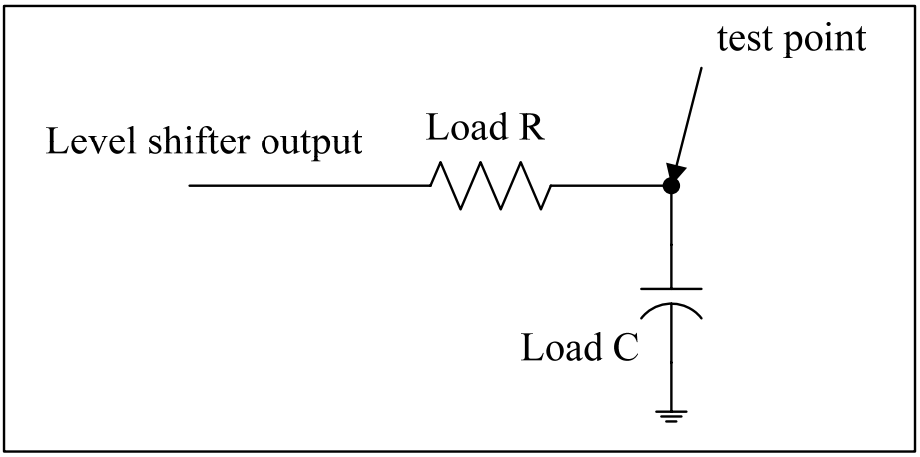

Figure109: LTPS Signal Load Test Point

Table62: AC Parameters of Level Shifter Outputs

	Total Load		Level Shifter Output							
	R(ohm)	C(pF)	High Level	Low Level	Item	Symbol	Min	Typ	Max	Unit
BICTL	1320	78	VGH	VGL	Rising Time	tr	-	-	2000	ns
					Falling Time	tf	-	-	2000	ns
CLA, CLB, CLC	3500	39	VGH	VGL	Rising Time	tr	-	-	500	ns
					Falling Time	tf	-	-	500	ns
FLM	900	42	VGH	VGL	Rising Time	tr	-	-	1000	ns
					Falling Time	tf	-	-	1000	ns
SFTCLK, SFTCLKB	895	61	VGH	VGL	Rising Time	tr	-	-	300	ns
					Falling Time	tf	-	-	300	ns
					Cross Point	rCross	40	50	60	%
SCLK1, SCLK2	895	61	VGH	VGL	Rising Time	tr	-	-	300	ns
					Falling Time	tf	-	-	300	ns
EX_FLM	910	42	VGH	VGL	Rising Time	tr	-	-	1000	ns
					Falling Time	tf	-	-	1000	ns
EX_CLK, EX_CLKB	910	68	VGH	VGL	Rising Time	tr	-	-	350	ns
					Falling Time	tf	-	-	350	ns
					Cross Point	rCross	40	50	60	%
ESR	1320	60	VGH	VGL	Rising Time	tr	-	-	2000	ns
					Falling Time	tf	-	-	2000	ns

SOURCE OUTPUT

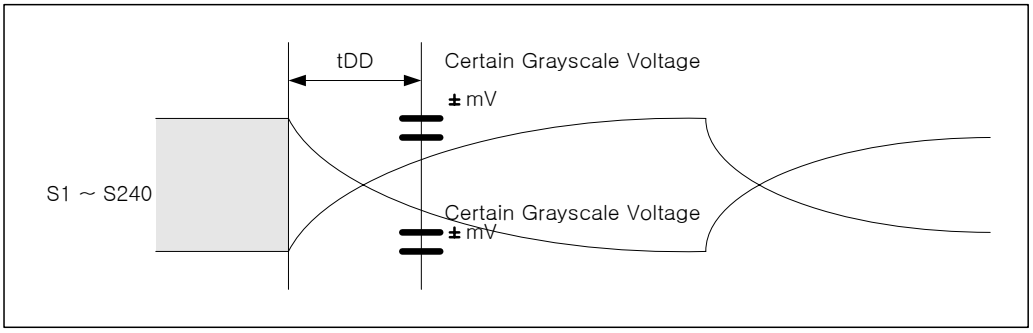

Figure110: AC Characteristics of Source Driver Output

Table63: AC Parameters of Source Driver Output

Symbol	Test Condition	Value
tDD	VCI1 = 2.75 V Fosc = 1324.8 kHz Grayscale to be reached = ±10mV Load Resistance R = 32 Kohm Load Capacitance C = 20pF SAP[2:0]=101	9 usec / 4V max. (with demux)

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VINT Source
- Functions and conditions of VINT output
- During 1H(=51.2us, 1 horizontal line) time, turn on Tr to reset Cst for about 10us
- Peak current = 3.15mA
- VINT ripple(at saturation position) < 100mV
- VINT Saturation time < 7us

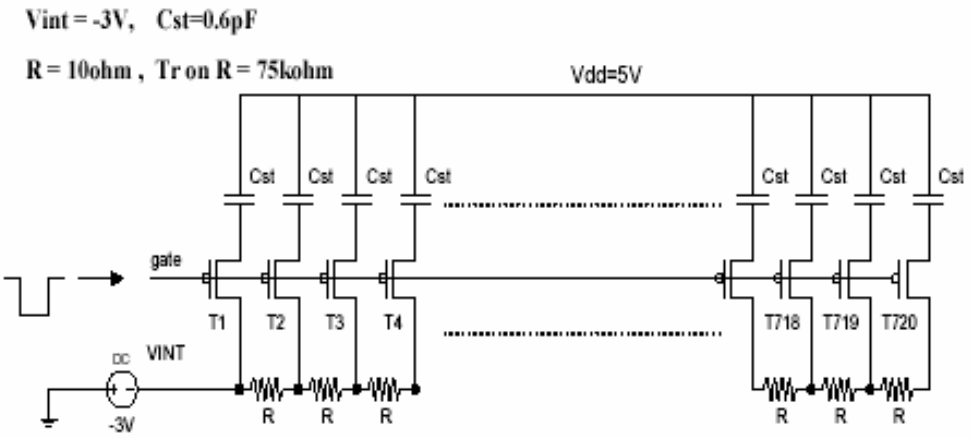


Figure VINT Source Load

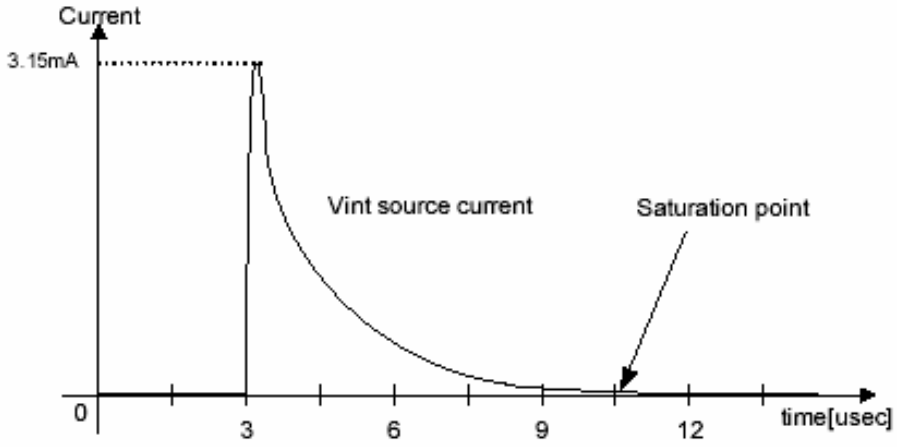


Figure Current Wave of VINT

Figure111: Current Wave of VINT

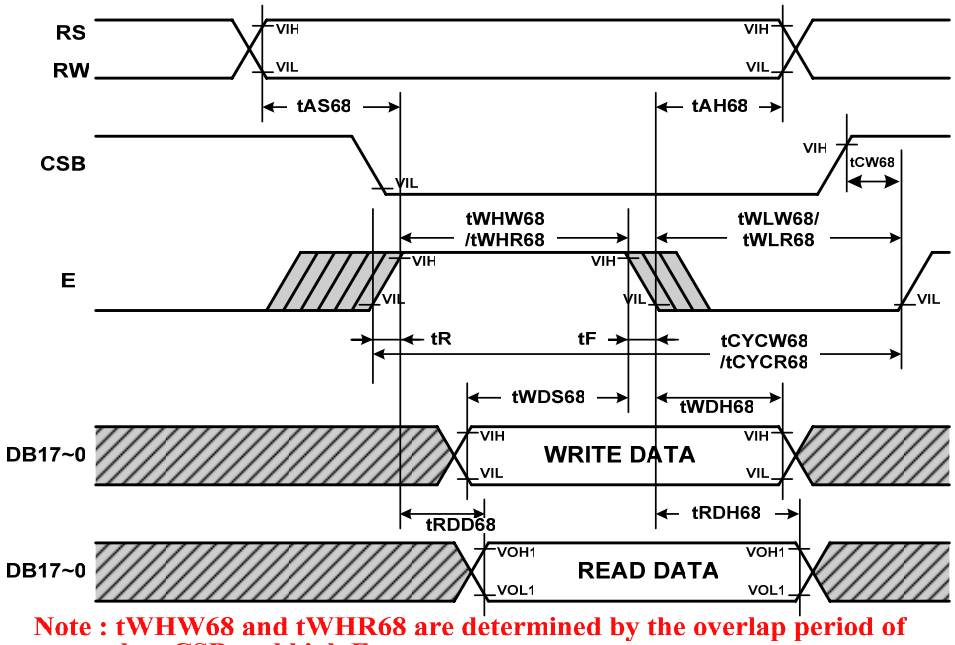
Preliminary

AC CHARACTERISTICS

Table64: Parallel Write Interface Characteristics (68 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW68	TBD	-	ns
	Read	tCYCR68	TBD	-	
Pulse rise / fall time		tR, tF	-	TBD	
Pulse width low	Write	tWHW68	TBD	-	
	Read	tWHR68	TBD	-	
Pulse width high	Write	tWLW68	TBD	-	
	Read	tWLR68	TBD	-	
RS,RW to CSB, E setup time		tAS68	TBD	-	
RS,RW to CSB, E hold time		tAH68	TBD	-	
CSB to E time		tCW68	TBD	-	
Write data setup time		tWDS68	TBD	-	
Write data hold time		tWDH68	TBD	-	
Read data delay time		tRDD68	-	TBD	
Read data hold time		tRDH68	TBD	TBD	



Note : tWHW68 and tWHR68 are determined by the overlap period of low CSB and high E

Figure112: AC Characteristics (68 Mode)

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Table65: Parallel Write Interface Characteristics (80 Mode)

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW80	TBD	-	ns
	Read	tCYCR80	TBD	-	
Pulse rise / fall time		tR, tF	-	TBD	
Pulse width low	Write	tWLW80	TBD	-	
	Read	tWLR80	TBD	-	
Pulse width high	Write	tWHW80	TBD	-	
	Read	tWHR80	TBD	-	
RS to CSB, WRB(RDB) setup time		tAS80	TBD	-	
RS to CSB, WRB(RDB) hold time		tAH80	TBD	-	
CSB to WRB(RDB) time		tCW80	TBD	-	
Write data setup time		tWDS80	TBD	-	
Write data hold time		tWDH80	TBD	-	
Read data delay time		tRDD80	-	TBD	
Read data hold time		tRDH80	TBD	TBD	

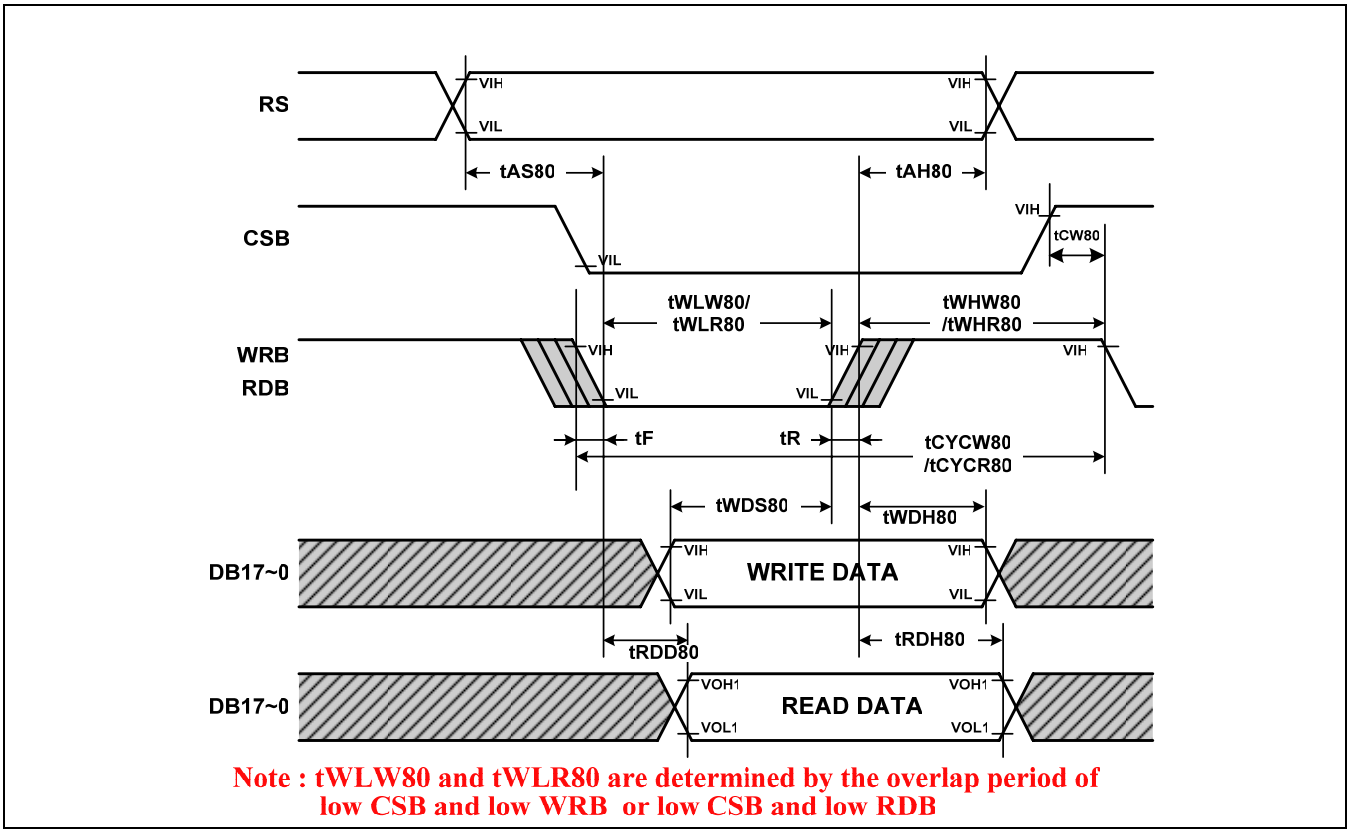

Figure113: AC Characteristics (80 Mode)

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Table66: Clock Synchronized Serial Write Mode Characteristics

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	tscyc	TBD	-	ns
Serial clock read cycle time	tscyc	TBD	-	ns
Serial clock rise / fall time	tR, tF	-	TBD	ns
Pulse width high for write	tSCHW	TBD	-	ns
Pulse width high for read	tSCHR	TBD	-	ns
Pulse width low for write	tSCLW	TBD	-	ns
Pulse width low for read	tSCLR	TBD	-	ns
Chip Select setup time	tCSS	TBD	-	ns
Chip Select hold time	tCSH	TBD	-	ns
Serial input data setup time	tSIDS	TBD	-	ns
Serial input data hold time	tSIDH	TBD	-	ns
Serial output data delay time	tSODD	-	TBD	ns
Serial output data hold time	tSODH	TBD	-	ns

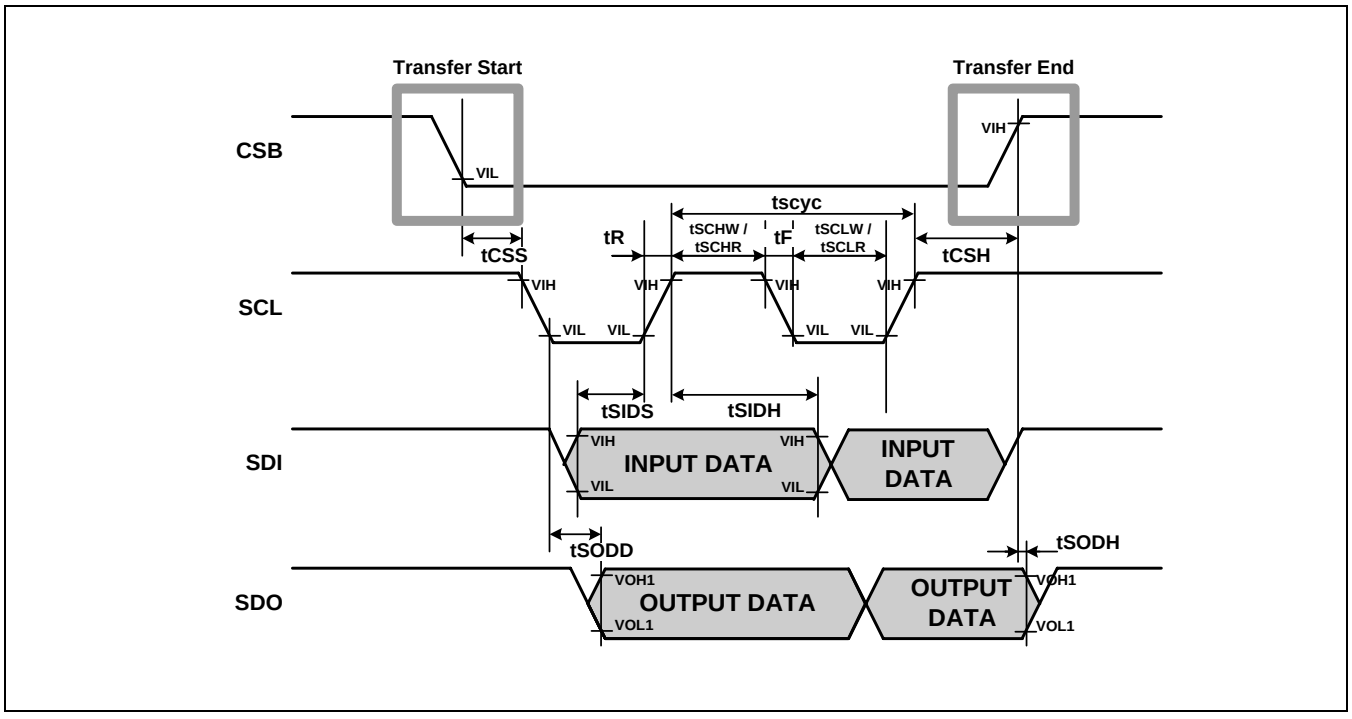

Figure114: AC Characteristics (SPI Mode)

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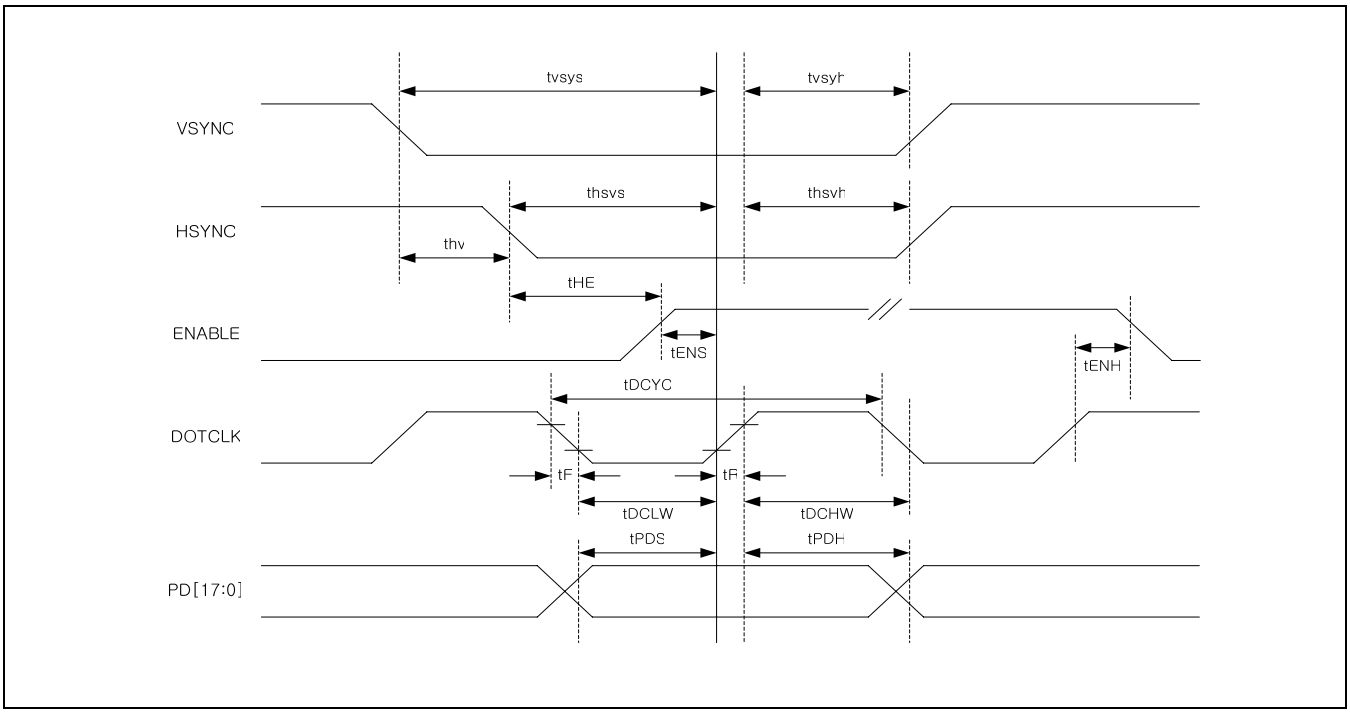
Table67: RGB Data Interface Characteristics

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T_A = -40 to +85°C)

Characteristic	Symbol	18/16bit RGB interface		6bit RGB interface		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	TBD	-	TBD	-	ns
DOTCLK rise / fall time	tR, tF	-	TBD	-	TBD	
DOTCLK Pulse width high	tDCHW	TBD	-	TBD	-	
DOTCLK Pulse width low	tDCLW	TBD	-	TBD	-	
Vertical Sync Setup Time	tvsys	TBD	-	TBD	-	
Vertical Sync Hold Time	tvsyh	TBD	-	TBD	-	
Horizontal Sync Setup Time	thsys	TBD		TBD		
Horizontal Sync Hold Time	thsyh	TBD		TBD		
ENABLE setup time	tENS	TBD	-	TBD	-	
ENABLE hold time	tENH	TBD	-	TBD	-	
PD data setup time	tPDS	TBD	-	TBD	-	
PD data hold time	tPDH	TBD	-	TBD	-	
HSYNC-ENABLE Time	tHE	TBD	HBP	TBD	HBP	tDCYC
VSYNC-HSYNC Time	thv	TBD	TBD	TBD	TBD	

Note : HBP is Horizontal Back-porch.



(When VSPL=0, HSPL=0, DPL=0, EPL=1)

Figure115: AC Characteristics (RGB Interface Mode)

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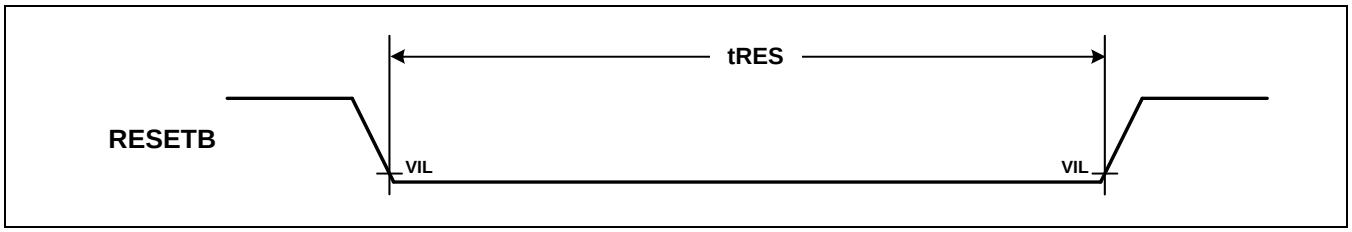
RESET TIMING



Note : Reset low pulse width shorter than 10us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

Figure116: AC characteristics (RESET timing)

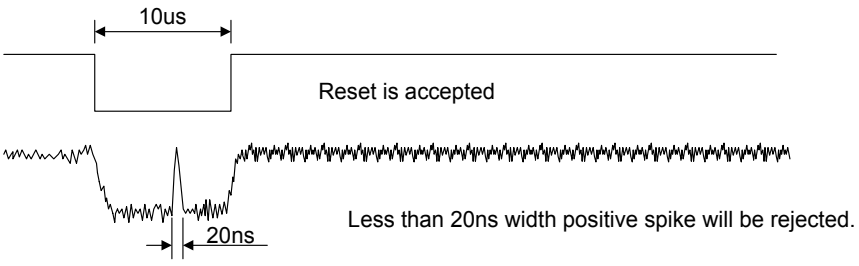
Parameter	Description	Min	Max	Unit
tRES	Reset low pulse width	10	-	us

Table68: Reset Operation regarding tRES Pulse Width

tRES Pulse	Action
Shorter than 5 us	No reset
Longer than 10 us	Reset
Between 5 us and 10 us	Not determined

1. User may or may not use RESETB pin. In order to use it, user should satisfy the conditions described in the above tables. But when not wants to use RESETB, user may fix this pin to VDD3 level because internally generated POR (Power-On-Reset) is used.

2. Spike Rejection also applies during a valid reset pulse as shown below:



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EXTERNAL POWER ON / OFF SEQUENCE

VDD3 must be applied earlier than VCI or at least applied simultaneously with VCI. When regulator cap is 1μF, RESETB must be applied after VCI have been applied. The applied time gap between VCI and RESETB is minimum 1ms. As regulator cap becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

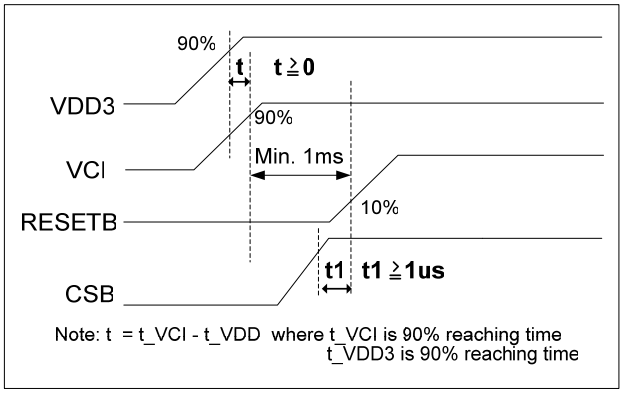

Figure117: External power on sequence

b) EXTERNAL POWER OFF SEQUENCE

VDD3 must be powered down later than VCI or at least powered down simultaneously with VCI. VCI must be powered down after RESETB have been powered down. The time gap of powered down between RESETB and VCI is minimum 1ms. Otherwise function is not guaranteed.

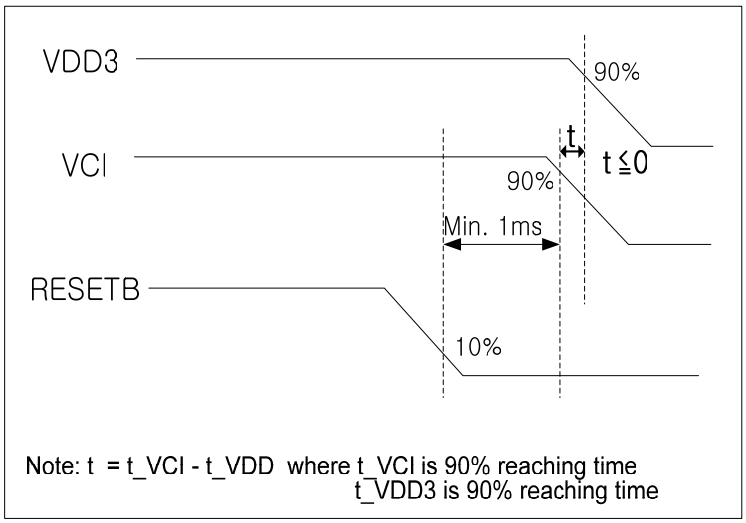

Figure118: External Power Off sequence

Preliminary

NOTICE

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.