

## USE of the ISD4000 with a Low Cost Motorola Microcontroller

ISD Applications Note #1, [How to use the ISD4000 with a Microcontroller](#), described code written for the COPS family of microcontrollers to do basic record and playback in the ISD4000 device family. The ISD-ES302 demo board uses that microcontroller and runs the listed software from Application Note #1.

This Applications Note describes how the Motorola 6805 series of microcontrollers may be used to perform the same function. Specifically, the attached code runs in a MC68HC705J1A 20 pin device and plugs into the ISD-ES302 demo board via an adapter board. Only one change was made on the ES-302 board itself, the addition of a diode. The adapter board and modification to the ES-302 will be described following the software discussion. Much of this design is covered in Applications Note #1, available in the ISD Data Book, 1996 2nd Edition and later data book. Refer to that Application Note for the main board schematic and related explanations. The flow chart for the software is essentially the same for both notes and will not be repeated here.

The one major difference between the code in Applications Note #1 and this one is that the COPS processor has a hardware SPI port and the 'J1A Motorola microcontroller does not. This software, therefore, has routines written to replace the hardware SPI port.

### Major software routines:

The list file of this software will be broken up into pieces and each routine described. Many notes can also be found in the software listing itself. An unassembled source file of this software is available as an Email attachment from ISD Applications Department. Send your request to [apps@isd.com](mailto:apps@isd.com) and ask for the Applications Note Number 3 Source code.

**Program Set Up and Listing Header:** This software was assembled using a 6805 cross assembler purchased from 2500 A.D. Software.

```

2500 A.D. 6805 Macro Assembler - Version 4.01b
-----
Input Filename : DEMO1.ASM
38
39      *
40      *
41      *
42      *
43      *
44      *
45      LIST ON

46      0000      .ABSOLUTE
47
48      *****
49      *Port Definitions      MC68HC705J1A DIP or SOIC Package
50      *PORT A
51      *****
52      0000      porta      equ      0
53      0040      portaDDR   equ      %01000000
54
55      0000      L2          equ      $00      pin 18 - Go to Begin pushbutton
56      0001      L5          equ      $01      pin 17 - Skip to Next pushbutton
57      0002      L6          equ      $02      pin 16 - Play Next pushbutton
58      0003      L1          equ      $03      pin 15 - REC pushbutton
59      0004      L4          equ      $04      pin 14 - STOP pushbutton
60      0005      RAC          equ      $05      pin 13 - Row Address Clock Input
61      0006      LOWBAT      equ      $06      pin 12 - LED control output
62      0007      L7          equ      $07      pin 11 - Play Last pushbutton
63      *
64      *****
65      *PORT B
66      *****
67      0001      portb      equ      1
68      001F      portbDDR   equ      %00011111
69
70      0000      PD          equ      $00      pin 8 - PD pin to ISD2500
71      0001      PLAREC      equ      $01      pin 7 - PLAY/REC pin to ISD2500
72      0002      SSBAR       equ      $02      pin 6 - Slave Select SPI Output
73      0003      SK          equ      $03      pin 5 - SPI Clock output
74      0004      SO          equ      $04      pin 4 - Serial Out
75      0005      SI          equ      $05      pin 3 - Serial In
76      *

```

```

76 *****
77 * Other Pin definitions
78 *****
79 *Pin 10 = VSS (GND)
80 *Pin 20 = RESET\ (active low)
81 *Pin 19 = IRQ\ ISD4000 Interrupt output
82 *Pin 9 = VCC (+5)
83 *Pin 1 = OSC1
84 *Pin 2 = OSC2
85
86 *SOFTWARE ASSUMES A 3.579545 MHz Crystal
87 *PERIOD IS .279365 uSEC, OR INTERNAL CLOCK OF .55873 uSEC
88
89 *CYCLE. -----
90 *
91 *****
92 *area definitions
93 *****
94
95          00C0      RamArea      equ      $00C0
96          00FF      StkTop       equ      $00FF
97          0300      RomArea      equ      $0300
98          07F8      IntVects     equ      $07F8
99 *
100 *****
101 *Vector area
102 *****
103          org      IntVects
104          fdb      TIMESVC
105          fdb      extsvc
106          fdb      swisvc
107          fdb      reset
108 *
109 *
110 *****
111 *Control Register Definitions
112 *****
113
114          0008      TSCR          equ      $8      TIMER STATUS AND CONTROL REG
115          0009      TCR           equ      $9      TIMER COUNTER REGISTER
116          000A      ISCR          equ      $A      IRQ STATUS AND CONTROL
117          0010      PDRA          equ      $10     PULL DOWN REGISTER A
118          0011      PDRB          equ      $11     PULL DOWN REGISTER B
119          07F1      MOR           equ      $07F1
120          07F0      COPR          equ      $07F0
121
122

```

**Flag Registers and System Equates:** The following listing shows the definition of the RAM area in the microcontroller as well as locations of flags, registers and equates. Note that there are two bytes reserved for flags when only one was necessary. Since this program was well within the memory boundaries of the microcontroller, it was not necessary to eliminate this unneeded byte.

```

123 *****
124 *Ram flags and registers
125 *****
126
127          00C0      org      RamArea
128 *****
129          00C0      R00       rmb      1
130 *****
131          0000      PLAYING   equ      $00      Indicates we are Playing
132
133          0001      RECDING   equ      $01      Indicates we are Recording
134          0002      MAKEIT0   equ      $02      Make it zero flag
135          0003      OPERATE   equ      $03
136          *****          equ      $04
137          *****          equ      $05
138          *****          equ      $06
139          *****          equ      $07
140 *****
141          00C1      R01       rmb      1
142 *****
143          *****          equ      $10
144          *****          equ      $11
145          *****          equ      $12
146          *****          equ      $13
147          *****          equ      $14
148          *****          equ      $15
149          *****          equ      $16
150          *****          equ      $17
151 *****
152 *****
153 *NOW SET UP THE REGISTERS USED IN THE PROGRAM
154 *****
155
156          00C2      STRTREGS
157          ADDR1     rmb      1      Address reg LOW
158          ADDR2     rmb      1      Address reg HIGH
159          RECADDL    rmb      1      holds addr of last record (LOW)
160          RECADDH    rmb      1      holds addr of last record (HIGH)
161          SPIONE     rmb      1      SPI Low byte - with control bits
162          SPITWO     rmb      1      SPI High byte - address
163          SEQCNT     rmb      1      Real Time Interrupt counter
164          TOFCNT     rmb      1      Timer Overflow Flag counter
165          00CA      TEMP      rmb      1      USED FOR VARIOUS STUFF

```

```

166 00CB      TEMP1      rmb      1      USED IN DELAY TIMERS
167 00CC      TEMP2      rmb      1      USED only in 16.879 mSEC TIMER
168 00CD      TEMPOUT     rmb      1      Store of acc during SPI activity
169 00CE      TEMPIN      rmb      1      Store of acc during SPI activity
170 *
171 00CF      ENDREG
172 *
173 *NOTE THAT THIS POINT CANNOT GO PAST $ WITHOUT LOOKING AT THE STACK USAGE
174 *****
175 *Define equates and other things
176 *****
177 0004      DDR          equ      4
178 0020      POWRERUP     equ      $20
179 00A0      SETREC       equ      $A0
180 0000      STOPPWRDN    equ      $00
181 0030      STOP        equ      $30      (IAB also set)
182 00E0      SETPLAY      equ      $E0
183 00B0      REC          equ      $B0
184 00E8      SETMC        equ      $E8
185 00F8      MC           equ      $F8
186 00F0      PLAY         equ      $F0
187 0030      RINT         equ      $30      (IAB also set)
188 0070      READADR      equ      $70      (no RUN, IAB set)
189
190
191 *
```

**Interrupt Routines:** The interrupt routines are defined below. Note that the timer interrupt service routine (TIMESVC) and the software interrupt service routine (SWISVC) are not needed in this software. An accidental interrupt to those routines results in an immediate return from interrupt instruction (rti).

The external interrupt routine shuts off the ISD2500 device on the board that is used as a microphone pre-amp and speaker driver. It also sends a STOP opcode to the ISD4000 that is probably not needed because an interrupt from the ISD4000 always results from the end of an operation. The external interrupt routine then checks to see that the interrupt has been cleared, i.e. that the INT pin of the ISD4000 is back HIGH. If it is not, then an early chip revision of the ISD4000 is in the system and the device is in the Overflow interrupt state. To insure compatibility with this early revision device, the routine then sends a SETPLAY opcode with an address of zero and then a STOP opcode to clear the address counter in the ISD4000 and clear the Overflow interrupt.

```

192 *****
193 *Interrupt service routines and subroutine
194 *****
195 00CF      .CODE
196 00CF      .RELATIVE
197 0300      org      RomArea
198 *
199 *
200 0300      TIMESVC
201 *
202 *NOTE: Fop=.5587302 uSec (for a color burst xtal)
203 *
204 *
205 0300      80          rti
206 0300      80          rti
207 0301      80          swisvc
208 0301      80          rti
209 *
210 *-----
211 *
212 *
213 *-----
214 *
215 *-----
216 *
217 *The external int comes from the ISD4000. We first execute a
218 *STOP command to try to clear the interrupt.
219 extsvc
220 0302      10 01      bset      PD,portb      power down ISD2500 audio chip
221 0304      1D 00      bclr      LOWBAT,porta   turn off the LED
222 0306      17 C0      bclr      OPERATE,R00    clear the OPERATE flag
223 0308      A6 30      lda       #STOP
224 030A      CD 04 5E    jsr      SPI_8          stop the operation
225 030D      CD 04 C7    jsr      TPBN          delay
226 *
227 *We should have a cleared int by now. If it's not cleared,
228 *we must be in Overflow.
229 0310      2F 11      bih       ENDINT          Branch if interrupt line is
230 *
231 *We in Overflow. Start play at zero then immediately stop
232 *This should clear the interrupt in a beta ISD4000 device
233 0312      3F C2      clr       ADDRl
234 0314      3F C3      clr       ADDRH
235 0316      A6 E0      lda       #SETPLAY      set up to play message with
236 addr
```

```

243 0318 CD 04 2E      jsr    ADDADDR      add the address to it
244 031B CD 04 6B      jsr    SPI_16      start the playback
245 031B CD 04 6B
246
247      *Now do the STOP
248 031E A6 30          lda    #STOP
249 0320 CD 04 5E      jsr    SPI_8        stop the operation
250
251 0323 80              ENDINT
252 0323 rti
253 0324
254
255      *
256      *-----
257      *----- END OF EXTERNAL INTERRUPT SERVICE ROUTINE -----
258      *-----
259      *
260      ;
261

```

**Initialization:** The reset initialization routine begins at address 324 (all address references are in hexadecimal). Note that the Mask Option Register (MOR) programming is shown for completeness but is “dummied out” so that this otherwise useless code is not executed. The Mask Option Register must be programmed by the EPROM programmer and must be set up manually in most programmers. Note also that the STOP command in line #321 is dummed out; the sleep instruction of the microcontroller is not used in this program.

```

262 ;*****
263 ; INITIALIZE REGISTERS
264 ; POWER UP AND PRESET ROUTINE
265 ;*****
266
267 0324      reset
268      *
269 0324 A6 40      USER      lda    #portaDDR      set up to read push buttons
270 0326 B7 04      sta    porta+DDR
271 0328 A6 1F      lda    #portbDDR
272 032A B7 05      sta    portb+DDR
273
274      *          lda    #$20
275      *          sta    MOR          enable Port A IRQs, no COP, enable
276      *                                     pull down resistors, enable OSC res.
277
278 032C A6 00      lda    #$00          Turn the LED off
279 032E B7 00      sta    porta
280
281 0330 A6 07      *          lda    #$07          SI=LOW+SO=LOW+SK=LOW+SSBAR=HIGH+
282 0332 B7 01      sta    portb          PLAYREC=HIGH + PD=HIGH
283
284 0334 A6 FC      lda    #$FC          enable pull-down res PA0 & PA1
285 0336 B7 10      sta    PDRA
286 0338 A6 3F      lda    #$3F          enable no pull downs on port B
287 033A B7 11      sta    PDRB
288 033C 3F C0      clr    R00
289 033E 3F C2      clr    ADDR1
290 0340 3F C3      clr    ADDRH
291 0342 3F C4      clr    RECADDL
292 0344 3F C5      clr    RECADDH
293 0346 3F CA      clr    TEMP
294
295 0348 5F          clr    x
296
297 0349 A6 0C      lda    #$0C          Clear and disable timer int.
298 034B B7 08      sta    TSCR
299
300 ;***** INITIALIZE ISD3300 *****
301
302 034D A6 20      lda    #POWRRUP
303 034F CD 04 5E      jsr    SPI_8          power up the ISD4000
304
305 0352 A6 20      lda    #POWRRUP
306 0354 CD 04 2E      jsr    ADDADDR      add pwr up info to the addr
307
308 0357 CD 04 6B      jsr    SPI_16      send in an address of all zeros
309
310 035A CD 04 A1      jsr    FLASH1      blink the led once
311
312 035D 9C          rsp
313 035E 9A          cli
314 035F
315
316      STOPPIT
317      *          stop
318
319
320
321
322
323

```

**Main Loop:** The main loop simply looks for push-button closures on 6 switches. When a switch is closed, the routine branches to the proper point down in the code to execute the indicated operation. The microcontroller spends most of it's time in this loop waiting for a switch closure.

```

324 *****
325 * TOP OF THE LOOP. EVERYTHING STARTS FROM HERE *
326 *
327 *****
328 * WAIT FOR AN INPUT HERE *****
329 *
330 *****
331 * MAIN LOOP WAITING FOR A SWITCH CLOSURE *****
332 *
333 * Read the pushbuttons and branch if they are "alive".
334 * READ
335 035F 00 00 11 brset L2,porta,GOTOBEG
336 0362 02 00 1E brset L5,porta,SKIP2NXT
337 0365 04 00 3E brset L6,porta,PLAYNXT
338 0368 06 00 60 brset L1,porta,RECIT
339 036B 08 00 0F brset L4,porta,STOPITX
340 036E 0E 00 0F brset L7,porta,PLAYLASX
341 0371 20 EC bra READ
342
343

```

**GOTOBEG:** The “Go To Beginning” routine only sets the flag bit MAKIT0 (for Make It Zero) located in the R00 flag register. The MAKIT0 bit will be used to indicate to other routines that record or playback should start from address zero of the ISD4000 when next executed. After setting the flag bit, this routine branches to the READX routine which runs a debounce timer. The READX routine is executed after any push-button sequence to effectively debounce the push buttons.

Also, in each of the next 3 routines, SKIP2NXT (Skip to the Next message), PLAYNXT (Play the Next message) and RECIT (Record a message) look at the MAKIT0 bit to see if the address counter should be first be cleared to all zeros before executing the operation. Thus the RECIT routine will be told to begin at zero if the GOTOBEG push button was pressed before the RECIT routine is called. If the push button was not pressed, RECIT will record starting at the end of the last record or play operation without resetting the address counter.

```

344 ***** GO TO Beginning *****
345 *
346 *The Go To Beginning Button is pushed
347 GOTOBEG
348 0373 06 C0 53 brset OPERATE,R00,READZ
349 0376 14 C0 bset MAKEIT0,R00
350
351 0378 CD 04 AC jsr FLASH2 blink the led twice
352 037B 20 4C bra READZ
353 *****
354

```

**Misc:** A couple of the branches are too long. An intermediate jump is needed.

```

357 037D CC 03 F9 STOPITX STOPIT
358 037D CC 03 F9 jmp
359
360 0380 CC 04 05 PLAYLASX PLAYLAST
361 0380 CC 04 05 jmp
362

```

**SKIP2NXT:** This routine sends a SETMC<sup>1</sup> opcode to the ISD4000 with an address of zero if the MAKIT0 bit is set or sends a MC opcode if it is not set. This routine does not start a record or play operation, but merely causes the address counter in the ISD4000 to be modified so that it is left pointed at the “next” message in the device.

```

363 ***** Message Cueing *****
364 *
365 *Now do a message cueing cycle . . . but first, do we do it from zero?
366 SKIP2NXT
367 0383 06 C0 43 brset OPERATE,R00,READZ
368
369 0386 05 C0 13 brclr MAKEIT0,R00,NOCUE0 if this flag clear,
370 * no cue from zero
371
372 *We do a message cueing cycle from address zero
373 bclr MAKEIT0,R00
374 0389 15 C0
375 038B 3F C2 clr ADDRl
376 038D 3F C3 clr ADDRH
377 038F CD 04 A1 jsr FLASH1 blink the LED once
378

```

<sup>1</sup> See the Opcode Summary in the ISD4000 Data Sheet for an explanation of the Instruction Opcodes

```

379
380 0392 A6 E8 lda #SETMC set up to do a msg cue + addr
381 0394 CD 04 2E jsr ADDADDR add the address to it
382 0397
383
384 0397 CD 04 6B jsr SPI_16 do msg cue (but don't play)
385
386
387 039A 20 2D bra READZ debounce and leave
388
389 *we do a message cueing cycle from the last address
390 NOCUE0
391 039C CD 04 A1 jsr FLASH1 blink the LED once
392
393 039F A6 F8 lda #MC
394 03A1 CD 04 5E jsr SPI_8 do msg cue (but don't play)
395
396 03A4 20 23 bra READZ debounce and leave
397
398 *****
399 03A6
400
401

```

**PLAYNXT:** This routine sends a SETPLAY opcode to the ISD4000 with an address of zero if the MAKIT0 bit is set. This causes playback to start at address zero. If the MAKIT0 flag bit is not set, a playback operation begins at whatever address is currently in the ISD4000's internal address pointer. While playback is occurring, only the STOP push button will be recognized by the software.

```

402 ***** Play Next Message *****
403
404 *Play the next message . . . unless Go to Beginning has been pressed
405 03A6 16 C0 79 PLAYNXT
406 03A6 06 C0 79 brset OPERATE,R00,READX check if we already oper.
407 03A9 16 C0 bset OPERATE,R00
408
409 03AB 12 01 bset PLAREC,portb Put the ISD2500 into Play
410 03AD 11 01 bclr PD,portb Power up the ISD2500
411
412 03AF 05 C0 10 brclr MAKEIT0,R00,NOPLA0 if flag clear, no play fm
413 zero
414
415 *We play a message from address zero
416 03B2 15 C0 bclr MAKEIT0,R00 clear the makit it zero flag
417 03B4 3F C2 clr ADDR1
418 03B6 3F C3 clr ADDRH
419 03B8
420 03B8 A6 E0 lda #SETPLAY set up to play a msg with addr
421 03BA CD 04 2E jsr ADDADDR add the address to it
422 03BD
423 03BD CD 04 6B jsr SPI_16 start the playback
424
425 03C0 1C 00 bset LOWBAT,porta turn on the LED
426
427 *Now fall through from starting at zero and send 8 more bits to continue play
428
429 *we really play the "next message"
430 NOPLA0
431 03C2 A6 F0 lda #PLAY load for play with IAB bit set
432 03C4 CD 04 5E jsr SPI_8 start the playback
433
434 03C7 1C 00 bset LOWBAT,porta turn on the LED
435
436 03C9 20 57 READZ bra READX debounce and leave
437
438 *****
439 03CB
440
441

```

**RECIT:** This routine sends a SETREC opcode to the ISD4000 with an address of zero if the MAKIT0 bit is set. This causes record to start at address zero. If the MAKIT0 flag bit is not set, a record operation begins at whatever address is currently in the ISD4000's internal address pointer. While record is occurring, only the STOP push button will be recognized by the software.

An additional function is performed during the RECIT routine and before recording begins. If the MAKIT0 bit is not set, i.e. the internal address is to be used for record, then this address is read out of the ISD4000 using the SPIIN subroutine (which will be explained later). This address is stored in a set of registers<sup>2</sup> so that the PLAYLAST routine can make use of it. If the MAKIT0 bit is set, then a zero is stored in these registers.

```

442 ***** Record Next Message *****
443
444 *Record the next message . . . unless Go to Beginning has been pressed
445 03CB RECIT

```

<sup>2</sup> Since the ISD4000 family uses an address longer than 8 bits, it takes two 8 bit registers to store the address. In the software, these registers are called RECADDL and RECADDH.

```

446
447 03CB 06 C0 54      brset  OPERATE,R00,READX  check to see if already oper
448 03CE 16 C0          bset   OPERATE,R00
449
450 03D0 13 01          bclr   PLAREC,portb    Put the ISD2500 into Record
451 03D2 11 01          bclr   PD,portb      Power up the ISD2500
452
453 03D4 05 C0 16      brclr   MAKEIT0,R00,NOREC0  if flag clear, no rec from
454
455
456                      *We record message from address zero
457 03D7 15 C0          bclr   MAKEIT0,R00      clear the makit it zero flag
458 03D9 3F C2          clr    ADDR0
459 03DB 3F C3          clr    ADDR1
460
461                      *Also clear the "record next" address bytes
462
463
464 03DD 3F C4          clr    RECADDL
465 03DF 3F C5          clr    RECADDH
466
467 03E1 A6 A0          lda     #SETREC      set up to record a message with
addr
468 03E3 CD 04 2E      jsr     ADDADDR      add the address to it
469 03E6 CD 04 6B      jsr     SPI_16       start the recording
470
471 03E9 1C 00          bset    LOWBAT,porta    turn on the LED
472
473 03EB 20 04          bra     NOREC1
474
475                      *Now send 8 more bits to continue record
476
477                      *we really Record the "next message"
478
479 03ED          NOREC0
480 03ED A6 70          lda     #READADR
481 03EF AD 4C          bsr     SPIIN        go read the current addr before
rec
482
483
484 03F1          NOREC1
485 03F1 A6 B0          lda     #REC
486 03F3 AD 69          bsr     SPI_8        start the recording
487
488 03F5 1C 00          bset    LOWBAT,porta    turn on the LED
489
490 03F7 20 29          bra     READX        debounce and leave
491
492 *****
493 03F9
494
495

```

**STOPIT:** This routine sends a STOP opcode to the ISD4000. This interrupts any operation in progress. If a record operation is interrupted, an EOM flag bit is stored in the device to mark the end of the message.

```

496 ***** Stop Recording or Playing *****
497
498                      *Stop whatever we are doing . . . but don't corrupt the address register
499 03F9          STOPIT
500 03F9 A6 30          lda     #STOP
501 03FB AD 61          bsr     SPI_8        stop the operation
502
503 03FD 1D 00          bclr    LOWBAT,porta    turn off the LED
504
505 03FF 17 C0          bclr    OPERATE,R00      turn off the "Operate" flag
506
507 0401 10 01          bset    PD,portb      Power down the ISD2500
508
509 0403 20 1D          bra     READX
510
511 *****
512 0405
513

```

**PLAYLAST:** This routine retrieves the bytes that hold the address stored at the beginning of the last RECIT operation. It then sends a SETPLAY opcode and the address to the ISD4000 so that playback now begins at the address where the "last" recording started from.

```

514 ***** Play Next Message *****
515
516                      *Play the last message we recorded
517 0405          PLAYLAST
518 0405 06 C0 1A      brset    OPERATE,R00,READX  check if we already oper
519 0408 16 C0          bset    OPERATE,R00
520
521 040A 12 01          bset    PLAREC,portb    Put the ISD2500 into Playback
522 040C 11 01          bclr    PD,portb      Power up the ISD2500
523
524
525                      *Go get the address we stored off just before we recorded (It's in
526                      *RECADDH + RECADDL). Put it in the address registers and
527
528
529 040E B6 C4          lda     RECADDL

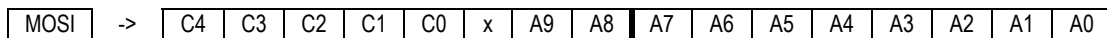
```

```

530 0410 B7 C2          sta    ADDRl
531
532 0412 B6 C5          lda    RECADDH
533 0414 B7 C3          sta    ADDRH
534
535 0416 A6 E0          lda    #SETPLAY      set up to play a message with
536
537 0418 CD 04 2E       jsr    ADDADDR      add the address to it
538 041B CD 04 6B       jsr    SPI_16      start the playback
539
540 041E 1C 00          bset    LOWBAT,porta turn on the LED
541
542 0420 20 A0          bra    NOPLA0      Send 2nd command to set IAB bit
543 *****
544 0422
545
546
547
548 *after doing any and all the stuff, you arrive here to debounce the switches
549 0422 B6 00          READX  lda    porta
550 0424 A4 9F          and    #$9F      only look at the push buttons
551 0426 26 FA          bne    READX      loop until the button is released
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```

**ADDADDR Subroutine:** Whenever we do any of the “SET” operations, we have to add a 10 bit address to the 5 bit ISD4000 opcode. The address starts with A0 in the LSB of the 16 bit word, with the opcode in the left-most 5 bits of the word. Graphically this looks like:



The two bytes to be shifted into the SPI port must be loaded such that the first bit shifted in is A0, the second is A1, etc. with the very last bit shifted into the SPI port being the C4 RUN bit. At that point the Slave Select pin will go HIGH to end the data input and start the operation as indicated by the bytes just shifted in.

In the ADDADDR subroutine, the accumulator brings in the opcode and the address is defined by the data in the ADDRl and ADDRH bytes. ADDRl contains A7 thru A0 and ADDRH holds A9 and A8 in the two LSB locations. This subroutine uses an AND and an OR operation to combine the opcode with bits A9 and A8 of the address and load SPIONE with this data. ADDRl is next written to SPITWO. SPIONE and SPITWO are the two bytes that will be sent out of the SPI port of the micro.

```

560 *****
561 *****
562 * SUBROUTINES START HERE!
563 *****
564 *****
565
566 *****
567 *SUBROUTINE ADDADDR
568 *****
569
570 *This Subroutine adds the address to the control bits already
571 *present in SPIONE. In doing so, it adds a second byte for
572 *16 bit transfers into the ISD4000. This subroutine is
573 *called with a control byte in the accumulator.
574
575 042E B7 C6          ADDADDR sta    SPIONE  put the accumulator into SPI one
576 042E
577
578 0430 B6 C3          lda    ADDRH  get the upper byte of the address
579 0432 A4 03          and    #$03
580 0434 BA C6          ora    SPIONE
581 0436 B7 C6          sta    SPIONE
582
583 0438 B6 C2          lda    ADDRl  Go get the lower byte
584 043A B7 C7          sta    SPITWO
585
586 043C 81            rts
587
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```

**SPIIN Subroutine:** This subroutine is used to read the address data out of the ISD4000 MISO pin before starting a record operation. This saves the “current address” so that a “play last record” operation is possible. Graphically the output side of the ISD4000 SPI port (MISO) looks like:



MISO	<--	OVF	EOM	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	x	0	0	0
------	-----	-----	-----	----	----	----	----	----	----	----	----	----	----	---	---	---	---

The OVF bit is presented to the MISO pin as soon as the Slave Select pin goes LOW. The first clock input to the ISD4000 SPI shifts the EOM to the MISO pin, and subsequent clocks shift the address data out, LSB first. Since we only read the MISO pin after the clock cycle, the OVF bit gets thrown away automatically. Note that the SHIFTIT routine (explained later) shifts the data into TEMPIN byte left to right. This causes the sense of the data to be inverted so that the EOM bit will be in the LSB position of the byte.

After the data is shifted out of the MISO pin, we are left with a byte holding P6 thru P0 plus the EOM bit and a second byte holding P9, P8 and P7. One more linked shift to the right of these two bytes dumps the EOM bit and positions the 10 bit address correctly for later use in the PLAYLAST routine.

It should be noted that whenever you read the ISD4000's SPI port data, you also are shifting data into the device. Accordingly, the calling routine must make sure the data written does not inadvertently start an unwanted operation, or interrupt an operation in progress. When SPIIN is called, the accumulator brings in the 5 bit opcode into the subroutine that is to be written to the MOSI port of the SPI. This routine assumes that an address will not be written into the SPI port at this time. Consequently the first byte written will be all zeros, followed by the second byte containing the opcode.

```

590 *****
591 *SUBROUTINE SPIIN
592 *****
593 * Read the SPI data from the chip, throw out the OVF and EOM
594 * bits, and store the address just retrieved in RECADDL and
595 * RECADDH. The accumulator comes in with the proper 5 bits
596 * of control so that nothing is disturbed.
597
598 SPIIN
599     bclr    SK,portb      Make sure the clock starts LOW
600     bclr    SSBAR,portb  Drop Slave Select
601
602     sta     SPIONE      Save the accumulator for later
603
604     *we shift zeros in first
605
606     clr     TEMP        put all zeros in temp
607     bsr     SHIFTIT
608
609     lda     TEMPIN      get the data just shifted in
610     sta     RECADDL
611
612     * note that EOM bit is still in RECADDL. We will
613     * fix this later.
614
615     lda     SPIONE      go get the original accumulator
616     sta     TEMP
617
618     bsr     SHIFTIT      go do the second byte
619
620     * TEMPIN now has upper 3 bits of the address in it. We wil
621     * shift 1 of those bits into RECADDL. The last 2 bits
622     * in TEMPIN and this becomes RECADDH.
623
624     lsr     TEMPIN
625     ror     RECADDL
626
627     lda     TEMPIN
628     sta     RECADDH
629
630     *
631     bset    SSBAR,portb  Slave Select goes HIGH to end
632     *                               cycle
633     bclr    SO,portb     Leave this LOW when finished
634     rts
635
636
637

```

**SPI\_8 Subroutine:** This subroutine is used to shift 8 bits into the MOSI pin of the ISD4000. The accumulator brings in the byte to be shifted. The SHIFTIT subroutine does the actual shifting of the data.

```

638 *****
639 *SUBROUTINE SPI_8
640 *****
641 *SPI driver subroutine - outputs 8 bits. This routine sends
642 *the SPIONE byte out the bit banged SPI port.
643
644 SPI_8
645     bclr    SK,portb      Make sure the clock starts LOW
646     bclr    SSBAR,portb  Drop Slave Select
647
648     sta     TEMP
649     bsr     SHIFTIT

```

```

650
651      0466      14 01      *      bset      SSBAR,portb      Slave Select goes HIGH to end
652                                     cycle
653      0468      19 01      *      bclr      SO,portb      Leave this LOW when finished
654      046A      81
655      rts
656

```

**SPI\_16 Subroutine:** This subroutine is used to shift 16 bits into the MOSI pin of the ISD4000. The SPITWO byte is shifted in first and the SPIONE bit is shifted in second. The SHIFTIT subroutine does the actual shifting of the data.

```

657      *SUBROUTINE SPI_16
658      *SPI driver subroutine - outputs 16 bits. This routine
659      *the SPIONE and SPITWO bytes out the bit banded SPI port.
660
661      SPI_16
662      bclr      SK,portb      Make sure the clock starts LOW
663      bclr      SSBAR,portb   Drop Slave Select
664      046B      17 01      lda      SPITWO
665      046D      15 01      sta      TEMP
666      046F      B6 C7      bsr      SHIFTIT
667      0471      B7 CA      lda      SPIONE
668      0473      AD 0B      sta      TEMP
669      0475      B6 C6      bsr      SHIFTIT
670      0477      B7 CA      lda      SPITWO
671      0479      AD 05      sta      TEMP
672      047B      14 01      bsr      SHIFTIT
673      047D      19 01      *      bset      SSBAR,portb      Slave Select goes HIGH to end
674      047F      81      *      bclr      SO,portb      Leave this LOW when finished
675      rts
676
677
678
679
680
681
682
683

```

**SHIFTIT Subroutine:** This subroutine does all the shifting of data into and out of the SPI port of the ISD4000. The TEMP register brings in the 8 bit data to be shifted out and the TEMPIN register brings data out of the routine. SHIFTIT talks directly to the ports of the microcontroller.

```

684      *SUBROUTINE SHIFTIT
685      *This subroutine shifts out 8 bits from the SPI Port
686
687      SHIFTIT
688      lda      #8
689      sta      TEMP1      put an 8 count into temp 1
690      0480      A6 08      lda      TEMP
691      0482      B7 CB      OUTAGN      lsr      OUTZERO      shift the LSB into carry bit
692      0484      B6 CA      OUTONE      bset      SO,portb      output a "1"
693      0486      44      bra      CONTSPI
694      0487      24 04      OUTZERO      bclr      SO,portb      output a "0"
695      0489      18 01
696      048B      20 02
697      048D      19 01
698
699      *Now toggle the clock to shift the data
700      CONTSPI      bset      SK,portb
701      048F      16 01      bclr      SK,portb
702      0491      17 01
703
704      *now look at incoming data
705
706      0493      0A 01 03      brset      SI,portb,INONE      it's a 0, clear carry bit
707      0496      98      clc
708      0497      20 01      bra      CONTIN
709
710      0499      99      INONE      sec      it's a 1, set the carry bit
711      049A      36 CE      CONTIN      ror      TEMPIN      bring the bit into the acc
712      049C      3A CB      dec      TEMP1
713      049E      26 E6      bne      OUTAGN
714      04A0      81      rts
715
716
717
718
719
720
721
722

```

**FLASH1 Subroutine:** The FLASH1 subroutine blinks the LED once.

```

723      *SUBROUTINE FLASH1
724      *This subroutine flashes the LED once
725
726

```

```

727
728          04A1          FLASH1
729          04A1      1C 00      bset      LOWBAT,porta      turn on the LED
730          04A3
731          04A3      A6 96      lda      #150
732          04A5      B7 CB      sta      TEMP1      use 150 at the delay
733
734          04A7      AD 22      bsr      KEYDLY      delay
735          04A9      1D 00      bclr     LOWBAT,porta      turn off the LED
736          04AB      81 00      rts
737
738
739

```

**FLASH2 Subroutine:** The FLASH2 subroutine blinks the LED twice.

```

740          *****
741          *SUBROUTINE FLASH2
742          *****
743          *This subroutine flashes the LED twice
744          FLASH2
745          04AC      1C 00      bset      LOWBAT,porta      turn on the LED
746
747          04AE      A6 96      lda      #150
748          04B0      B7 CB      sta      TEMP1      use 150 at the delay
749
750          04B2      AD 17      bsr      KEYDLY      delay
751          04B4      1D 00      bclr     LOWBAT,porta      turn off the LED
752
753          04B6      A6 96      lda      #150
754          04B8      B7 CB      sta      TEMP1      use 150 at the delay
755
756          04BA      AD 0F      bsr      KEYDLY      delay
757          04BC      1C 00      bset      LOWBAT,porta      turn on the LED
758
759          04BE      A6 96      lda      #150
760          04C0      B7 CB      sta      TEMP1      use 150 at the delay
761
762          04C2      AD 07      bsr      KEYDLY      delay
763          04C4      1D 00      bclr     LOWBAT,porta      turn off the LED
764          04C6      81 00      rts
765
766
767

```

**TPBN Subroutine:** This subroutine is used to generate delays in the program. Calling TPBN directly gives approximately a 1/4 second delay. KEYDLY can also be called as a subroutine. In this case, the accumulator brings in a variable that initiates a delay shorter than TPBN.

```

768          *****
769          *SUBROUTINE TPBN
770          *****
771          *USED FOR TIMING VARIOUS STUFF IN THE PROGRAM
772          *
773
774          *TPBN IS THE PUSH BUTTON DELAY IN PUSH BUTTON MODE
775          TPBN      lda      #250      DELAY 250 MILLISECONDS (approx)
776          04C7      A6 FA      sta      TEMP1
777          04C9      B7 CB
778          04CB      B6 CB      KEYDLY  lda      TEMP1      (3)
779          04CD      27 0A      beq      FINDLY      (3)
780          04CF      3A CB      dec      TEMP1      (5)
781
782
783          *****
784          *WAIT1 GENERATES A DELAY (1.154 mSEC)
785          *****
786          *WAIT1 GENERATES A 1.154 MILLISECOND DELAY. IT DOES NOT DISTURB THE
787          *ACCUMULATOR. FROM A BSR (CALLING THIS ROUTINE) THROUGH THE RTS (ENDING
788          *THIS ROUTINE, IT TAKES 2065 CYCLES x 4.3636 uSEC = 1.154 MSec. THIS
789          *
790          *LOOPS 256 TIMES.
791
792          04D1      3F CC      WAIT1  clr      TEMP2      (5)
793          04D3      3C CC      WAIT2  inc      TEMP2      (5)
794          04D5      26 FC      bne      WAIT2      (3)
795
796          04D7      20 F2      bra      KEYDLY      (3)
797
798          04D9      81 00      FINDLY  rts
799
800
801          *
802
803
804
805
806
807
808
809
810          * NOTE: THE LAST USABLE ADDRESS IS $7CF
811          ;
812
813

```

814  
815

## Push Button Operation Notes:

816 \*Instructions:  
817 \*Six of the 9 push-buttons are labeled on the PCB. Pushing the Yellow  
818 \*"Go to Beg" button will reset the address pointer to the front of the  
819 \*chip or address 000. The indication that this has been done will be a  
820 \*double flash of the LED, D11, in the bottom left corner of the PCB.  
821 \*  
822 \*Pushing the Red "Record" button will turn on the Red LED to indicate  
823 \*that the chip is now recording anything it hears at the microphone M1  
824 \*near the top center of the board. The board will continue to Record  
825 \*until the end of the chip is reached or the Black "Stop" button is pressed.  
826 \*At that time the LED will go out and the board will stop Recording.  
827 \*  
828 \*Pushing the White "Play Last" button will playback what you have just  
829 \*recorded. This message will play through to its end or stop when you  
830 \*press the Black "Stop" button  
831 \*  
832 \*Pushing the Yellow "Go to Beg" button, and then the White "Play Next"  
833 \*button will play messages from the beginning of memory through to its  
834 \*end or stop/pause when you press the Black "Stop" button. To resume  
835 \*playback push play-next again if playback is paused. To play the next  
836 \*message press play next again.  
837 \*  
838 \*The Blue "Skip to Next" button will let you bypass a message and play  
839 \*the one after that message. For example, had you recorded three messages,  
840 \*beginning at the front of the chip, and gone back to the beginning after  
841 \*the last message then you could press the White "Play Next" button to play  
842 \*message #1, press the Blue "Skip to Next" button to bypass message #2 and  
843 \*then Press the White "Play\_Next" to play message #3.  
844  
845  
846

## Cross Reference Listing:

Defined	Symbol Name	Value	References
575	ADDADDR	042E	243 309 381 421 468 536
158	ADDRH	00C3	240 292 376 418 459 533 578
157	ADDRL	00C2	239 291 375 417 458 530 583
Pre	CODE	00C0	195
716	CONTIN	049A	712
705	CONTSPI	048F	699
120	COPR	= 07F0	
Pre	DATA	= 0000	
177	DDR	= 0004	270 272
251	ENDINT	0323	234
171	ENDREG	00CF	
798	FINDLY	04D9	779
728	FLASH1	04A1	313 378 391
744	FLASH2	04AC	352
347	GOTOBEG	0373	334
714	INONE	0499	710
116	ISCR	= 000A	
97	IntVects	= 07F8	103
778	KEYDLY	04CB	734 750 756 762 796
57	L1	= 0003	337
54	L2	= 0000	334
588	L4	= 0004	338
555	L5	= 0001	335
56	L6	= 0002	336
61	L7	= 0007	339
60	LOWBAT	= 0006	223 425 434 472 488 503 540 729 735
745			
134	MAKEIT0	= 0002	751 757 763
185	MC	= 00F8	349 369 373 412 416 453 457
119	MOR	= 07F1	393
804	MSGTABL	04DA	
390	NOCUE0	039C	369
430	NOPLA0	03C2	412 542
479	NOREC0	03ED	453
484	NOREC1	03F1	474
135	OPERATE	= 0003	224 348 367 406 407 447 448 505 519
520			
695	OUTAGN	0486	719
698	OUTONE	0489	
701	OUTZERO	048D	696
Pre	PAGE0	= 0000	
69	PD	= 0000	221 410 451 507 523
117	PDRA	= 0010	287
118	PDRB	= 0011	289
70	PLAREC	= 0001	409 450 522
186	PLAY	= 00F0	431
132	PLAYING	= 0000	
518	PLAYLAST	0405	361
360	PLAYLASX	0380	339
405	PLAYNXT	03A6	336
178	POWRRUP	= 0020	305 308
806	PTTABL	04DA	
130	R00	00C0	224 290 348 349 367 369 373 406 407
412			416 447 448 453 457 505 519 520

```

Lines Assembled : 846           Assembly Errors : 0

```