	Computer Architecture	e and Organization	L T P J C
D • • • •	VEE 1001		
Pre-requisite	ITE1001		Syllabus version
Course Objective	ş•		1.0
	e architecture of computer system.		
	te the various design aspects of com	nputer system	
	rize with the latest technologies		design, instruction
Expected Course	Outcome:		
1) Learn the f	undamentals of architecture in comp	puter systems.	
2) Learn, desi	gn and implement the various algor	ithms of computer arithm	etic operations.
3) Describe th	e various data representation techni	iques in number systems.	
4) Compreher	d the various architectures and orga	anization of memory syste	ems.
5) Understand	the concepts of virtual memory in	memory management.	
6) Evaluate th	e latest technologies of memory, I/O	O, ALU design and instru	ction execution
7) Compreher	d and understand the concepts of de	evice subsystems in mem	ory management.
Student Learning	Outcomes (SLO): 1, 2, 4		
	ty to apply knowledge of mathema	tics, science, and engineer	ring
TITIAVING AN AUN		d concepts and of contemp	~
	understanding of the subject related		orary issues
[2] Having a clear	Making Skills of creating unique		
[2] Having a clear [4] Having Sense-		insights in what is being	•
[2] Having a clear [4] Having Sense- (Higher level t	Making Skills of creating unique ninking skills which cannot be codi	insights in what is being fied)	g seen or observed
[2] Having a clear [4] Having Sense- (Higher level t	Making Skills of creating unique ninking skills which cannot be codi	insights in what is being fied) ure	g seen or observed 9 hour
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect e von Neumann machine; Instruction	insights in what is being fied) ure on formats; Pipeline - fetcl	g seen or observed 9 hour n/execute cycle,
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decoding	Making Skills of creating unique ninking skills which cannot be codi	insights in what is being fied) ure on formats; Pipeline - fetclister files; Instruction type	g seen or observed 9 hour n/execute cycle,
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decoding	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect evon Neumann machine; Instruction and execution; Registers and registers	insights in what is being fied) ure on formats; Pipeline - fetclister files; Instruction type	g seen or observed 9 hour n/execute cycle,
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decodin modes; Subroutine	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect evon Neumann machine; Instruction and execution; Registers and registers	insights in what is being fied) ure on formats; Pipeline - fetclister files; Instruction type	9 hour n/execute cycle, es and addressing
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decodir modes; Subroutine Module:2 Com Data Representati	Making Skills of creating unique ninking skills which cannot be codi mamentals Of Computer Architect evon Neumann machine; Instruction and execution; Registers and registerly and return mechanisms; Other outer Arithmetic on, Hardware and software implession.	insights in what is being fied) ure on formats; Pipeline - fetcl ister files; Instruction type design issues.	9 hour n/execute cycle, es and addressing 5 hour unit for common
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decodin modes; Subroutine Module:2 Com Data Representati arithmetic operati	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect e von Neumann machine; Instruction ag and execution; Registers and registers and return mechanisms; Other outer Arithmetic on, Hardware and software implements: addition, subtraction, multiplements.	insights in what is being fied) ure on formats; Pipeline - fetcl ister files; Instruction type design issues.	9 hour n/execute cycle, es and addressing 5 hour unit for commo
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decodin modes; Subroutine Module:2 Com Data Representati arithmetic operati	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect e von Neumann machine; Instruction ag and execution; Registers and registers and return mechanisms; Other outer Arithmetic on, Hardware and software implements: addition, subtraction, multiplements.	insights in what is being fied) ure on formats; Pipeline - fetcl ister files; Instruction type design issues.	9 hour n/execute cycle, es and addressing 5 hour unit for common
[2] Having a clear [4] Having Sense- (Higher level t Module:1 Fund Organization of th instruction decodin modes; Subroutine Module:2 Comp Data Representati arithmetic operati point)-floating poi	Making Skills of creating unique ninking skills which cannot be codi amentals Of Computer Architect e von Neumann machine; Instruction ag and execution; Registers and registers and return mechanisms; Other outer Arithmetic on, Hardware and software implements: addition, subtraction, multiplements.	insights in what is being fied) ure on formats; Pipeline - fetcl ister files; Instruction type design issues.	9 hour n/execute cycle, es and addressing 5 hour unit for commo

order functions from square roots to transcendental functions; Representation of non-numeric data

(character codes, graphical data)

Module:4	Memory System Organiz	zation And Archit	tecture	4 hours		
Memory systems hierarchy; Coding, data compression, and data integrity; Electronic, magnetic						
and optical technologies; Main memory organization, Types of Main memories, and its						
characteristics and performance; Latency, cycle time, bandwidth, and interleaving; Cache						
memories (address mapping, line size, replacement and write-back policies)						
Module:5	Virtual Memory			4 hours		
Virtual memory systems-paging, segmentation, address mapping, page tables, page replacement						
algorithms;	Reliability of memory syste	ems; error detectin	g and erro	r correcting systems		
Module:6	Interfacing And Commu	nication		8 hours		
I/O fundam	entals: handshaking, bufferi	ng; I/O techniques	: program	med I/O, interrupt-driven I/O,		
DMA; Buse	es: bus protocols, local and	geographic arbitra	ation. Inte	errupt structures: vectored and		
prioritized,	interrupt overhead, interrup	ts and reentrant co	de			
Module:7	Device Subsystems			7 hours		
External storage systems; organization and structure of disk drives and optical memory; Flash						
memories, Basic I/O controllers such as a keyboard and a mouse;RAID architectures; I/O						
Performanc	e; SMART technology and	fault detection				
Module:8	Contemporary issues:			3 hours		
		Total Lecture ho	urs:	45 hours		
Text Book(s)						
1. J. L. Hennessy & D.A. Patterson, Computer architecture: A quantitative approach, Fifth						
Edition, Morgan Kaufman, 2012.						
Reference Books						
1. W. Stallings, Computer organization and architecture, Seventh Edition, Prentice-Hall, 2013						
2. M. M. Mano, Computer System Architecture, Third Edition, Prentice-Hall 2008.						
3. J. P. Hayes, Computer architecture and Organization, Third edition, McGraw Hill, 2012.						
	Recommended by Board of Studies 05-03-2016					
Approved b	y Academic Council	No. 40	Date	18-03-2016		