CA Laboratory

Assignment-6 Report

- Chirantan(200020013)
- Tanish H T(200020050)

Configuration of Cache:

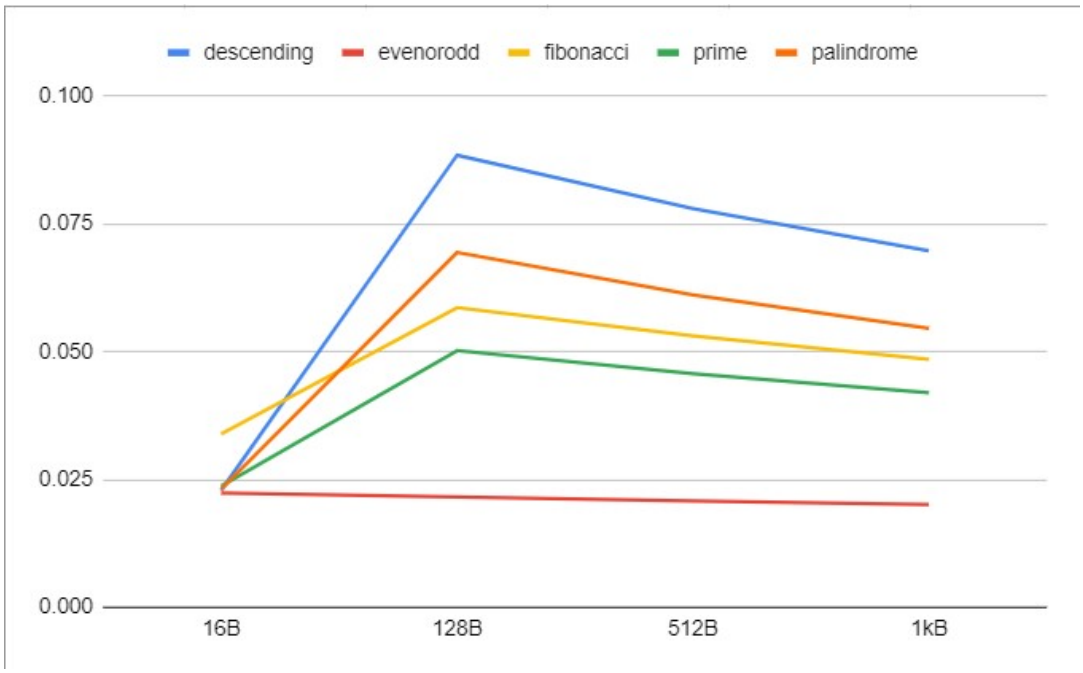
Cache Size	**16B**	**128B**	**512B**	**1KB**
Latency(in cycles)	1	2	3	4
Line Size	4B			
Associativity	2			
Write Policy	Write Through			

IPC Values for different Cache Parameters:

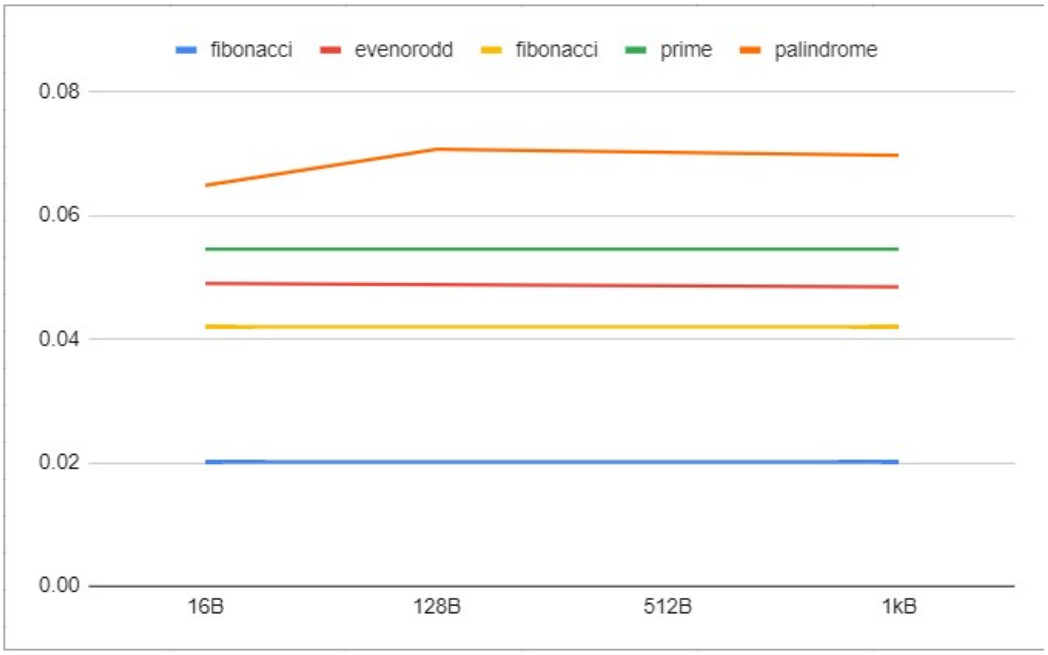
Program	**Without Cache**	**L1d=1024B**			
		L1i=16B	**L1i=128B**	**L1i=512B**	**L1i=1024B**
descending	0.024398	0.025002256	0.10448887	0.12601626	0.09750088
evenorodd	0.024194	0.02238806	0.021582734	0.02238806	0.021201413
fibonacci	0.024685	0.022807017	0.04797048	0.05631769	0.046044864
palindrome	0.024867	0.030265596	0.063885264	0.075038284	0.0601227
prime	0.024854	0.03243848	0.04347826	0.047463175	0.04172662
Program	**Without Cache**	**L1i=1024B**			
		L1d=16B	**L1d=128B**	**L1d=512B**	**L1d=1024B**
descending	0.024398	0.080710955	0.100580975	0.10761461	0.09750088
evenorodd	0.024194	0.021428572	0.021276595	0.021428572	0.021201413
fibonacci	0.024685	0.048628427	0.04693141	0.048628427	0.046044864
palindrome	0.024867	0.060344826	0.06019656	0.060344826	0.0601227
prime	0.024854	0.047463175	0.041786745	0.041907515	0.04172662

Graphs:

IPC vs L1i Cache Size



IPC vs L1d Cache Size



Observations:

Looking at the above graphs, we observe that the latency increases with increase in L1i cache size. There is an optimum size where it is at its peak. When we do the same process for the L1d cache, after reaching the optimum point, it stays the same

Looking at the latency values as L1i cache size increases from 16B to 128B (L1d=1024B), we observe that for the fibonacci program, there is a significant increase in throughput(in terms of IPC)

Looking at the latency values as L1d cache size increases from 16B to 128B (L1i=1024B), we observe that for the descending program, there is a significant increase in throughput(in terms of IPC)