Computer Architecture Laboratory

Assignment-5

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Required Statistics:

Object File	**No. of Cycles**	**Throughput**
descending.out	14960	0.024398
evenorodd.out	248	0.024194
fibonacci.out	3808	0.024685
prime.out	1368	0.024854
palindrome.out	2252	0.024867

Discussion:

Here, we upgrade our simulator to a discrete event simulator. The event queue is a list of events, which is ordered by time. The event is called upon when its corresponding timestamp is equal to the processor clock time. We need to remember that, once an event is executed, it may lead to generation of new events as well. We have modeled the latency of many parts of our simulator.. Such as the main memory, ALU, etc.

We observe the throughput to be between 0.024 and 0.025. Programs having to deal with more hazards are expected to take more clock cycles in order for the instructions to be executed thoroughly without any errors.