

Internship Report

Intern Name: CHITRESH SHARMA

Internship Duration: 01 July 2025 – 31 July 2025

Mentor: I V KARTEEK, Dy.Mgr (Tech)

Project Guide: K. MADHURI, Sr. Dy. General Manager

Organization: CR&D, ECIL

Topic: Internship on Verilog Digital Design, AC 701 Board Projects, SHA - 256 Implementation and MicroBlaze Soft Processor

1. Introduction

The one-month internship focused on providing a hands-on training in VLSI - FPGA design using **Verilog HDL** and the **Xilinx Vivado** tool chain. I was introduced to the hardware description languages (verilog), digital logic design, and FPGA implementation workflows. The goal was to develop both theoretical knowledge and practical skills in FPGA design and verification.

2. Objectives

- To write efficient Verilog code for various digital circuits.
- Learn the methodology of writing test benches and simulating designs in Vivado for functional verification.
- To be able to design, simulate, and implement digital circuits on FPGA.
- To learn the use of Vivado for synthesis, implementation, and bitstream generation.
- To have a hands-on experience deploying projects onto the AC701 board, including debugging and hardware verification.
- To develop practical skills by working on example projects such as LED blinking and UART communication.
- Get guidance in understanding and implementing the SHA-256 hashing algorithm in hardware.

3. Training Activities

Week 1:

Covered Verilog fundamentals, combinational and sequential logic design and writing simple modules. Intern demonstrated good understanding of syntax and logic design basics.

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|---|-------------------------------|
| 1. 2:1 MUX | 7. D Flip Flop |
| 2. 4:1 MUX using 2:1 MUX | 8. Normal FSM -Traffic lights |
| 3. 3:8 Decoder | 9. Moore FSM |
| 4. Counter | 10. Mealy FSM |
| 5. Bi - Directional Counter | 11. Sequence Detector |
| 6. Shift Register - SISO, SIPO, PISO, PIPO. | 12. UART - TX & RX |

Week 2:

Hands-on sessions included:

- Programming the FPGA with generated bitstreams.
- Interfacing with onboard peripherals such as LEDs, switches, and UART.

- Debugging hardware functionality using onboard tools and Vivado Integrated Logic Analyzer (ILA).
- Validating full project functionality with hardware testing.

Week 3:

Implementation of SHA-256 Algorithm

The SHA-256 cryptographic hash function was selected as an advanced project.

- Studied the algorithm and its hardware architecture.
- Developed Verilog modules for key operations (e.g., message scheduling, compression).
- Verified functionality with simulation testbenches.
- Synthesized and implemented the design on the AC701 board, testing the hash output with known inputs.

Week 4:

Introduction to Microblaze soft Processor

- Creating a basic MicroBlaze system and peripheral interfacing using Block Designs
- Hands-on with UART, GPIO via SDK on AC701 board

4. Skills Gained

- Gained hands-on experience with FPGA hardware and peripheral interfacing.
- Developed problem-solving skills by overcoming challenges related to timing and UART communication.

5. Conclusion

Overall, the internship was very useful in learning Verilog coding, simulation, and hardware implementation. The SHA-256 & MicroBlaze soft Processor project added valuable experience in cryptographic hardware design and software implementation of the projects using embedded c.



Project Guide

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