

Instruction Level Parallelism

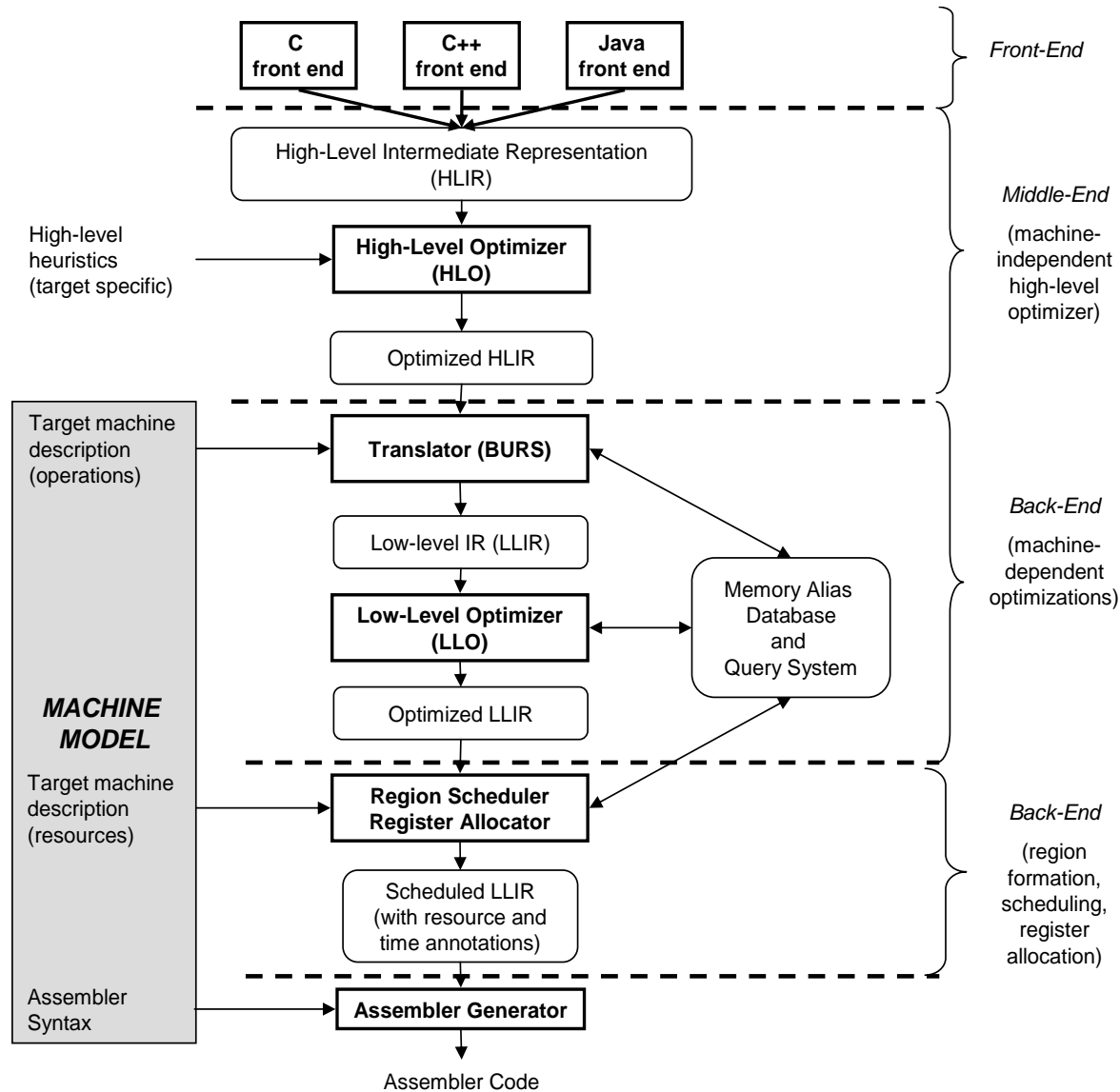
Compilers for High Performance
Architectures



Instruction Level Parallelism

- Introduction
- Basic Optimizations
- Control Flow
- Loop Optimizations
- Instruction Scheduling
- Loop Scheduling
- Register Allocation

Structure of a ILP compiler



VLIW/EPIC Architectures

- Best way to start a compiler class is to talk about hardware!!
- Our target processor for this class is a VLIW/EPIC
 - VLIW = Very Long Instruction Word
 - EPIC = Explicitly Parallel Instruction Computing
- Examples:
 - IA-64: aka Itanium I and II, Itanic, Merced, McKinley
 - Embedded processors –
 - All high-performance embedded CPUs are VLIW
 - TI-C6x, Philips Trimedia, Starcore, ST200, Qualcomm Hexagon

VLIW/EPIC Philosophy

- Compiler creates complete plan of run-time execution
 - At what time and using what resource
 - POE communicated to hardware via the instruction set
 - Processor obediently follows POE
 - No dynamic scheduling, out of order execution (these second guess the compilers plan)
- Compiler allowed to play the statistics
 - Many types of info only available at run-time (branch directions, locations accessed via pointers)
 - Traditionally compilers behave conservatively → handle worst case possibility
 - Allow the compiler to gamble when it believes the odds are in its favor
 - Profiling
- Expose microarchitecture to the compiler
 - branch execution, number and type of units, latencies, etc

Defining Feature I - MultiOp

add	sub	load	load	store	mpy	shift	branch
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- Superscalar
 - Operations are sequential
 - Hardware figures out resource assignment, time of execution
- MultiOp instruction
 - Set of independent operations that are to be issued simultaneously (no sequential notion within a MultiOp)
 - 1 instruction issued every cycle – provides notion of time
 - Resource assignment indicated by position in MultiOp
 - POE communicated to hardware via MultiOps

Defining Feature II - Exposed Latency

- Superscalar
 - Sequence of atomic operations
 - Sequential order defines semantics
 - Unit assumed latency (UAL)
 - Each conceptually finishes before the next one starts
- VLIW/EPIC – non-atomic operations
 - Register reads/writes for 1 operation separated in time
 - Semantics determined by relative ordering of reads/writes
- Assumed latency (NUAL if > 1 for at least one op)
 - Contract between the compiler and hardware
 - Instruction issuance provides common notion of time

What if I don't care about VLIWs?

- How do we compile for superscalars?
- How do we compile for RISCs?
- All the basic compiler analyses and transformations are the same for all processor types
 - They were developed for RISCs
- Superscalar compilers work by pretending the processor is a VLIW
 - But must worry about hardware undoing what the compiler did
 - Other resources to worry about (ie reorder buffer, reservation stations, etc.)
 - Not all hardware features available

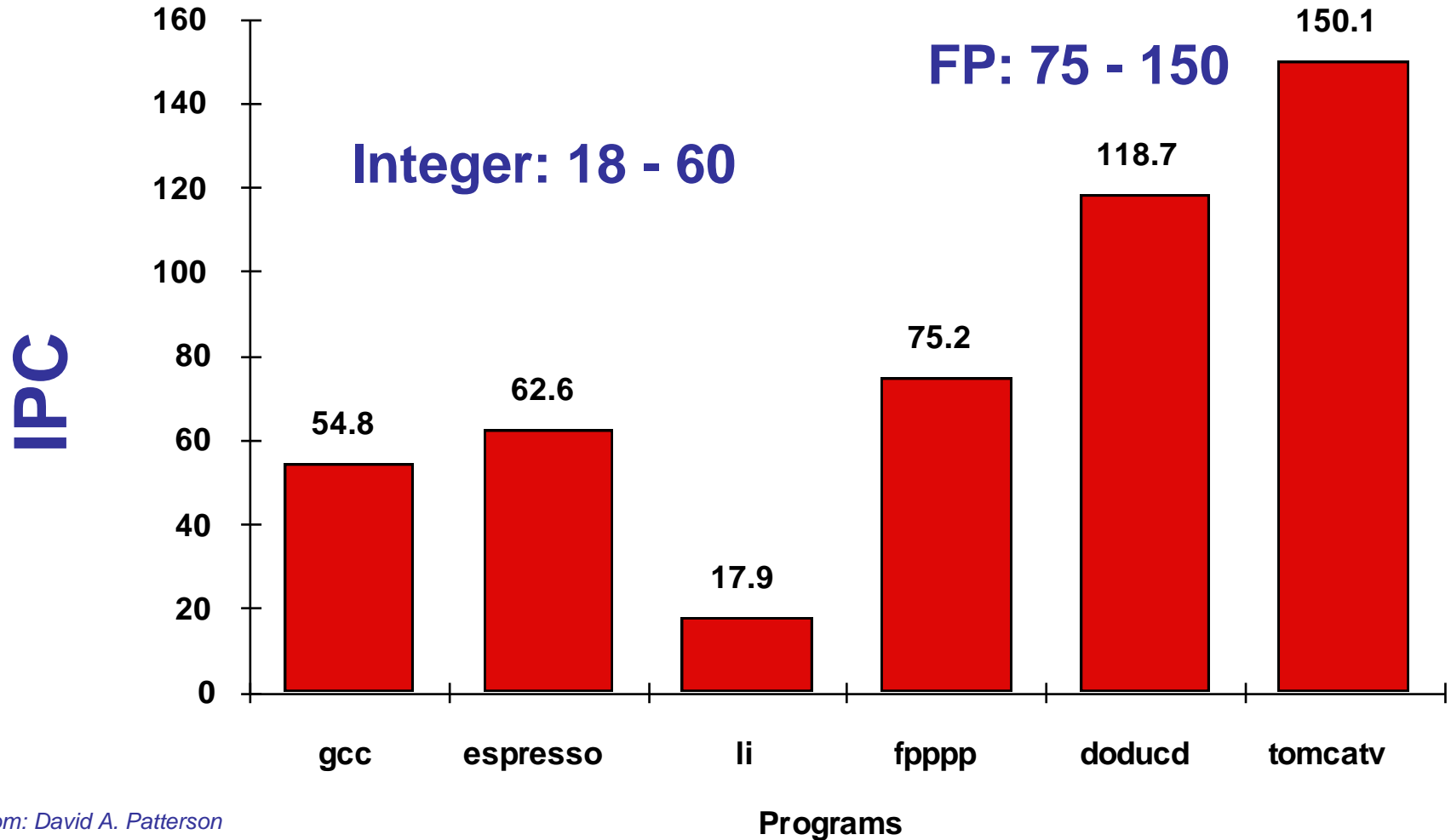
Limits of ILP (1)

- Many Conflicting studies (1980s/90s) of amount of ILP
 - Debated issues
 - Benchmarks (FP Vectorizable Fortran vs. Integer C)
 - Hardware sophistication
 - Compiler sophistication
- How much ILP is available using existing mechanisms with increasing HW budgets?
- What other HW/SW mechanisms do we need to invent to keep on processor performance curve?

Limits of ILP (2)

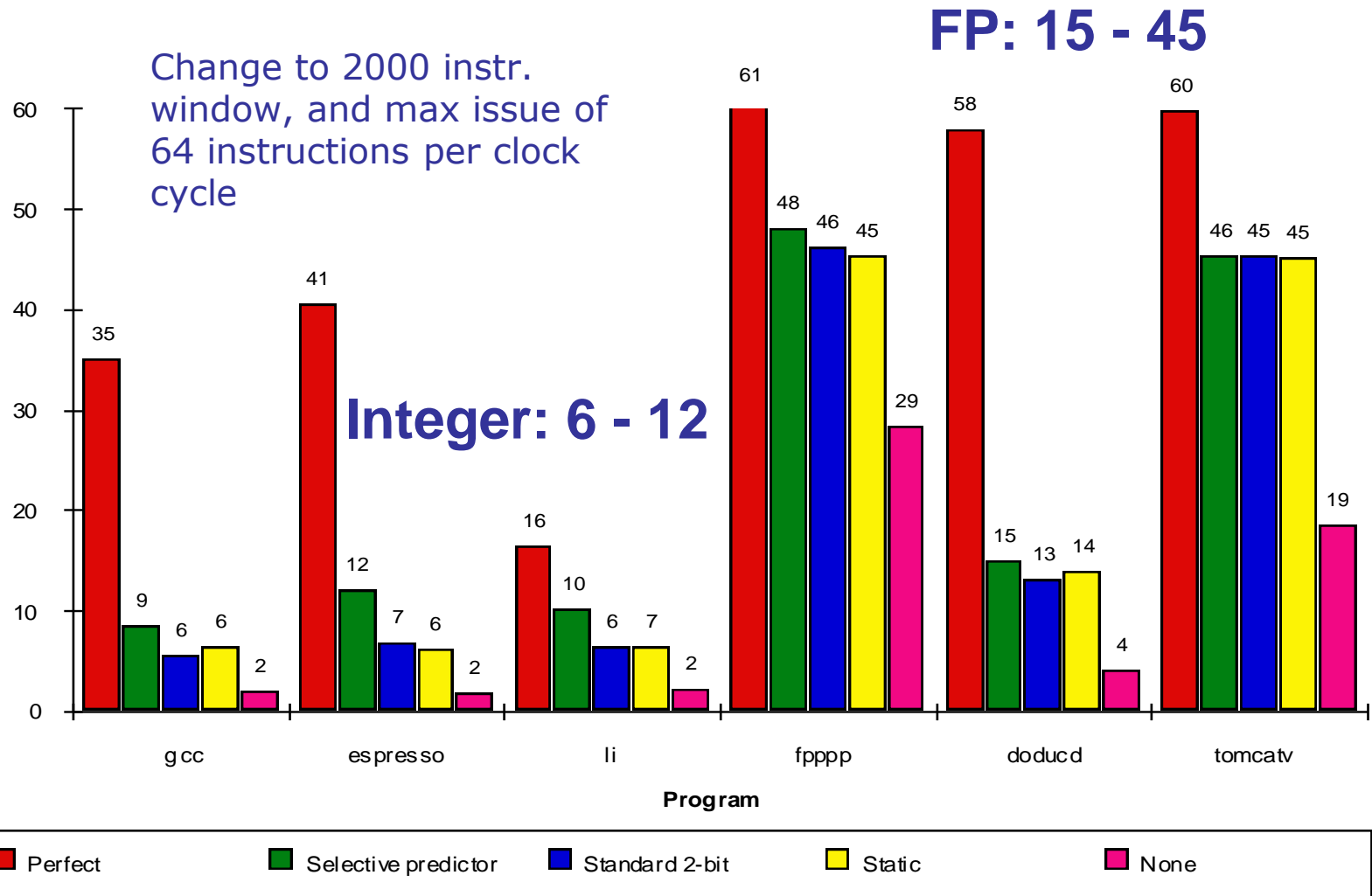
- Initial Model
 - MIPS-like RISC compiler and architecture
- Assumptions for ideal/perfect machine to start:
 - Register renaming–infinite virtual registers and all WAW & WAR hazards are avoided
 - Branch & Jump prediction–perfect; no mispredictions:
 - Machine with perfect speculation & an unbounded buffer of instructions available
 - Memory-address alias analysis–addresses are known & a store can be moved before a load provided addresses not equal
- One-cycle latency for all instructions
- Unlimited number of instructions issued per clock cycle

Ideal Machine



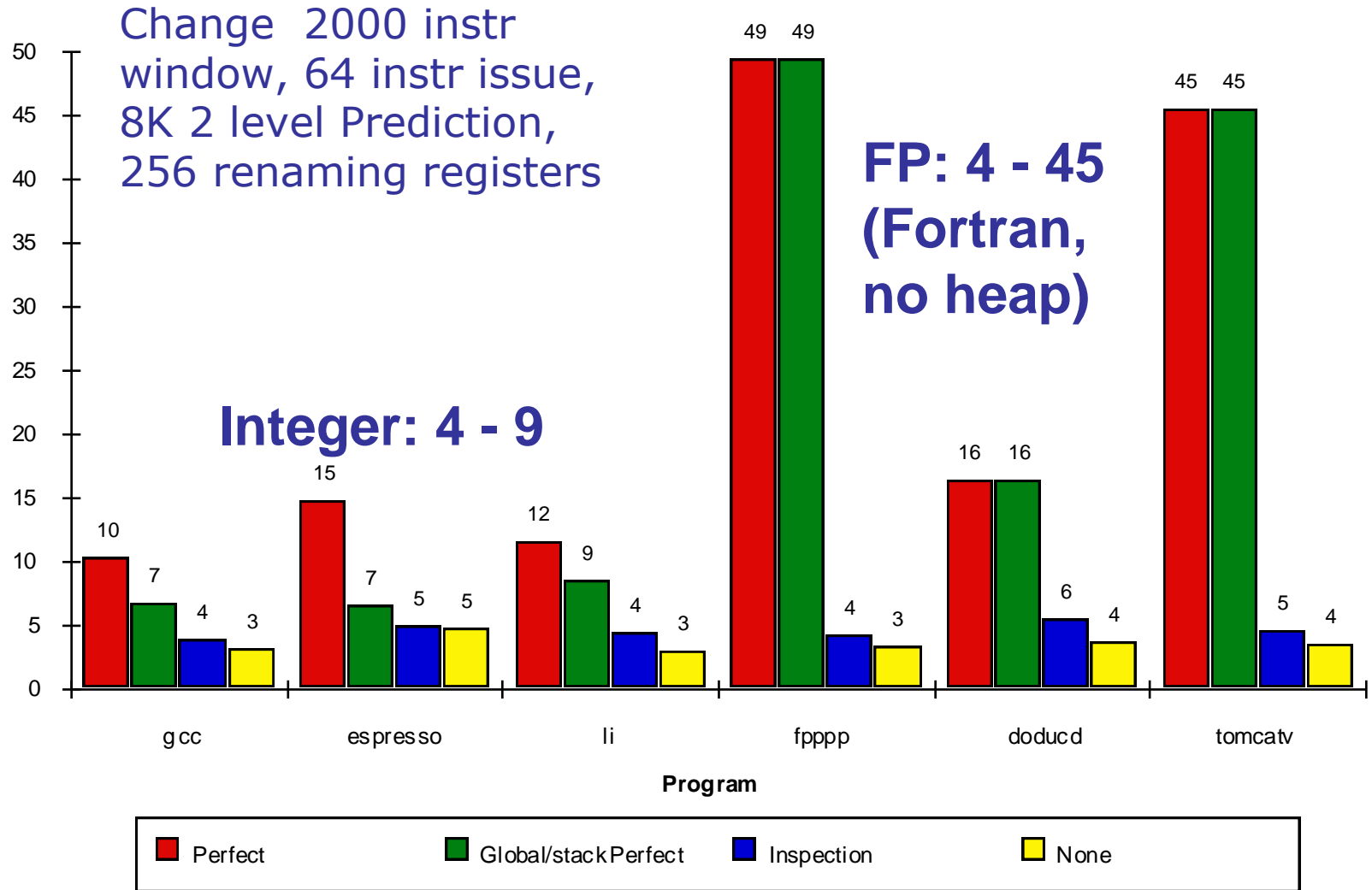
Realistic HW: Branch Impact

IPC



Realistic HW: Register Impact

IPC



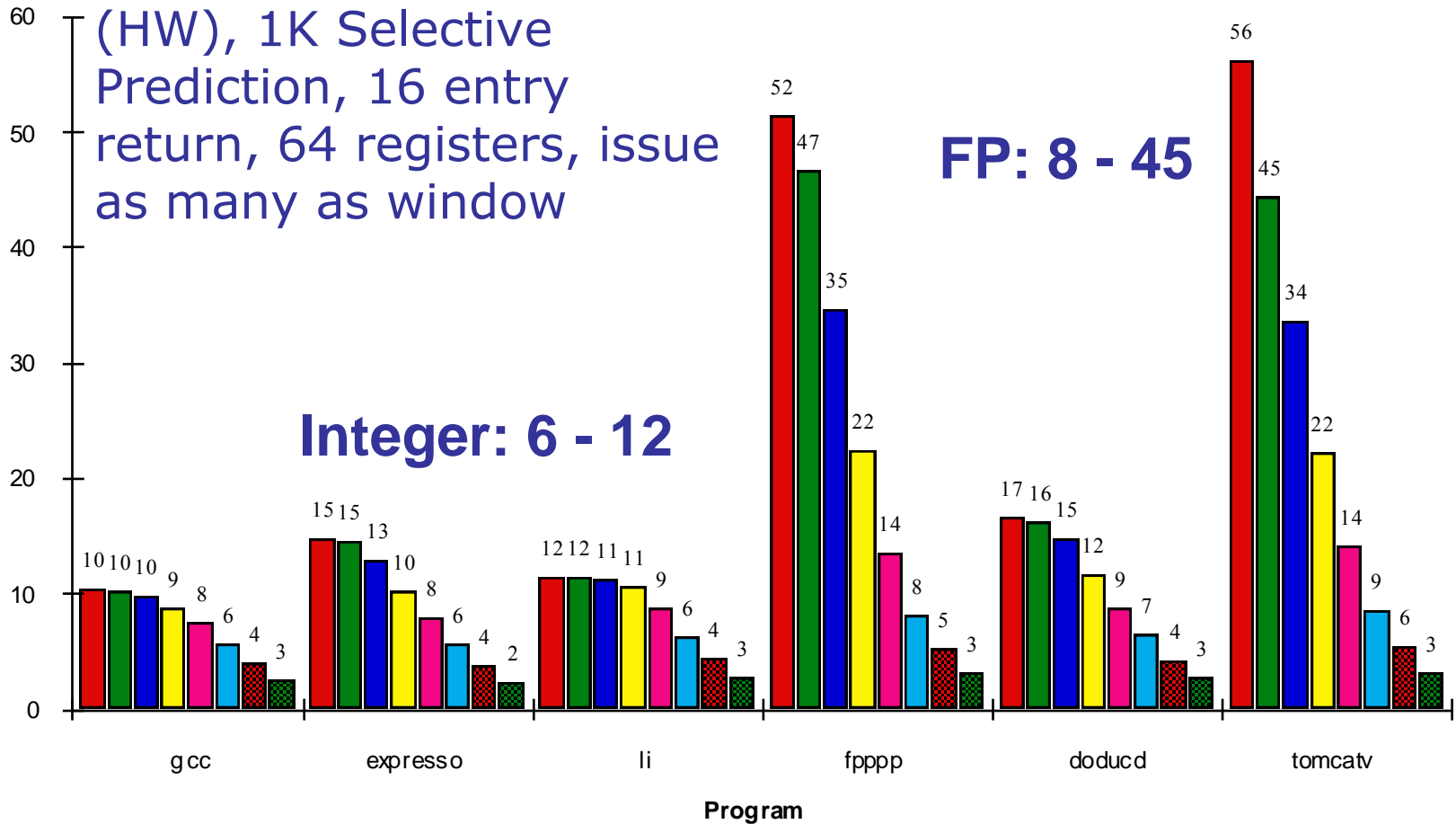
Realistic HW: Fetch Window Impact

Perfect disambiguation
(HW), 1K Selective
Prediction, 16 entry
return, 64 registers, issue
as many as window

IPC

Integer: 6 - 12

FP: 8 - 45



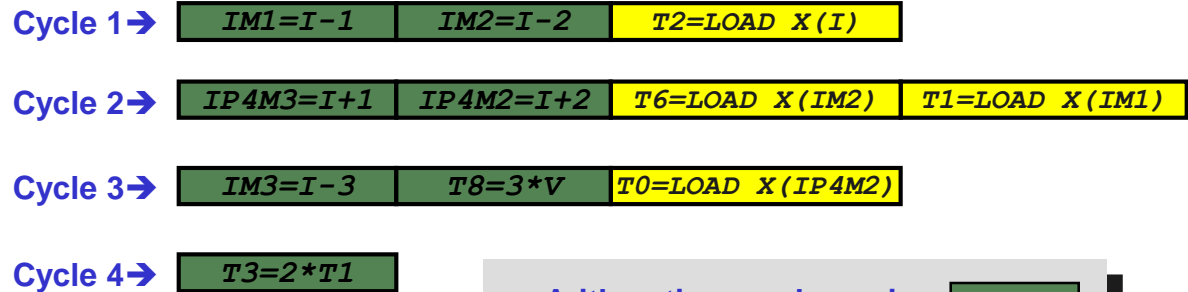
Legend: Infinite (Red), 256 (Green), 128 (Blue), 64 (Yellow), 32 (Pink), 16 (Cyan), 8 (Dark Red), 4 (Dark Green)

Instruction-Level Parallelism

Source Code:

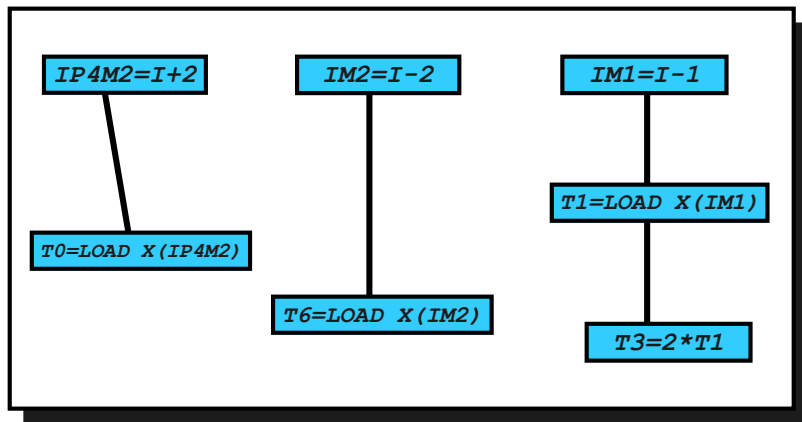
```
IM1 = I-1
IM2 = I-2
IM3 = I-3
T1 = LOAD X(IM1)
T2 = LOAD X(I)
T3 = 2*T1
T6 = LOAD X(IM2)
T8 = 3*V
IP4 = I+4
IP4M2 = I+2
IP4M3 = I+1
T0 = LOAD X(IP4M2)
```

Might Execute Like This:

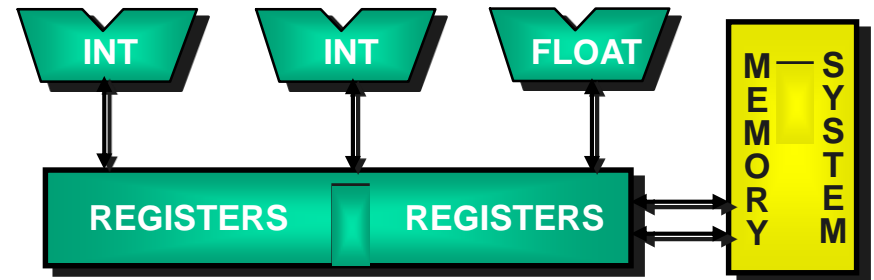


Arithmetic ops shown in: **green**
Loads and stores shown in: **yellow**

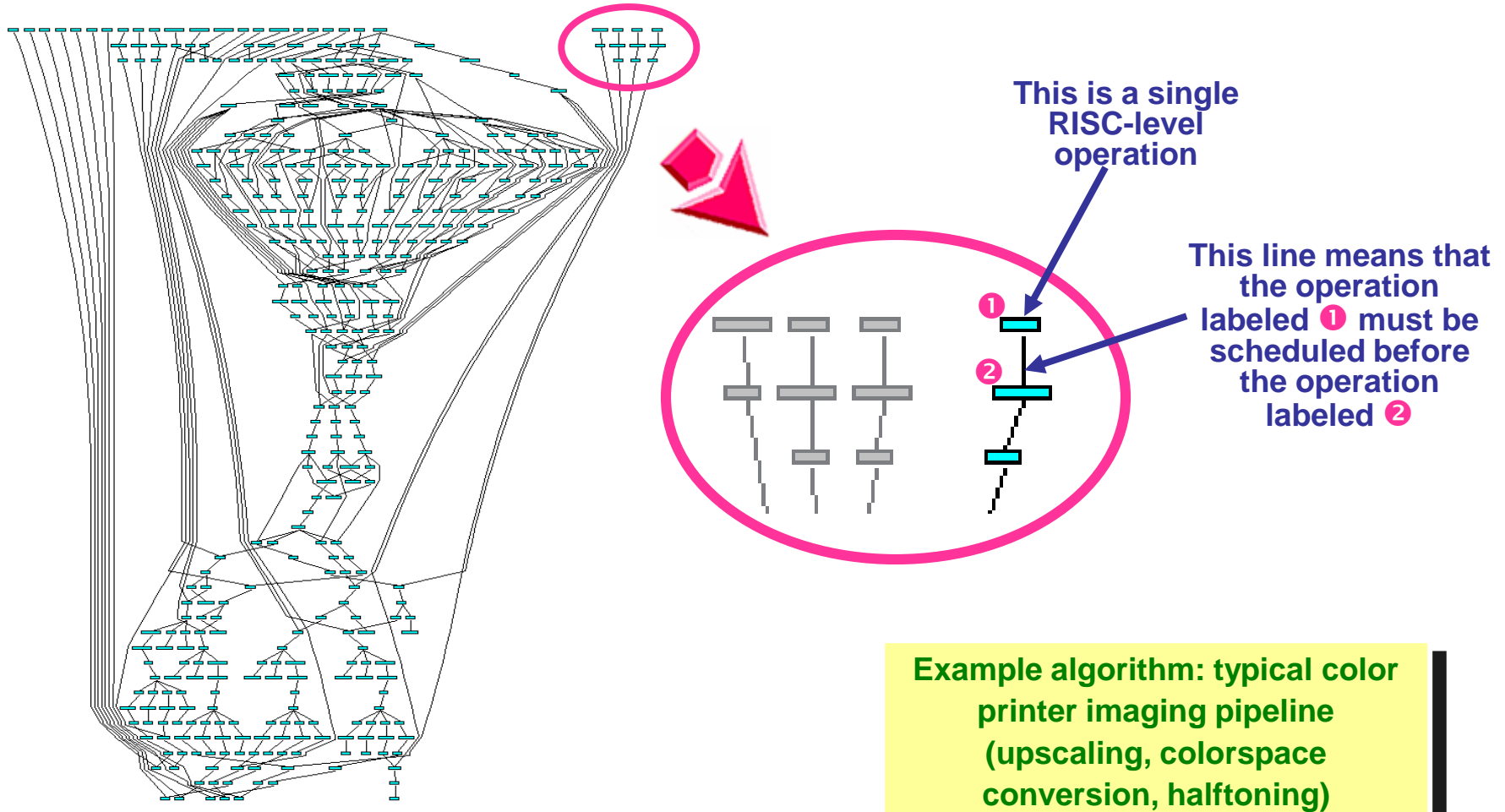
Data Dependences:



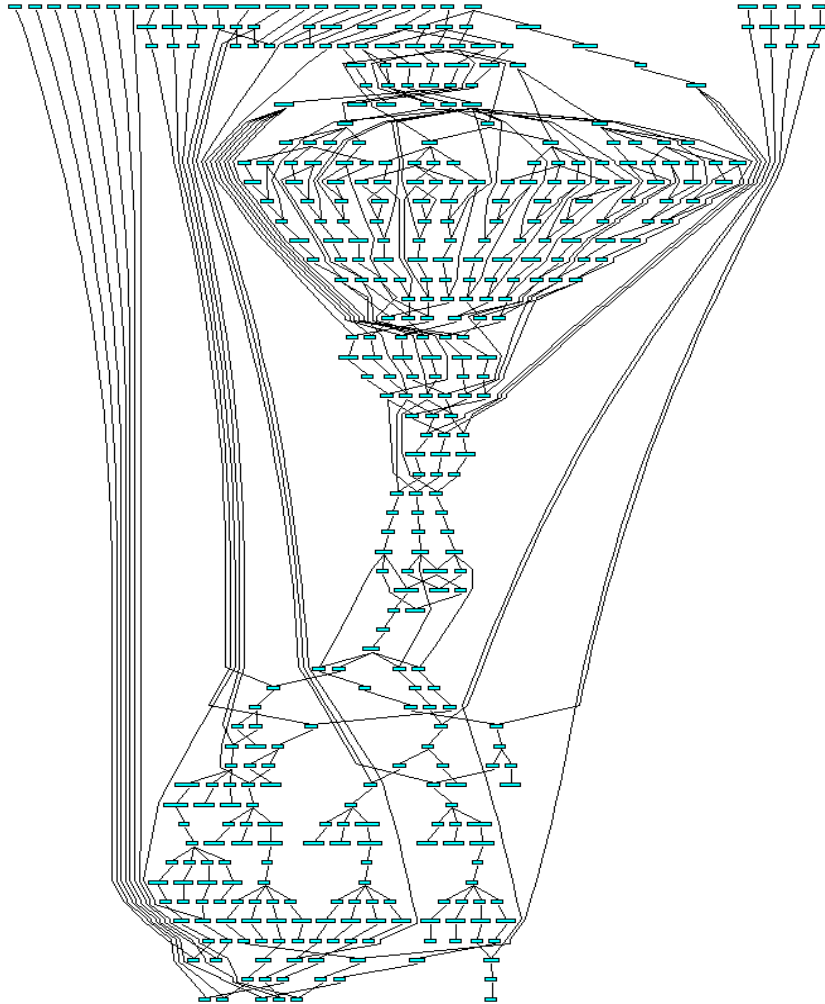
Using Extra ILP Hardware:



Example: imaging pipeline one pixel computation



Example: imaging pipeline one pixel dependences and schedule

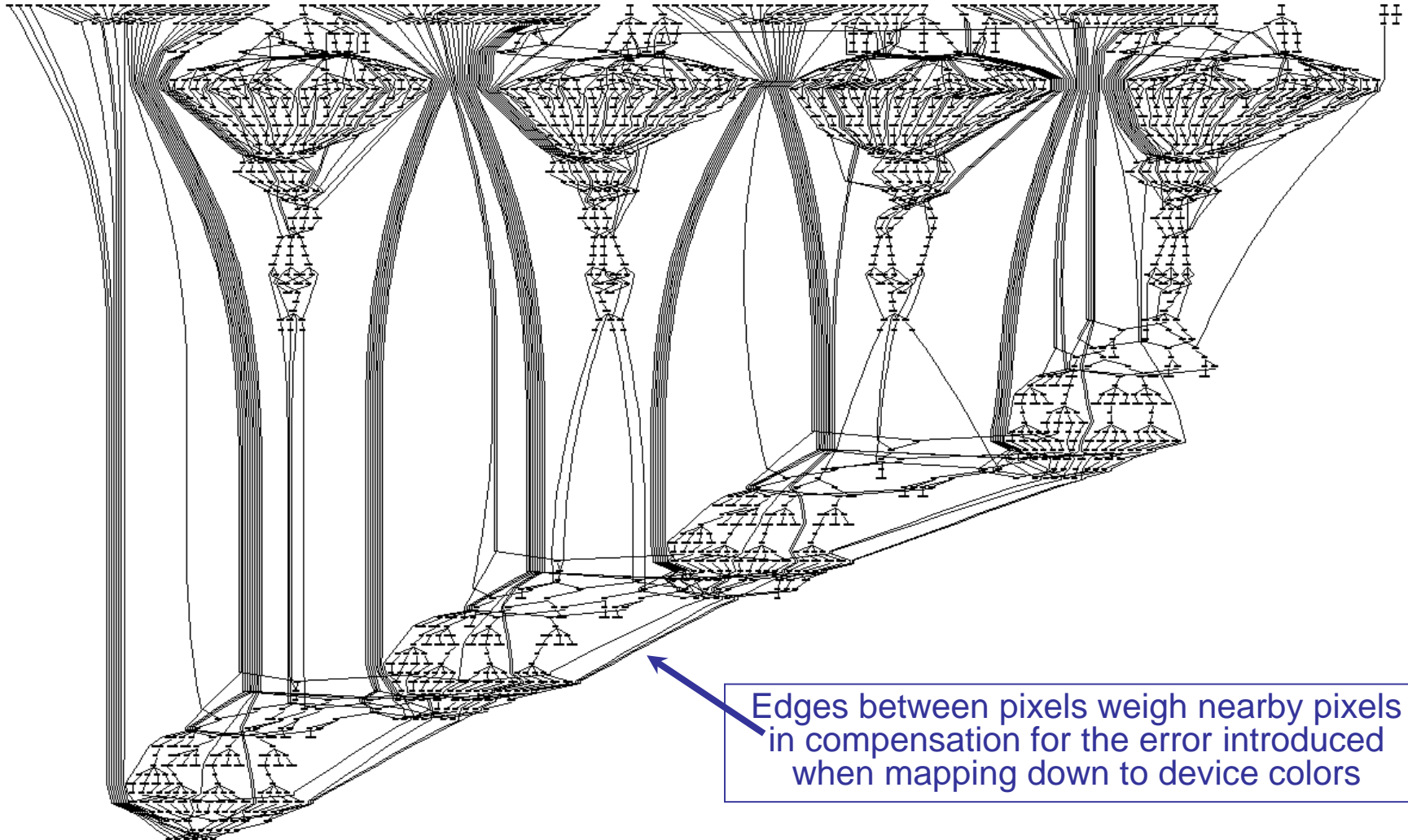


0	EXTR	ADD	LD	ADD	ADD	ADD	ADD	ADD
1	REL	LD	ADD	ADD	ADD	ADD	ADD	ADD
2	IF	LD	VSHFTD	BANDOR	EXTR	ADD	ADD	ADD
3	VSHFTD	BANDOR	EQT	EXTR	INCL	LD	LD	LD
4	VSHFTD	BANDOR	EQT	EXTR	EXTR	ZVDEP	LD	
5	EQT	EQT	EXTR	ADD	EXTR	EXTR	LD	EXTR
6	EQT	EXTR	ADD	ADD	EXTR	LD	LD	
7	SLCT	EQT	ADD	EXTR	LD	ADD		
8	SLCT	ADDS	EXTR	EXTR	ADD	ADD		
9	SLCT	LD	ADDS	EXTR	ADD	ADD		
10	LD	ADDS	ADD					
11	LD							
12	ADD	ADD	ADD					
13	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
14	ADD	ADD	LD	LD	ADD	ADD	ADD	ADD
15	LD	LD	LD	LD	ADD	ADD	ADD	ADD
16	LD	LD	LD	LD	ADD	ADD	LD	ADD
17	ADD	ADD	SUB	SUB	LD	LD	LD	LD
18	LD	ADD	ADDS	ADDS	SUB	SUB	LD	LD
19	ADD	ADD	ADD	LD	ADDS	ADDS	SUB	SUB
20	ADD	ADD	LD	LD	SUB	ADDS	ADDS	SUB
21	LD	LD	LD	EXTR	ADDS	LD	LD	ADDS
22	LD	LD	LD	ADD	EXTR	EXTR	LD	LD
23	LD	LD	SUB	EXTR	ADD	ADD	EXTR	EXTR
24	ADDS	SUB	ADD	SUB	EXTR	ADD	ADD	EXTR
25	SUB	SUB	LD	ADDS	SUB	ADDS	ADD	ADD
26	ADDS	ADDS	LD	ADDS	LD	SUB	SUB	
27	LD	LD	EXTR	LD	ADDS	ADDS		
28	ADD	EXTR	EXTR	LD	LD			
29	EXTR	EXTR	ADD	EXTR	ADD			
30	ADD	ADD	SUB	ADD	EXTR	EXTR		
31	SUB	ADDS	SUB	ADD	ADD			
32	ADDS	LD	ADDS	SUB				
33	LD	LD	ADDS					
34	EXTR	LD						
35	EXTR	ADD	EXTR					
36	ADD	ADD	EXTR					
37	SUB	EXTR	ADD					
38	ADDS	EXTR	ADD					
39	LD	ADD	LD					
40	LD							
41	EXTR	EXTR						
42	ADD	EXTR						
43	EXTR	REL						
44	ADD							
45	LD	SLCT						
46	EXTR							
47	EXTR							
48	REL							
49								
50	SLCT							
51	EXTR							
52	ADD							
53	LD							
54								

55	SUB	SUB	SUB	ADD				
56	EXTR	EXTR	EXTR	ADD				
57	ADD	ADD	ADD	EXTR				
58	ADD	ADD	ADD	EXTR	ADD			
59	EXTR	EXTR	EXTR	REL				
60	EXTR	ADD	EXTR	ADD	EXTR	ADD		
61	REL	REL	REL	SLCT				
62	EXTR							
63	SLCT	SLCT	SLCT	SUB	ST			
64	EXTR	EXTR	EXTR	EXTR				
65	SUB	SUB	SUB	EXTR	EXTR	ST	ST	ADD
66	EXTR	EXTR	EXTR	REL	REL	ST		
67	EXTR	EXTR	EXTR	EXTR	EXTR	EXTR		
68	REL	REL	REL	REL	REL	REL	SLCT	
69	SLCT							
70	SLCT	SLCT	SLCT	ZVDEP				
71	SLCT	SLCT	SLCT	EXTR				
72	ZVDEP	ZVDEP	ZVDEP	ADDS	ADDS	ADDS	ADDS	
73	EXTR	EXTR	EXTR	LD	LD	LD	LD	
74	ADDS	ADDS	ADDS	ADDS	ADDS	ADDS	ADDS	ADDS
75	LD	LD	ADDS	ADDS	ADDS	ADDS	EXTR	EXTR
76	LD	LD	LD	LD	LD	ADD	EXTR	ADD
77	EXTR	LD	LD	LD	LD	EXTR	EXTR	EXTR
78	ADD	EXTR	EXTR	EXTR	LD	EXTR	ST	ST
79	EXTR	ADD	EXTR	ADD	ADD	EXTR	EXTR	
80	EXTR	EXTR	EXTR	EXTR	EXTR	ADD	ST	ADD
81	EXTR	EXTR	EXTR	EXTR	ST	ST	ST	
82	ST	ST						

The schedule: 1 pixel processed in 83 cycles

Example: imaging pipeline four pixels unrolled



Example: imaging pipeline four pixels scheduled

1	AD	LD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
2	LD	LD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
3	LD	VSHFTD	BANDOR	EXTR	ADD	LD	ADD	LD	ADD
4	LD	VSHFTD	BANDOR	EDIT	EXTR	1WLL	VSHFTD	LD	ADD
5	VSHFTD	BANDOR	EXTR	EXTR	EXTR	2XOF	ADD	ADD	ADD
6	EXTR	EXTR	EXTR	ADD	ADD	VSHFTD	BANDOR	EXTR	EXTR
7	SLIT	EDIT	ADD	VSHFTD	EXTR	EXTR	EXTR	EXTR	EXTR
8	SLIT	ACOG	2XOF	BANDOR	EXTR	EDIT	EDIT	EDIT	EDIT
9	SLIT	LD	ACOG	ADD	EXTR	EXTR	EXTR	EXTR	EXTR
10	LD	ACOG	1WLL	ADD	EDIT	ADD	SLIT	EDIT	EDIT
11	LD	BANDOR	EXTR	ADD	ACOG	VSHFTD	EXTR	EXTR	EXTR
12	ADD	ADD	ADD	EDIT	SLIT	LD	LD	LD	LD
13	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
14	ADD	ADD	LD	LD	ADD	ADD	ADD	ADD	ADD
15	LD	LD	LD	LD	ADD	ADD	ADD	ADD	ADD
16	LD	LD	LD	LD	ADD	ADD	ADD	ADD	ADD
17	ADD	SLB	SLB	LD	LD	ADD	LD	LD	LD
18	ADD	LD	ACOG	ACOG	SLB	SLB	LD	LD	LD
19	ADD	ADD	ADD	ADD	ACOG	SLB	SLB	SLB	SLB
20	ADD	ADD	ADD	LD	SLB	ACOG	ACOG	SLB	SLB
21	EXTR	LD	ACOG	ACOG	ADD	ACOG	ADD	ADD	ADD
22	LD	ADD	EXTR	ADD	ADD	ADD	ADD	ADD	ADD
23	ADD	EXTR	LD	ADD	ADD	ADD	ADD	ADD	ADD
24	EXTR	ADD	LD	EXTR	ADD	ADD	ADD	ADD	ADD
25	LD	LD	LD	ADD	SLB	LD	LD	EXTR	EXTR
26	LD	LD	SLB	ACOG	ADD	EXTR	EDIT	ADD	ADD
27	SLB	SLB	ACOG	LD	EXTR	EXTR	EXTR	EXTR	EXTR
28	ACOG	ACOG	LD	ADD	ADD	SLB	SLIT	ADD	ADD
29	EXTR	EXTR	SLB	ACOG	ADD	SLB	SLB	SLB	SLB
30	LD	LD	LD	EXTR	ADD	ACOG	LD	LD	LD
31	EXTR	ADD	LD	ADD	ADD	ADD	ADD	ADD	ADD
32	SLB	SLB	ADD	EXTR	SLB	EXTR	LD	LD	LD
33	ACOG	ACOG	ADD	ACOG	EXTR	ADD	LD	LD	LD
34	LD	LD	SLB	LD	LD	ACOG	LD	SLB	SLB
35	ACOG	SLB	LD	LD	SLB	LD	LD	ACOG	ACOG
36	EXTR	EXTR	LD	EXTR	ACOG	ACOG	ADD	ADD	ADD
37	ADD	ADD	ADD	LD	SLB	ADD	ADD	ADD	ADD
38	SLB	EXTR	EXTR	LD	LD	ACOG	LD	LD	LD
39	ACOG	EXTR	EXTR	ADD	LD	LD	LD	LD	LD
40	ADD	LD	SLB	EXTR	EXTR	BANDOR	EXTR	EXTR	EXTR
41	LD	EXTR	SLB	SLB	ACOG	EXTR	ADD	ADD	ADD
42	ADD	EXTR	LD	ADD	SLB	ACOG	ACOG	EXTR	EXTR
43	EXTR	LD	LD	LD	ACOG	LD	LD	LD	LD
44	ADD	EXTR	LD	EXTR	VSHFTD	BANDOR	EXTR	EXTR	EXTR
45	SLB	EXTR	LD	SLB	ADD	EXTR	EXTR	EXTR	EXTR
46	ACOG	REL	SLB	EXTR	ACOG	ADD	ADD	LD	LD
47	LD	SLB	ACOG	ADD	SLB	EDIT	2XOF	EXTR	EXTR
48	SLIT	LD	ACOG	ACOG	ADD	ADD	ADD	ADD	ADD
49	EXTR	EXTR	EXTR	EXTR	LD	SLIT	ADD	ADD	ADD
50	REL	ADD	EXTR	LD	ADD	ADD	EXTR	ADD	ADD
51	1F	EXTR	ADD	LD	EXTR	LD	LD	EDIT	EDIT
52	ADD	SLB	EXTR	ADD	LD	LD	LD	LD	LD
53	LD	ACOG	EXTR	ADD	SLB	ADD	ADD	ADD	ADD
54	LD	LD	ADD	ACOG	SLB	ACOG	ADD	ADD	ADD
55	EXTR	SLB	LD	ACOG	ACOG	ADD	ACOG	ADD	ADD
56	REL	EXTR	ACOG	LD	LD	LD	LD	LD	LD
57	ADD	LD	SLB	ADD	ADD	ADD	ADD	ADD	ADD
58	SLIT	EXTR	SLB	SLB	ADD	EXTR	EXTR	EXTR	EXTR
59	EXTR	EXTR	EXTR	ACOG	ACOG	EXTR	EXTR	EXTR	EXTR
60	ADD	LD	ADD	LD	SLB	2XOF	BANDOR	EXTR	EXTR
61	LD	SLB	ACOG	VSHFTD	BANDOR	EXTR	ADD	EDIT	EDIT
62	ACOG	EXTR	EXTR	LD	EDIT	ADD	ADD	EXTR	EXTR
63	SLB	LD	ADD	EXTR	ADD	ADD	EDIT	EDIT	EDIT
64	EXTR	LD	EXTR	EDIT	ADD	ADD	ADD	ADD	ADD
65	ADD	EXTR	ADD	ADD	ADD	ADD	LD	SLIT	SLIT
66	ADD	ADD	EXTR	SLIT	ADD	LD	LD	LD	LD
67	EXTR	EXTR	ADD	ACOG	ADD	LD	ADD	ADD	ADD
68	EXTR	EXTR	ADD	SLB	LD	LD	SLB	SLB	SLB
69	REL	LD	ACOG	ADD	ADD	SLB	EXTR	ADD	ADD
70	LD	ACOG	ADD	ADD	ADD	ACOG	ADD	ADD	ADD
71	SLIT	EXTR	ADD	ADD	LD	ADD	ACOG	ACOG	ACOG
72	EXTR	REL	EXTR	ADD	LD	ADD	ADD	ADD	ADD
73	SLB	EXTR	EXTR	LD	ADD	ADD	ADD	ADD	ADD
74	EXTR	SLIT	SLB	LD	ADD	LD	EXTR	EXTR	EXTR
75	EXTR	EXTR	ACOG	EXTR	LD	LD	LD	LD	LD
76	REL	REL	LD	LD	LD	SLB	ADD	ADD	ADD
77	LD	SLB	LD	SLB	LD	ACOG	LD	ACOG	ACOG
78	SLIT	EXTR	EXTR	ACOG	SLB	ACOG	LD	LD	LD
79	SLIT	ADD	LD	LD	ACOG	LD	ACOG	LD	LD

81	EXTR	2MVEP	EXTR	LD	LD	EXTR	LD	LD
82	EXTR	ADD	EXTR	SUB	EXTR	SUB	ADD	LD
83	ADD	LD	ADD	ACOG	EXTR	ADD	SUB	ACOG
84	LD	ADD	LD	ADD	SUB	ACOG	LD	SUB
85	SUB	EXTR	LD	ACOG	LD	LD	LD	ACOG
86	EXTR	EXTR	REL	EXTR	EXTR	LD	LD	LD
87	ADD	ADD	EXTR	ADD	LD	SUB	SUB	
88	SLDT	ADD	SUB	EXTR	ACOG	EXTR	ACOG	
89	ADD	EXTR	SUB	ADD	ACOG	SUB	ADD	LD
90	ADD	ADD	ADD	SUB	ADD	LD	ACOG	ACOG
91	LD	ACOG	LD	LD	LD	EXTR	LD	LD
92	ADD	LD	EXTR	ADD	ADD	ADD	ADD	ADD
93	SUB	EXTR	ADD	ADD	EXTR	SUB	VSHFTD	EXTR
94	EXTR	ADD	ADD	EXTR	EXTR	LD	EXTR	1M4
95	ADD	ADD	SUB	LD	BAHGER	LD	EXTR	
96	EXTR	EXTR	ACOG	ACOG	VSHFTD	BAHGER	EXTR	LD
97	EXTR	ADD	ADD	EXTR	EXTR	EXTR	ADD	ADD
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100	EXTR	EXTR	EXTR	ADD	SLDT		EXTR	
101	ADD	SUB	EXTR	ADD	SUB	ACOG	SLDT	
102	EXTR	EXTR	LD	ACOG	ADD	ACOG	ADD	ADD
103	EXTR	EXTR	LD	ADD	ADD	ADD	ADD	ADD
104	REL	REL	EXTR	LD	ADD	ADD	ADD	ADD
105	REL	EXTR	ADD	LD	ADD	LD		
106	SLDT	ADD	ADD	LD	LD	LD		
107	SLDT	SLDT	EXTR	LD	ADD	ADD		
108	2MVEP	ADD	EXTR	ADD	SUB	ADD	LD	SUB
109	EXTR	EXTR	LD	ADD	SUB	EXTR	ACOG	ADD
110	ACOG	ACOG	ADD	LD	ADD	ADD	ADD	ADD
111	LD	EXTR	ADD	ADD	ADD	ADD	ADD	ADD
112	REL	LD	LD	LD	EXTR	LD	LD	LD
113	EXTR	LD	LD	LD	LD	LD	LD	
114	SLDT	ADD	EXTR	SUB	SUB	EXTR	LD	
115	EXTR	ADD	LD	ACOG	ACOG	LD	ADD	LD
116	EXTR	ADD	EXTR	ADD	LD	LD	SUB	SUB
117	REL	LD	SUB	SUB	ACOG	ACOG	LD	SUB
118	SUB	SUB	SUB	ADD	LD	LD	ACOG	
119	SUB	SUB	LD	LD	ADD	ADD	SUB	
120	EXTR	EXTR	EXTR	SUB	LD	EXTR	EXTR	ACOG
121	SUB	SUB	ADD	EXTR	ADD	ACOG	ADD	LD
122	EXTR	EXTR	EXTR	ADD	EXTR	SUB	LD	
123	EXTR	EXTR	ADD	ADD	ACOG	LD	LD	EXTR
124	REL	REL	EXTR	SUB	EXTR	LD	ADD	EXTR
125	REL	ADD	ACOG	LD	LD	ADD		
126	SLDT	SLDT	SUB	LD	EXTR	SUB		
127	EXTR	LD	ACOG	ADD	SUB	SUB	ACOG	
128	SLDT	SUB	LD	EXTR	ACOG	ACOG		
129	2MVEP	EXTR	EXTR	EXTR	LD	ADD	ADD	ADD
130	EXTR	ADD	EXTR	EXTR	EXTR	SUB	LD	ADD
131	ACOG	REL	REL	ACOG	ADD	ACOG	LD	EXTR
132	ADD	ADD	EXTR	LD	EXTR	ADD		
133	LD	ADD	SLDT	ADD	ADD	EXTR	ADD	
134	ACOG	LD	SLDT	EXTR	EXTR	LD	ADD	BT
135	LD	EXTR	LD	2MVEP	ADD	LD	SUB	LD
136	LD	ADD	EXTR	LD	EXTR	EXTR	ACOG	LD
137	EXTR	ADD	EXTR	ACOG	ACOG	LD	EXTR	LD
138	EXTR	ADD	EXTR	ACOG	ACOG	LD	EXTR	LD
139	EXTR	ADD	EXTR	ACOG	ACOG	ADD	LD	LD
140	EXTR	ADD	EXTR	REL	LD	EXTR	LD	ADD
141	REL	EXTR	ADD	LD	EXTR	SUB	ADD	
142	REL	SLDT	EXTR	REL	EXTR	ACOG		
143	SLDT	EXTR	ADD	EXTR				
144	EXTR	SLDT	SUB	LD	SLDT	LD		
145	SUB	EXTR	EXTR	LD	LD	LD	EXTR	EXTR
146	EXTR	SUB	EXTR	EXTR	LD	EXTR	ADD	EXTR
147	EXTR	EXTR	EXTR	REL	REL	EXTR	EXTR	
148	REL	REL	EXTR	SLDT	EXTR	ADD		
149	REL	REL	SLDT	ADD	LD			
150	SLDT	SLDT	LD	EXTR				
151	SLDT	SLDT	2MVEP	EXTR	BT	EXTR		
152	2MVEP	SLDT	EXTR	EXTR	LD	ADD	REL	
153	EXTR	LD	SUB	LD	ACOG	ACOG	ADD	ADD
154	ACOG	EXTR	LD	EXTR	ADD	ADD	SUB	
155	LD	ACOG	ADD	ACOG	EXTR	ACOG	ADD	EXTR
156	LD	ADD	ACOG	EXTR	ADD	ADD	ADD	ADD
157	ACOG	ACOG	EXTR	EXTR	ACOG	ADD	EXTR	LD
158	EXTR	EXTR	LD	LD	LD	LD	LD	
159	LD	LD	ADD	ADD	EXTR	SUB	SUB	SUB

150	EXTR	ADD	LD	EXTR	ADD	EXTR	EXTR	EXTR
151	EXTR	EXTR	EXTR	ADD	EXTR	REL	ST	ADD
152	LD	EXTR	EXTR	REL	EXTR	ADD	EXTR	
153	LD	EXTR	REL	SLDT	EXTR	ADD		
154	EXTR	LD	SLDT	ADD	EXTR	REL		
155	EXTR	ADD	EXTR	SLDT	SUB	ST		
156	EXTR	EXTR	ADD	SUB	EXTR	EXTR	SLDT	
157	ADD	EXTR	EXTR	SUB	ST	EXTR		EXTR
158	EXTR	EXTR	EXTR	ADD	REL	REL	SUB	ST
159	REL	REL	EXTR	EXTR	ST	EXTR		
160	REL	REL	SLDT	EXTR				
161	SLDT	SLDT	REL	REL				
162	LD	SLDT	SLDT	2MVEP				
163	ADD	LD	2MVEP	SLDT	EXTR	SLDT		
164	EXTR	2MVEP	ADD	ADD	ADD	SLDT		
165	EXTR	ADD	ADD	EXTR	LD	EXTR	LD	2MVEP
166	ADD	EXTR	LD	ADD	LD	ADD	EXTR	
167	EXTR	ADD	ADD	EXTR	LD	EXTR	ADD	ADD
168	EXTR	EXTR	ADD	ADD	ADD	ADD	LD	ADD
169	SUB	ADD	ADD	ADD	EXTR	ADD	LD	ADD
170	SUB	ADD	EXTR	LD	ADD	EXTR	EXTR	ADD
171	LD	ST	EXTR	ST	EXTR	EXTR	ADD	EXTR
172	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
173	EXTR	SUB	ST	REL	ADD	EXTR	ST	
174	ADD	SUB	LD	EXTR	ADD	SLDT	ST	
175	EXTR	ST	EXTR	ADD	SLDT	EXTR		EXTR
176	EXTR	ST	EXTR	ADD	SUB	ST		ST
177	LD	ADD	EXTR	ADD	SUB	REL	ST	EXTR
178	EXTR	SUB	EXTR	LD	EXTR	EXTR	EXTR	
179	ST	EXTR	EXTR	SLDT	ST	REL	REL	
180	LD	LD	EXTR	REL	REL	EXTR		
181	EXTR	ST	SUB	SLDT	ST			
182	EXTR	EXTR	LD	SLDT	EXTR	SLDT		
183	ADD	LD	ADD	SLDT	EXTR			2MVEP
184	EXTR	EXTR	EXTR	ST	2MVEP	REL	REL	EXTR
185	EXTR	ST	ST	EXTR	ADD	ADD		
186	EXTR	ADD	ADD	EXTR	LD	LD	SLDT	
187	SUB	ADD	ADD	EXTR	SUB	ADD	2MVEP	EXTR
188	ADD	LD	ADD	EXTR	LD	EXTR	EXTR	ADD
189	LD	ST	EXTR	EXTR	ADD	ADD		
190	EXTR	LD	ADD	EXTR	LD	ADD	EXTR	EXTR
191	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	ST
192	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
193	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
194	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
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343	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
344	EXTR	EXTR	LD	EXTR	ADD	EXTR	ADD	REL
345	EXTR							

The schedule: 4 pixels processed in $229/4 = 57.25$ cycles per pixel.