Introduction

Compilers for High Performance Architectures

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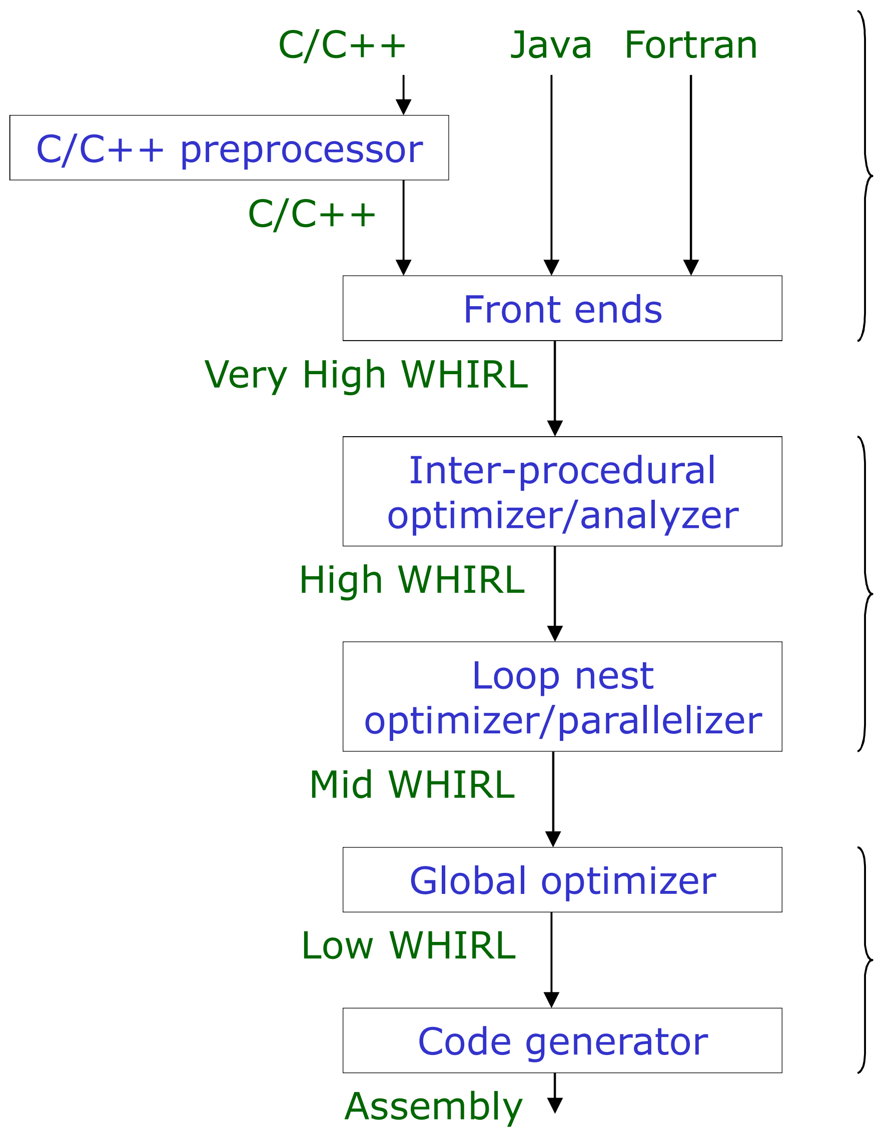
Course Outline

1. Introduction (we are now at it)
2. Instruction Level Parallelism Optimizations (Josep Llosa)
   - Instruction Level Parallelism
   - Machine Independent Optimizations
   - Instruction Scheduling
   - Register Allocation
3. Memory Hierarchy Optimizations (Josep Ramon Herrero)
   - Basic Concepts
   - Basic transformations
   - Combination of transformations
4. Thread Level Parallelism Optimizations (Marc González)
   - Thread level Parallelism
   - Analysis and detection of parallelism
   - Programming models
   - Parallel execution
   - Memory models

Awakening Some Interest in Compilers

- Traditional strength at UPC - Architecture
  - Superscalar processors, do everything in hardware
- Little on compilers
  - Hardware people have to understand compilers
    - No attention to compilers -> bad processor design
    - Architects with no compiler knowledge tend to introduce compiler unfriendly hardware features which cannot be effectively exploited
  - Compilers required to effectively exploit hardware features
    - Expose ILP for the processor (even superscalar)
    - Exploit memory locality
    - Parallelize code for multiprocessors/multicomputers
  - Optimizing applications
    - Understanding how the compiler works helps to optimize source level code

Structure of a real compiler: ORC



Front end
Traditional compilers class
(parsing, analysis, etc…)
NOT this course topic

Middle end
Covered in topics:
3) Memory optimizations
4) TLP optimizations

Back end
Covered in topic:
2) ILP optimizations

Structure of a real compiler: ORC

- IPA: Inter-procedural analyzer
  - Analyzes a routine and transfers the information beyond the scope of the routine
  - Some Optimizations:
    - Inlining
    - Cloning
    - Dead function/variable elimination
    - Constant propagation
- LNO: Loop nest optimizer/parallelizer
  - Performs high level transformation to better use cache memory and to enhance/expose thread level parallelism (parallelization only partially implemented)
  - Some Optimizations:
    - Loop fission
    - Loop fusion
    - Unroll & jam
    - Loop interchange
    - Loop peeling
    - Loop tiling
    - Data prefetching

Structure of a real compiler: ORC

- WOPT: Global Optimizer
  - Performs machine independent optimizations at the procedure level
  - Some Optimizations:
    - Dead code elimination
    - Partial redundancy elimination
    - Strength reduction
    - Induction variable elimination
    - Register promotion
- CG: Code Generator
  - Performs machine dependent optimizations and code generation/optimization
  - Some Optimizations:
    - If conversion
    - Software pipelining
    - Predication
    - Global instruction scheduling
    - Register allocation
    - Local instruction scheduling

Course Grades

What to do to pass the course:

- Attendance control: Attend all classes, missed classes mean a reduced score in participation.
  - Every missed class reduces 0.2 points the attendance score
  - 0 to 2 missed classes is acceptable -> no points deducted
  - 3 missed classes 0.6 will be deducted
  - 10 or more missed classes no attendance score
- Course presentation:
  - Each student must prepare a class on a particular topic (more on that later)
- Report:
  - Write a report on your topic
- Read other students reports:
  - Ask questions during other students presentations

- 40% deliverable of assignment
- 40% presentation of assignment
- 20% attendance and participation in class

About presentations

- Students will work in groups of 2 students
- Each group must prepare a 25 minutes class on a particular topic
  ⇒ 25 minutes is a hard limit you will be interrupted if you overextend
- There is a list of starting papers for each topic
  ⇒ Research other related papers
- Do NOT describe individual papers
  ⇒ Present the topic in a related & coherent way
- Don’t take everything you read as a fact
  ⇒ Be critical

About presentations

- The objective is NOT to show the professors that you know a lot about your topic

  ⇒ The objective is that the other students learn what you know

- Don’t explain everything you have read in 25 minutes

  ⇒ Limit the scope of you presentation to fit in 25 minutes you can make a short overview and explain in depth the most important aspects

- Presentations will be done at class time the last weeks of the course (exact schedule to be announced)

About Reports

- Each group must write a report on his topic
- Approximate size of report should be ~20 pages
  - This is not a hard limit, there is no problem if you can explain all you need in 15 pages or if you need 25 or 30, is just so you know the amount of work we expect (i.e. no need to write 100 pages ☺)
- If something does not fit in the class and you think is interesting, the report is the place to have it.

- Reports should be available before presentations start
  - Deadlines to be anounced
- All students HAVE TO read all the reports
- During presentations, students HAVE TO make questions related either to the presentation or to the report.

Assignment topics

- Instruction Level Parallelism Optimizations
  - Speculation & Predication
  - Acyclic code scheduling
  - Modulo scheduling for control intensive loops
  - Advanced register allocation
  - Scheduling & Register allocation
  - Instruction scheduling for clustered VLIW
- Memory Hierarchy Optimizations
  - Software prefetch
  - Improving instruction cache
  - Data cache optimizations
  - Compilation techniques for SIMD Architectures
- Thread Level Parallelism Optimizations
  - Parallelism detection
  - Dependence tests
  - Enabling parallelism
  - Parallelism execution

Speculation and Predication

- S. A. Mahlke, W. Y. Chen, R. A. Bringmann, R. E. Hank, W. W. Hwu, B. R. Rau, and M. S. Schlansker, “Sentinel Scheduling: A Model for Compiler-Controlled Speculative Execution,” ACM Transactions on Computer Systems, vol. 11, no. 4, pp. 376-408, Nov. 1993
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- Y. Choi, A. Knies, L. Gerke, and T.-F. Ngai, “The Impact of If-Conversion and Branch Prediction on Program Execution on the Intel Itanium Processor,” Proceedings of the 34th Annual International Symposium on Microarchitecture, pp. 182-191, Dec. 2001

Acyclic code scheduling

- A new viewpoint on code generation for directed acyclic graphs S. Liao, K. Keutzer, S. Tjiang, S. Devadas January 1998 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 3 Issue 1
- Avoidance and suppression of compensation code in a trace scheduling compiler
  Stefan M. Freudenberger, Thomas R. Gross, P. Geoffrey Lowney. July 1994, ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 16 Issue 4
- Performance evaluation of instruction scheduling on the IBM RISC System/6000. David Bernstein, Doron Cohen, Yuval Lavon, Vladimir Rainish. December 1992. ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture, Volume 23 Issue 1-2
- The impact of if-conversion and branch prediction on program execution on the Intel® Itanium¿ processor Youngsoo Choi, Allan Knies, Luke Gerke, Tin-Fook Ngai December 2001 Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture

Modulo scheduling for control intensive loops

- P. Tirumalai, M. Lee, M. Schlansker. Parallelization of loops with exits on pipelined architectures. Proceedings of the 1990 ACM/IEEE conference on Supercomputing.
- Daniel M. Lavery, Wen-mei W. Hwu. Modulo scheduling of loops in control-intensive non-numeric programs. Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture.
- Nancy J. Warter-Perez, Noubar Partamian. Modulo scheduling with multiple initiation intervals. Proceedings of the 28th annual international symposium on Microarchitecture.
- SangMin Shim, Soo-Mook Moon. Split-path enhanced pipeline scheduling for loops with control flows. Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture.

Advanced Register allocation.

- E. Eichenberger, Edward S. Davidson. Register allocation for predicated code. Proceedings of the 28th annual international symposium on Microarchitecture.
- Bernhard Scholz, Erik Eckstein. Register allocation for irregular architectures ACM SIGPLAN Notices , Proceedings of the joint conference on Languages, compilers and tools for embedded systems: software and compilers for embedded systems, Volume 37 Issue 7.
- Jinpyo Park, Soo-Mook Moon. Optimistic register coalescing. ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 26 Issue 4.
- B. R. Rau, M. Lee, P. P. Tirumalai, M. S. Schlansker. Register allocation for software pipelined loops. SIGPLAN Not., volume 27, number 7, 1992, pages 283-299.

Scheduling & register allocation

- Register allocation with instruction scheduling. Shlomit S. Pinter. June 1993, ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1993 conference on Programming language design and implementation, Volume 28 Issue 6
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Instruction scheduling for clustered VLIW

- Giuseppe Desoli. Instruction Assignment for Clustered VLIW DSP Compilers: A New Approach. HP Laboratories Cambridge, HPL-98-13 February, 1998
- Emre Özer, Sanjeev Banerjia, Thomas M. Conte. Unified assign and schedule: a new approach to scheduling for clustered register file microarchitectures. Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture
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Software prefetch

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- TC Mowry, MS Lam, A Gupta. Design and evaluation of a compiler algorithm for prefetching. ACM SIGPLAN Notices Volume 27 , Issue 9, September 1992.
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Improving Instruction Cache

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- Karl Pettis and Robert C. Hansen. 1990. Profile guided code positioning. SIGPLAN Not. 25, 6 (Jun. 1990), 16–27. DOI:https://doi.org/10.1145/93548.93550
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Data Cache Optimizations

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- Steve Carr and Ken Kennedy. 1994. Improving the ratio of memory operations to floating-point operations in loops. *ACM Trans. Program. Lang. Syst.* 16, 6 (November 1994), 1768-1810.
- Steve Carr, Kathryn S. McKinley, and Chau-Wen Tseng. 1994. Compiler optimizations for improving data locality. *SIGPLAN Not.* 29, 11 (November 1994), 252-262.
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Compilation techniques for SIMD Architectures

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Parallelism Detection

- "Efficient and Precise Array Access Analysis", Y. Paek, J. Hoeflinger, D Padua ACM Transactions on Programming Languages and Systems (TOPLAS) Volume 24 , Issue 1 (January 2002) Pages: 65 - 109
- "Efficient Interprocedural Analysis for Program parallelization and restructuring", Z. Li and P. Yew SIGPLAN, June 1988.
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Dependence Tests

- Banerjee/Wolfe test
  - M.Wolfe, U.Banerjee, "Data Dependence and its Application to Parallel Processing", Int. J. of Parallel Programming, Vol.16, No.2, pp.137-178, 1987
- Range test
  - William Blume and Rudolf Eigenmann. Non-Linear and Symbolic Data Dependence Testing, IEEE Transactions of Parallel and Distributed Systems, Volume 9, Number 12, pages 1180-1194, December 1998.
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- I Test
  - Xiangyun Kong, David Klappholz, and Kleanthis Psarris, "The I Test: A New Test for Subscript Data Dependence," Proceedings of the 1990 International Conference on Parallel Processing, Vol. II, pages 204-211, August 1990.

Enabling Parallelism

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Parallelism Execution

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- Milind Kulkarni, Keshav Pingali, Bruce Walter, Ganesh Ramanarayanan, Kavita Bala, L. Paul Chew, "Optimistic Parallelism Requires Abstractions", PLDI2007
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