GIST EECS

HW#2 (Digital IC)

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(1) Inverter DC analysis

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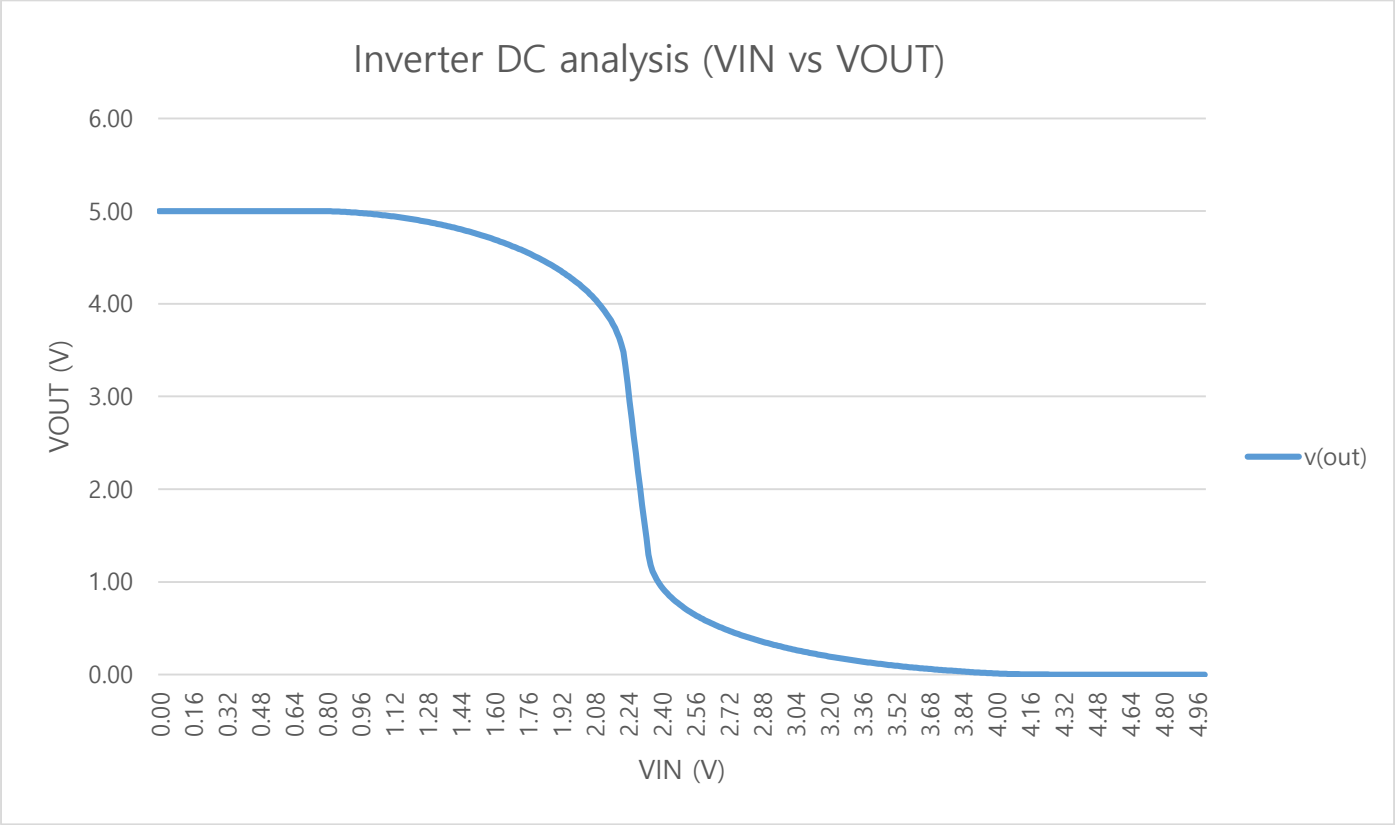
* inv.sp for SPICE3F5

.MODEL NMOS NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=5.36726E+15 VTO=0.743469 KP=8.00059E-05 GAMMA=0.543
+ PHI=0.6 U0=655.881 UEXP=0.157282 UCRIT=31443.8
+ DELTA=2.39824 VMAX=55260.9 XJ=0.25U LAMBDA=0.0367072
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
* Weff = WDrawn - Delta_W
* The suggested Delta_W is 1.9970E-07

.MODEL PMOS PMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=4.3318E+15 VTO=-0.738861 KP=2.70E-05 GAMMA=0.58
+ PHI=0.6 U0=261.977 UEXP=0.323932 UCRIT=65719.8
+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
* Weff = WDrawn - Delta_W
* The suggested Delta_W is 3.1280E-07

Vdd vdd 0 5.0
Vin in 0 0.0
M1 out in 0 0 NMOS W=2.4 L=1.2
M2 out in vdd vdd PMOS W=4.8 L=1.2

.op
.dc Vin 0 5 0.01
.print dc V(in) V(out)
.end
~
```



➔ The output voltage drops steeply when input voltage is around at 2.3V.

Vin (input Voltage)	PMOS	NMOS	Misc.
Vin < Vtn	Triode	Cut-off	Vtn : NMOS threshold voltage Vtp : PMOS threshold voltage
Vtn < Vin < VDD/2	Triode	Saturation	
Vin = VDD/2	Saturation	Saturation	
VDD/2 < Vin < VDD - |Vtp|	Saturation	Triode	
VDD - |Vtp| < Vin	Cut-off	Triode	

(2) NMOSFET I-V Characteristic for drain to source node (with gate voltage variation)

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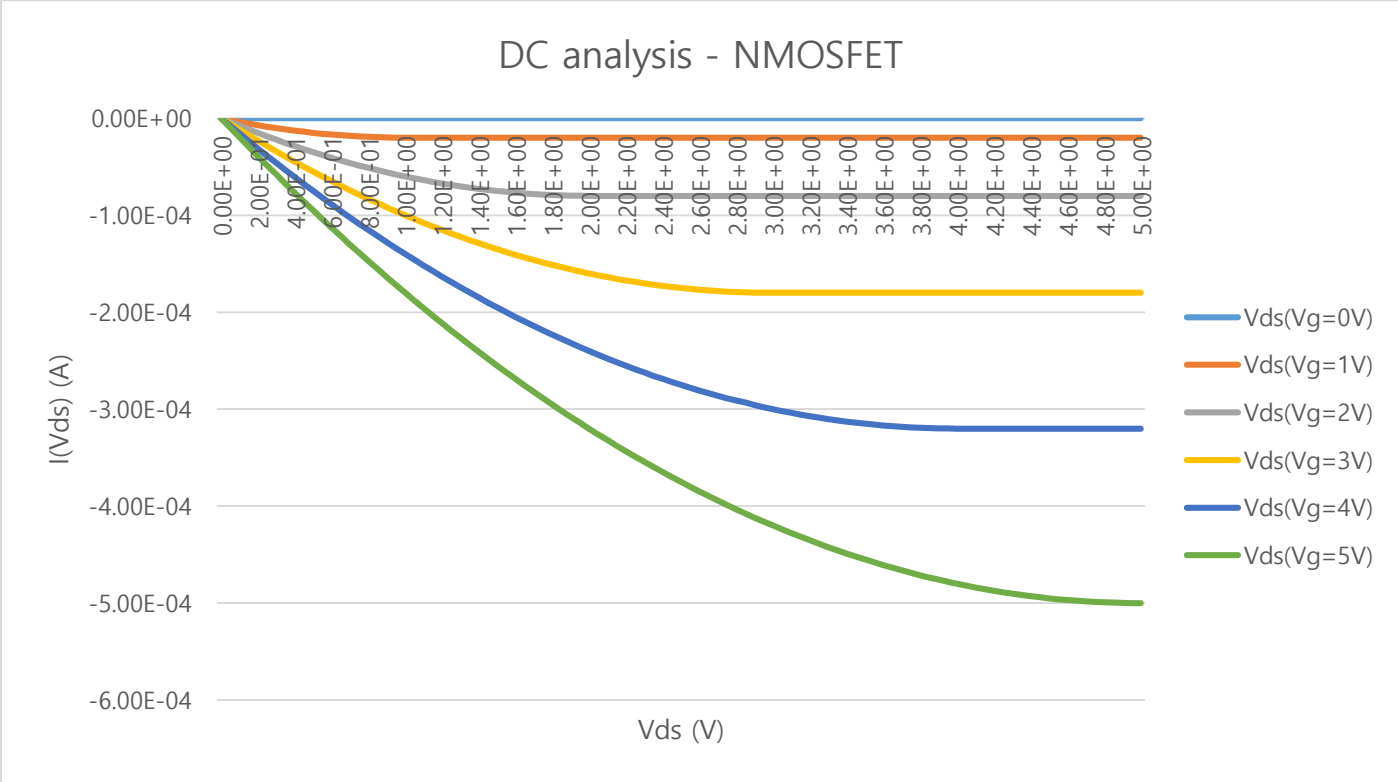
* mosiv.sp for SPICE3F5

include models_1p2mu.sp

Vgs g 0 0
Vds d 0 0
M1 d g 0 0 NMOS W=2.4 L=1.2

.dc Vds 0 5.0 0.05 Vgs 0 5.0 1.0
.print dc V(g) I(Vds)
.end
```



➔ current from drain to source node (Ids) increases when voltage dropped between drain to source node (Vds) increases. In addition, the current increases when gate voltage (Vgs) increases.

➔ The point where Ids saturates is depend on Vgs. The Vds value where Ids saturates become smaller as Vgs decreases.

(3) RC circuit (settling time)

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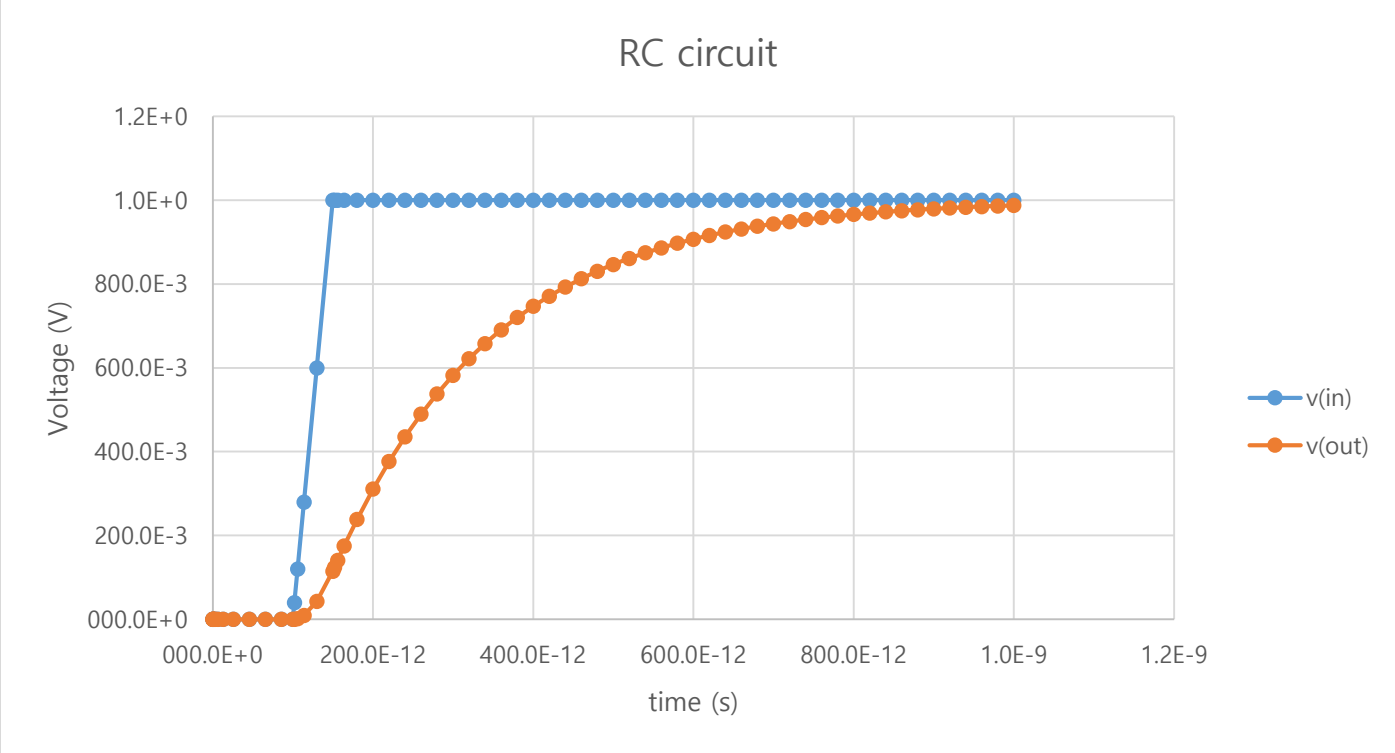
* rc.sp for SPICE3F5

Vin in 0 pwl 0ps 0 100ps 0 150ps 1.0 1ns 1.0
R1 in out 2K
C1 out 0 100f

.tran 20ps 1ns
.print tran V(in) V(out)
.end
~
```



➔ Since capacitor require few times to be charged, the output voltage of the RC circuit requires certain settling time to be equal to the input voltage.

➔ This is generally called "Passive Low Pass Filter (LPF)", which blocks high frequency signals, but passes low frequency ones.