DIC L3: Introduction (3)

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1.4. CMOS logic (3)

- CMOS NAND
  - If either input A or B is 0, at least one of the NMOSFETs will be OFF, breaking the path from Y to GND.

A	B	$Y = A$ NAND B
0	0	1
0	1	1
1	0	1
1	1	0

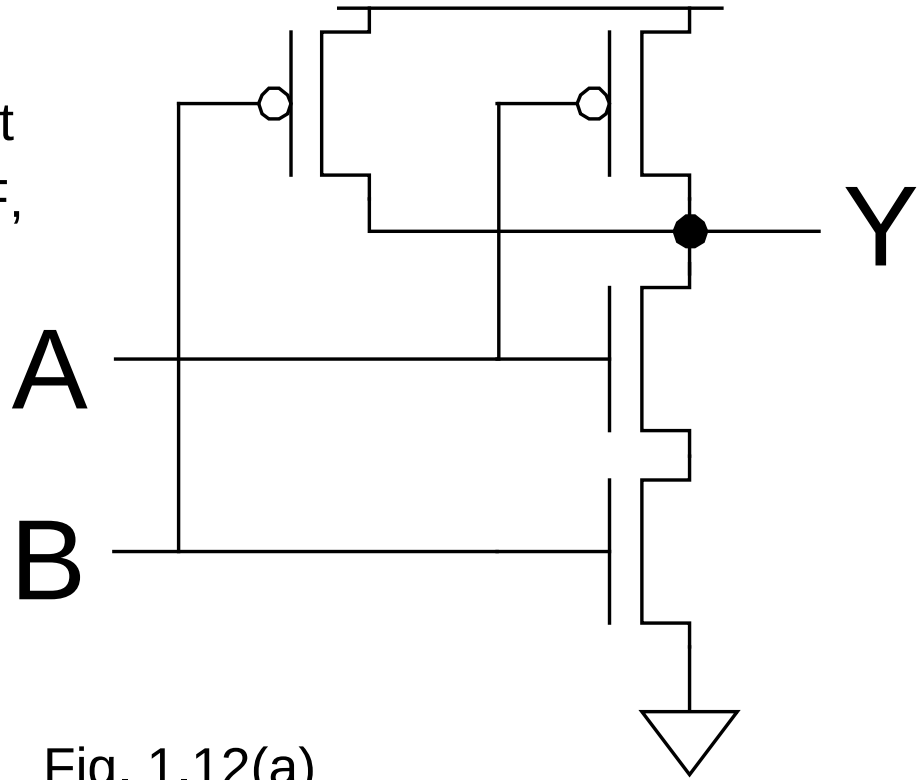


Fig. 1.12(a)

1.4. CMOS logic (4)

- Series and parallel
  - NMOS: 1 = ON
  - PMOS: 0 = ON
  - Series: Both must be ON.
  - Parallel: Either can be ON.

- Conduction complements
  - Pull-up ⟷ pull-down

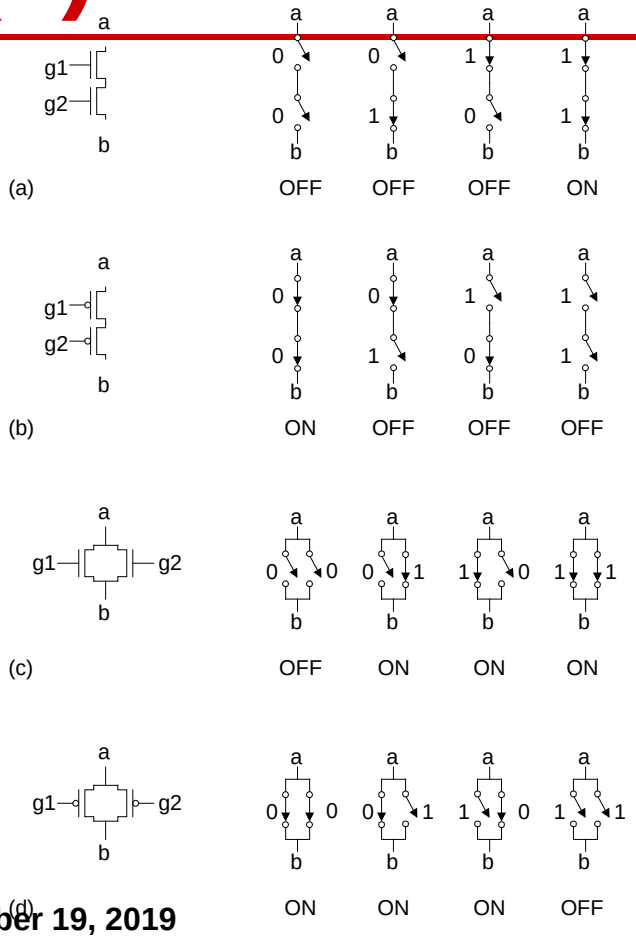


Fig. 1.15

1.4. CMOS logic (5)

- CMOS NOR

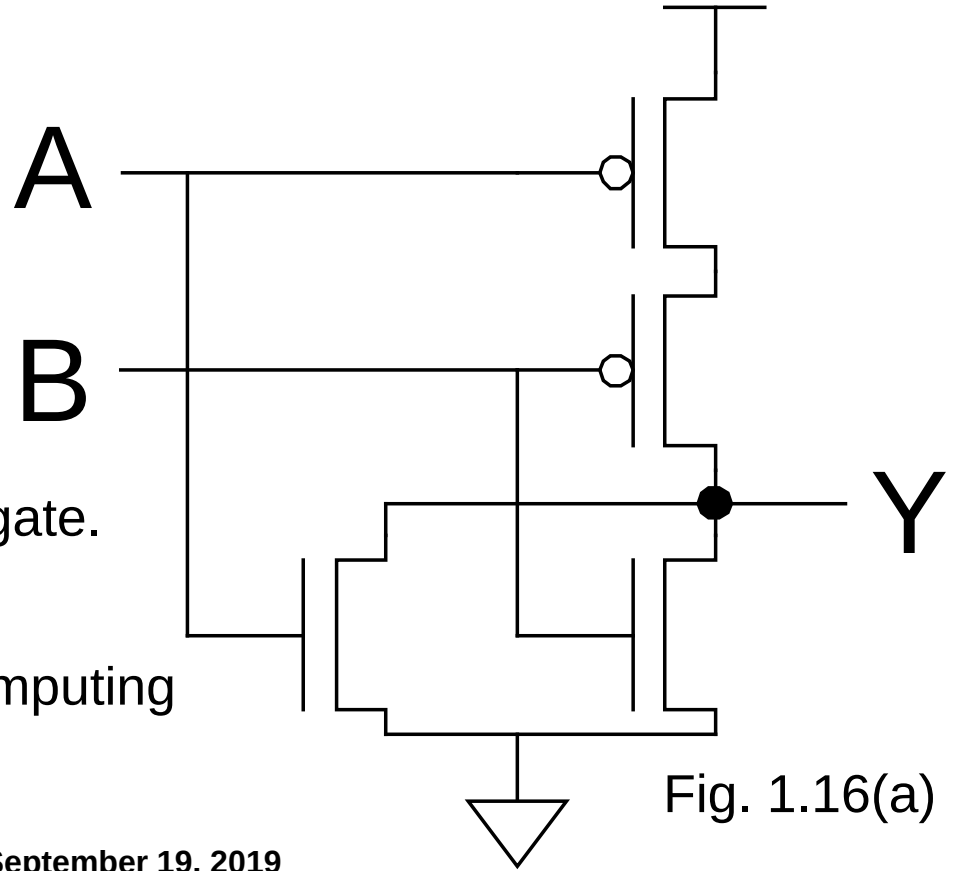
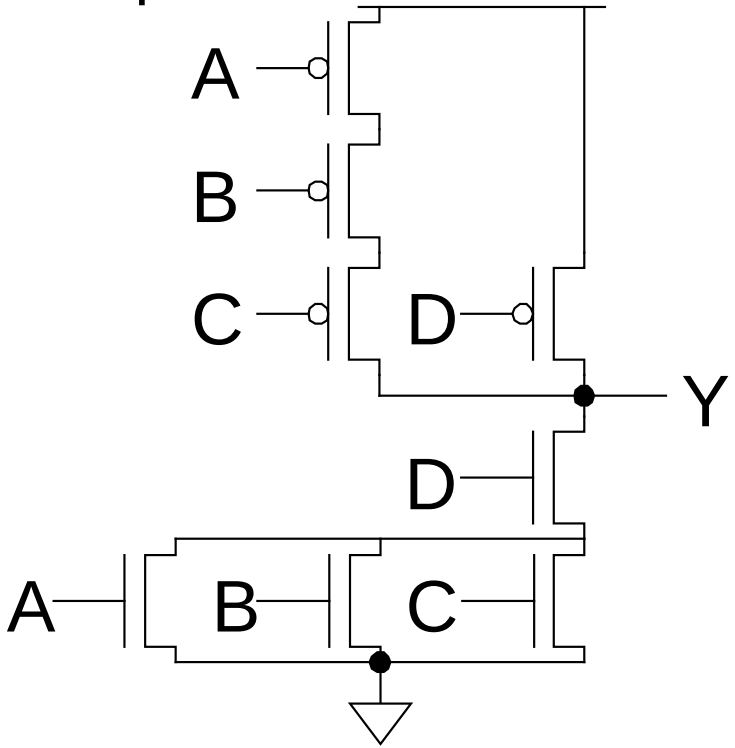


Fig. 1.16(a)

- Example 1.1
  - Sketch a 3-input CMOS NOR gate.
- Example 1.2
  - Sketch a static CMOS gate computing $Y = \overline{(A + B + C) \cdot D}$

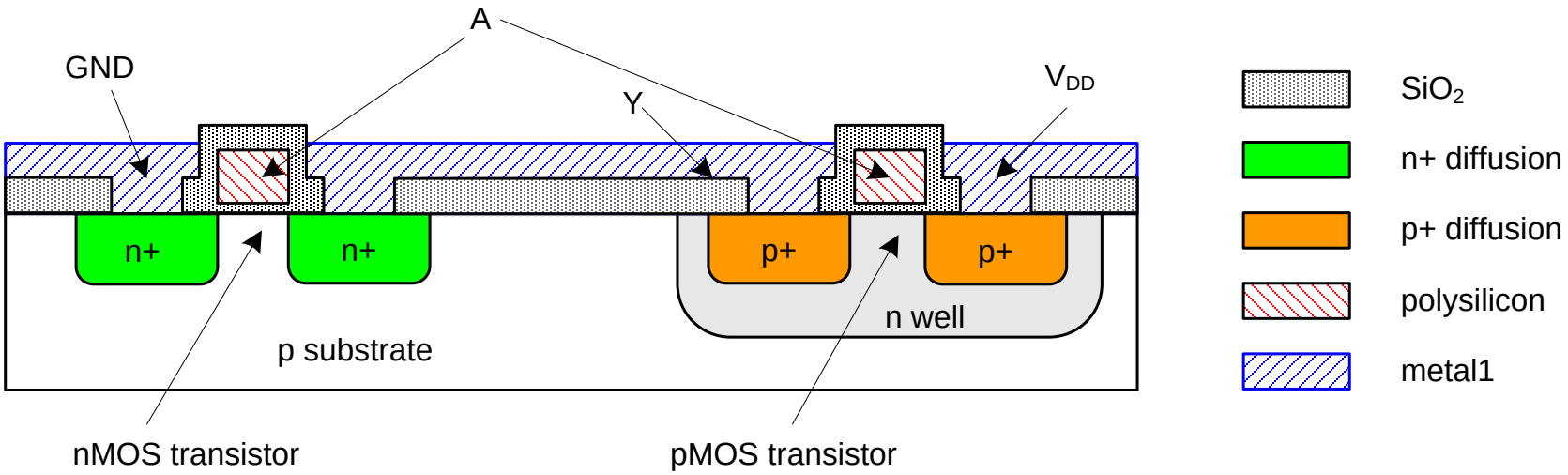
1.4. CMOS logic (6)

- The answer of Example 1.2



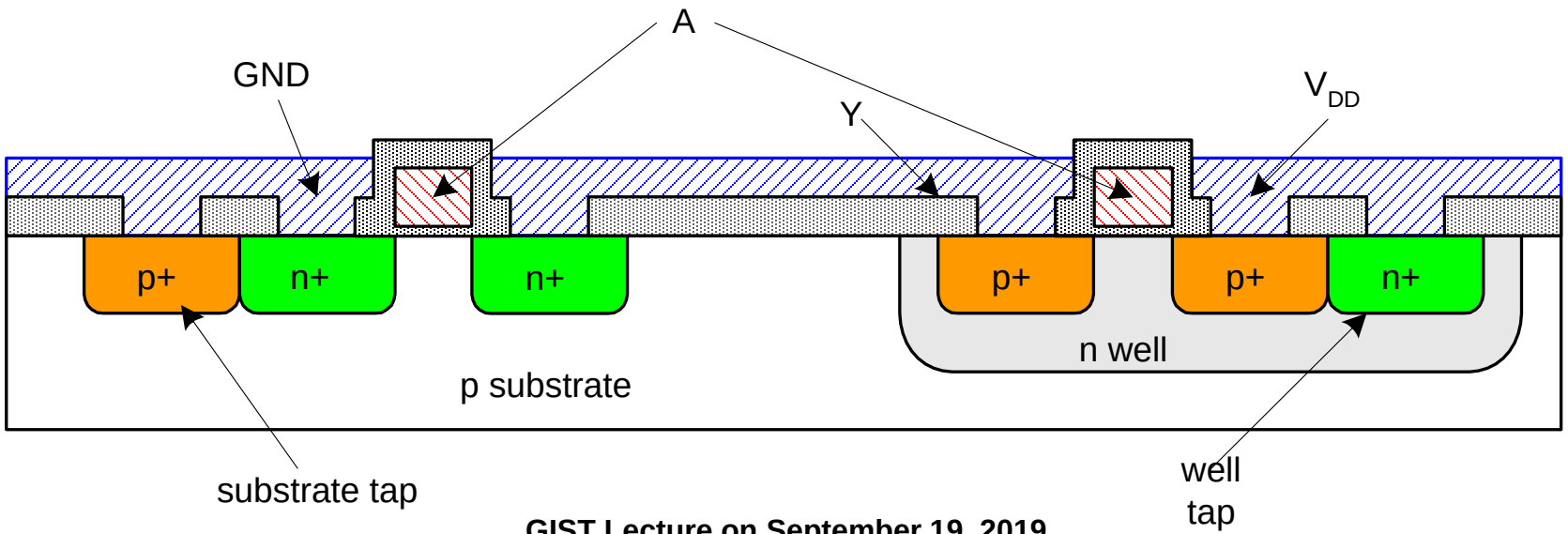
1.5. CMOS fabrication (1)

- Inverter cross-section



1.5. CMOS fabrication (2)

- Well and substrate taps



1.5. CMOS fabrication (3)

- Semiconductor process steps

1.5. CMOS layout (1)

- Inverter cross-section

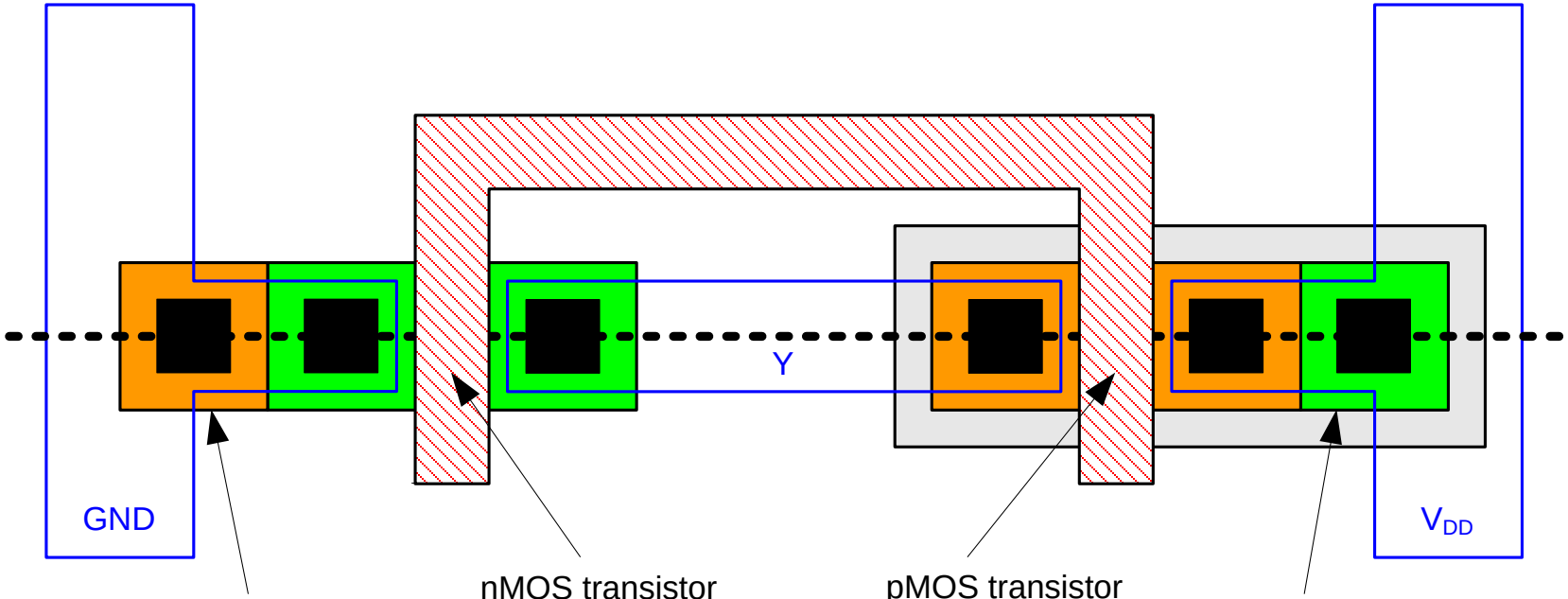


Fig. 1.35(a)

1.5. CMOS layout (2)

- Detailed mask views

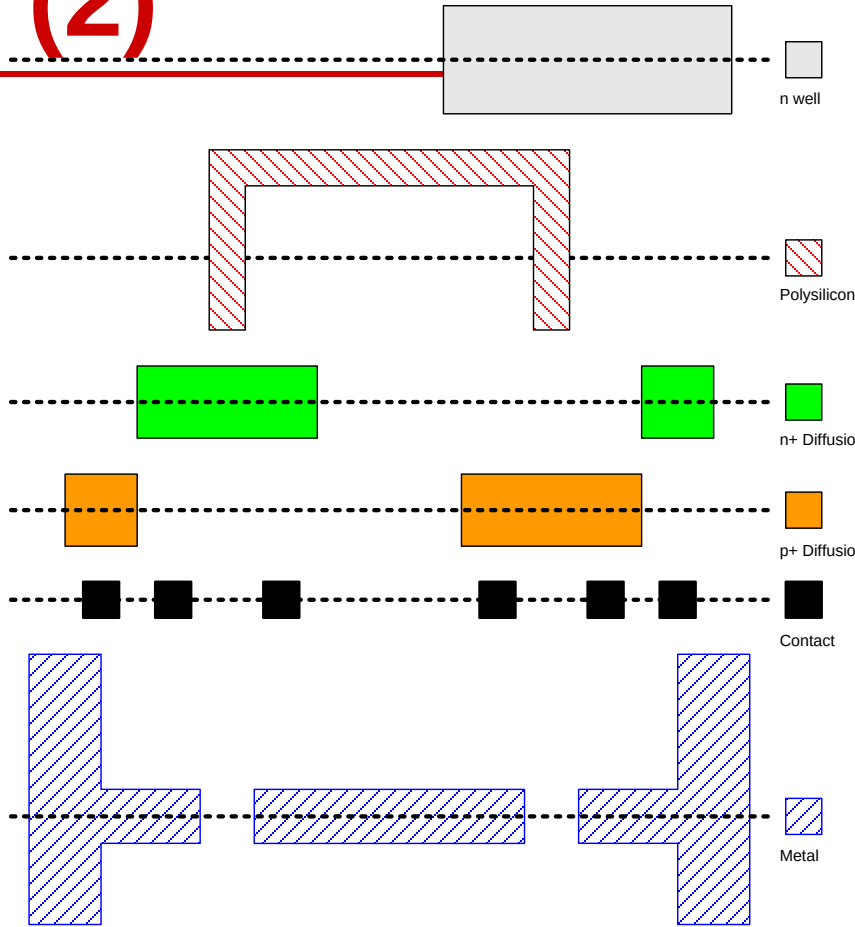


Fig. 1.35(b)-(g)

1.5. CMOS layout (3)

- Design rules in the textbook

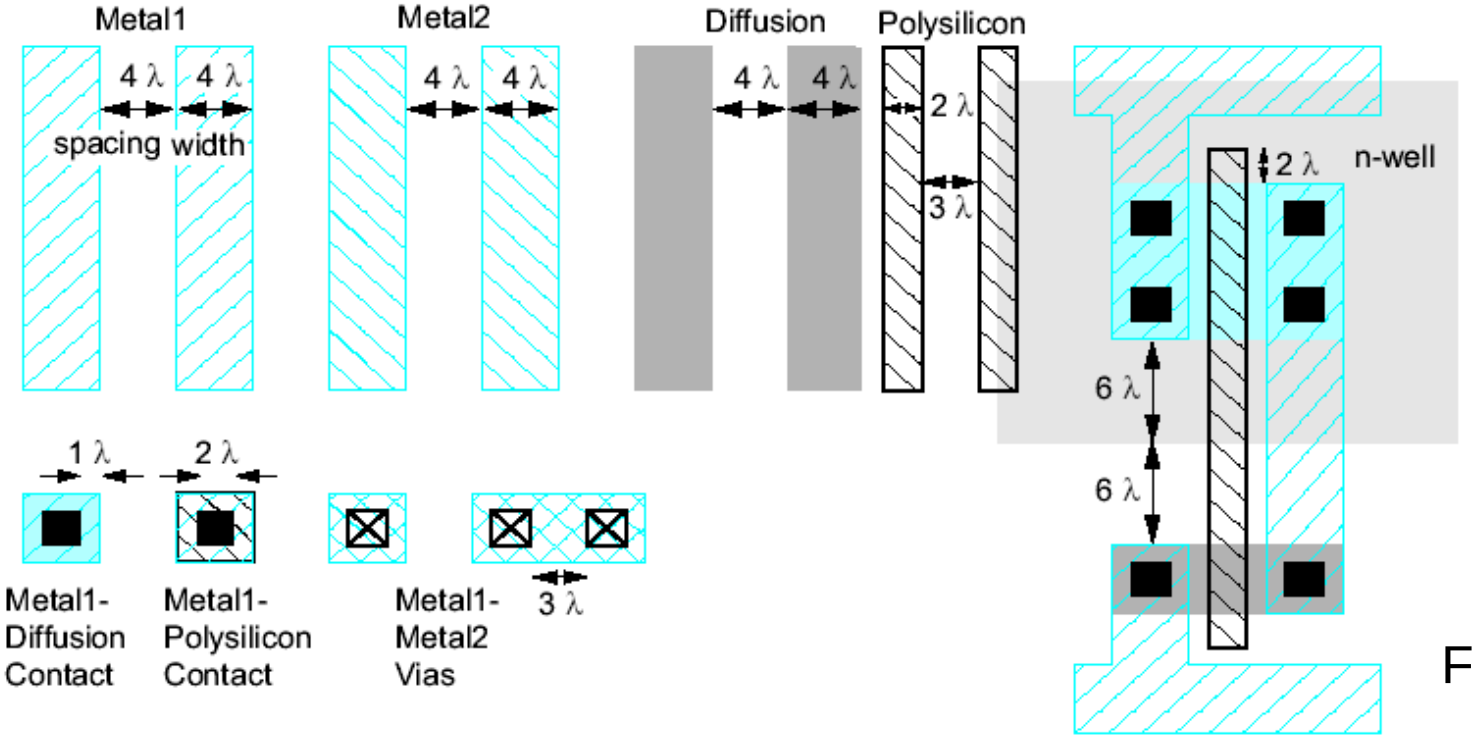
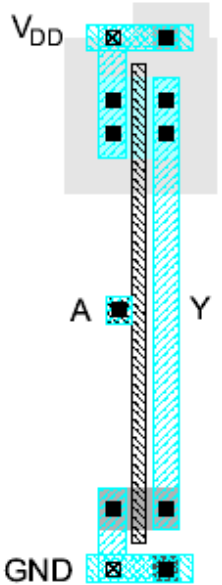
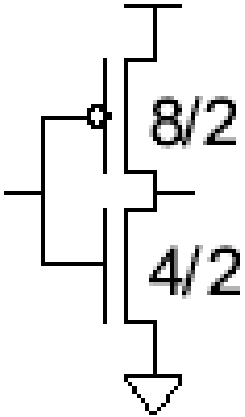


Fig. 1.39

1.5. CMOS layout (4)

- Inverter layout





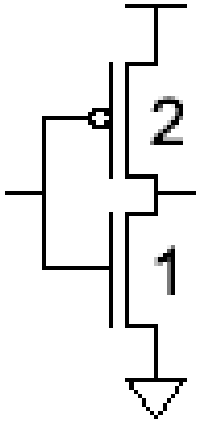


Fig. 1.40