DIC L2: Introduction (2)

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1.3. MOS transistors (6)

- PMOS
  - Similar, but doping and voltages are reversed.
  - Body is tied to V_{DD}.
  - V_{GS} is negative.

Metal (Polysilicon gates are gone.)

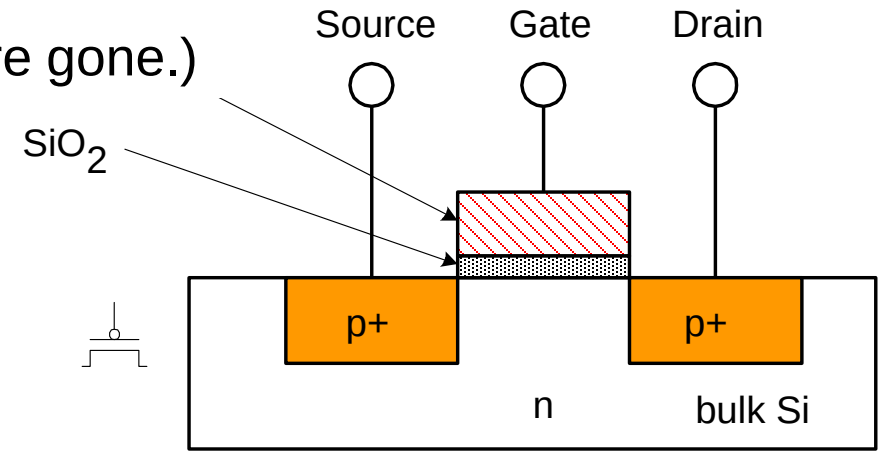
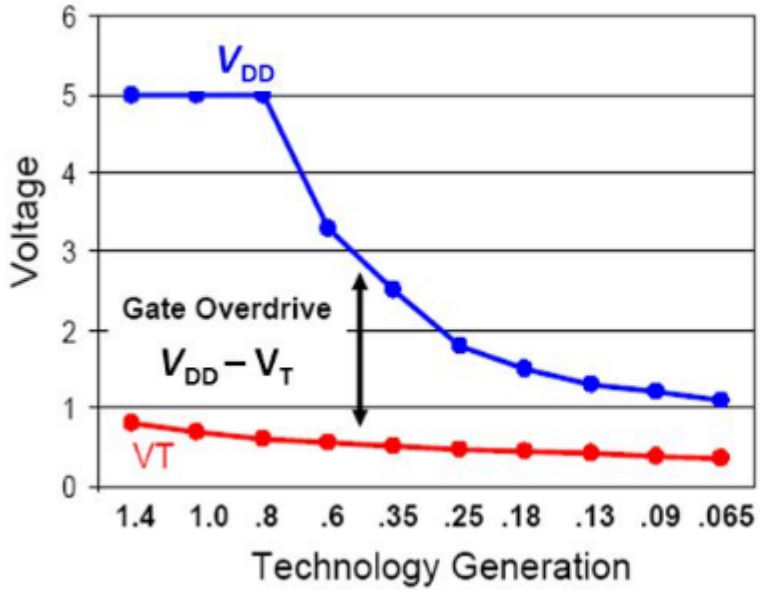


Fig. 1.9(b)

1.3. MOS transistors (7)

- Power supply voltageMOS
  - In 1980's, V_{DD} was 5 V.
- IEDM(or VLSI) papers
  - 130nm: 2000
  - 90nm: 2003
  - 65nm: 2004
  - 45nm: 2007
  - 32nm: 2008
  - 22nm: 2012
  - 14nm (or 16nm): 2014



Source: P. Packan (Intel), 2007 IEDM Short Course

1.3. MOS transistors (8)

- Transistors as switches
  - V_G controls path from source to drain.

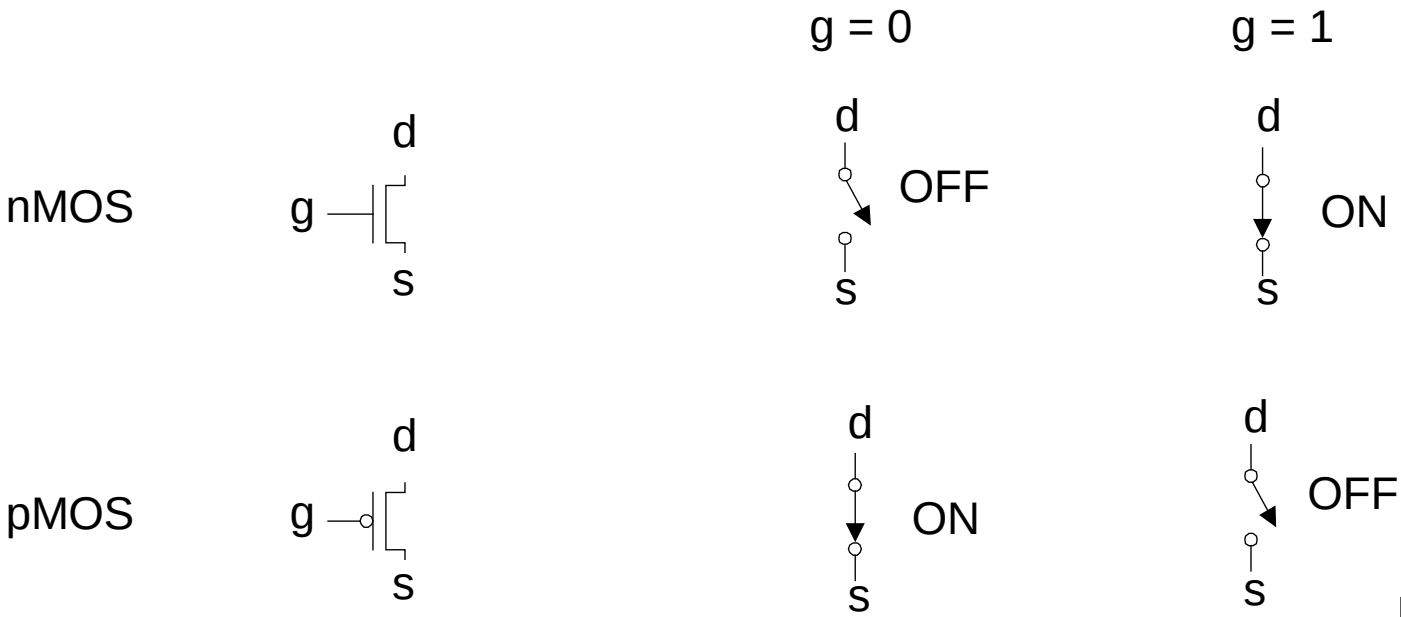


Fig. 1.10

1.4. CMOS logic (1)

- CMOS inverter
  - When the input A is 0,

    the NMOS transistor is OFF and

    the PMOS transistor is ON.
  - Thus, the output Y is pulled up to 1.

A	$Y = NOT\ A$
0	1
1	0

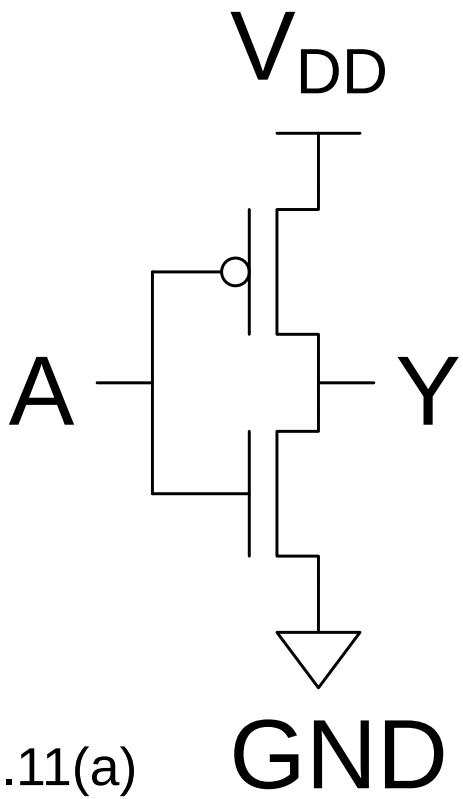


Fig. 1.11(a)

1.4. CMOS logic (2)

- CMOS NAND
  - If either input A or B is 0, at least one of the NMOSFETs will be OFF, breaking the path from Y to GND.

A	B	$Y = A$ NAND B
0	0	1
0	1	1
1	0	1
1	1	0

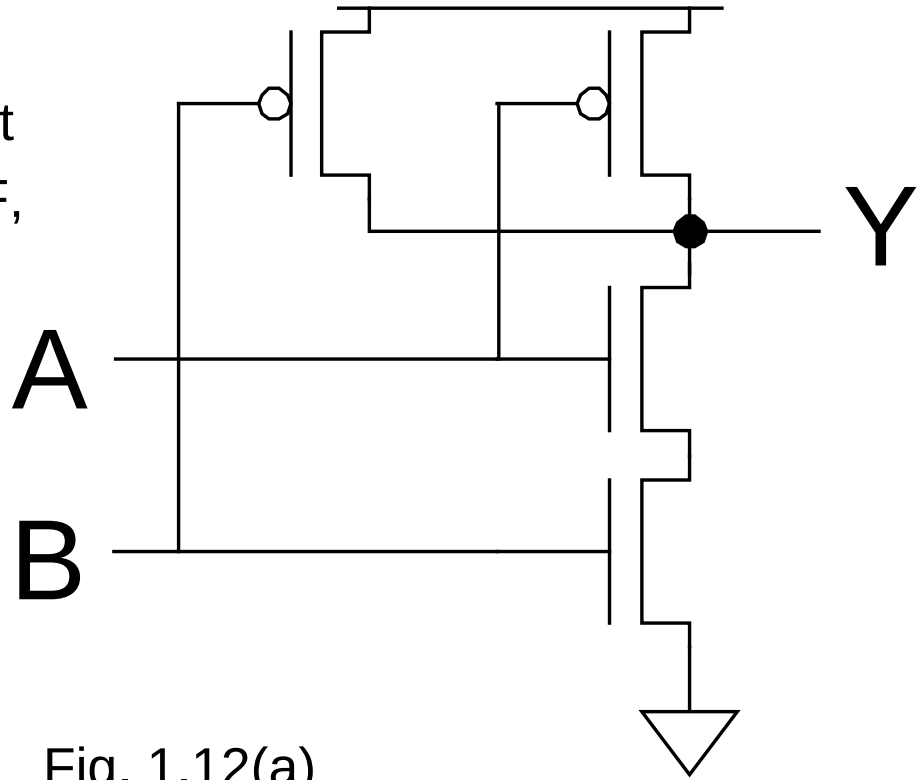
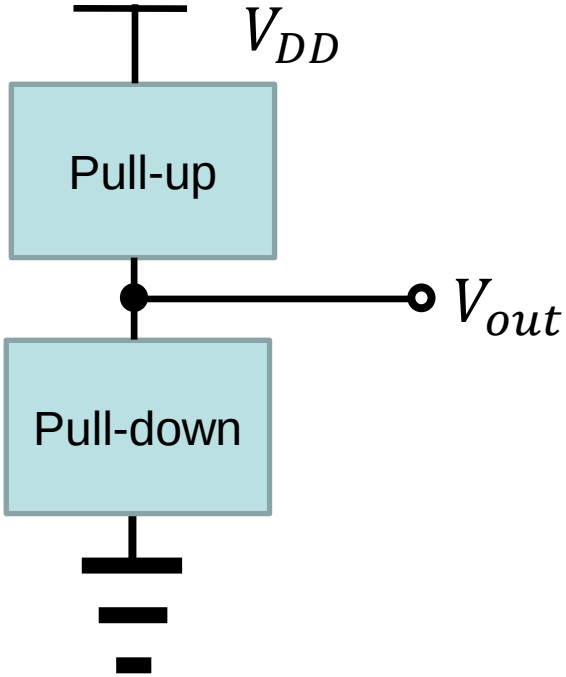


Fig. 1.12(a)

1.4. CMOS logic (3)

- Complementary CMOS gates
- Pull-down and pull-up networks
  - NMOS pull-down
  - PMOS pull-up



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z	1
Pull-down ON	0	Crowbarred (X)

1.4. CMOS logic (4)

- CMOS NOR

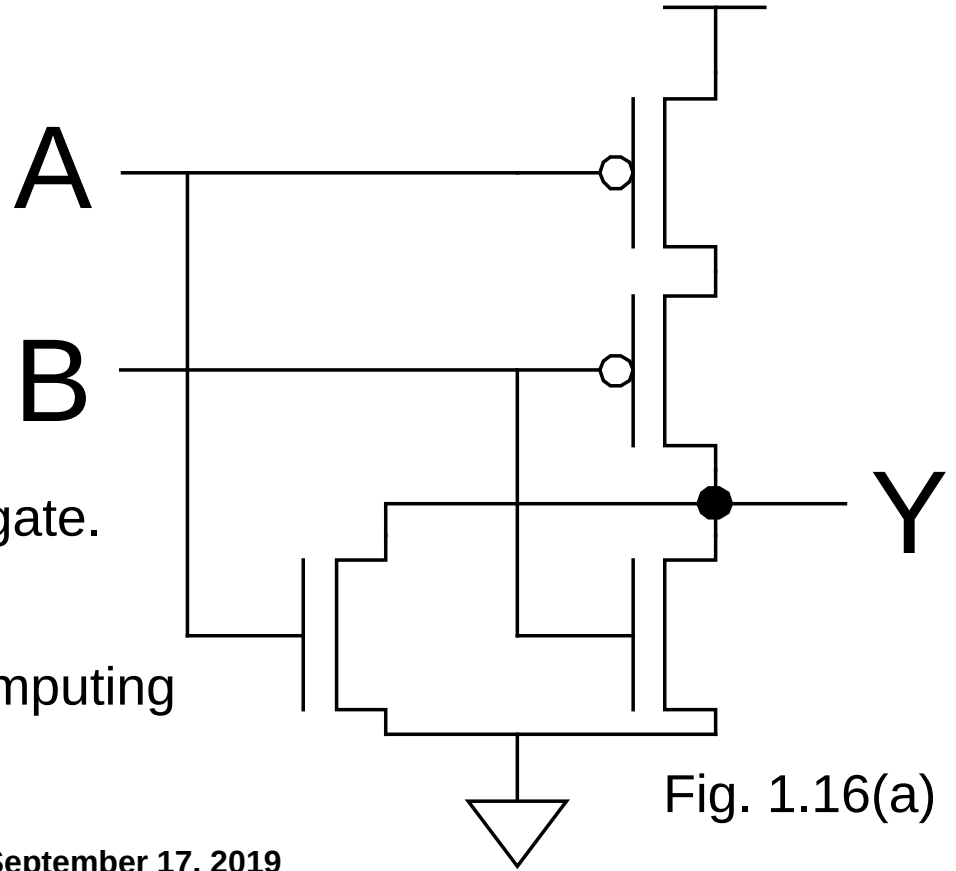
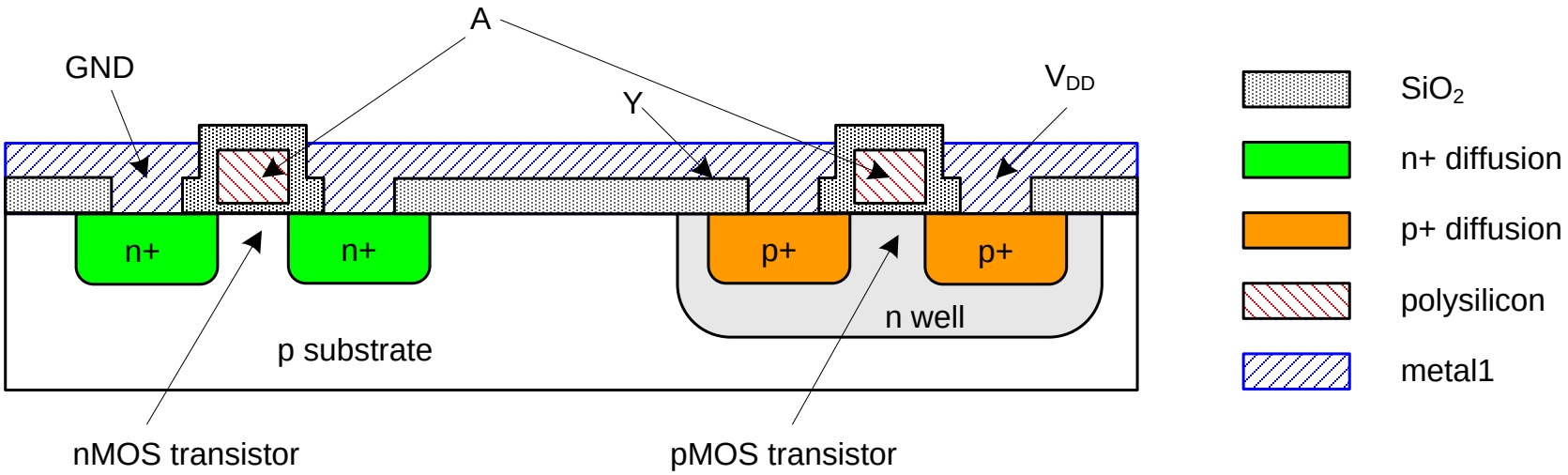


Fig. 1.16(a)

- Example 1.1
  - Sketch a 3-input CMOS NOR gate.
- Example 1.2
  - Sketch a static CMOS gate computing $Y = \overline{(A + B + C) \cdot D}$

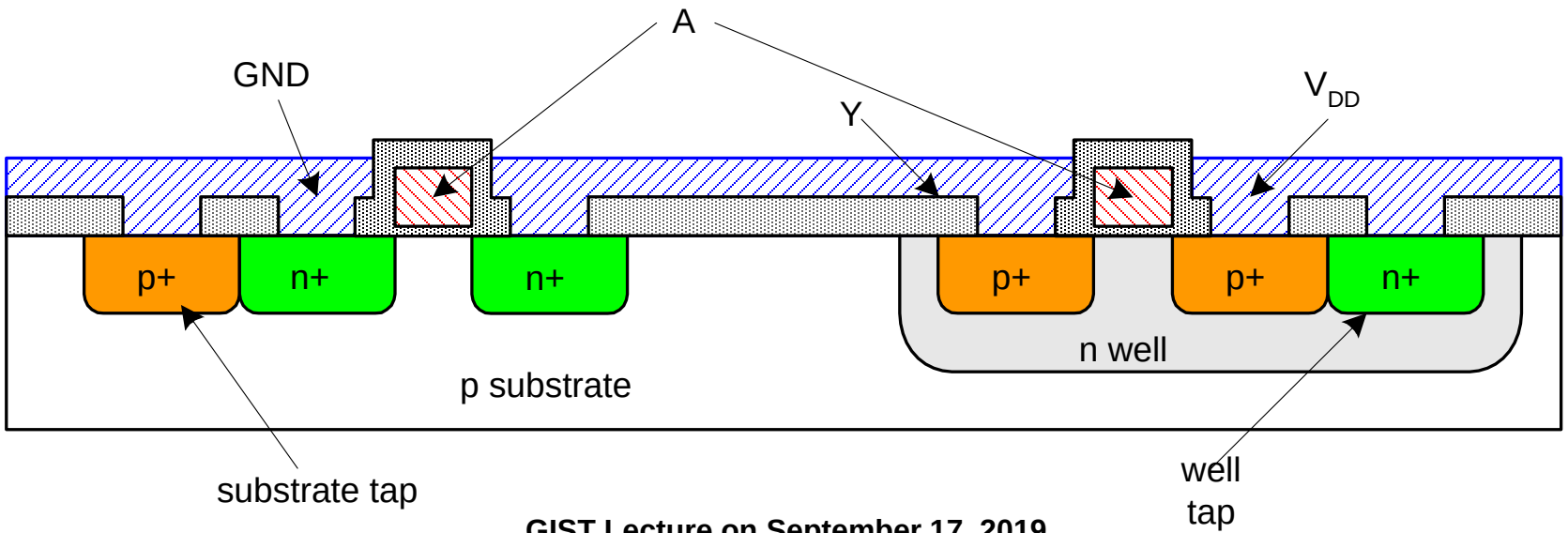
1.5. CMOS fabrication (1)

- Inverter cross-section



1.5. CMOS fabrication (2)

- Well and substrate taps



1.5. CMOS fabrication (3)

- Semiconductor process steps

1.5. CMOS layout (1)

- Inverter cross-section

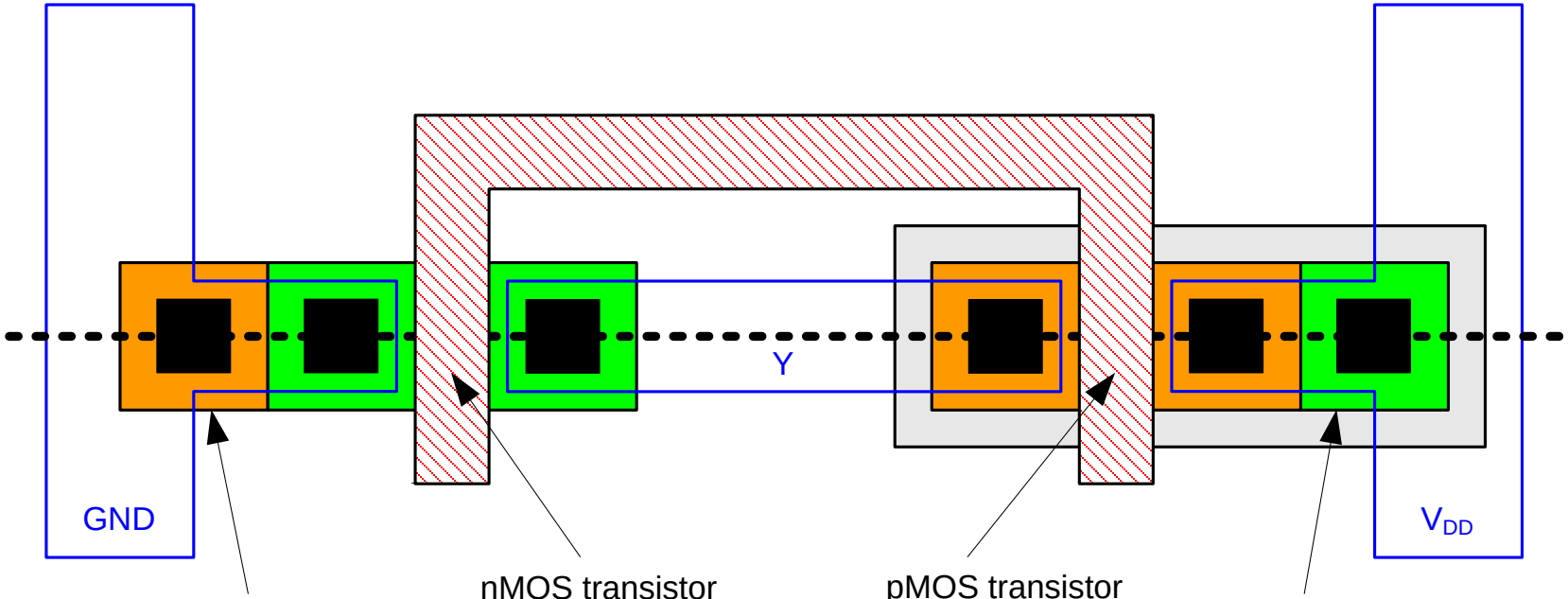


Fig. 1.35(a)

1.5. CMOS layout (2)

- Detailed mask views

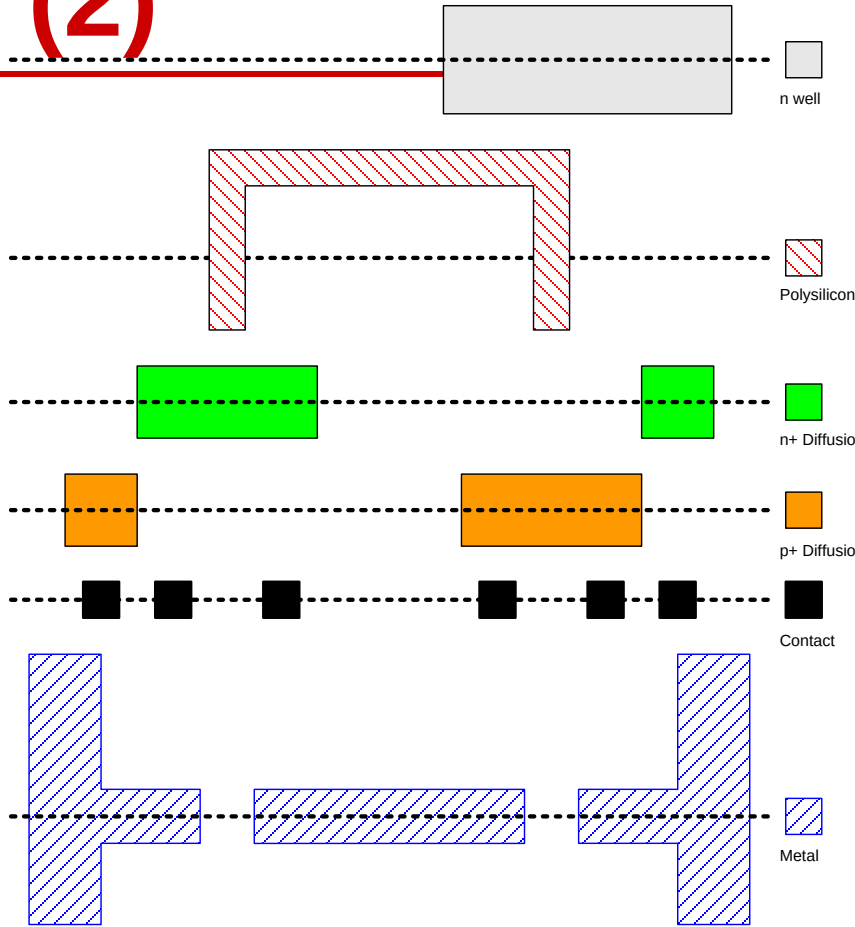


Fig. 1.35(b)-(g)

1.5. CMOS layout (3)

- Design rules in the textbook

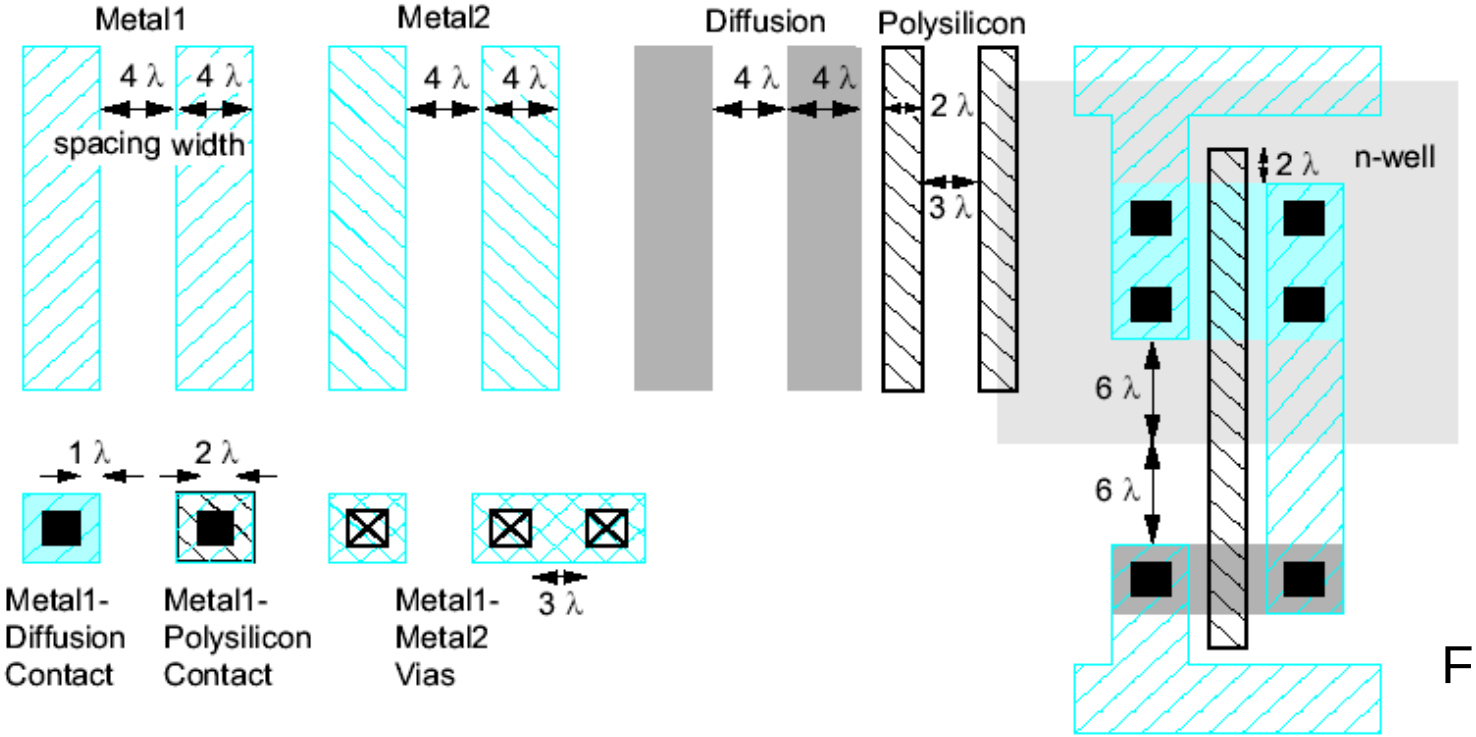
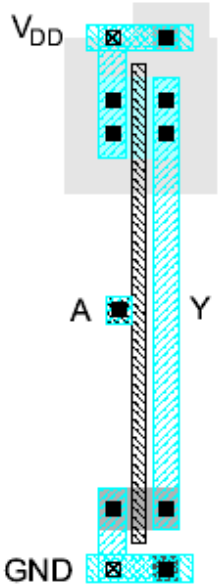
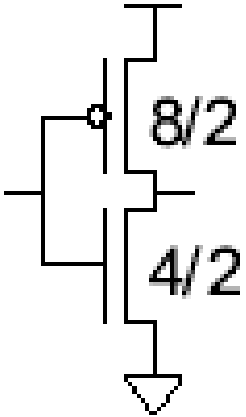


Fig. 1.39

1.5. CMOS layout (4)

- Inverter layout





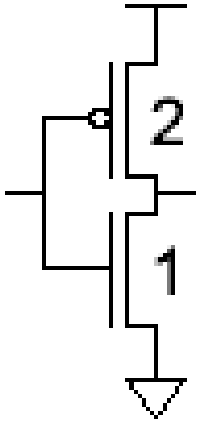


Fig. 1.40