
DIC L9: MOSFET (3)

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2.4. Nonideal IV (1)

- Review of ideal IV characteristics

- After some manipulation, we have

Subthreshold $I_d = 0$

Linear $I_d = \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$

Saturation $I_d = \frac{\beta}{2} (V_{gs} - V_t)^2$

- Here,

$$\beta = \mu_n C_{OX} \frac{W}{L}$$

Drain current



Drain voltage

2.4. Nonideal IV (2)

- 65nm IBM

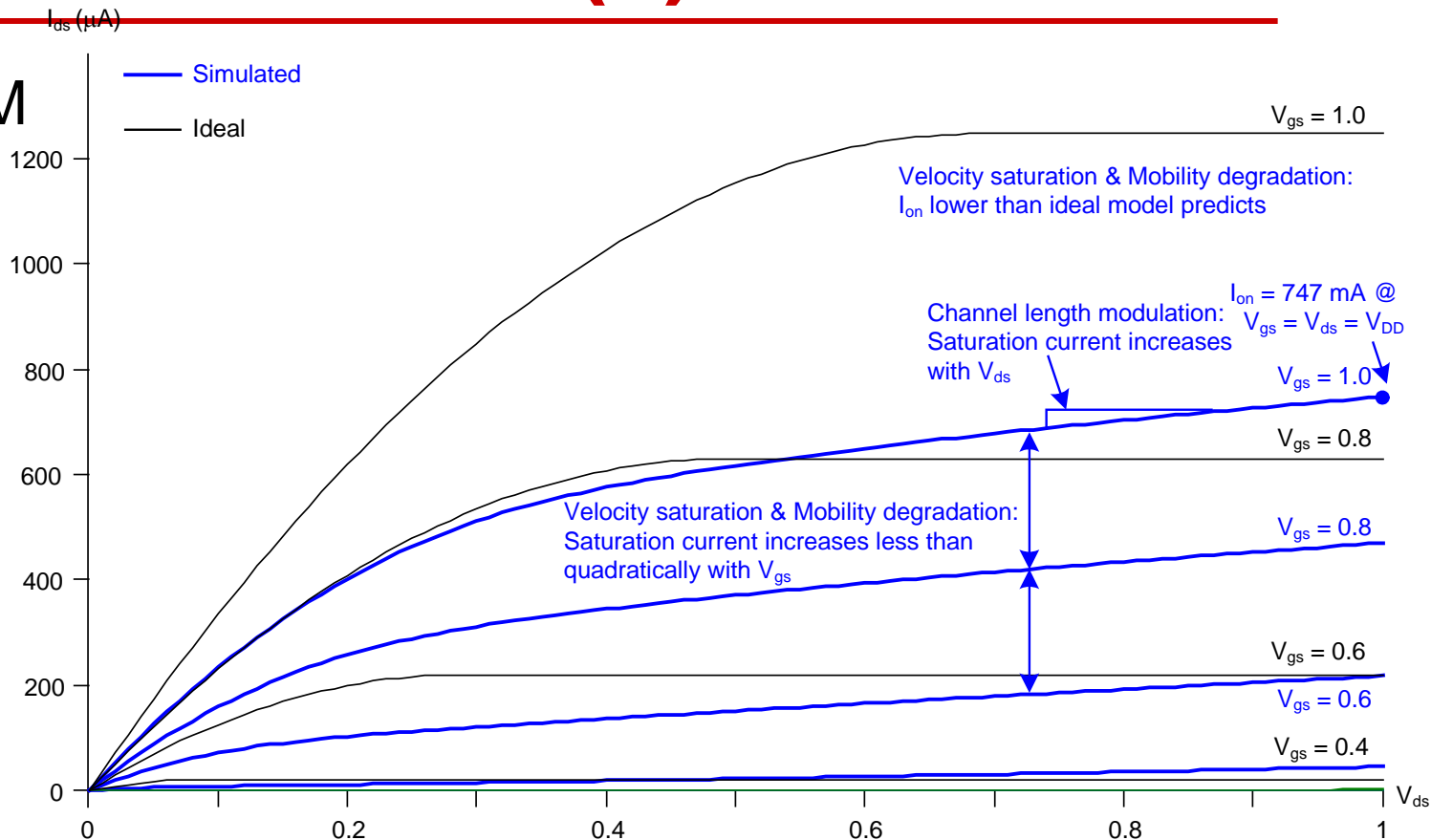
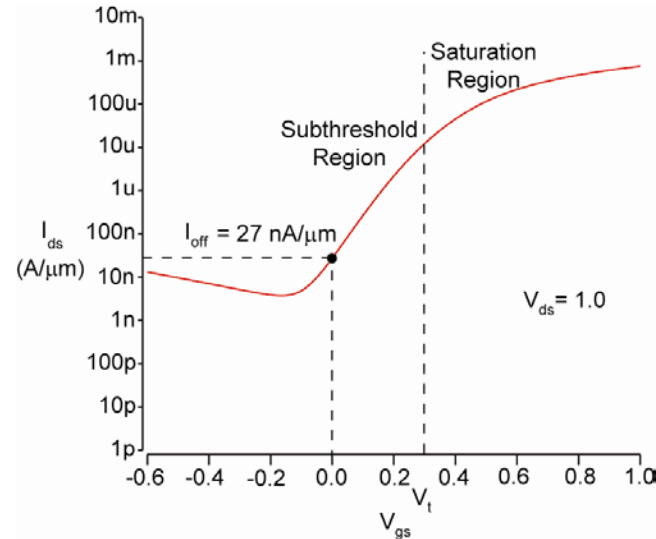
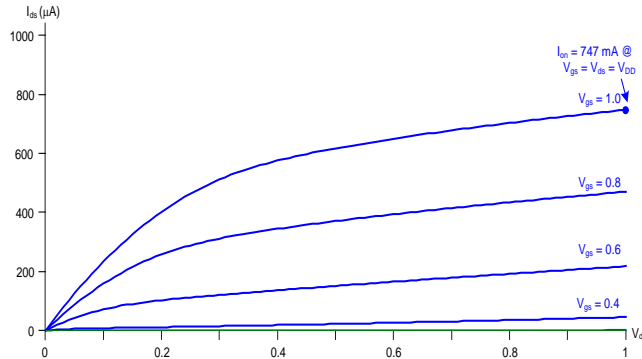


Fig. 2.14

2.4. Nonideal IV (3)

- ON and OFF currents (Drain currents)
 - ON current: $V_{gs} = V_{ds} = V_{DD}$
 - OFF current: $V_{gs} = 0, V_{ds} = V_{DD}$ (In the ideal model, it vanishes.)



2.4. Nonideal IV (4)

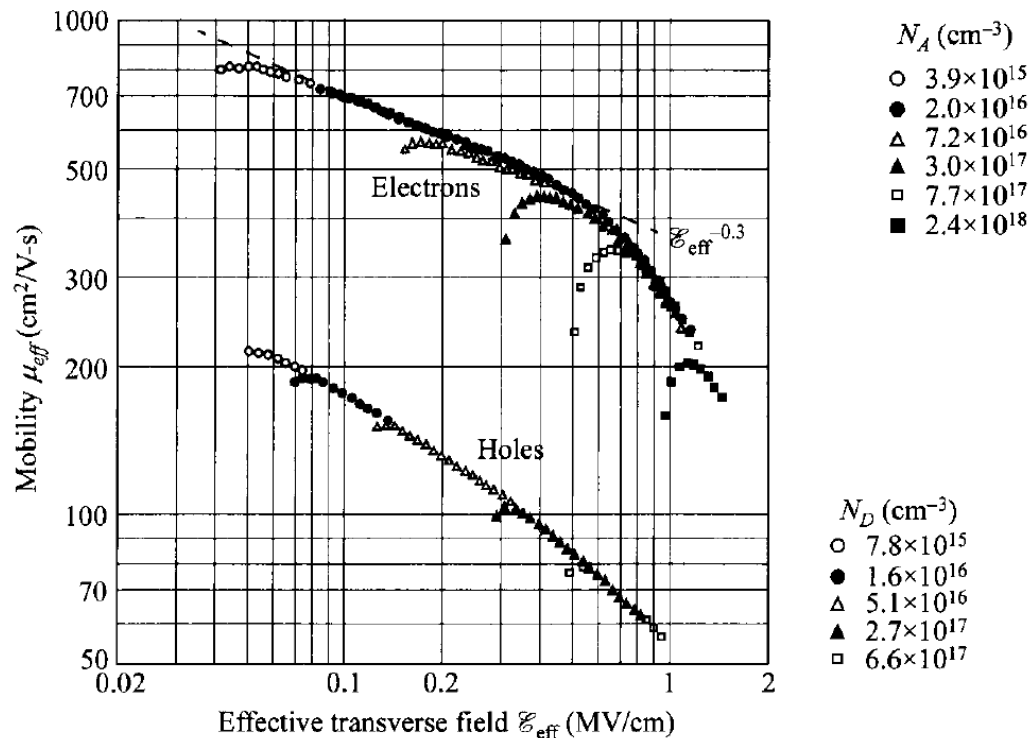
- Mobility degradation due to the vertical E-field
 - Collisions with oxide interface

$$\mu_{\text{eff}-n} = \frac{540 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \left(\frac{V_{gs} + V_t}{0.54 \frac{\text{V}}{\text{nm}} t_{\text{ox}}} \right)^{1.85}} \quad \mu_{\text{eff}-p} = \frac{185 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \frac{\left| V_{gs} + 1.5V_t \right|}{0.338 \frac{\text{V}}{\text{nm}} t_{\text{ox}}}} \quad \text{Eq. (2.23)}$$

- Why do we have different behaviors for electrons and holes?

2.4. Nonideal IV (5)

- Experimental data (So-called “universal” mobility)



Inversion-layer
mobility (Sze's
book)

2.4. Nonideal IV (6)

- Example 2.3
 - Calculation of the mobilities at $|V_{gs}| = 1.0$ V. Assume that $t_{ox} = 1.05$ nm and $|V_t| = 0.3$ V.

```
>> 540 / (1 + ((1.0+0.3)/(0.54*1.05))^1.85)
```

```
ans =
```

```
95.7177
```

```
>> 185 / (1 + ((1.0+1.5*0.3)/(0.338*1.05))^1.0)
```

```
ans =
```

```
36.3768
```

2.4. Nonideal IV (7)

- Velocity saturation
 - Saturation velocity (Canali model)
 - Electrons: 1.07×10^7 cm/sec
 - Holes: 8.37×10^6 cm/sec
 - Simple model

$$v = \begin{cases} \frac{\mu_{\text{eff}} E}{1 + \frac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \quad E_c = \frac{2v_{\text{sat}}}{\mu_{\text{eff}}}$$

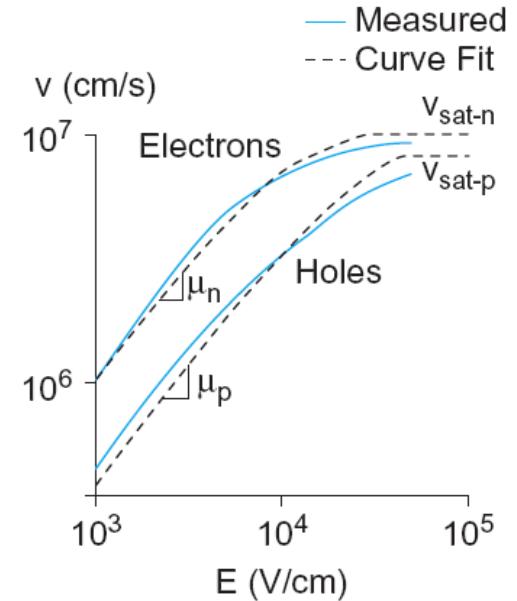


Fig. 2.15

2.4. Nonideal IV (8)

- Example 2.4

- Then, the critical fields are given by 208 kV/cm (electrons) and 444 kV/cm (holes), respectively.
- Assume that the channel length is 50 nm.
- Then, at 1.04 V (NMOS) and 2.22 V (PMOS), the carrier velocities are saturated.
- The NMOS transistor is velocity saturated in normal operation.

>> 2 * 1e7 / 96

ans =

2.0833e+05

>> 2 * 8e6 / 36

ans =

4.4444e+05

2.4. Nonideal IV (9)

- Leakage
 - Subthreshold slope
 - DIBL
 - GIDL

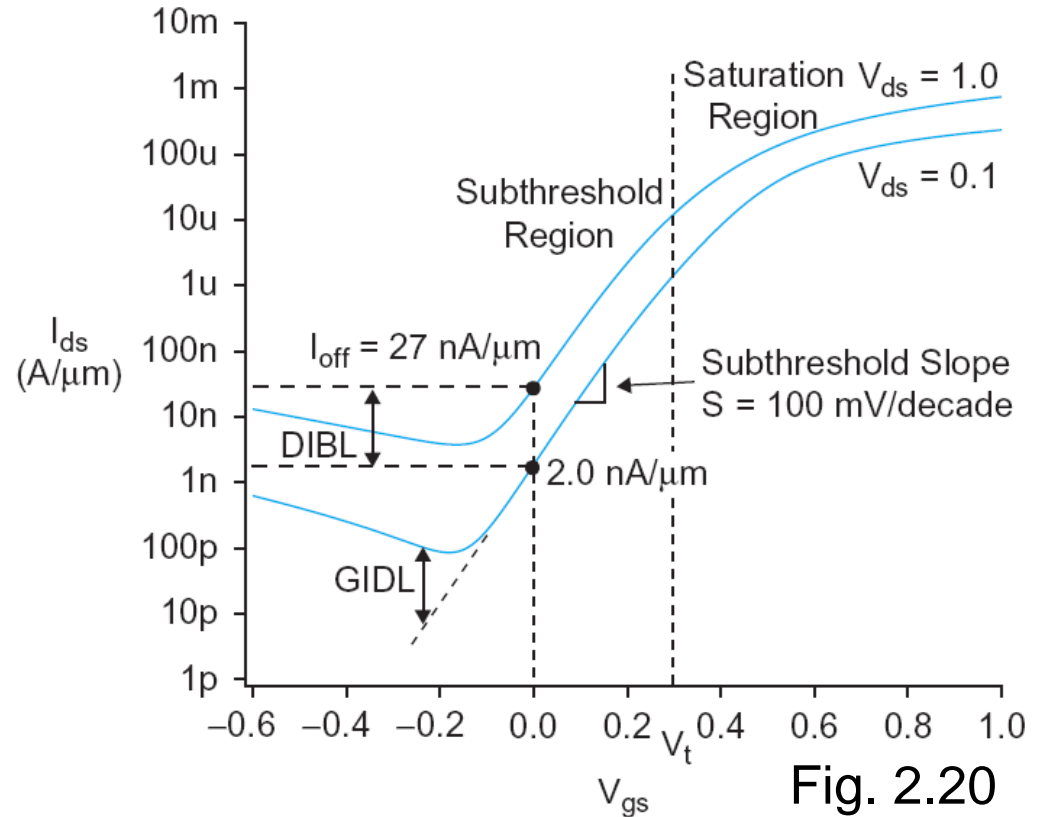


Fig. 2.20