HW 2

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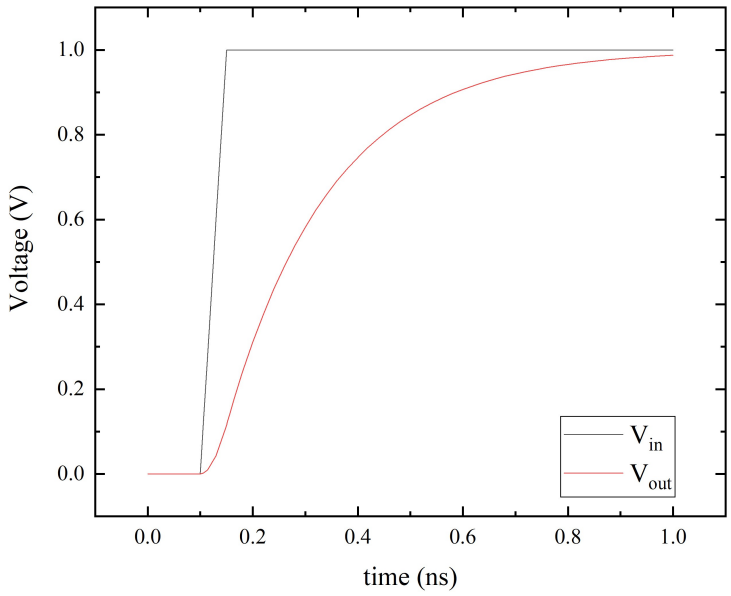
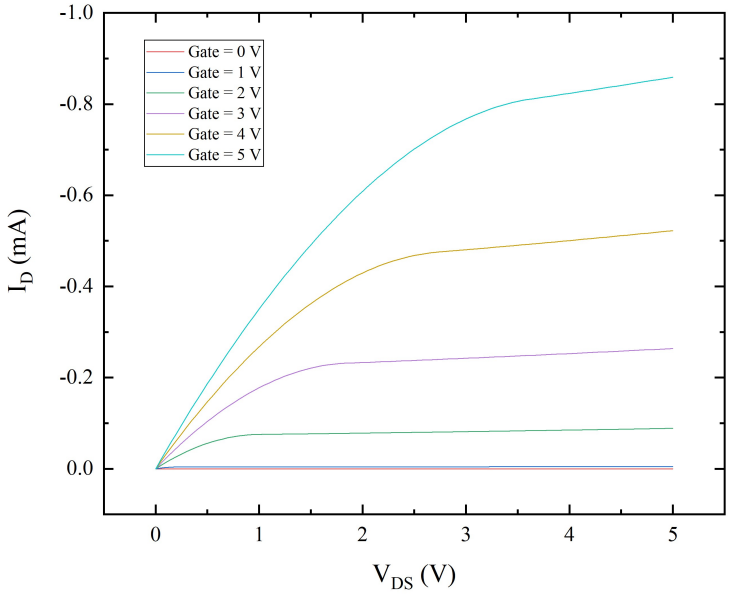
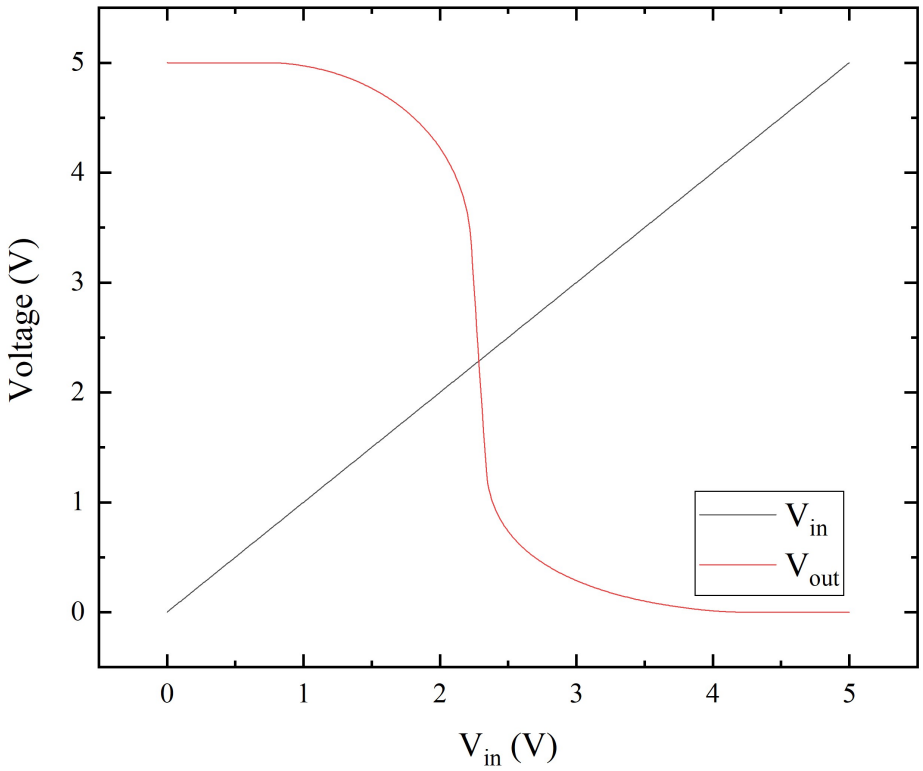


[Example 1] I observed some delay from capacitor in RC circuit simulation. Although input voltage V_{in} increases linearly during 0.1 ns to 0.15 ns, exponential response of output voltage V_{out} was observed.



[Example 2] Saturation of drain current at sufficiently high drain-source voltage V_{DS} was observed for each gate voltage. According to simulation results, higher gate voltage implies higher drain current.



[Example 3] Input voltage V_{in} was inverted to output voltage V_{out}, so that slope of the output voltage had different sign to the input. Also, output voltage had some transition characteristic around 2.5 V of input voltage.