Digital Integrated Circuit Assignment

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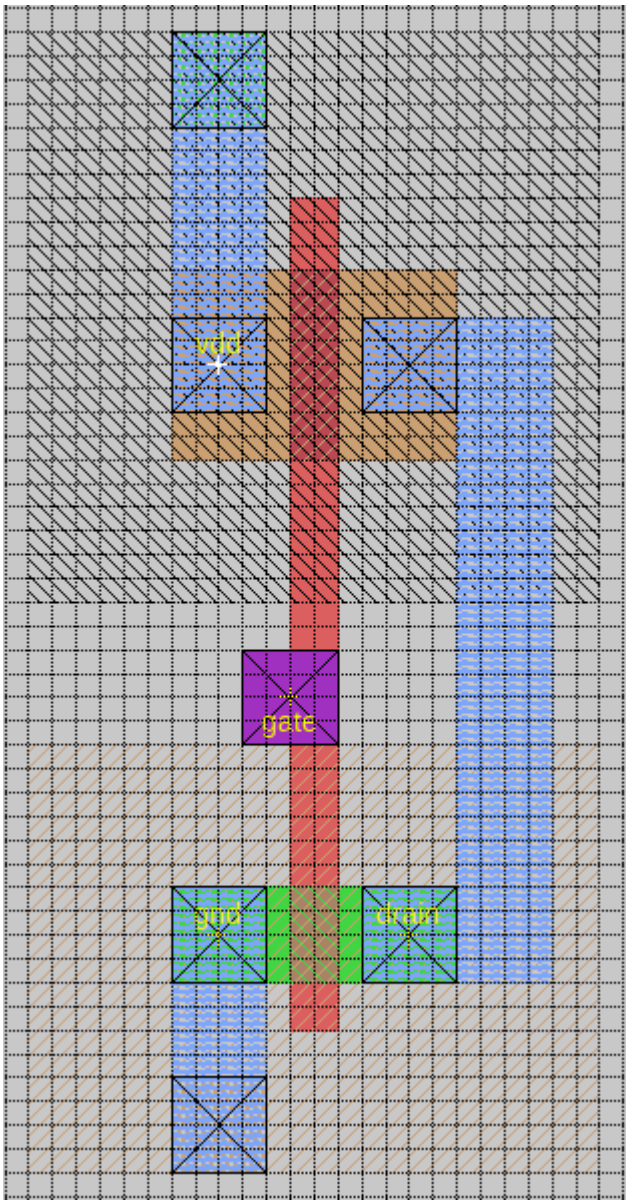
- Inverter layout



- Inverter extraction result

```
timestamp 1569500013
version 8.0
tech scmos
style lambda=1.0(scna20_orb)
scale 1000 1 100
resistclasses 26670 59550 23860 19690 27260 2000000 49 26 2505830
node "drain" 129 1128 -2 17 ndiff 20 18 40 26 0 0 0 0 0 0 0 0 144 80 0 0 0 0
node "gate" 416 1900 -6 27 pc 0 0 0 0 78 78 0 0 0 0 0 0 16 16 0 0 0 0
node "gnd" 93 0 -15 9 pw 20 18 16 16 0 0 0 0 0 0 0 0 48 32 0 0 0 0
node "vdd" 2628 0 -15 33 nw 16 16 40 26 0 0 0 0 0 0 0 0 64 40 0 0 576 96
cap "gate" "gnd" 2544
cap "gate" "vdd" 2622
cap "drain" "gnd" 1880
cap "vdd" "drain" 2256
device mosfet nfet -4 17 -3 18 2 4 "gnd" "gate" 4 0 "gnd" 4 0 "drain" 4 0
device mosfet pfet -4 39 -3 40 2 8 "vdd" "gate" 4 0 "vdd" 8 0 "drain" 8 0
```