Digital Integrated Circuit HW#2

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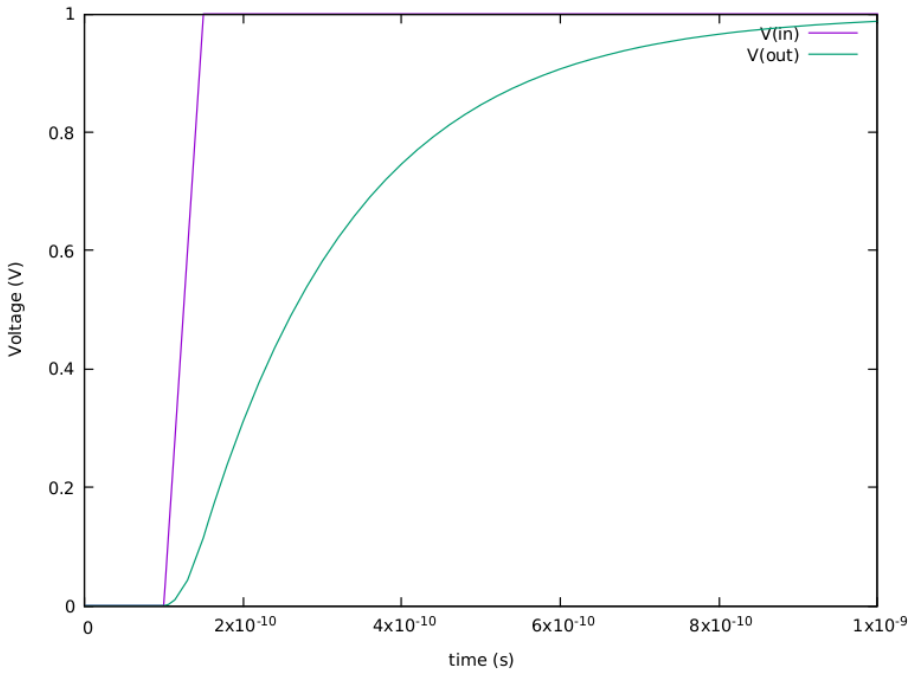
| Example1 |

This is the RC circuit response graph. The input voltage is zero until 0.1ns and it raises linearly until 0.15ns. After 0.15ns, input voltage is 1V. The output voltage is also zero until 0.1ns. After 0.1ns, output voltage increases exponentially from zero to 1V.

[Source Code]

```
*rc.sp for SPICE3F5

Vin in 0 pwl 0ps 0 100ps 0 150ps 1.0 1ns 1.0
R1 in out 2k
C1 out 0 100f

.tran 20ps 1ns
.plot tran v(in) v(out)
.end
```

[Graph]



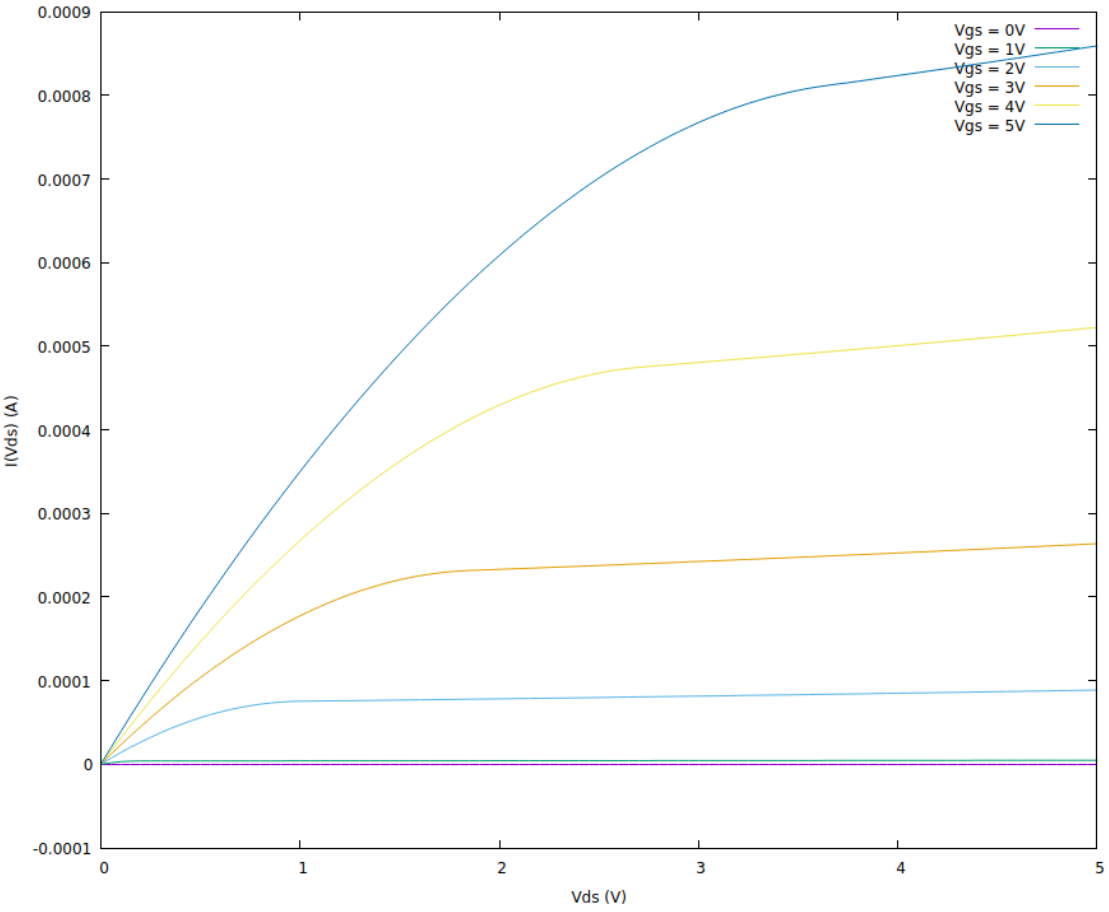
| Example2 |

From that graph, we can find that the magnitude of drain current is proportional to gate voltage at the same drain voltage. Also, high drain voltage is needed to reach the saturation region in a MOS.

[Source Code]

```
* mosiv.sp for SPICE3F5

* models_1p2mu.sp

* Taken from
* http://bwrcs.eecs.berkeley.edu/Classes/IcBook/FILES/models.html

* SPICE LEVEL 2 Model for 1.2 mu Process

.MODEL NMOS NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=5.36726E+15 VTO=0.743469 KP=8.00059E-05 GAMMA=0.543
+ PHI=0.6 U0=655.881 UEXP=0.157282 UCRIT=31443.8
+ DELTA=2.39824 VMAX=55260.9 XJ=0.25U LAMBDA=0.0367072
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
* Weff = WDrawn - Delta_W
* The suggested Delta_W is 1.9970E-07

.MODEL PMOS PMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=4.3318E+15 VTO=-0.738861 KP=2.70E-05 GAMMA=0.58
+ PHI=0.6 U0=261.977 UEXP=0.323932 UCRIT=65719.8
+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
* Weff = WDrawn - Delta_W
* The suggested Delta_W is 3.1280E-07

Vgs g 0 0
Vds d 0 0
M1 d g 0 0 NMOS W=2.4 L=1.2

.dc Vds 0 5.0 0.05 Vgs 0 5.0 1.0
.print dc V(g) I(Vds)
.end
```

[Graph]


0.0009
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
-0.0001
I(Vds) (A)
0
1
2
3
4
5
Vds (V)
Vgs = 0V
Vgs = 1V
Vgs = 2V
Vgs = 3V
Vgs = 4V
Vgs = 5V

| Example3 |

From this graph, we can find that output voltage is inverted from the input voltage. Namely, input voltage graph has a positive slope and increase linearly, but the output voltage graph has a negative slope and it decreases rapidly at around 2.5s.

[Source Code]

```
*inv.sp for SPICE3F5

* models_1p2mu.sp

* Taken from
* http://bwrcs.eecs.berkeley.edu/Classes/IcBook/FILES/models.html

* SPICE LEVEL 2 Model for 1.2 mu Process

.MODEL NMOS NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
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+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
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+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
* Weff = WDrawn - Delta_W
* The suggested Delta_W is 3.1280E-07

Vdd vdd 0 5.0
Vin a 0 0.0
M1 y a 0 0 NMOS W=2.4 L=1.2
M2 y a vdd vdd PMOS W=4.8 L=1.2

.dc Vin 0 5 0.01
.print dc V(a) V(y)
.end
```

[Graph]