DIC L9: MOSFET (3)

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2.4. Nonideal IV (1)

- Review of ideal IV characteristics
  - After some manipulation, we have

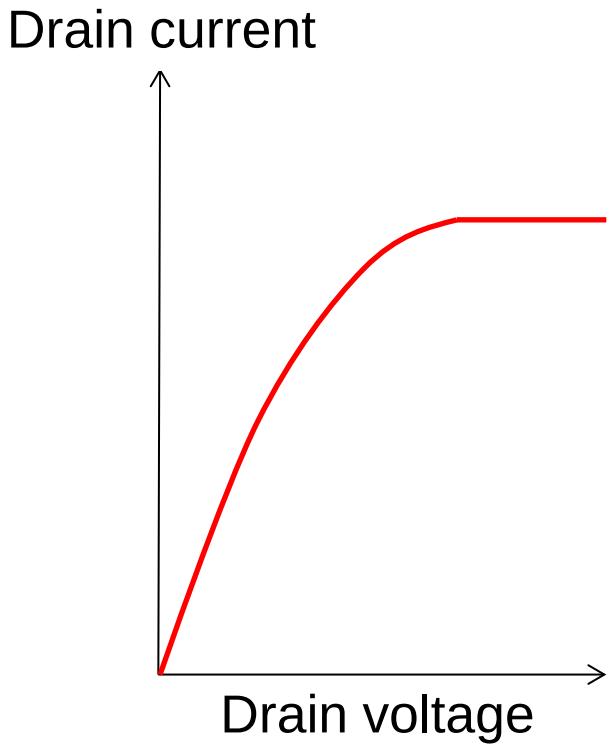
Subthreshold $$I_d = 0$$

Linear $$I_d = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

Saturation $$I_d = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

  - Here,

$$\beta = \mu_n C_{OX}\frac{W}{L}$$



2.4. Nonideal IV (2)

- 65nm IBM

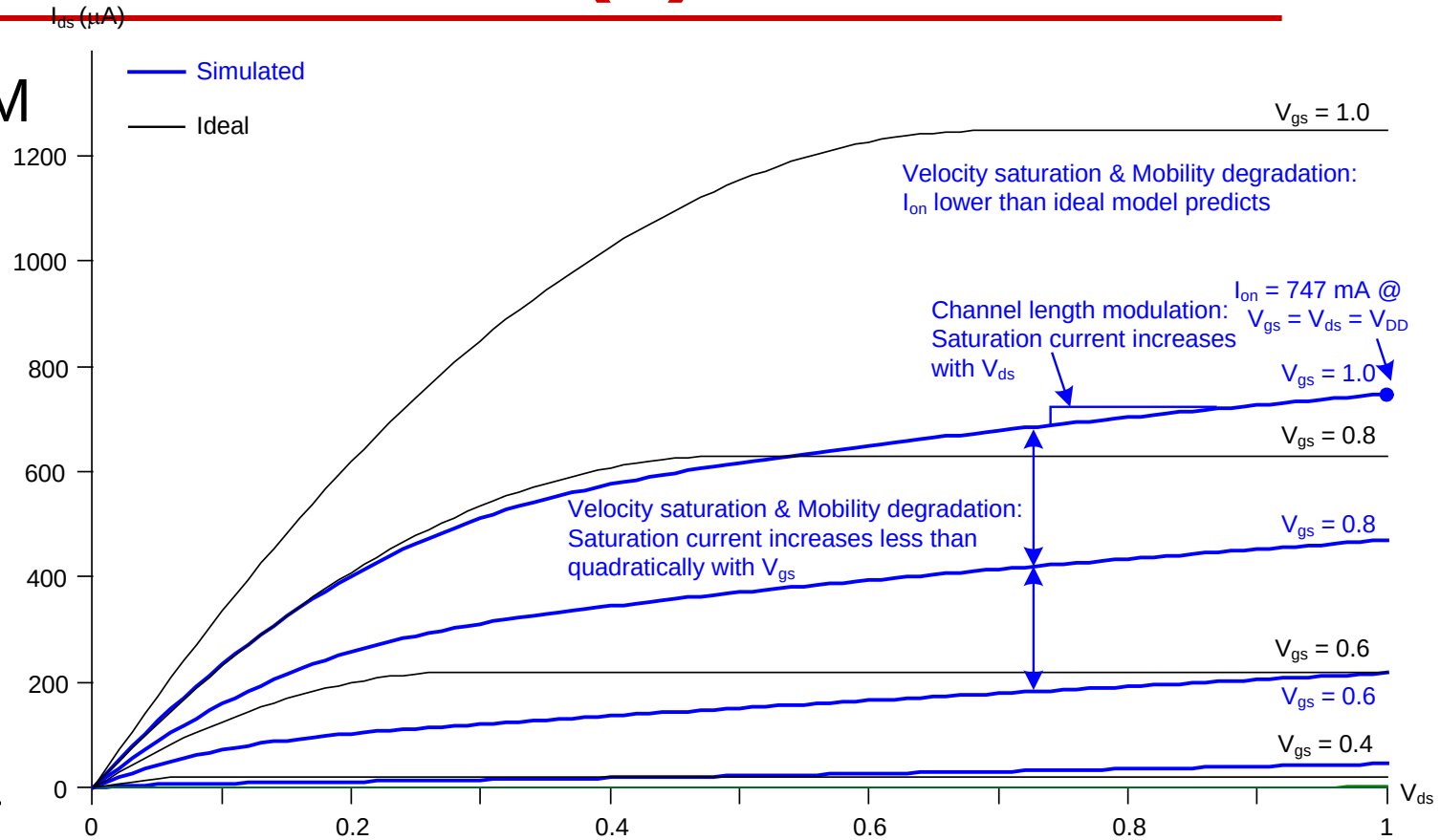
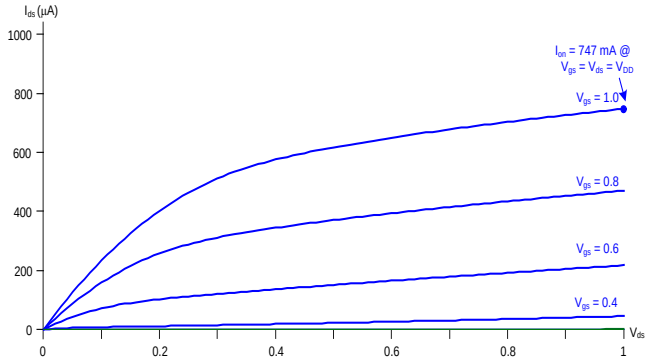
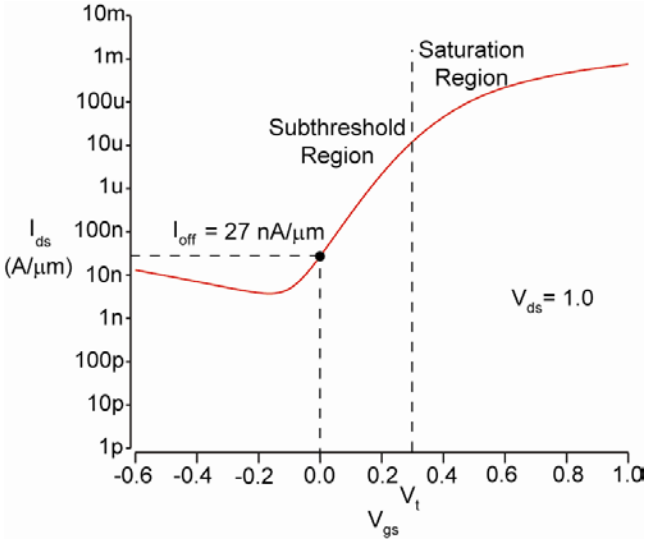


Fig. 2.14

2.4. Nonideal IV (3)

- ON and OFF currents (Drain currents)
  - ON current: $V_{gs} = V_{ds} = V_{DD}$
  - OFF current: $V_{gs} = 0, V_{ds} = V_{DD}$ (In the ideal model, it vanishes.)

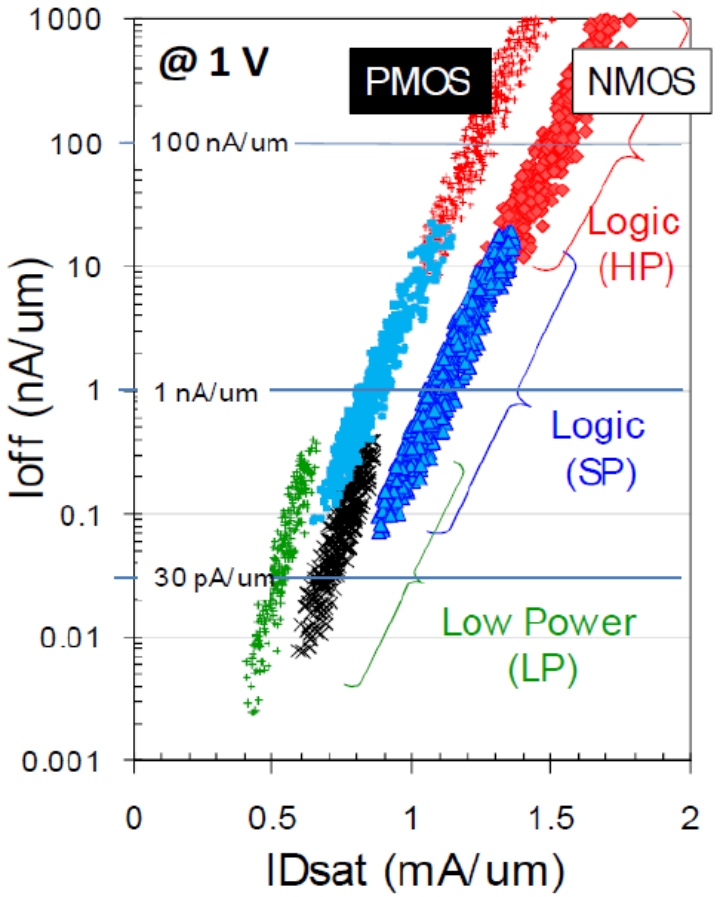




2.4. Nonideal IV (4)

- Intel 32 nm transistor
  - Different leakage options
  - Ioff in log scale
  - Ion in linear scale
  - HP (High performance)
  - SP (Standard performance/power)
  - LP (Low power)

(M. Bohr's 2011 IEDM abstract)



2.4. Nonideal IV (5)

- Intel 22 nm transistor

Table I. 22nm modular SoC transistor options and device characteristics

Transistor Type	High Speed Logic		Low Power Logic		High Voltage	
Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)	0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)	90	90	90	108	min. 180	min. 450
Lgate (nm)	30	34	34	40	min. 80	min. 280
N/PMOS Idsat/Ioff (mA/um)	1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V 30 pA/um	0.35 / 0.33 @ 0.75 V 15 pA/um	0.92 / 0.8 @ 1.8 V 10 pA/um	1.0 / 0.85 @ 3.3 V 10 pA/um

(Intel's 2012 IEDM abstract)