# Juhyung Lee 20194072

**Selected Technology:** K. Rim, S. Koester, M. Hargrove, J. Chu, P. M. Mooney, J. Ott, T. Kanarsky, P. Ronsheim, M. Ieong, A. Grill, H.-S. P. Wong, "Strained Si NMOSFETs for High Performance CMOS Technology", *Symp. On VLSI Tech.*, 59-60 (2001). [https://ieeexplore.ieee.org/document/934946]

# **Brief description**

In this paper, strained Si (SS) layer on Si<sub>0.8</sub>Ge<sub>0.2</sub> was fabricated epitaxially by UHVCVD. In order to fabricate SS NMOSFET, they used standard CMOS process with STI isolation, and NMOSFET using unstrained Si was fabricated under same condition for comparison.

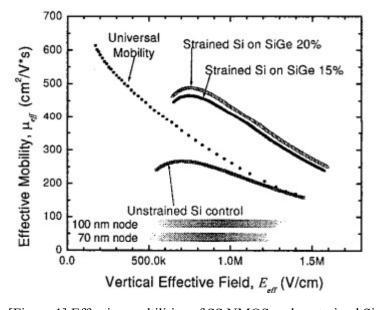
## **Common properties**

■ Channel width: 0.28 μm

Effective channel length: 67 nmGate oxide thickness: 3.15 nm

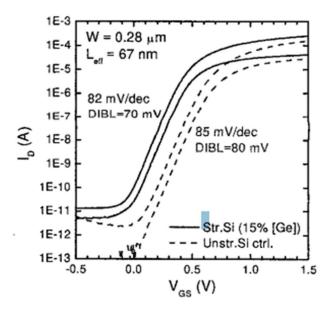
#### **Electrical characteristics**

■ Electric mobility



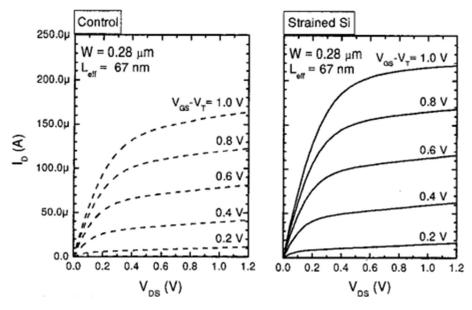
[Figure 1] Effective mobilities of SS NMOS and unstrained Si NMOS were investigated. Both NMOS have mobility degradation due to the vertical field. Nevertheless, SS NMOS achieved higher mobility than unstrained Si NMOS. Since high mobility induces that drain current increases more steeply about drain-source voltage, SS NMOS has better electrical characteristic than unstrained NMOS.

## ■ Drain current vs Gate voltage



[Figure 2] Drain current behavior according to gate-source voltages of the two NMOS were measured. First, subthreshold slope of SS NMOS is lower than the other one. This results remarks that SS NMOS needs smaller gate voltage to increase drain voltage. Thus, subthreshold slope of SS NMOS is better than the unstrained one. Moreover, DIBL of SS NMOS is also lower than the other one. Then, short channel effect of SS NMOS should be smaller than the other one.

# ■ Drain current vs Drain voltage



[Figure 3] Left graph indicates I-V characteristic of the unstrained Si NMOS, and right graph shows same characteristic of the SS NMOS. The results notes that SS NMOS has better electrical characteristic due to its steep increase of drain current about drain voltage with the condition of same gate overdrive voltage.