DIC L4: Layout (1)

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

1.5. CMOS layout (2)

Detailed mask views

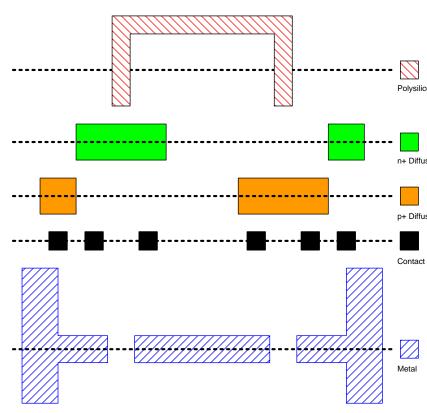


Fig. 1.35(b)-(g)

GIST Lecture on September 24, 2019

1.5. CMOS layout (3)

Design rules in the textbook

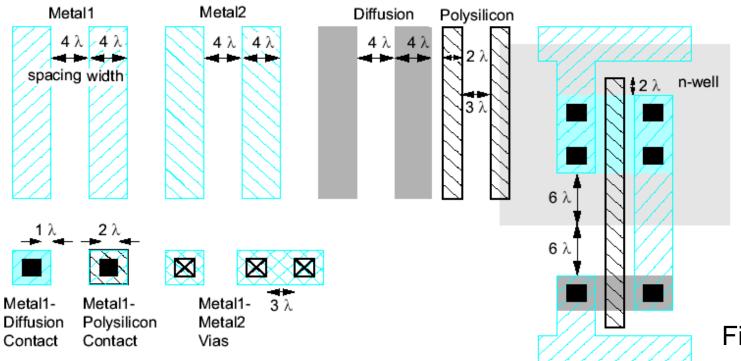
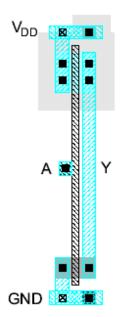


Fig. 1.39

1.5. **CMOS** layout (4)

Inverter layout



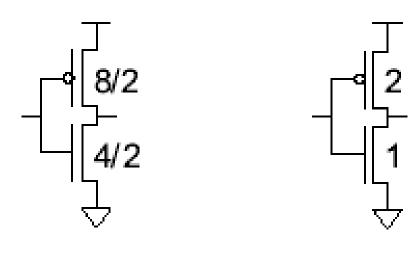


Fig. 1.40

GIST Lecture on September 24, 2019

1.5. **CMOS** layout (5)

Inverter layout

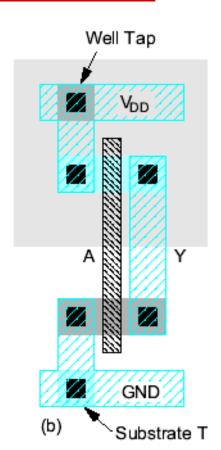


Fig. 1.41(b)

1.5. **CMOS** layout (6)

- 3-input NAND
 - Serially connected NMOS transistors
 - Paralley connected PMOS transistors

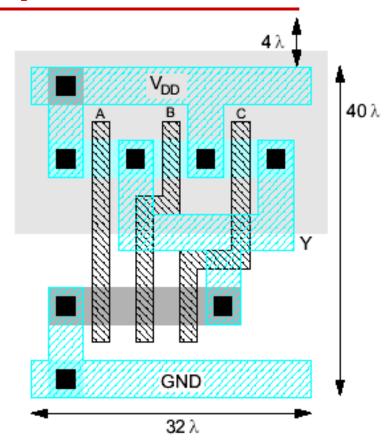


Fig. 1.42

1.5. **CMOS** layout (6)

- 3-input NAND
 - Serially connected NMOS transistors
 - PMOS transistors are in parallel.

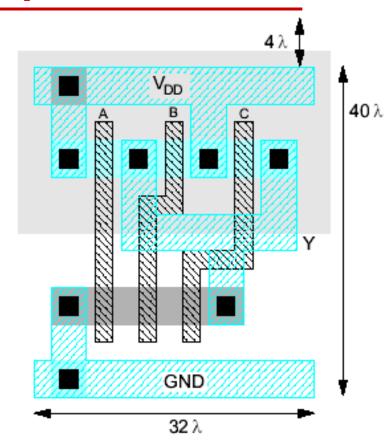


Fig. 1.42

1.5. **CMOS** layout (6)

- Let us install the "Magic" VLSI layout tool.
 - Prerequisite: Linux O/S
 - Visit

http://opencircuitdesign.com/magic

Download the source file.

tar -xvzf [filename]

- Then, install the magic program.
 - You may install some packages.
 - Use tcsh.

1.5. **CMOS** layout (7)

- In this course, the 180 nm technology is used.
 - Copy the "sample6m.tech" file.

