

LAB5 - Alien Calculator

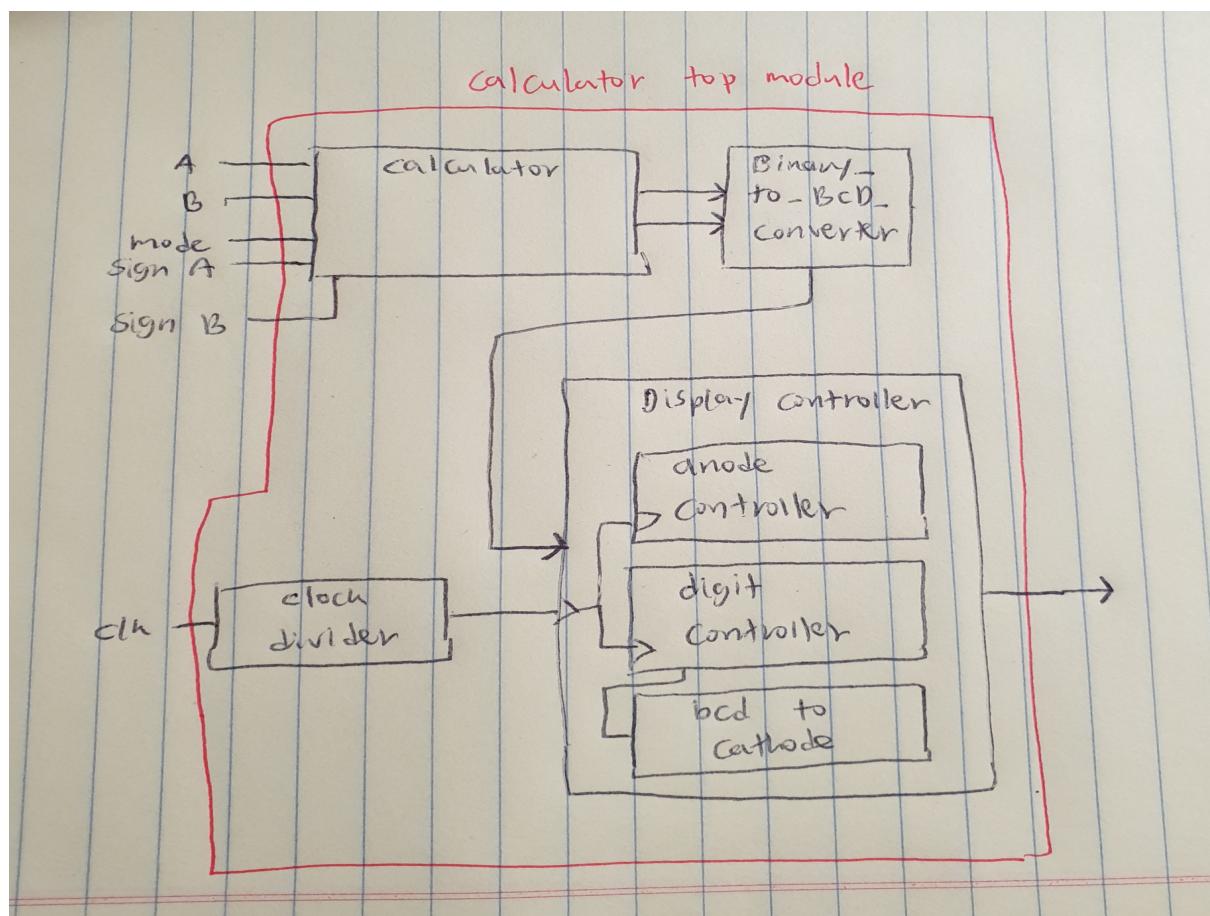
Group Jihun :

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This lab5 is about designing an Alien calculator that handles addition, subtraction, and multiplication of two 4bit numbers that each has an extra 1 bit for its own sign by instantiation using vivado software and test the results with FPGA board.



1) clock_divider module was created to divide clock for seven segment display

(input clk, output reg [2:0] divided_clk)

2) display_controller module was created to have 4 different functions

- generate refresh clock
- anode controller (seven seg display controller)
- digit controller (which digit to show)
- bcd to cathode (translating bcd number to corresponding cathode variables)

(input [2:0] clock, [3:0] portA, portB, input signA, signB, [1:0] mode, [3:0] result_ones, [3:0] result_tens, input result_sign, output reg [6:0] cathode, output reg [7:0] anode)

3) binary_to_bcd_converter module was created to convert binary number to bcd

format using idea of shift

(input [7:0] number, output [3:0] ones, output [3:0] tens)

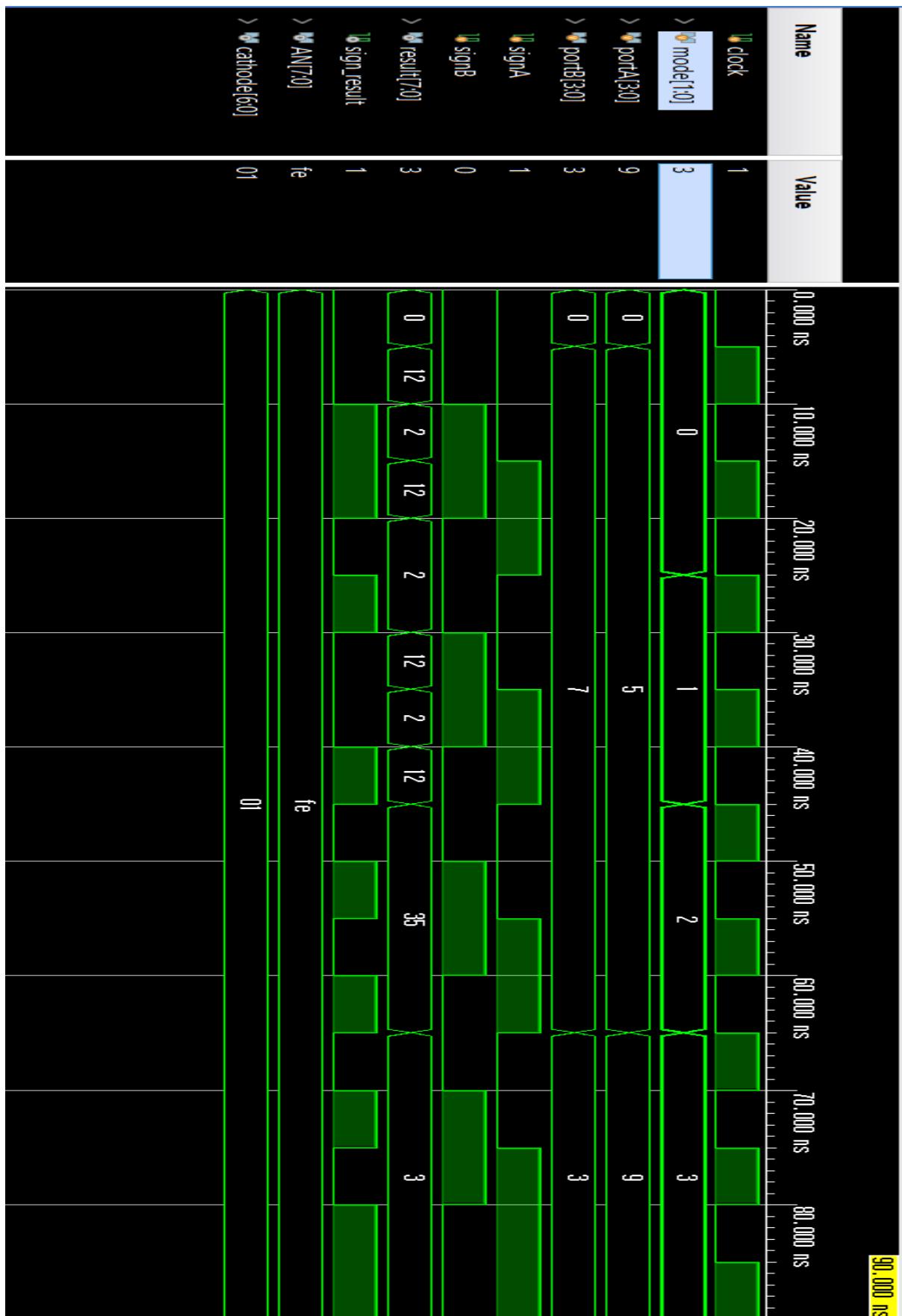
4) calculator module was created to have the functions of addition, subtraction, multiplication, and division (extra feature).

(input [3:0] A, B, input sign_A, sign_B, input [1:0] mode, output reg [7:0] result, output reg result_sign)

5) calculator_top module was created to connect all other modules together.

6) calculator_top.xdc file was created and connected to the correct ports.

7) simulation was performed,



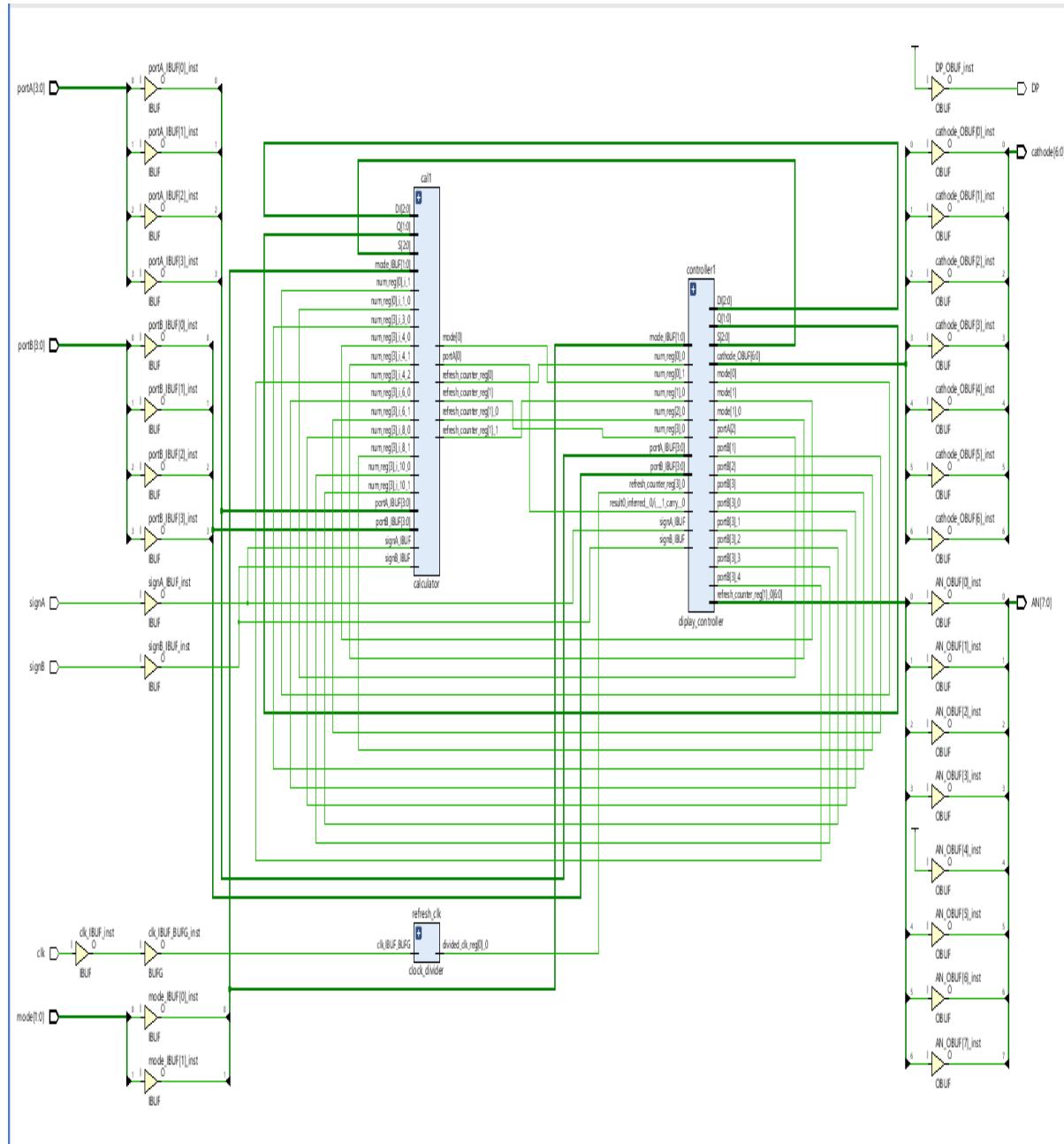
Video link:

<https://youtu.be/Vq9J-m0bdp0>

or

<https://drive.google.com/file/d/1wM39O4ceyxF0Vwz4pXxonlgVM08qMVhj/view?usp=sharing>

Elaborated Design:



Utilization:

Power report:

Summary

Settings

Summary (0.126 W, Margin: N/A)

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Power Supply

Utilization Details

- Hierarchical (0.029 W)
- Clocks (0.001 W)
- Signals (0.001 W)
 - Data (0.001 W)
 - Set/Reset (<0.001 W)
- Logic (0.001 W)
- I/O (0.027 W)

Total On-Chip Power: 0.126 W **Design Power Budget:** Not Specified **Power Budget Margin:** N/A **Junction Temperature:** 25.6°C

Thermal Margin: 59.4°C (12.9 W) Effective θJA: 4.6°C/W

Power supplied to off-chip devices: 0 W Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power

Category	Power (W)	Margin (%)
Dynamic:	0.029 W	(23%)
Clocks:	0.001 W	(2%)
Signals:	0.001 W	(3%)
Logic:	0.001 W	(3%)
I/O:	0.027 W	(92%)
Device Static:	0.097 W	(77%)