LAB1 - 2 to 1 Mux

Group A :

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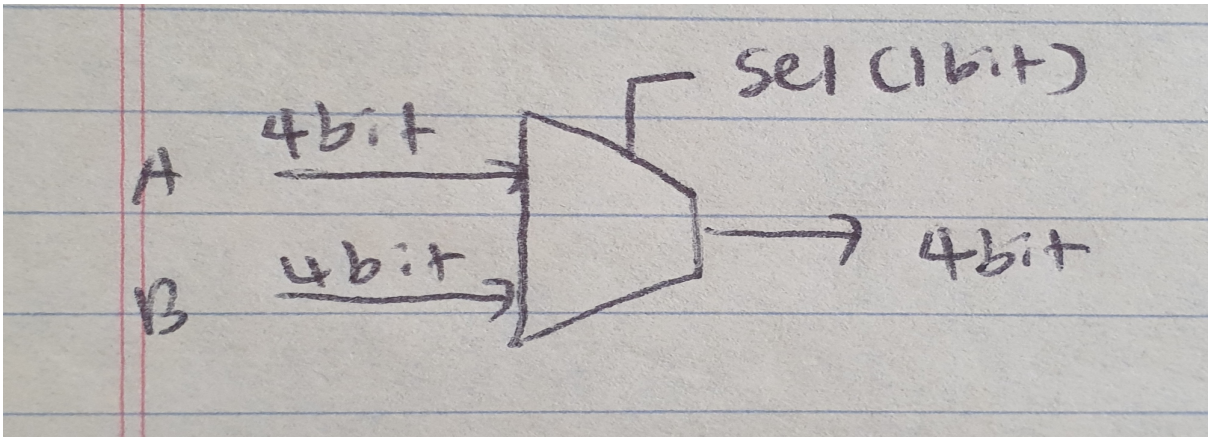
This lab1 is about designing a 2 to1 multiplexer by using vivado software and test the results with FPGA. 2 input ‘a’ and ‘b’ will each be 4 bits, ‘sel’ which is select line will be just 1 bit. Output ‘f’ will be also 4 bits. The function of 2 to 1 multiplexer is pretty simple. If selected line ‘sel’ equals 0, output ‘f’ will be same as input ‘a’. Else, if the selected line ‘sel’ equals 0, output ‘f’ will be the same as input ‘b’.



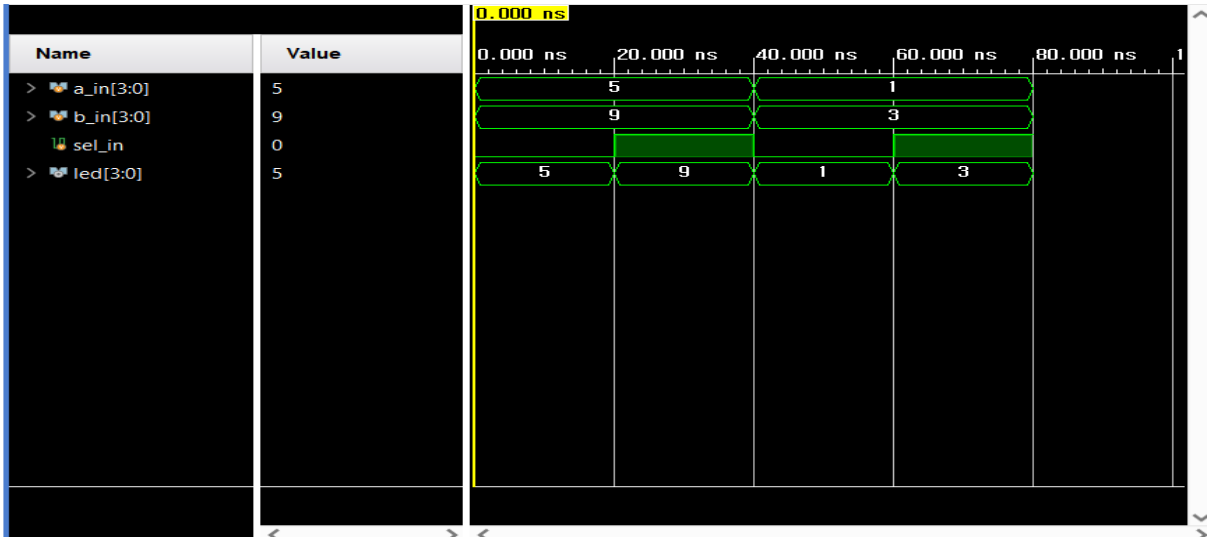
To make input ‘a’ and ‘b’ 4bits, ‘[3:0]’ was used. Same for output ‘f’, [3:0] was used. Once ports are set correctly, always block was used to implement if else statement.

```
module mux2to1(
                        input wire [3:0] a,
                        input wire [3:0] b,
                        input wire sel,
                        output reg  [3:0] f

                    );

        always @(a,b,sel)
        begin
                    if(sel==0)
                    f=a;
                    else
                    f=b;
        end

endmodule
```

After setting up the source file, test bench was created to test, if 2 to1 multiplexer designed functions as it intended.

```
module mux2to1_tb(

                );

                reg [3:0] a_in;
                reg [3:0] b_in;
                reg sel_in;

                wire [3:0] led;

                mux2to1 M (
                        .a(a_in),
                        .b(b_in),
                        .sel(sel_in),
                        .f(led)
                            );
```

```
initial
    begin
                a_in =4'b0101;
                b_in =4'b1001;
                sel_in = 0;
                #20

                a_in =4'b0101;
                b_in =4'b1001;
                sel_in = 1;
                #20

                a_in =4'b0001;
                b_in =4'b0011;
                sel_in = 0;
                #20

                a_in =4'b0001;
                b_in =4'b0011;
                sel_in = 1;
                #20

                $finish;

        end

endmodule
```



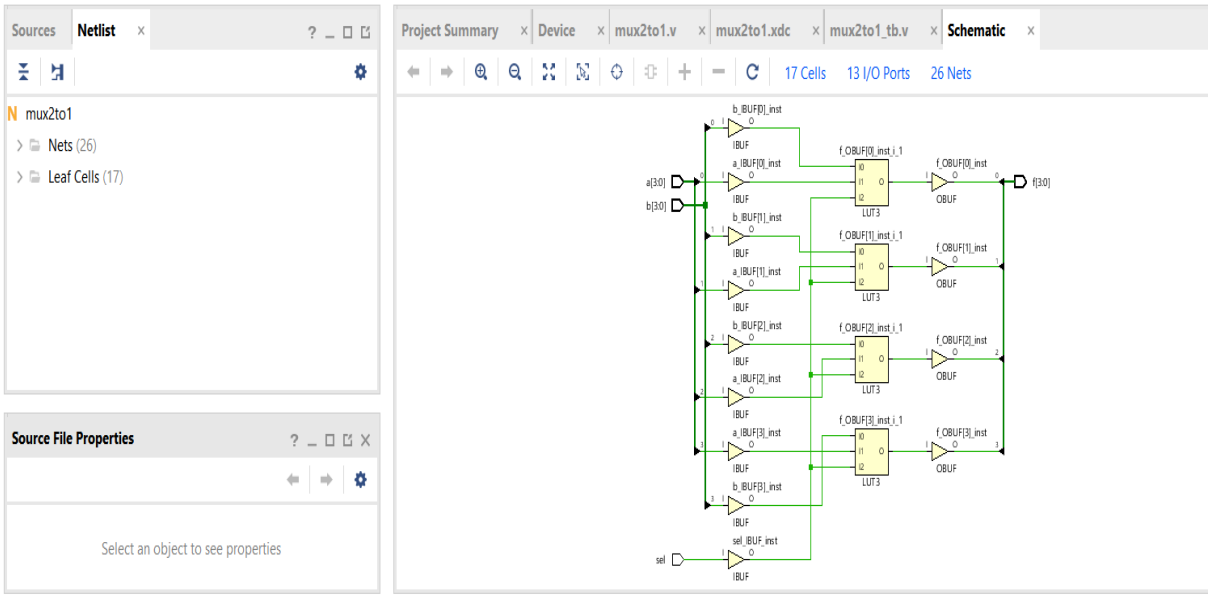
After checking simulation results, 2 to 1 multiplexer is functioning correctly. xdc file was modified to properly work and the result was tested on FPGA.

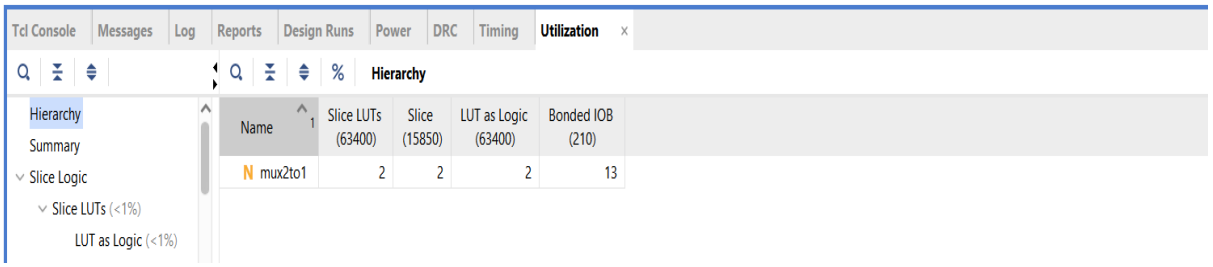
Video link:

https://drive.google.com/file/d/1x5HYhGIeaSPITdKOiEAVvxS3RKGg-sDl/view?usp=sharing

or

https://youtube.com/shorts/45CRVI5ur-A?feature=share


Sources
Netlist
mux2to1
Nets (26)
Leaf Cells (17)
Source File Properties
Select an object to see properties
Project Summary
Device
mux2to1.v
mux2to1.xdc
mux2to1_tb.v
Schematic
17 Cells
13 I/O Ports
26 Nets
a[3:0]
b[3:0]
sel
f[3:0]
IBUF
OBUF
LUT3


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Timing
Utilization
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Name
Slice LUTs (63400)
Slice (15850)
LUT as Logic (63400)
Bonded IOB (210)
mux2to1
2
2
2
13