DIGITAL CIRCUITS

Week-2, Lecture-2
Introduction

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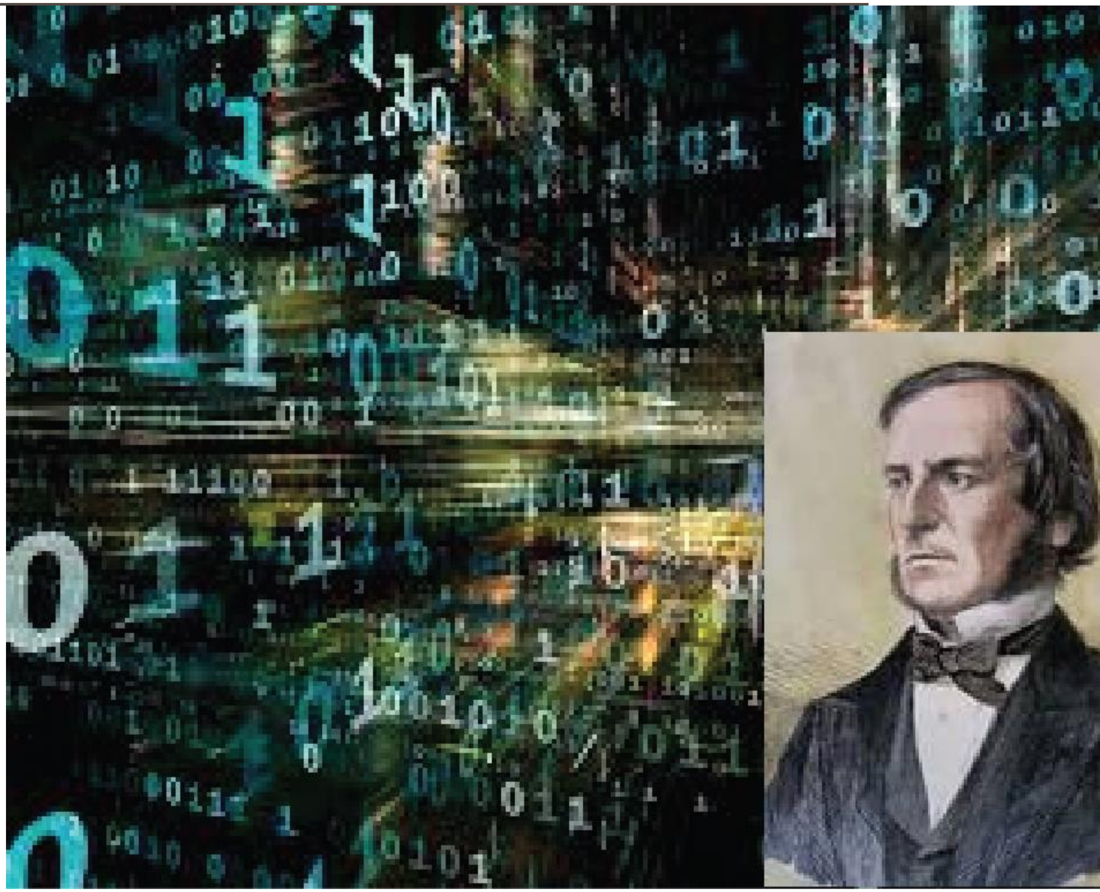
8th August, 2018



Digital Circuits: Announcements/Revision

Digital Circuits

Logic Functions and Logic Gates

Logic Expression: Precedence of Operators

- () : Bracket
- NOT
- AND
- OR

- What will be the order of computation for the following expression:

$$\boldsymbol{f}(x_1, x_2, x_3) = \overline{\boldsymbol{x_1}}.(\boldsymbol{x_2} + \boldsymbol{x_3}.\boldsymbol{x_1})$$

- Computation 1: Bracket
  - $\boldsymbol{x_3}.\boldsymbol{x_1}$ AND
  - $\boldsymbol{x_2}+\boldsymbol{x_3}.\boldsymbol{x_1}$ OR
- Computation 2: $\overline{\boldsymbol{x_1}}$ NOT
- Computation 3: $\overline{\boldsymbol{x_1}}.(\boldsymbol{x_2} + \boldsymbol{x_3}.\boldsymbol{x_1})$ AND

Logic function: Complement of a function

- Complement can be defined for complex function also
- $f(x_1, x_2) = (x_1 + x_2)$
- $\bar{f}(x_1, x_2) = \overline{(x_1 + x_2)}$

- NOT of OR is known as NOR operation
- Similarly NOT of AND operation is known as NAND operation

- Find the truth table for this function

$\boldsymbol{x_1}$	$\boldsymbol{x_2}$	$\boldsymbol{f}(x_1, x_2) = \boldsymbol{x_1} + \boldsymbol{x_2}$	$\bar{f}(x_1, x_2) = \overline{(x_1 + x_2)}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

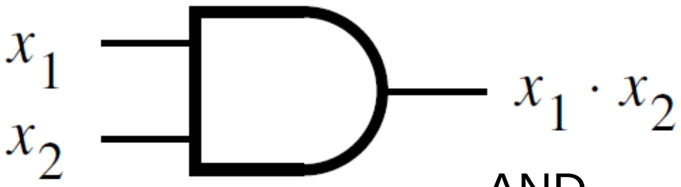
Logic gates: AND, OR, NOT (Basic Gates)

What is a *Logic Gate*?

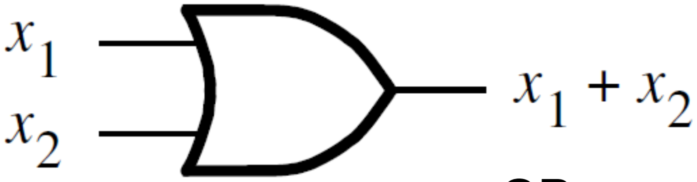
- Hardware implementation of logic operation such as NOT, AND, OR, NAND, NOR etc. in terms of transistors etc. is known as ***Logic Gate***

- A logic gate has one or more inputs and only one output
- Output depends on the value of inputs
- Convenient to represent in terms of schematic

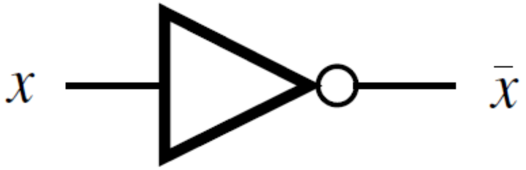
- A bubble at the input or the output denotes taking complement



AND

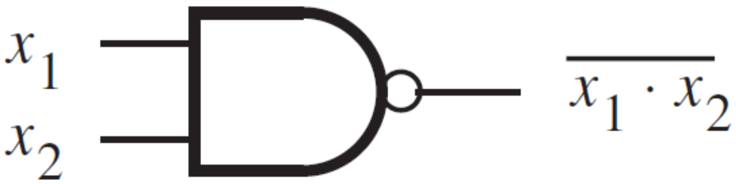


OR

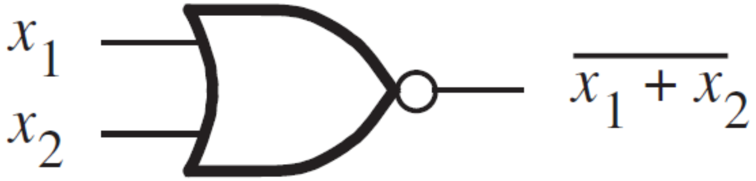


NOT

Logic gates: NAND, NOR



NAND

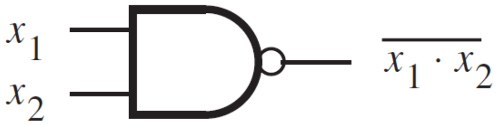


NOR

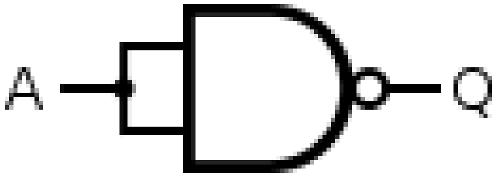
- NAND/NOR gates are widely used because it is easy to realize/fabricate them using transistors

- AND/OR/NOT gates can be realized using only NAND gates
- AND/OR/NOT gates can also be realized using only NOR gates
- NAND/NOR gates are called ***universal gates***

NAND, NOR: Universal gates

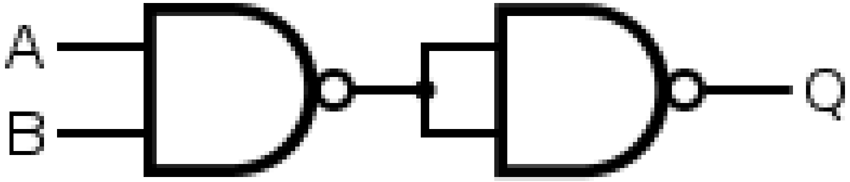


NAND

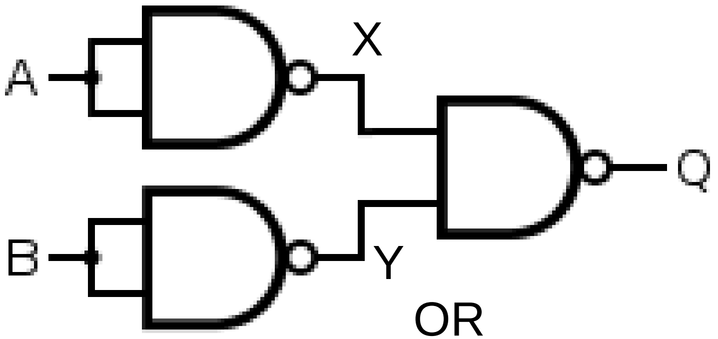


NOT

A	*Q*
0	1
1	0



AND

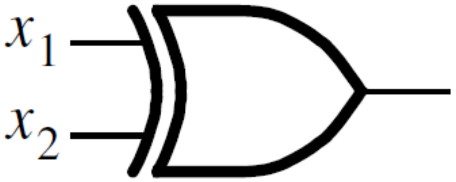


OR

A	*B*	*X*	*Y*	*Q*
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Similarly, it can be shown that NOT, OR, AND operation can be realized using NOR gates alone

Logic gates: XOR, XNOR



$f = x_1 \oplus x_2$

XOR

x_1	x_2	$XOR(x_1, x_2) = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

$f = \overline{x_1 \oplus x_2}$

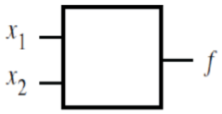
XNOR

x_1	x_2	$XNOR(x_1, x_2) = \overline{(x_1 \oplus x_2)}$
0	0	1
0	1	0
1	0	0
1	1	1

Positive and Negative Logic

- Logic Gates are designed in terms of voltage levels
    - ➢ Two levels are defined: H (High) and L (Low)
- The ***interpretation*** of these voltages in terms of "0" and "1" can be in two ways

x_1	x_2	$f(x_1, x_2)$
L	L	L
L	H	L
H	L	L
H	H	H



Positive Logic:

- H (High) is "1" and L (Low) is "0"

x_1	x_2	$f(x_1, x_2)$
0	0	0
0	1	0
1	0	0
1	1	1

Negative Logic:

- H (High) is "0" and L (Low) is "1"

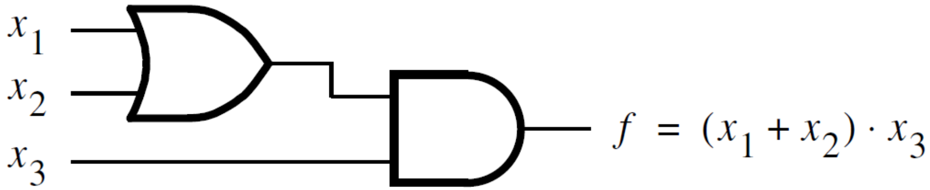
x_1	x_2	$f(x_1, x_2)$
1	1	1
1	0	1
0	1	1
0	0	0

Triangles indicate negative logic

Negative Logic system is rarely used, and we will assume positive logic system in this course

Logic Network or Logic Circuit

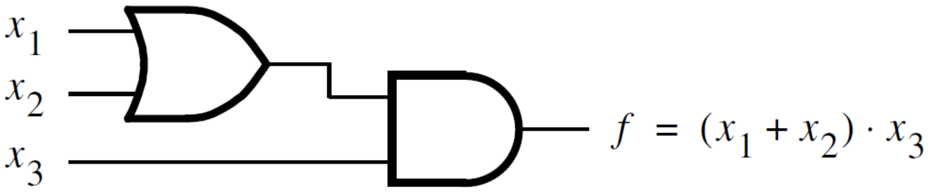
- NOT, AND, OR gates can be used to implement any logic function
- A complex logic function is implemented by interconnecting logic gates



- ***Logic Network*** or ***Logic Circuit*** is an interconnection of logic gates

- Same Logic Function can be implemented by different Logic Networks
- A designer task is to find a Logic Network with less complexity (less number of gates)

Tasks for a Logic Circuit Designer



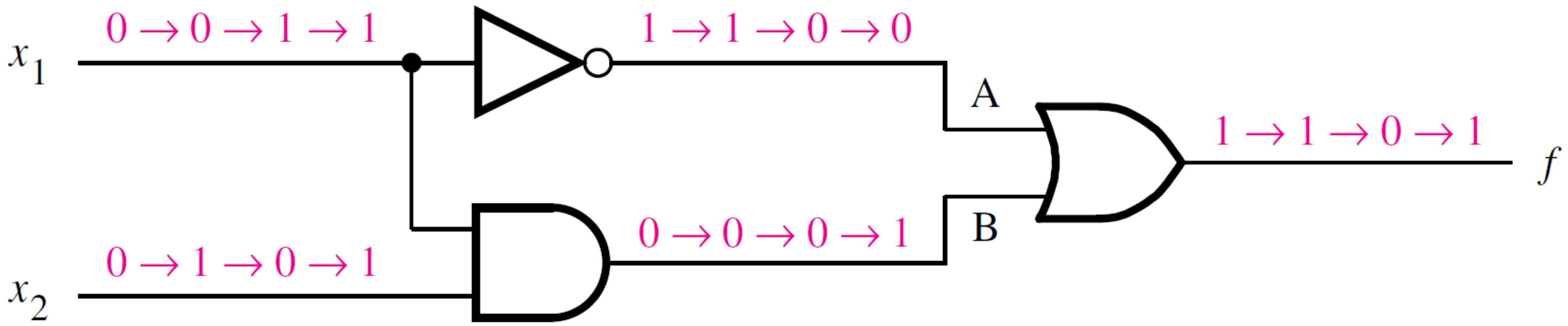
Synthesis:

- Given a logic function, find a ***logic network*** that implements it
- There are many solutions, choose the best

Analysis:

- Given a logic network, determine the ***logic function*** that is implemented

Logic Network Analysis: Function $f(x_1, x_2)$



Analysis: Find the function that is represented by the above Logic Network

Approach:

a) Write the Logic Function

b) Write the Truth Table

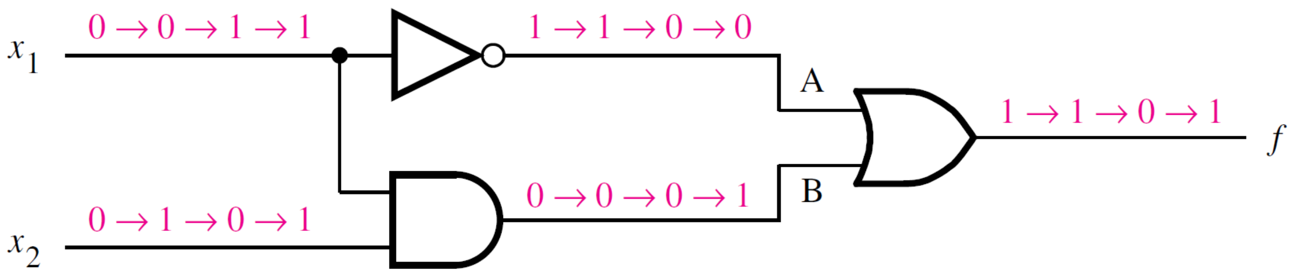
Logic Function:

$A = \overline{x_1} \qquad B = x_1 . x_2$

$f(x_1, x_2) = \overline{x_1} + x_1 . x_2$

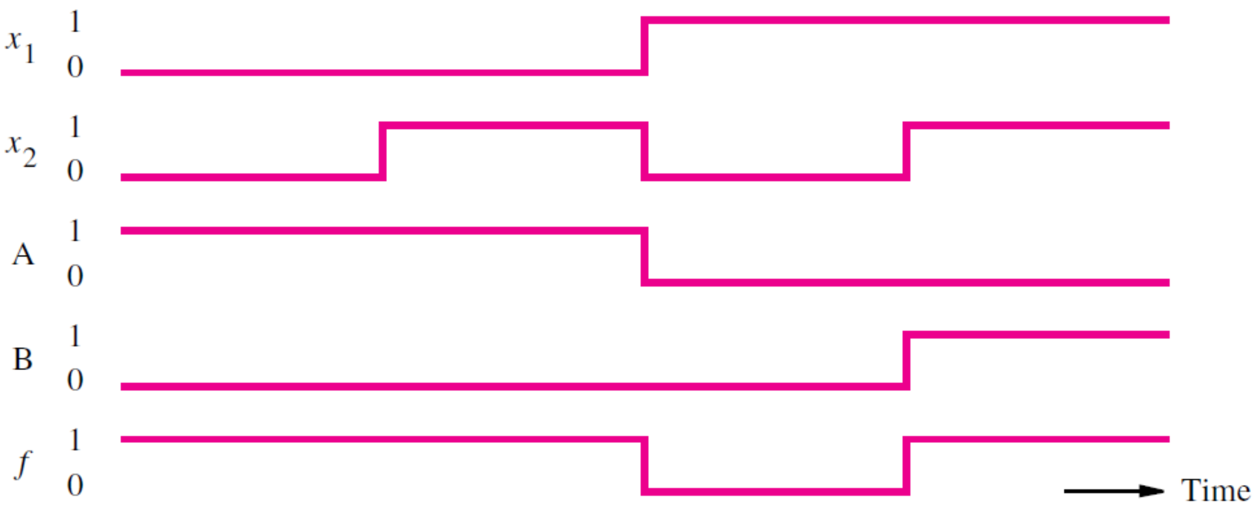
x_1	x_2	A	B	$f(x_1, x_2)$
0	0	1	0	1
0	1	1	0	1
1	0	0	0	0
1	1	0	1	1

Logic Network Analysis: Timing Diagram



Timing Diagram: Changes in signals at different point of time represented graphically.

x_1	x_2	A	B	$f(x_1, x_2)$
0	0	1	0	1
0	1	1	0	1
1	0	0	0	0
1	1	0	1	1



Assumption: output of a gate changes instantaneously when its input changes