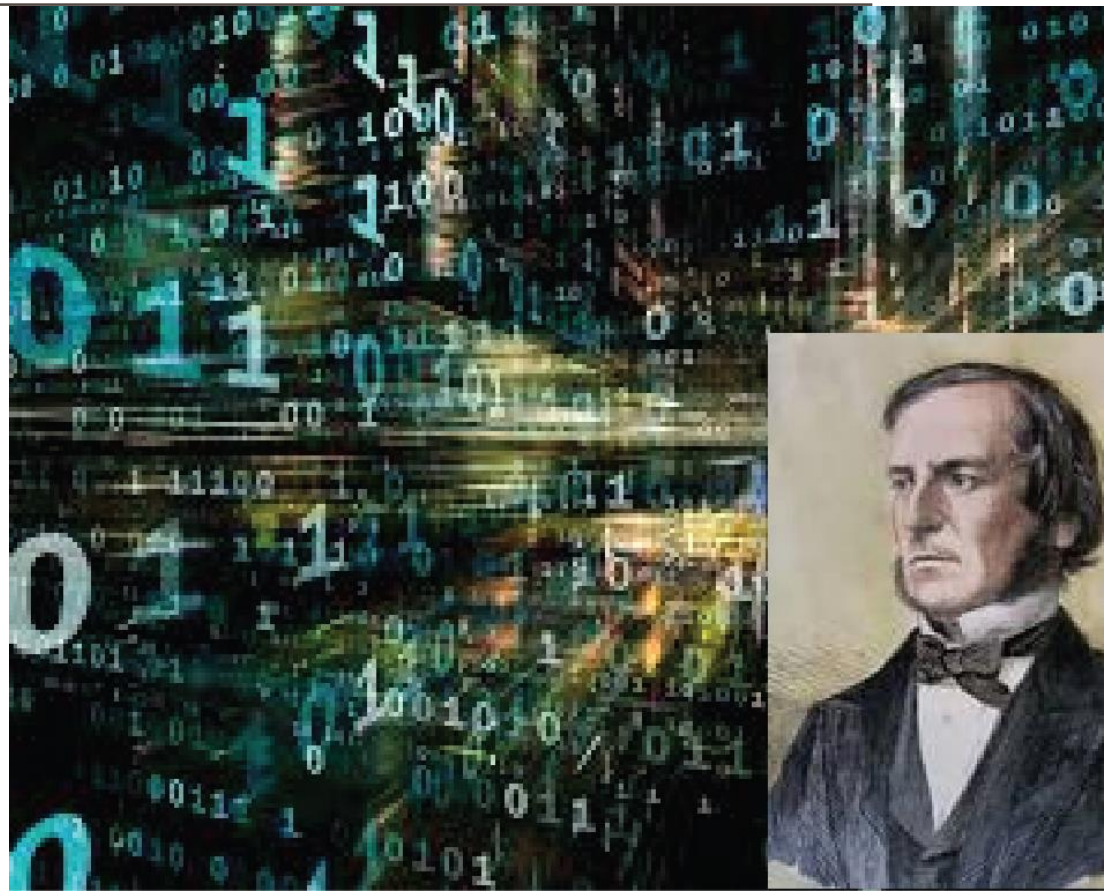
DIGITAL CIRCUITS

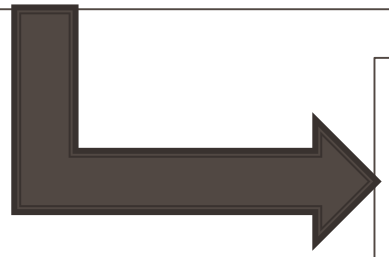


Week-11, Lecture-4
Sequential Circuits

Sneh Saurabh
27th October, 2018

Digital Circuits: Announcements/Revision

Sequential Circuits

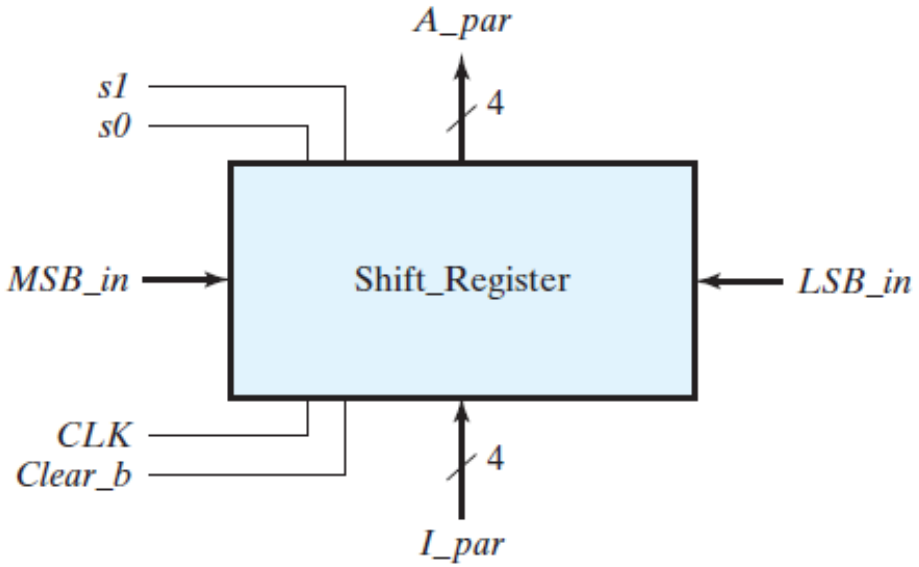


Registers and Counters

Universal Shift Register: Functionality

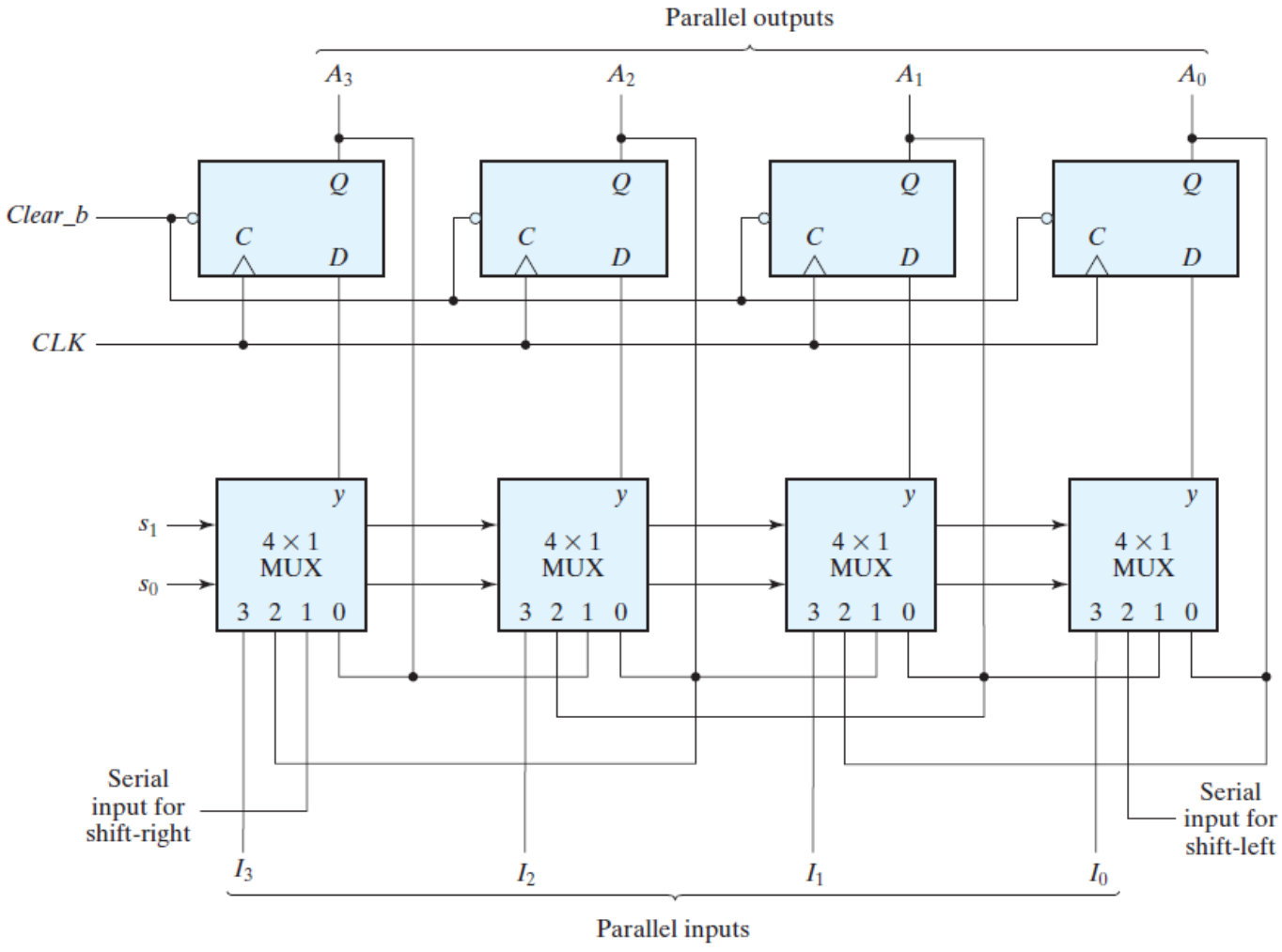
- Unidirectional/Bi-directional shift registers:
  - A register capable of shifting in one direction only is a unidirectional shift register.
  - One that can shift in both directions is a bidirectional shift register.

- If the register has both shifts and parallel-load capabilities, it is referred to as a ***universal shift register***



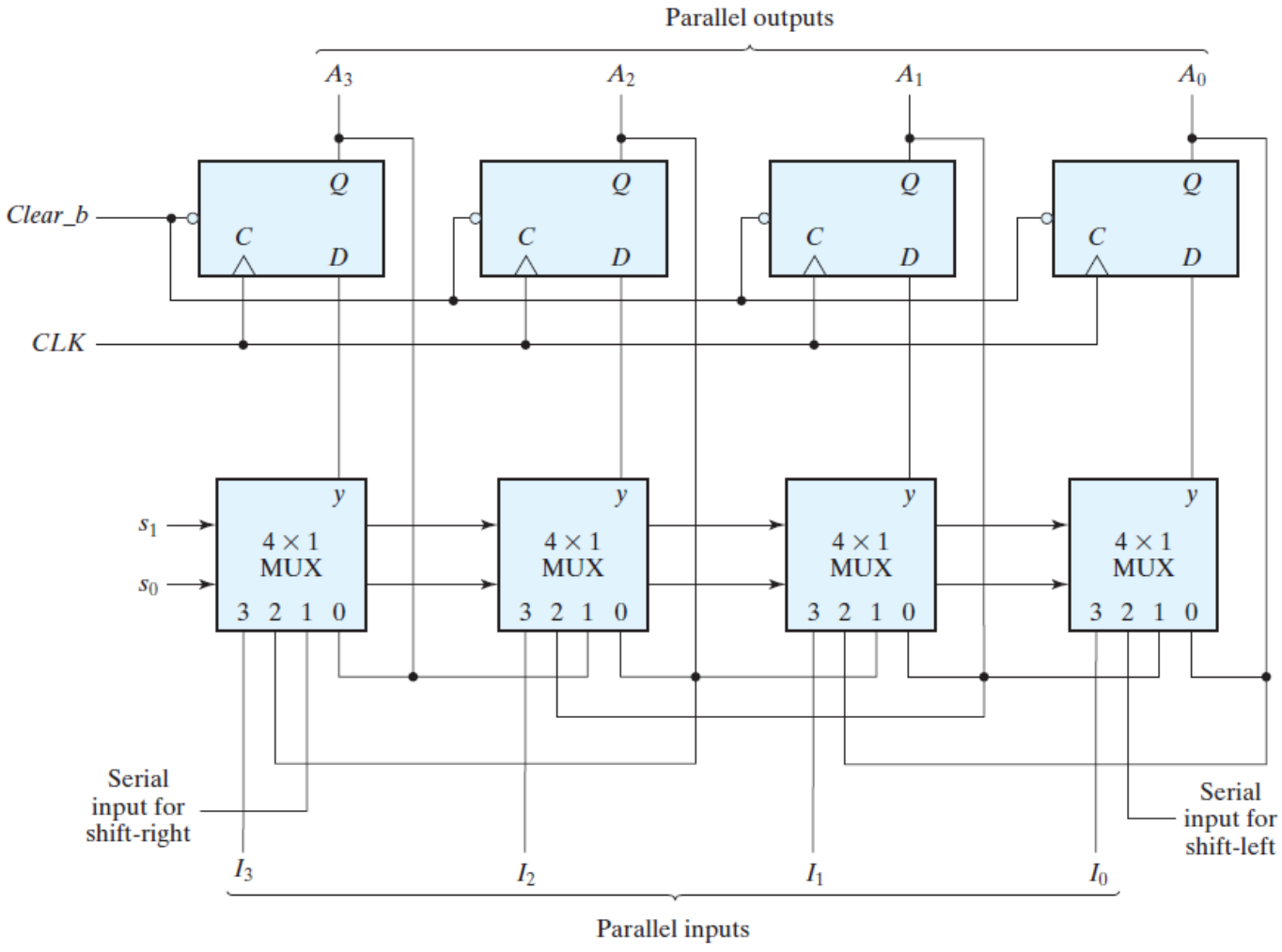
Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Universal Shift Register: Implementation



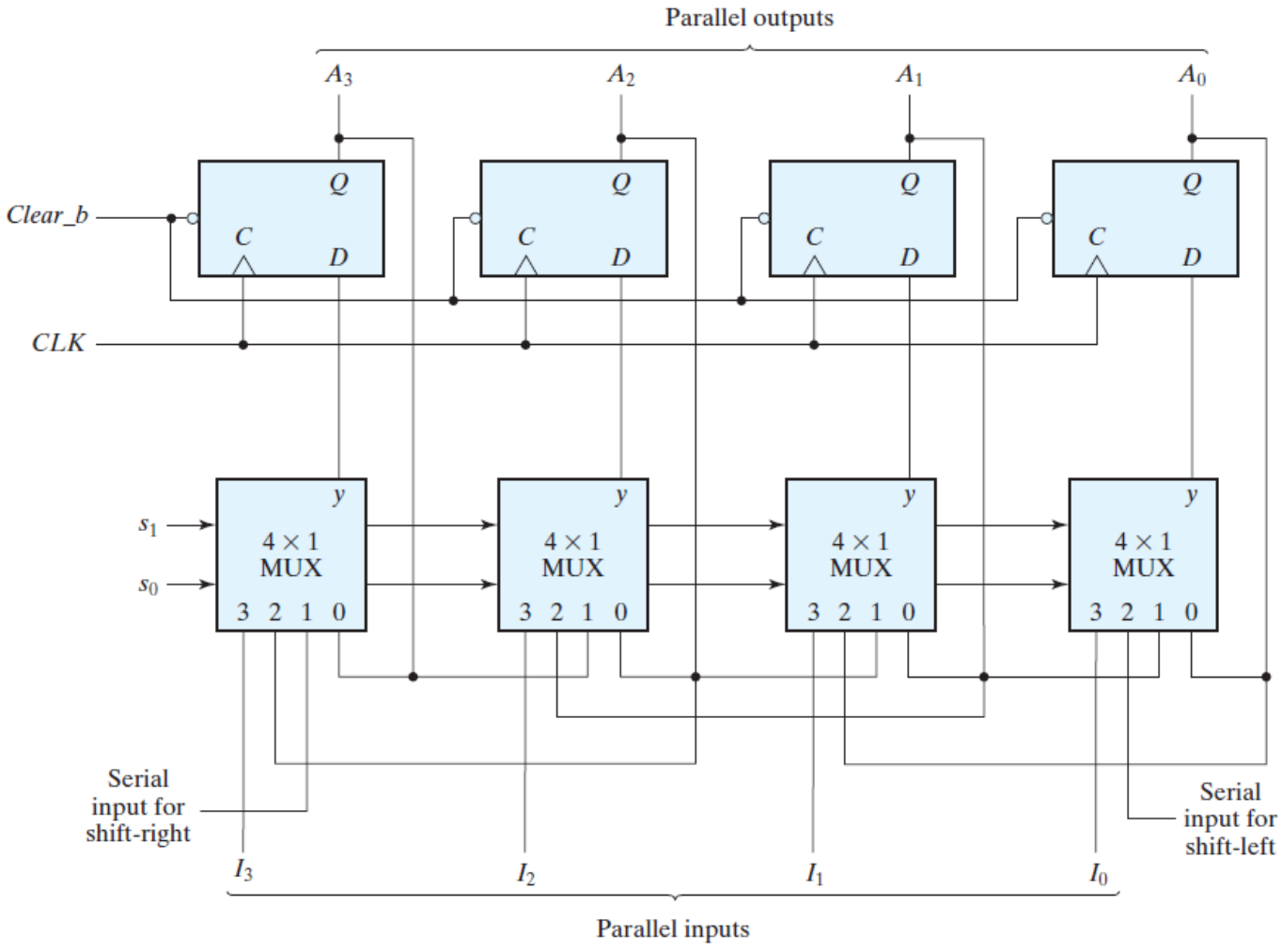
- When $s_0 s_1 = 00$, the present value of the register is applied to the D inputs of the flip-flops
- ***No change in output***

Universal Shift Register: Shift Right



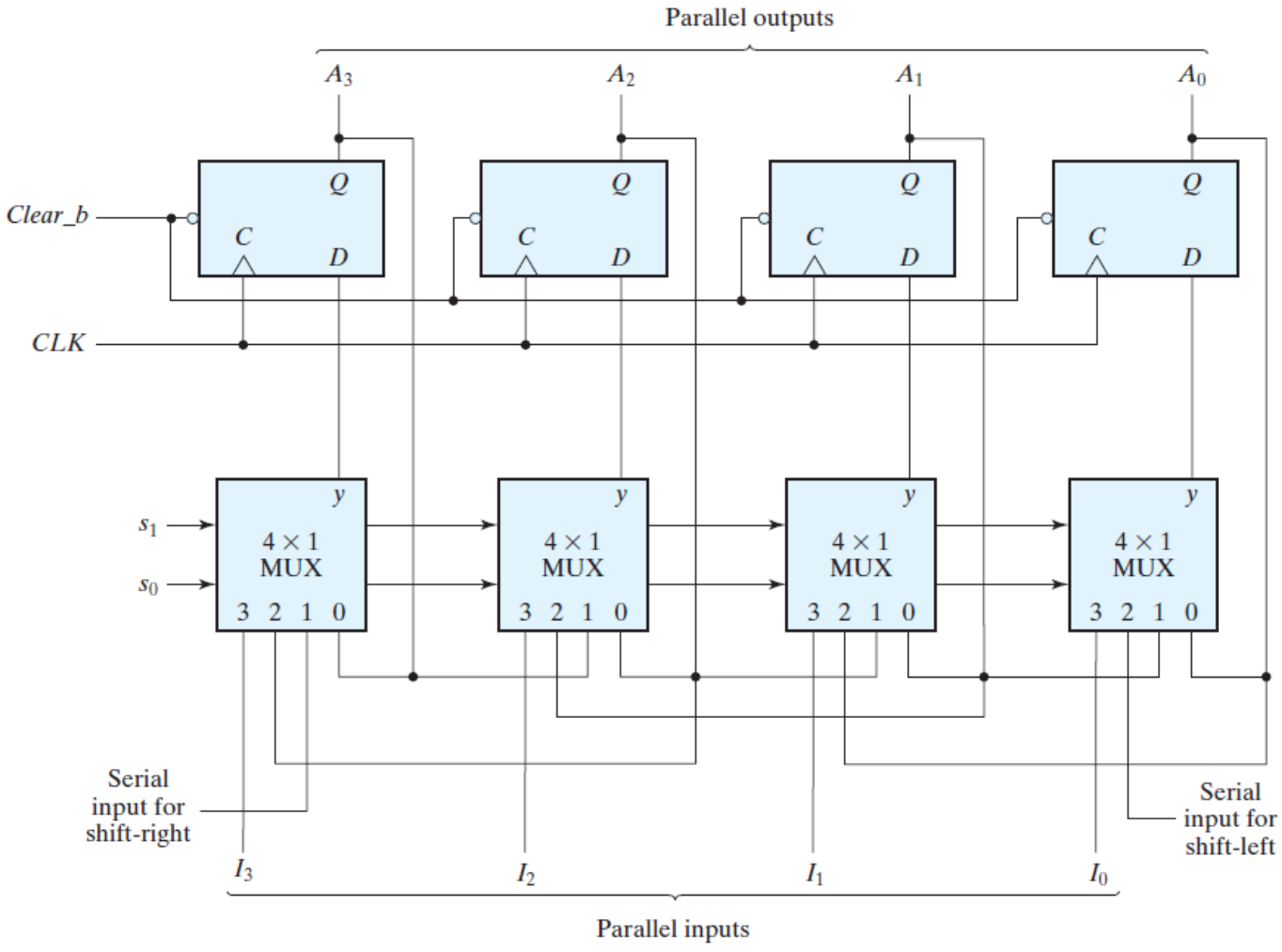
- When $s_0 s_1 = 01$, the D pin gets input from the left flip-flop
- ***Shift Right Operation is performed***

Universal Shift Register: Shift Left



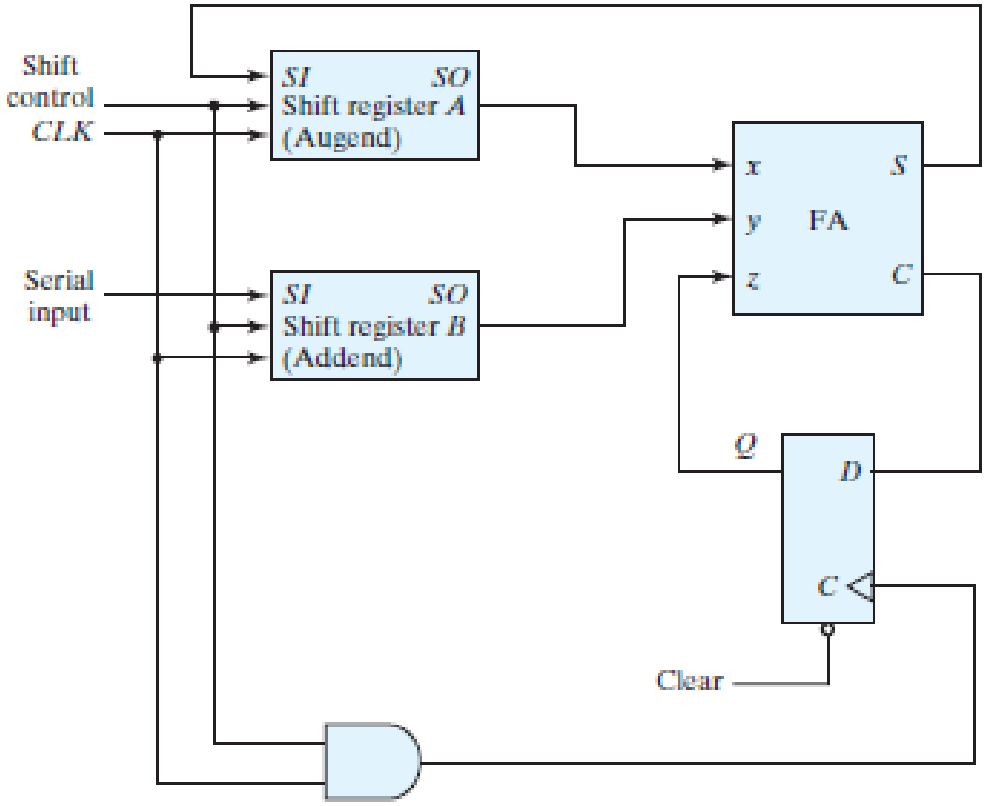
- When $s_0 s_1 = 10$, the D pin gets input from the right flip-flop
- ***Shift Left Operation is performed***

Universal Shift Register: Parallel Load



- When $s_0 s_1 = 11$, the D pin gets input from I_0, I_1 …
- ***Parallel Load is performed***

Serial Adder

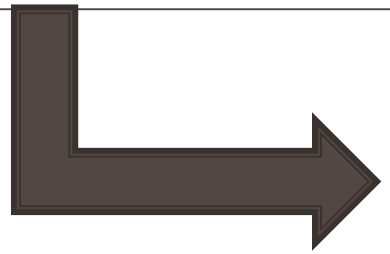


- Only one full-adder is used to add two binary numbers
- More number of clock cycles required
- Only one hardware (Adder) is required

Homework:

- Analyze the operation (from M. Morris Mano, Section 6.2)

Sequential Circuits



Counters

Counters: Basics

- A group of flip-flops that goes through a ***prescribed sequence*** of states upon the application of ***input pulses*** is called a counter

- **Prescribed sequence**: Can be binary number sequence or some other sequence
- One that follows binary number sequence is called **binary counter**
  - ➢ An n-bit binary counter consists of n flip-flops and count from 0 to (2^n-1)

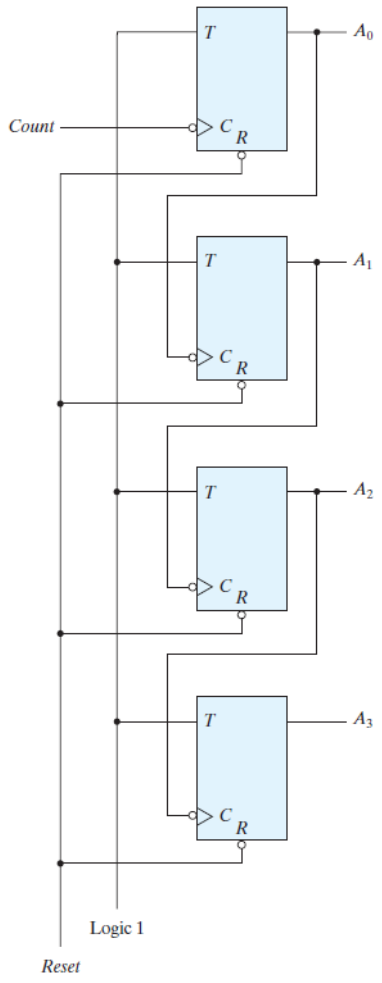
- **Inputs pulse**: clock or some other external signal

Two types:

1. **Asynchronous or Ripple Counter**: Clock signal for different flip-flops can be different (Q output of a flip-flop serves as clock input for some other flip-flop)
2. **Synchronous Counter**: All flip-flops clocked by the same clock pulse

Binary Ripple Counter

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

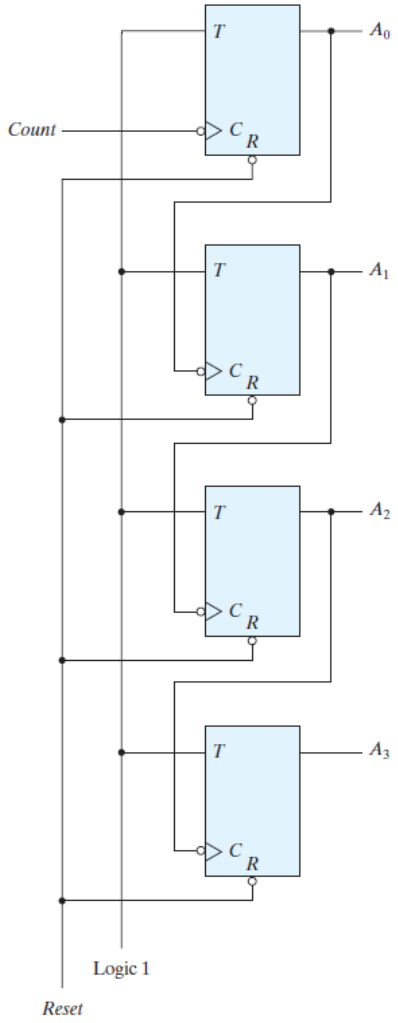


- T pin is tied to "1"
- The output of each flip-flop is connected to the Clock input of the next flip-flop in sequence
- LSB flip-flop receives clock pulse

- All clock pins are negative edged triggered
  - ➢ Whenever there is a fall edge at clock input the output Q will toggle

- The signal propagates in a form of a ripple from one stage to another
- Example: 0011 to 0010, then to 0000, and finally to 0100

Binary Ripple Counter



Problem:

What will happen if the flip-flops are **positive edge triggered** (instead of **negative edge triggered)** in the adjoining circuit?

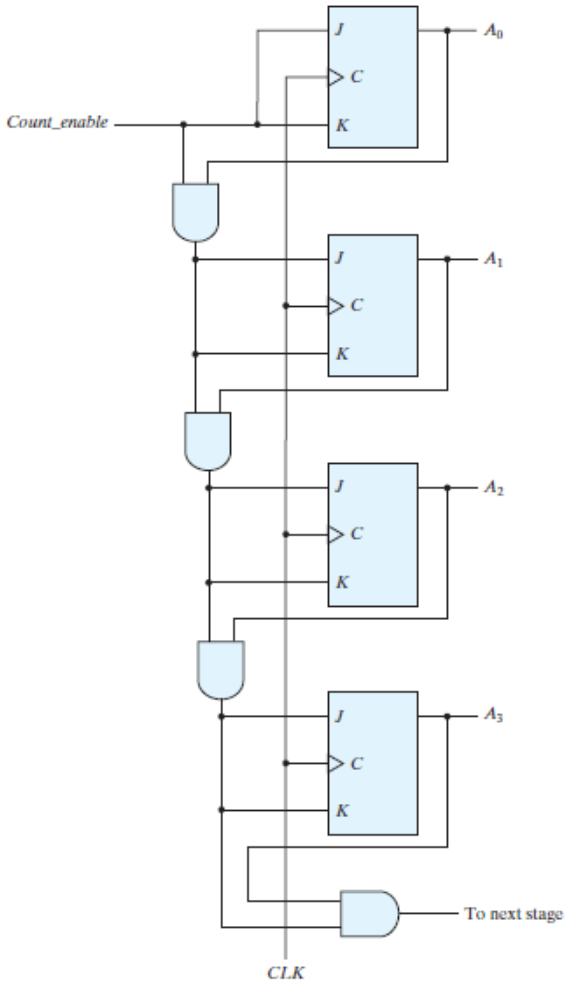
- LSB is complemented at every clock-pulse
- Any other bit in the sequence is complemented if its previous least significant bit goes **from 0 to 1.**

- It works as a down counter

A_3	A_2	A_1	A_0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
…	…	…	…

Synchronous Binary Counter

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



- It works on the observation that the flip-flop is complemented when all the bits in the lower significant positions are equal to 1 .

- $Count\_enable = 0$, then $J = K = 0$

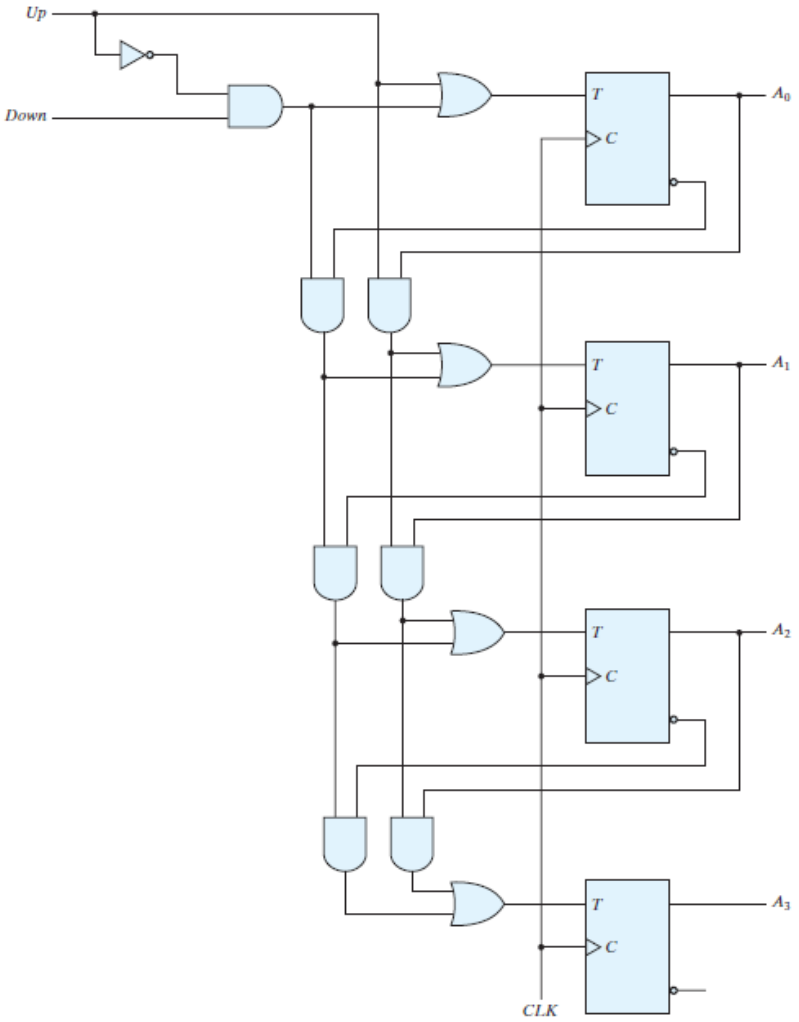
- $Count\_enable = 1$, then $J = K = 1$ if all previous least significant stages are equal to 1

Synchronous Binary Up/Down Counter

A_3	A_2	A_1	A_0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0

- **Down Counter**: A bit in any other position is complemented if all lower significant bits are equal to 0

- Up and Down Counters can be combined



Digital Circuits: Practice Problems

Problems 6.1-6.12

from “Digital Design”– M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).

Problems 7.18

from Fundamentals of Digital Logic with Verilog Design - S. Brown, Z. Vranesic