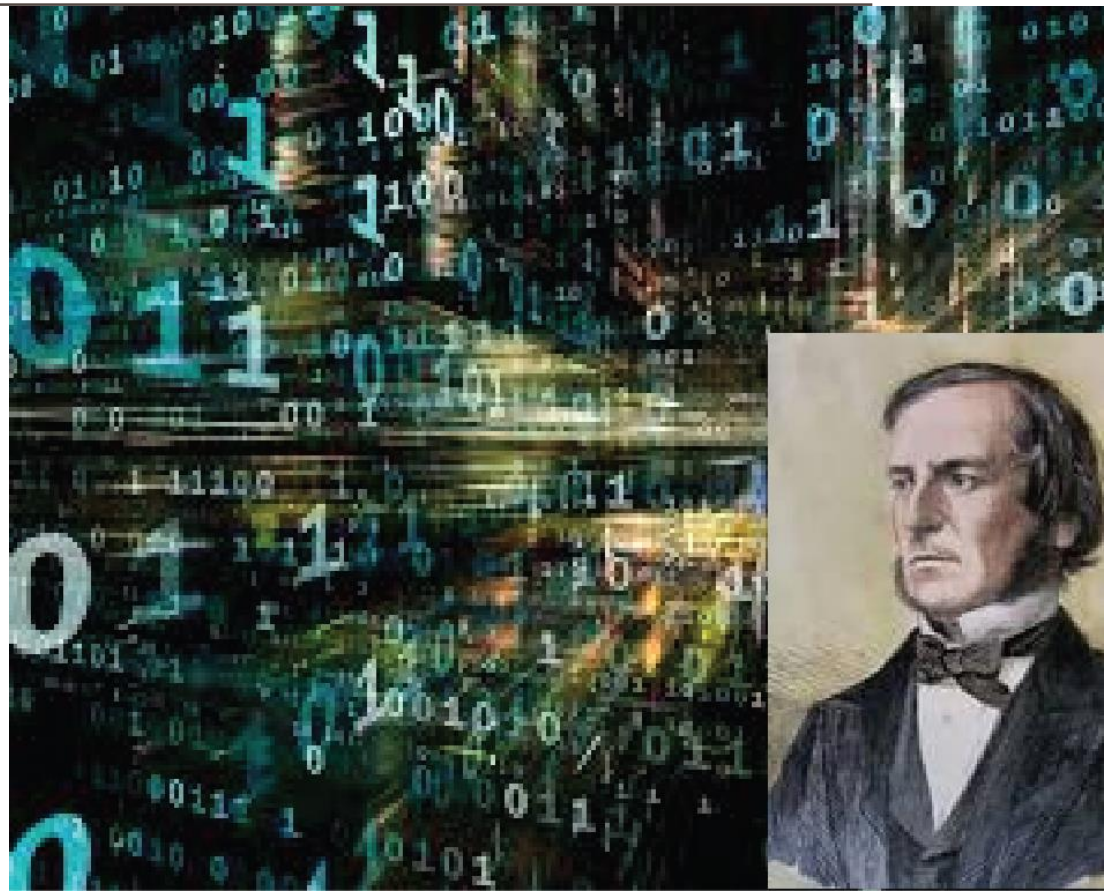
DIGITAL CIRCUITS

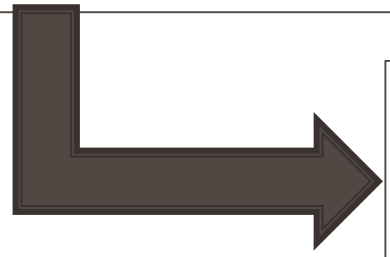
Week-14, Lecture-2
Sequential Circuits



Sneh Saurabh
14th November, 2018

Digital Circuits: Announcements/Revision

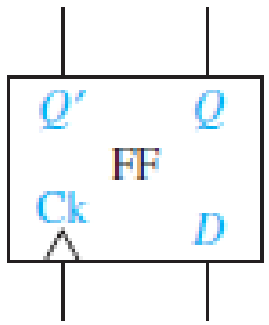
Sequential Circuits

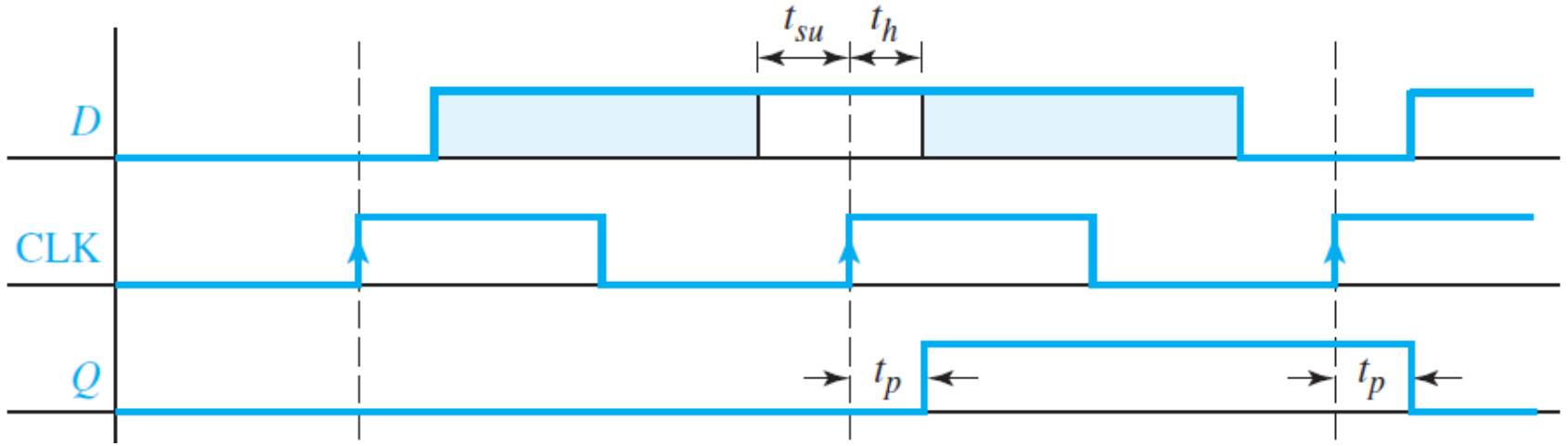


Pipelining

Timing constraints on Flip-flops due to delay

Flip-flop: Constraints





Constraints:

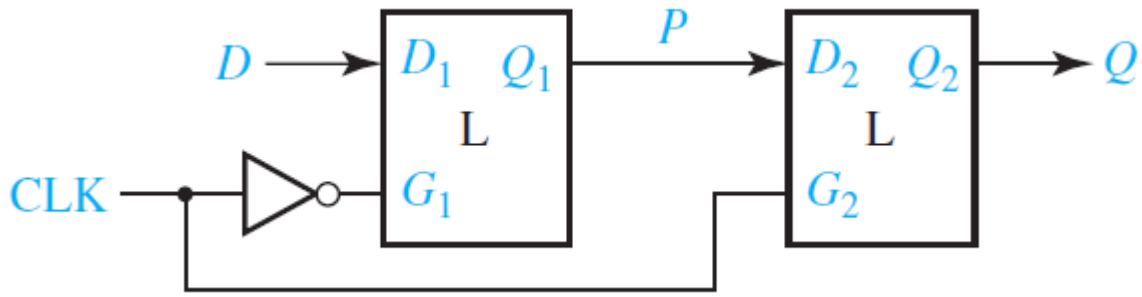
a) **Setup Time (t_{su}):** amount of time that D must be stable before the active edge.

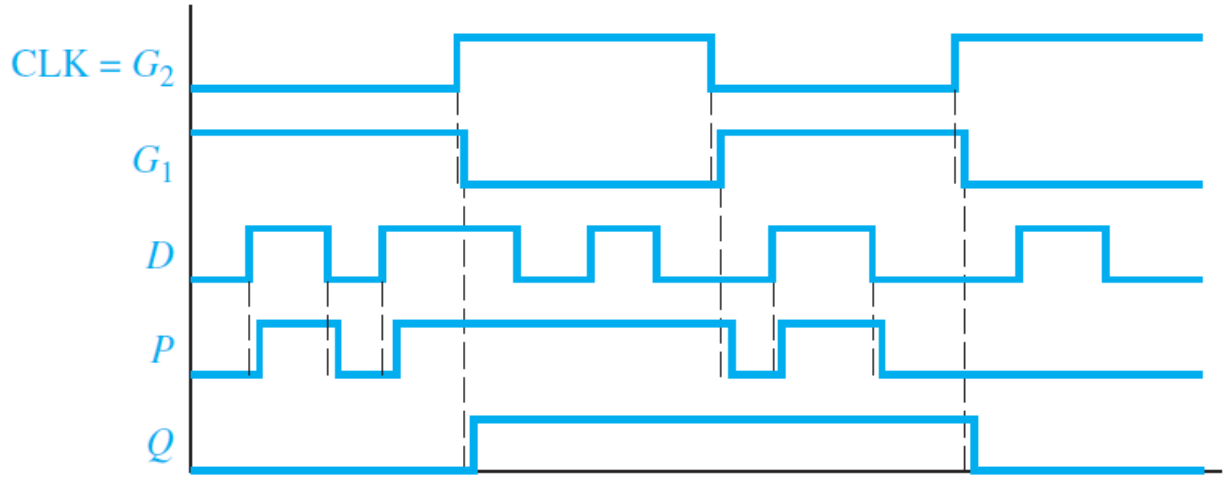
b) **Hold Time (t_h):** amount of time that D must hold the same value after the active edge

Delay:

Clock-to-Q propagation delay (t_p): the amount of time elapsed between the clock changes until the Q output changes.

Flip-flop: Origin of Setup Time

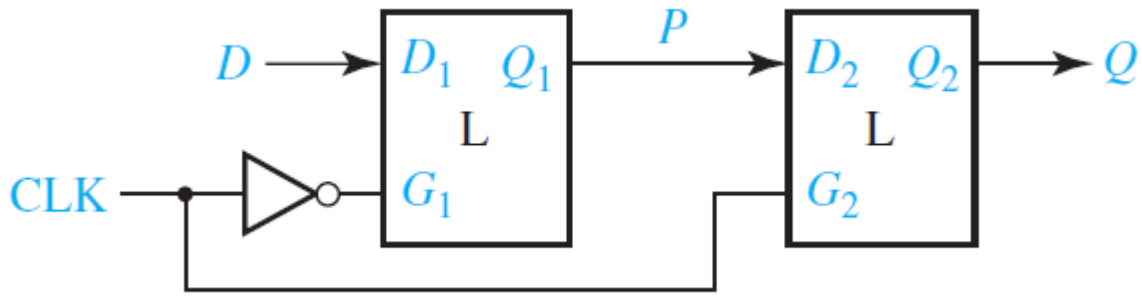


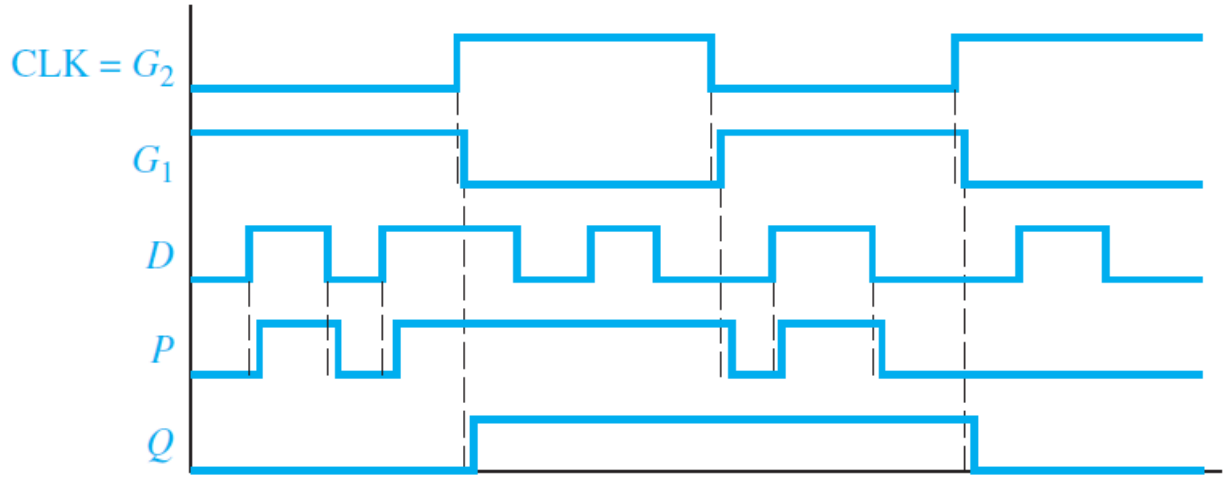


Setup Time (t_{su}):

- Amount of time required for data at D to propagate through master latch and get sampled by the slave latch
- Setup time decided by the delay of the master latch
- Time interval before the positive edge of clock that the signal on the D input must be stable
- If the input is changed during this time, the output of the slave latch becomes unpredictable

Flip-flop: Origin of Hold Time

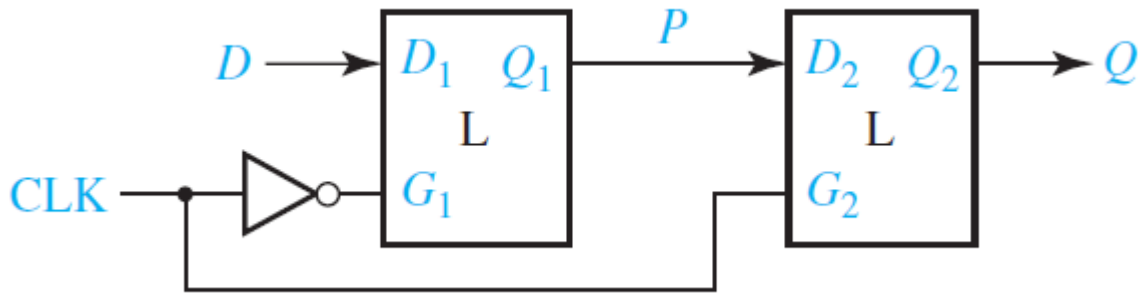


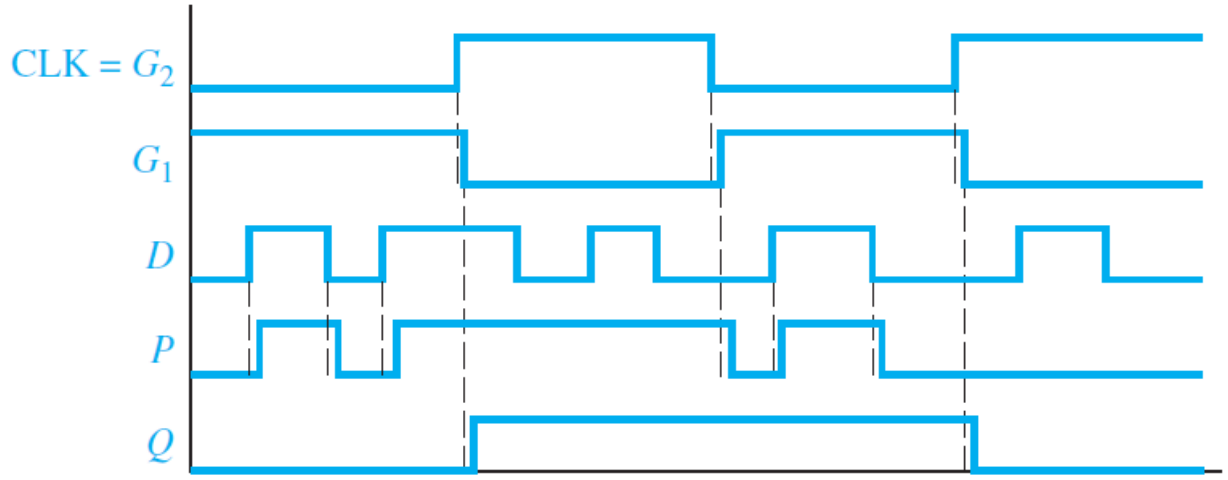


Hold Time (t_h):

- When Clock goes from Low to High, then (due to delay of inverter) for a short duration both latches are enabled
- If the input changes during this time, we don't know whether output corresponds to previous input or present input (unpredictable)
- This is called hold time: time after the active clock edge during which the input must be stable

Flip-flop: Origin of Clock-to-Q propagation delay

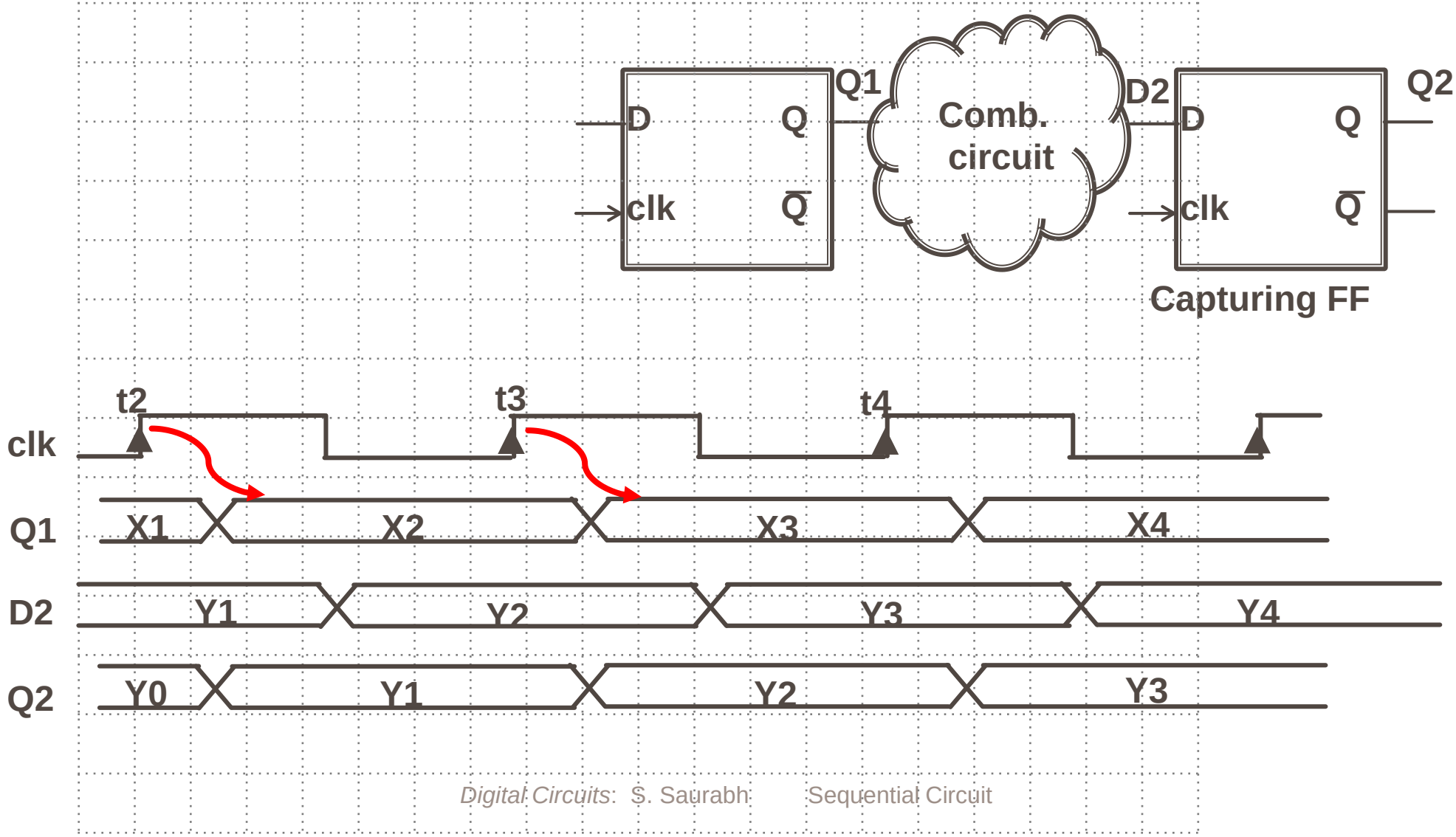




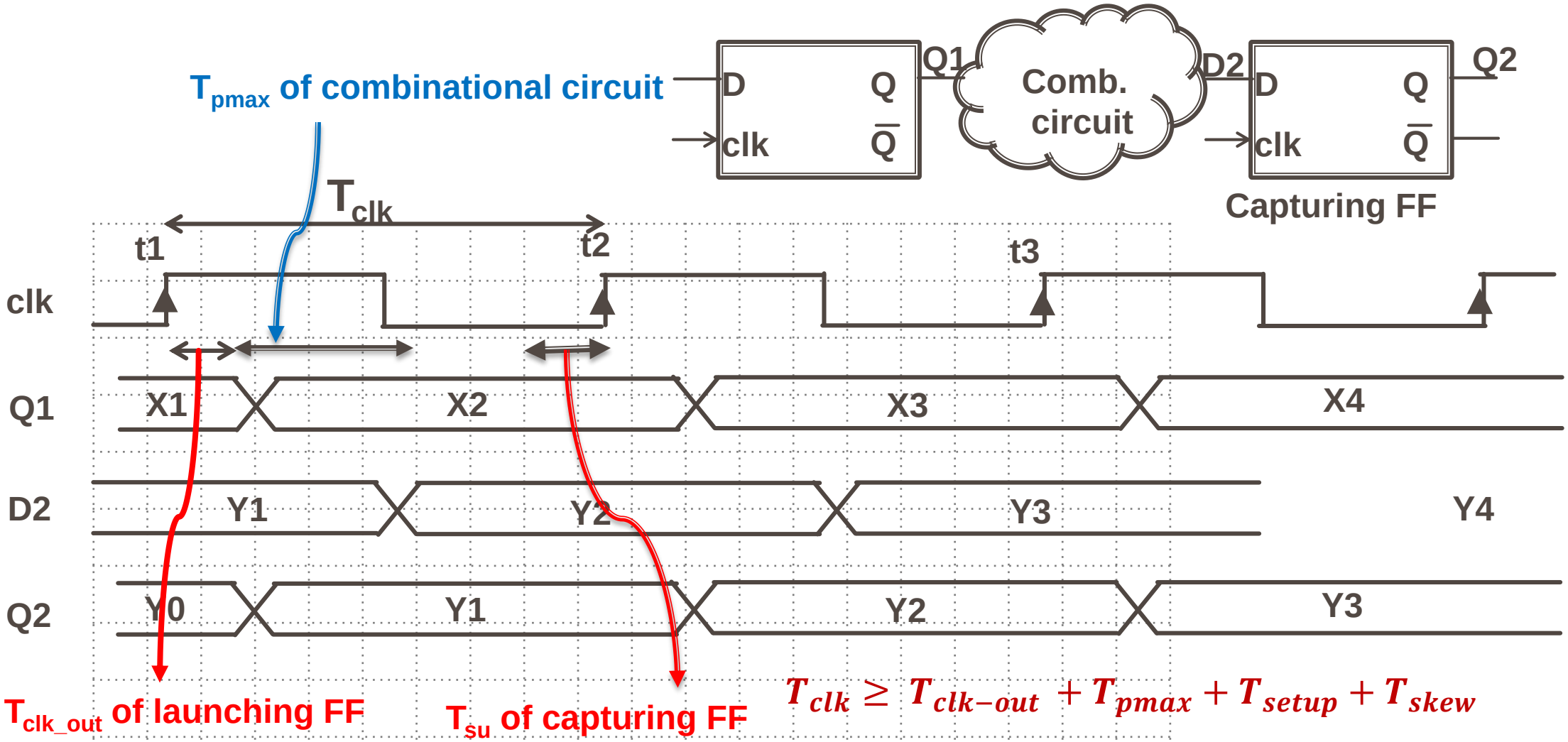
Clock-to-Q propagation delay (t_p):

- When active edge of clock appears at the slave latch, it takes time for the data to propagate from D_2 to Q
- This decides the Clock-to-Q propagation delay
- It is also denoted as $t_{clk-out}$

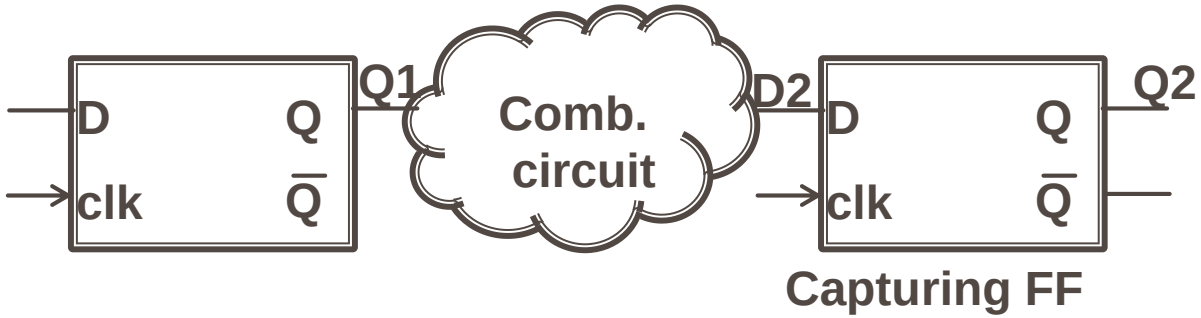
Constraints on Sequential Circuit: Setup Constraint (1)



Constraints on Sequential Circuit: Setup Constraint (2)



Constraints on Sequential Circuit: Setup Constraint (3)



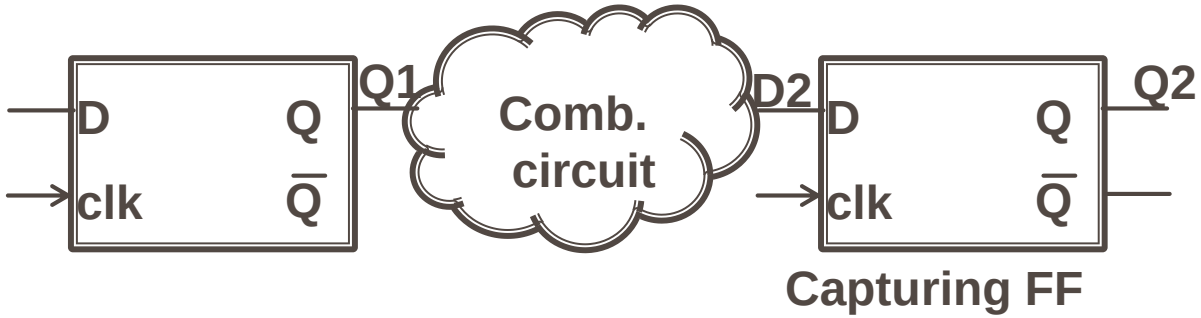
$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

Clock Skew (T_{skew}):

- Difference in arrival time of the active clock edge at launch flip-flop ($t_{c-launch}$) and capture flip-flop ($t_{c-capture}$)
- $T_{skew} = t_{c-launch} - t_{c-capture}$

- If active edge of clock arrives late at the launch flip-flop then the effect is similar to adding delay on the launching data
- The effect is opposite if clock arrives late at the capture flip-flop (more time is allowed for data to propagate)

Constraints on Sequential Circuit: Setup Constraint (4)



$$T_{clk} \geq T_{clk-out} + T_{pmax} + T_{setup} + T_{skew}$$

How to reduce T_{clk} or increase the frequency of operation?

- Reduce T_{pmax}, $T_{clk-out}$ or T_{setup}

Constraints on Sequential Circuit: Setup Constraint (5)

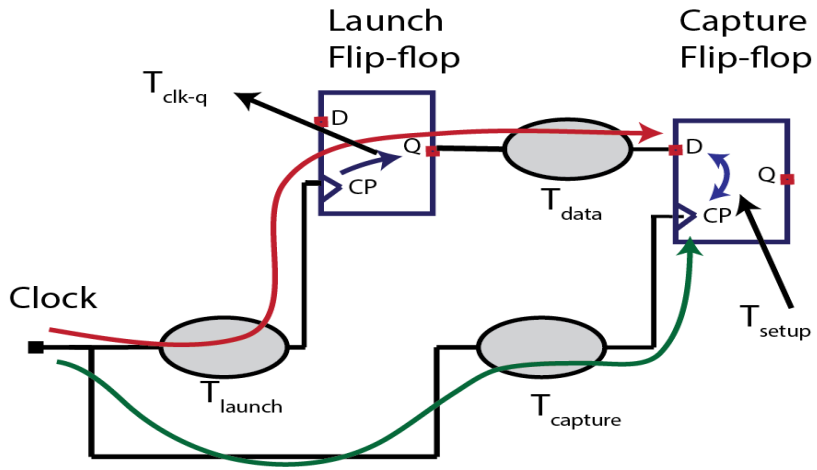
Problem:

The critical path for a circuit is shown alongside. Find the maximum clock frequency that this circuit can work.

For launch flip-flop: $T_{setup} = 10\ ps$, $T_{clk-q} = 20\ ps$,

For capture flip-flop: $T_{setup} = 30\ ps$, $T_{clk-q} = 25\ ps$

$T_{launch} = 140\ ps \quad T_{capture} = 90\ ps\ T_{data} = 400\ ps$



Answer:

$$\boldsymbol{T_{period} > T_{clk-q} + T_{data} + T_{setup} + (T_{launch} - T_{capture})}$$

$$\boldsymbol{T_{period} > 20 + 400 + 30 + 140 - 90}$$

$$\boldsymbol{T_{period} > 500\ ps \Rightarrow f_{clk} < 2\ GHz}$$