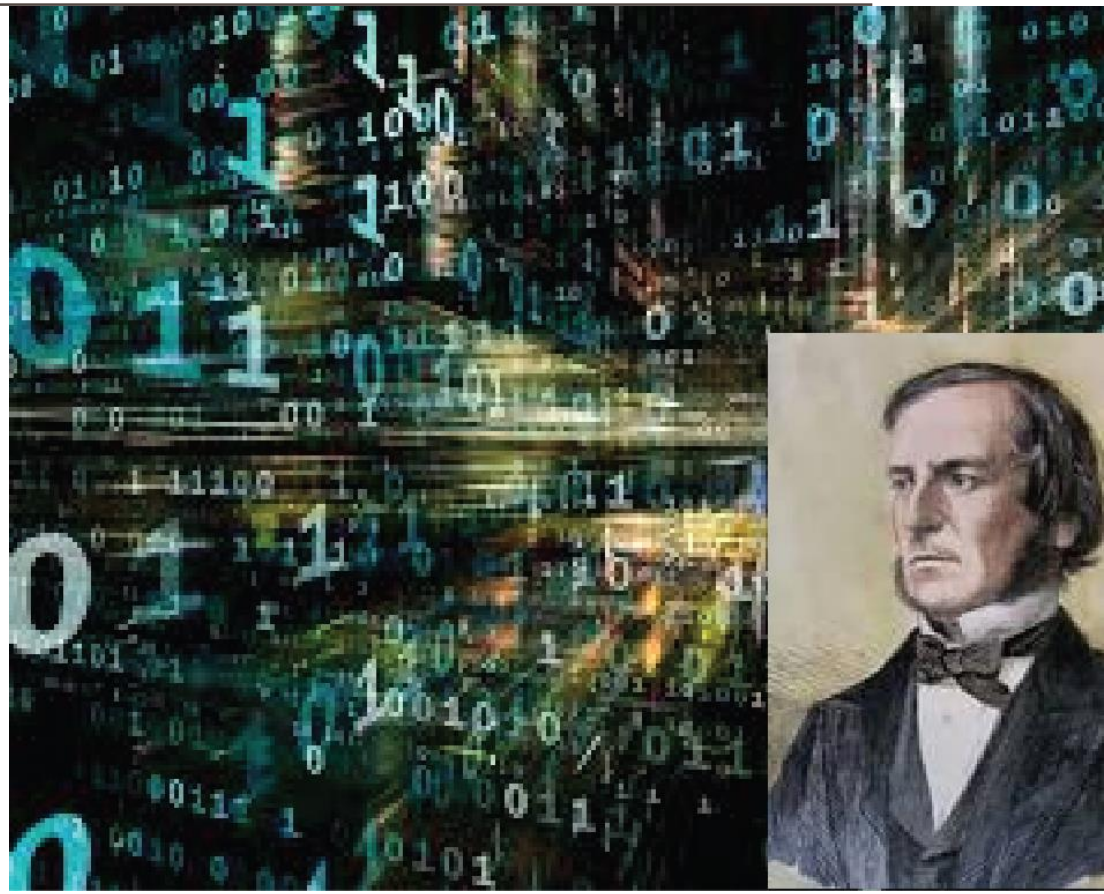
DIGITAL CIRCUITS

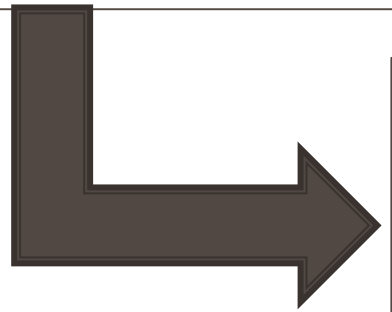
Week-11, Lecture-1
Sequential Circuits

Sneh Saurabh
23rd October, 2018



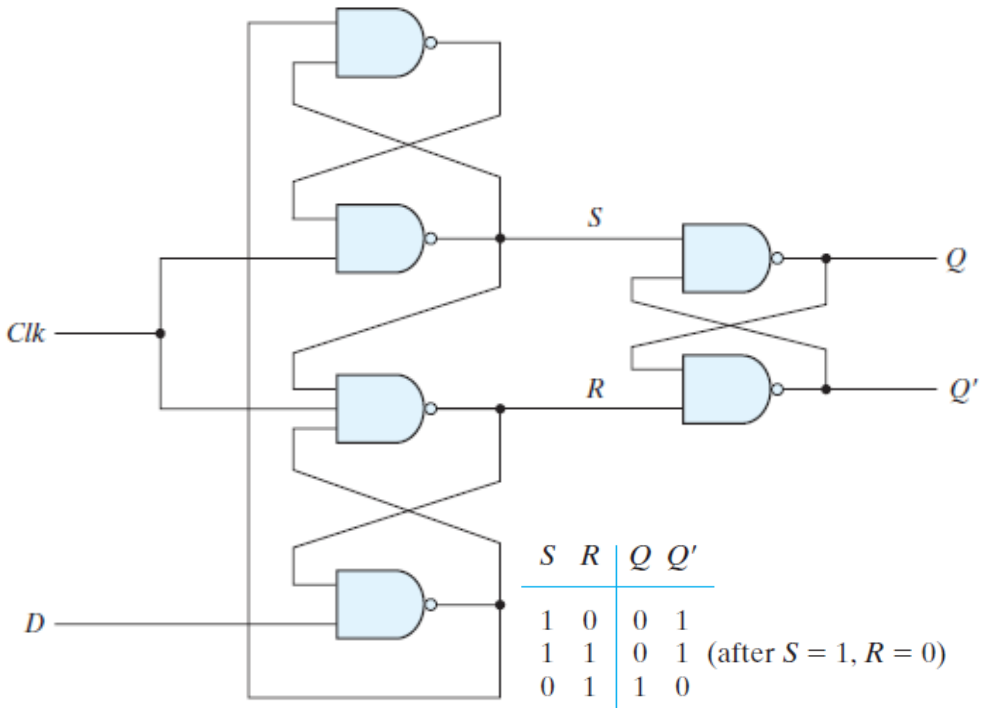
Digital Circuits: Announcements/Revision

Sequential Circuits



Flip-flops

Flip-flop Implementation: positive edge-triggered (1)



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

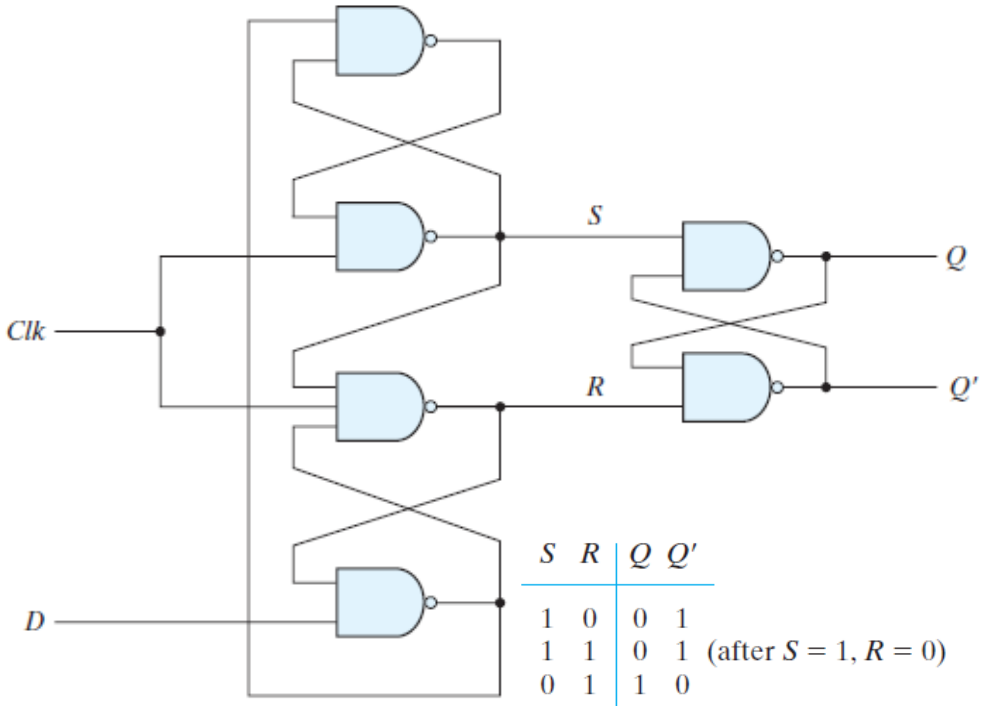
Can you derive the functionality?

Three SR latches: Two connected to Clk and D, One connected to the output

- When $Clk = 0$, SR latch connected to the output has $S = R = 1$, and present state is maintained
  - Input D can be 0 or 1, it will not matter

- When clock changes to $Clk = 1$
  - If $D = 0$, R changes to $R = 0$, and S remains at S=1 and Q=0 state reached
  - If $D = 1$, $R = 1$ remains, and S changes to $S = 0$ and $Q = 1$ state reached

Flip-flop Implementation: positive edge-triggered (2)



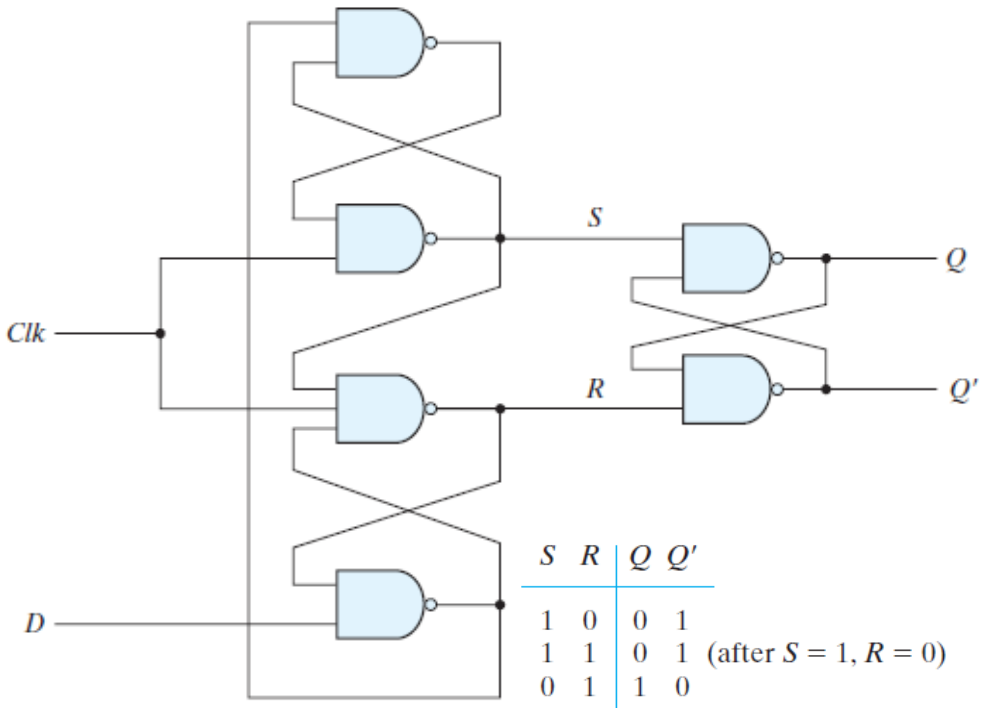
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

To ensure edge-triggered operation

- At $Clk = 1$ changes in D should not be recorded further (only the value of D when positive edge occurred should decide Q/Q')

- At the positive edge $Clk = 1$, assume that $D = 0$
  - S = 1, R=0 is reached (as already explained)
  - If now D changes $D = 1$, no impact on the output of the bottom NAND gate

Flip-flop Implementation: positive edge-triggered (3)



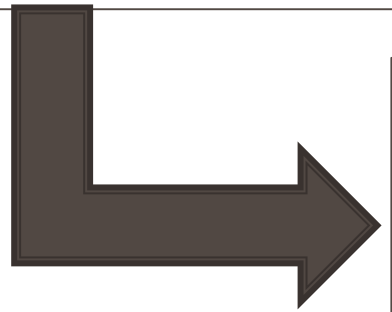
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

To ensure edge-triggered operation

- At $Clk = 1$ changes in D should not be recorded further (only the value of D when positive edge occurred should decide Q/Q')

- At the positive edge $Clk = 1$, assume that $D = 1$
  - S = 0, R=1 is reached (as already explained)
  - If now D changes to $D = 0$, the output of the bottom NAND gate changes from 0 to 1
    - Since S=0, R remains at 1, (no impact of this change)
    - Since S=0, the output of the top NAND gate remains at 1 (no impact of this change) and S remains at 0

Sequential Circuits



Flip-flops with Clear/Preset

Flip-flops with Clear/Preset

Clear:

- It takes the flip-flop Q pin to 0
- Also called “Reset”

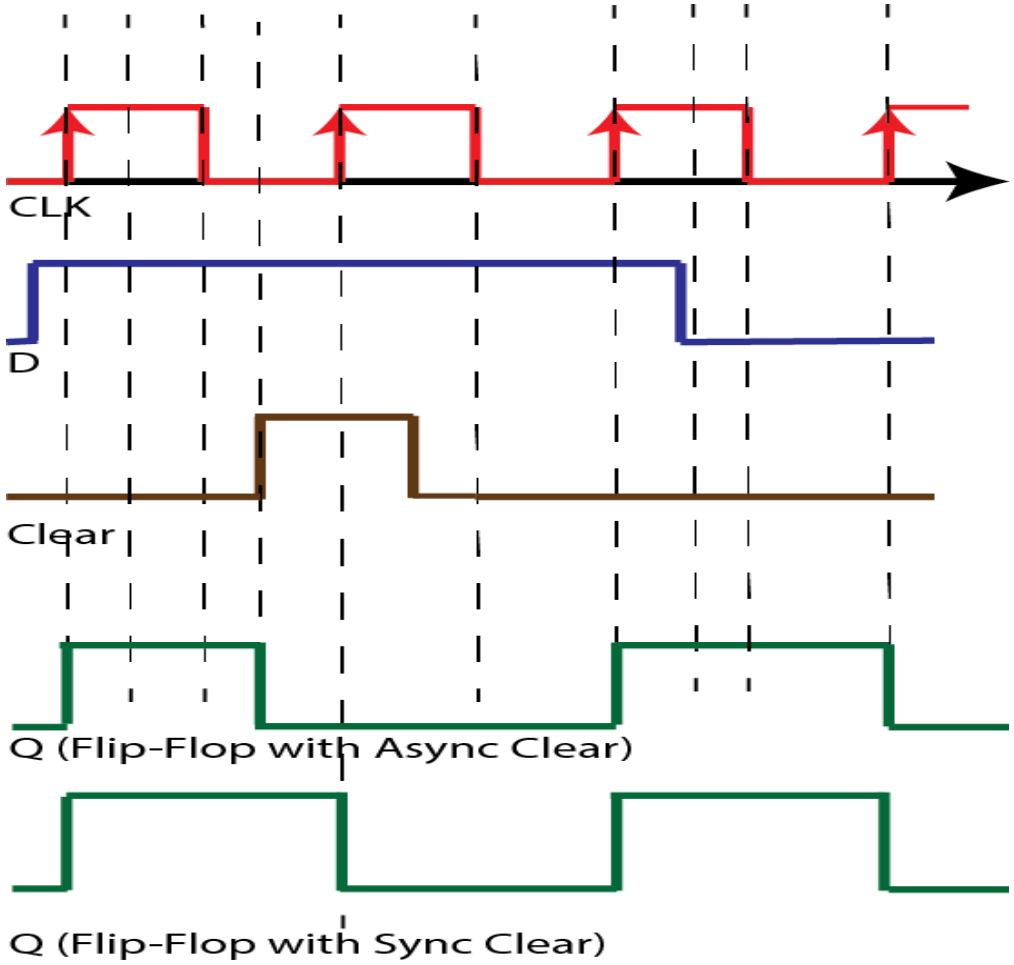
Preset:

- It takes the flip-flop Q pin to 1
- Also called “Set”

Two Types based on when the effect takes place:

- Asynchronous Clear/Preset:
  - ➢ The effect of Clear/Preset on Q is observed immediately (without waiting for clock edge)
- Synchronous Clear/Preset
  - ➢ The effect of Clear/Preset on Q is observed only when appropriate clock edge arrives

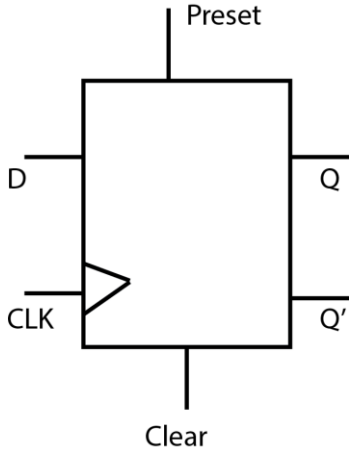
Flip-flops with Clear/Preset: Asynchronous vs. Synchronous

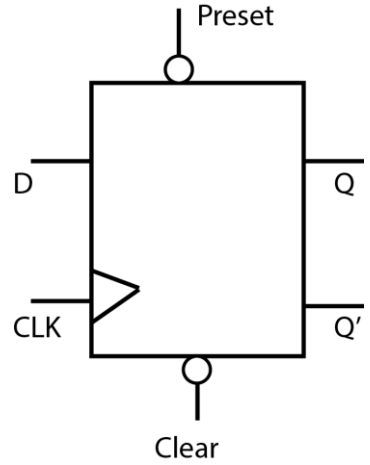


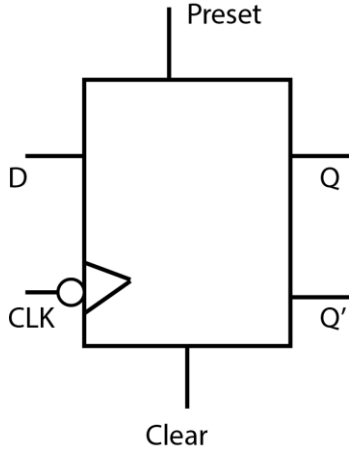
Flip-flops with Clear/Preset

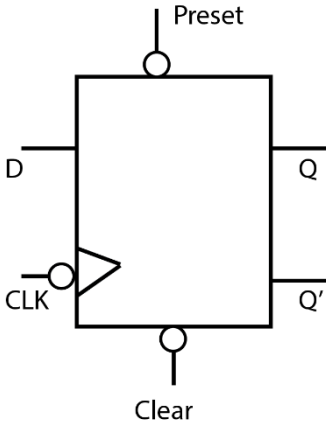
Two Types based on level :

- Active High Clear/Preset
- Active Low Clear/Preset

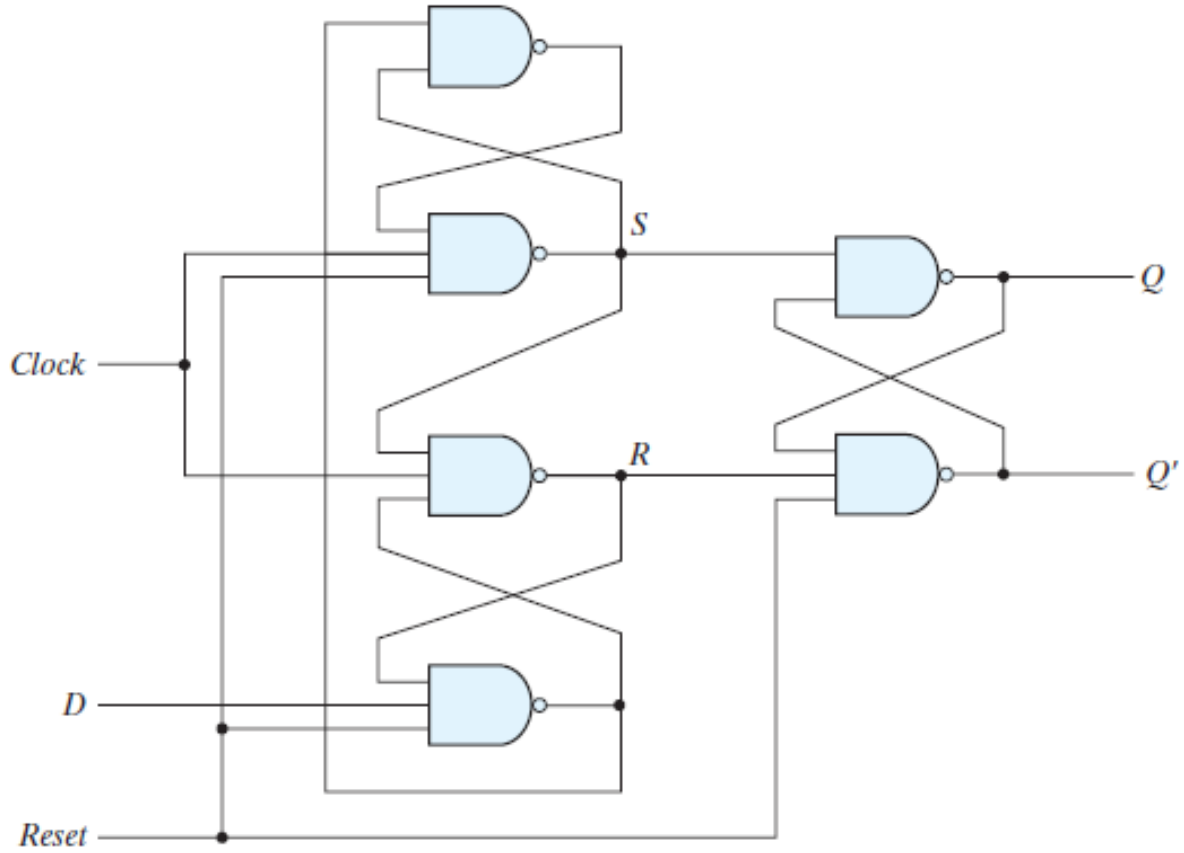








Flip-flop with Asynchronous Clear/Preset

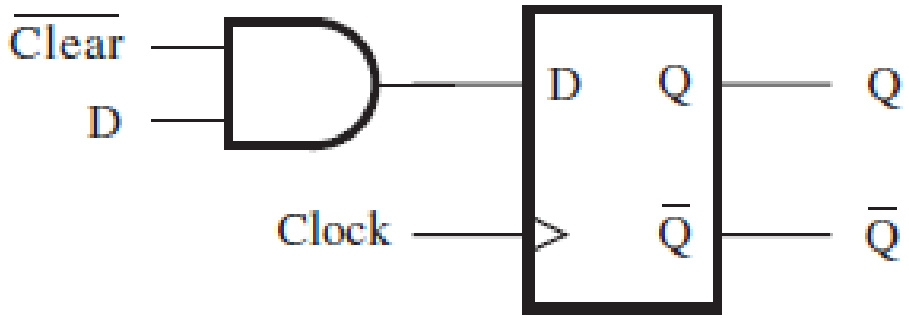


Operation:

- "Reset" or "Clear" is active low in this case
- When $Reset = 0$, Q' is forced to 1 and S is forced to 1
- Q is changes to 0 immediately, irrespective of Clock

R	Clk	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

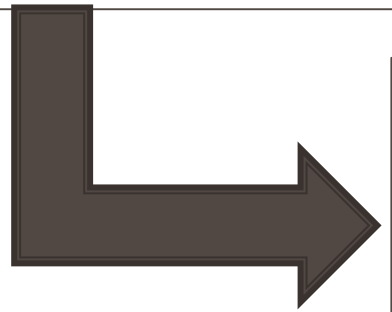
Flip-flop with Synchronous Clear/Preset



Operation:

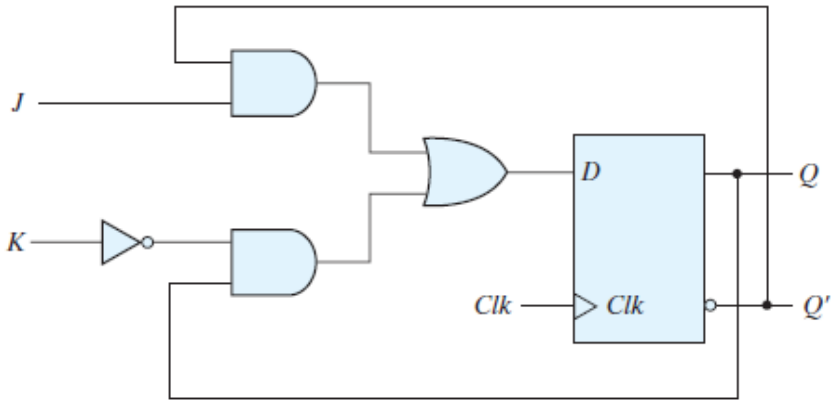
- "Clear" is active high in this case
- When $Clear = 1$, and **Clock edge arrives**, Q is changes to 0

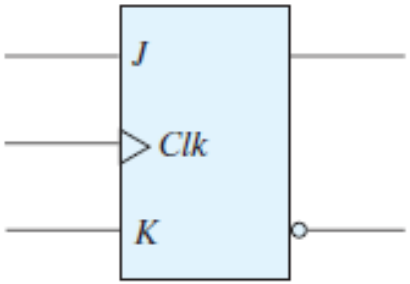
Sequential Circuits



Other types of Flip-flops

JK Flip-Flop using D flip-flop





Problem:

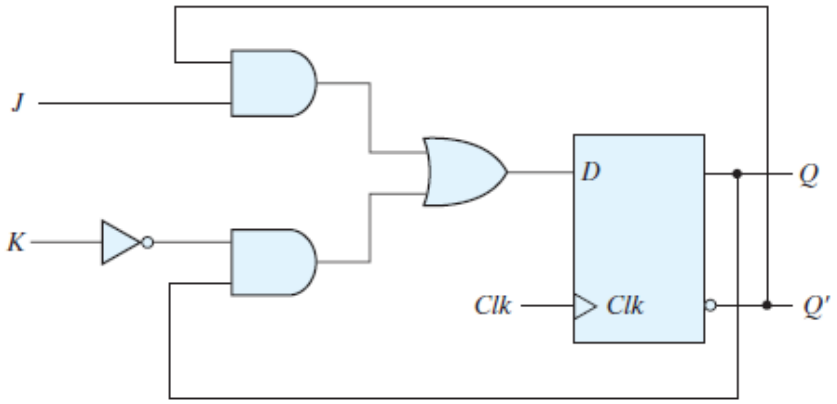
A JK flip-flop is realized using a D flip-flop using the circuit shown alongside.

Obtain the functionality of the JK flip-flop in a form of ***characteristics table***.

Characteristics Table

- A tabular representation of the functionality of a sequential circuit such as a flip-flop
- The next state of the circuit is represented as a function of inputs and the present state
  - Next State: The state that results after clock transition $Q(t+1)$
  - Present State: The state just before the application of clock edge $Q(t)$

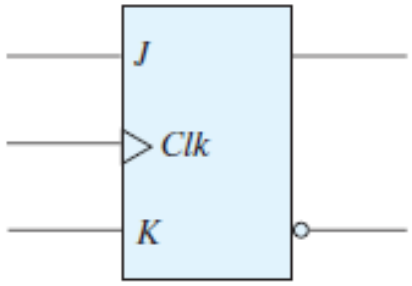
JK Flip-Flop: Characteristics Table



Problem:

A JK flip-flop is realized using a D flip-flop using the circuit shown alongside.

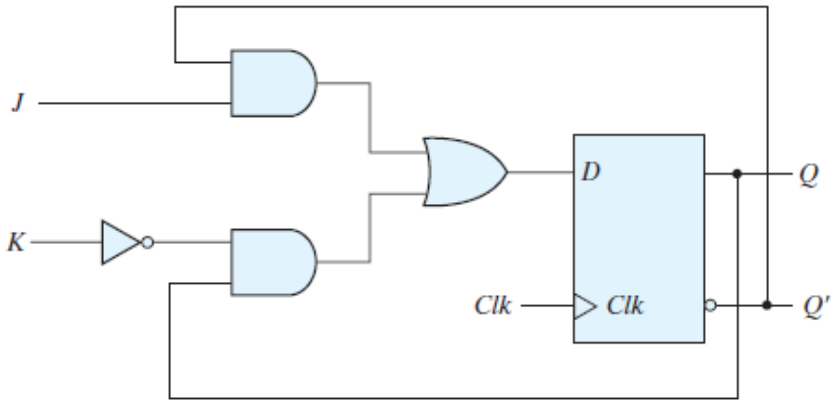
Obtain the functionality of the JK flip-flop in a form of ***characteristics table***.

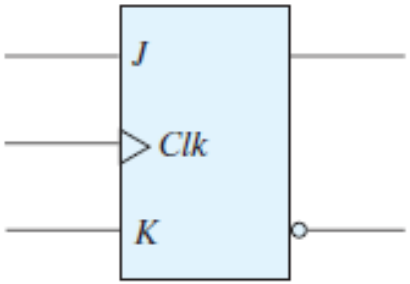


J	K	$Q(t+1)$
0	0	
0	1	
1	0	
1	1	

J	K	$Q(t+1)$	Comment
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

JK Flip-Flop: Characteristics Equation





Problem:

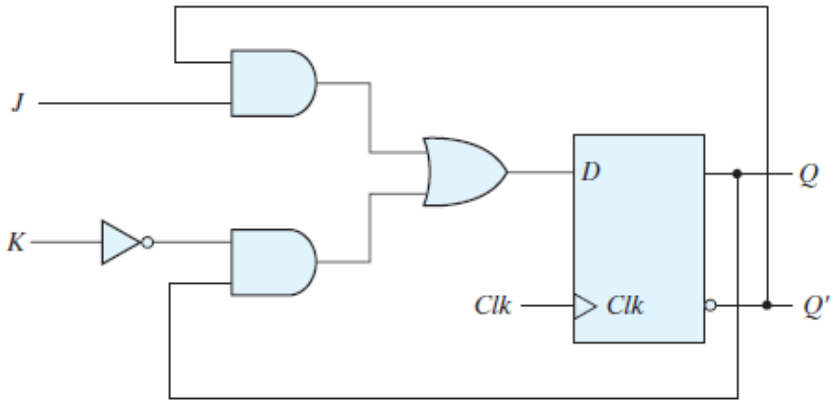
A JK flip-flop is realized using a D flip-flop using the circuit shown alongside.

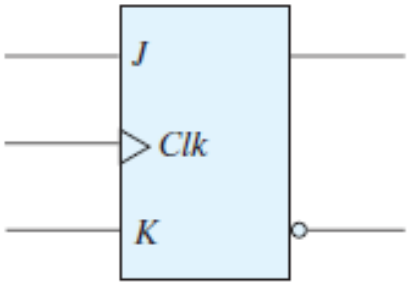
Obtain the functionality of the JK flip-flop in a form of ***characteristics equation***

Characteristics Equation

- Representation of the functionality of a sequential circuit such as a flip-flop in the form of an algebraic expression
- $Q(t+1) = f(inputs, Q(t))$

JK Flip-Flop: Characteristics Equation





Problem:

A JK flip-flop is realized using a D flip-flop using the circuit shown alongside.

Obtain the functionality of the JK flip-flop in a form of ***characteristics equation***

To obtain characteristics equation from circuit

- Express the function at "D" in terms of inputs and $Q(t)$

$$Q(t+1) = JQ' + K'Q$$