Digital Circuits

Experiment 2

Combinational Circuits for Binary Addition

We will use various kinds of CMOS gates as required for the implementation of the logic. Apart from the four kinds of CMOS gates you have studied in **Experiment 1**, we will also use the Exclusive OR (XOR) gate (CD4070) in this experiment. The pin connections of all the ICs are the same as given in **Fig. 1 (a)** of the write-up for **Experiment 1**.

Part A. De Morgan's Theorems

De Morgan's theorems state that:

$$(A + B)' = A' \bullet B' \qquad \text{and} \qquad (A \bullet B)' = A' + B'.$$

Verify these theorems by proceeding step by step as follows:

1. Set up a circuit consisting of two NOR gates and one AND gate out of the given IC chips to perform the function $Y = A' \bullet B'$, using a NOR gate with its two inputs connected together to perform the NOT function.
2. Obtain the truth table of this circuit by proceeding as done in steps 1, 2 and 3 of Part A, and verify that the truth table is the same as that of a NOR gate.
3. Repeat steps 1 and 2 using an OR gate instead of an AND gate to verify that the truth table of the function $Y = A' + B'$ is the same as that of a NAND gate.

Part B. Binary Half Adder using Gates

A binary Half Adder adds two bits A and B to generate SUM and CARRY bits as output according to the following Boolean expressions for the outputs :

$$SUM = A' \bullet B + A \bullet B' = A \oplus B \qquad \text{and} \qquad CARRY = A \bullet B.$$

1. Set up the circuit of a Half Adder using an XOR gate and an AND gate out of the given IC chips. Apply the inputs A and B from two input switches and observe the outputs S1 and C1 on two LED displays for all combinations of the inputs.
2. Tabulate these values and verify the operation of the Half Adder.

Part C. Binary Full Adder using Gates

A binary Full Adder adds two bits A and B along with a carry in C to generate SUM and CARRY bits as output. It can be implemented with two Half Adders and one AND gate. In this implementation, one Half Adder is used to add the bits A and B to generate intermediate sum and carry bits S1 and C1. Another Half Adder is then used to generate the final SUM by adding the carry in bit C to the S1 bit generated by the first Half Adder:

$$SUM = S1 \oplus C$$

Note that the logic for the SUM output of a Full Adder is thus :

$$SUM = A \oplus B \oplus C$$

The carry bit C2 (= S1 • C) generated by this Half Adder is combined with S1 to generate the final CARRY output given by the expression:

CARRY = C1 + C2

The logic for the CARRY output of a Full Adder is thus :

CARRY = A • B + S1 • C = A • B + A • C + B • C

Write down the complete truth table of a Full Adder, including columns for the intermediate outputs S1, C1 and C2, and verify the logic for the SUM and CARRY outputs of a Full Adder.

1. Set up another Half Adder using another XOR and another AND gate out of the same ICs used in step **B.1**, and connect the C input and the S1 output generated by the first Half Adder as its inputs to generate the final SUM output and the C2 output.
2. Verify that the logic for CARRY can also be implemented with an XOR gate (i.e. CARRY = C1 ⊕ C2), thereby eliminating the need for a separate OR chip and making the complete realisation of the Full Adder possible using two IC chips. Generate the final CARRY output from the intermediate carry outputs C1 and C2, using one of the unused gates in the XOR chip.
3. Verify the truth table experimentally by applying the inputs A, B and C through three input switches and displaying the S1, C1, C2, SUM and CARRY outputs.

Part D. Binary Full Subtractor using Gates

A binary Full Subtractor subtracts the Subtrahend bit B and a Borrow-in bit C from the Minuend bit A to generate DIFFERENCE and BORROW bits as output. Write down the complete truth table of a Full Subtractor and verify that the DIFFERENCE and BORROW outputs are given by the following logic expressions:

DIFFERENCE = A ⊕ B ⊕ C and

BORROW = A' • B + A' • C + B • C

Thus the DIFFERENCE output of a Full Subtractor has the same logic as that of the SUM output of a Full Adder, and the BORROW output of a Full Subtractor can be obtained from the CARRY output of a Full Adder simply by replacing A by A'.

1. Use the last remaining gate in the given XOR chip to generate A', and modify the Full Adder circuit appropriately for performing subtraction.
2. Verify the truth table experimentally by applying the inputs A, B and C through three input switches and displaying the DIFFERENCE and BORROW outputs on LEDs.