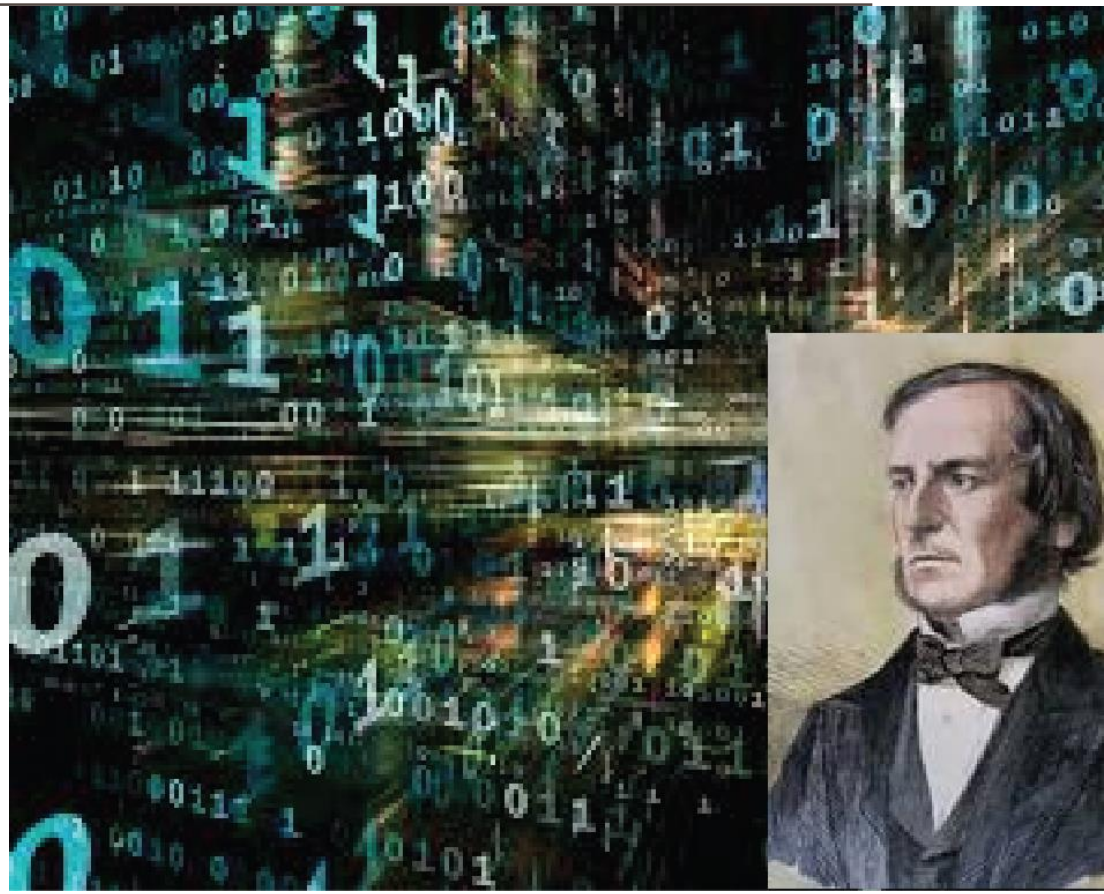
DIGITAL CIRCUITS

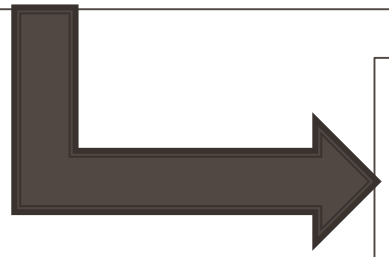
Week-11, Lecture-3
Sequential Circuits



Sneh Saurabh
26th October, 2018

Digital Circuits: Announcements/Revision

Sequential Circuits



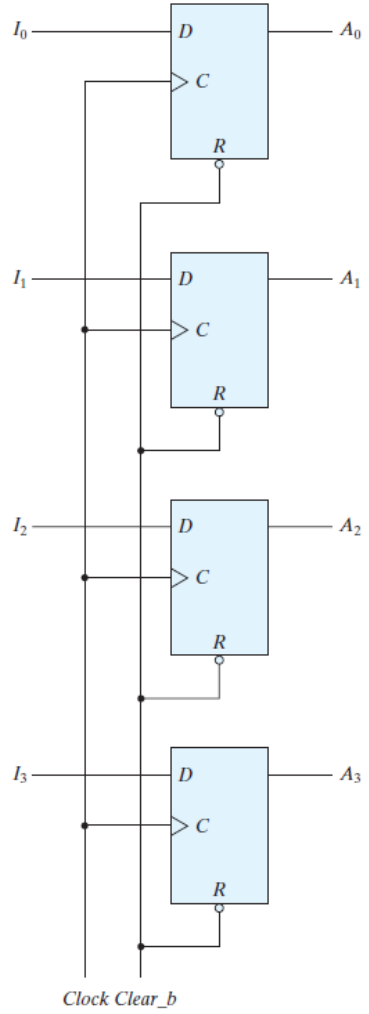
Registers and Counters

Registers

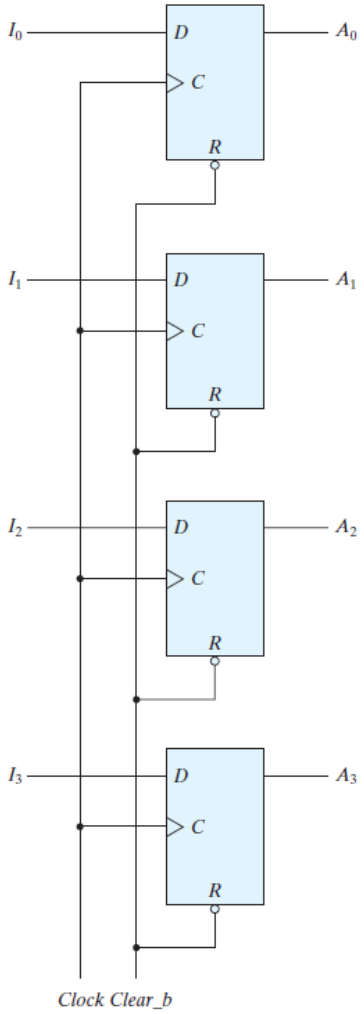
- A register is a **group of flip-flops** each one of which share a **common clock**
- An **n-bit register** consists of a group of n flip-flops capable of storing n bits of binary information

- In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks

- A **synchronous counter** is also a register that goes through a pre-defined sequence of binary states



Registers: Problem of naïve implementation



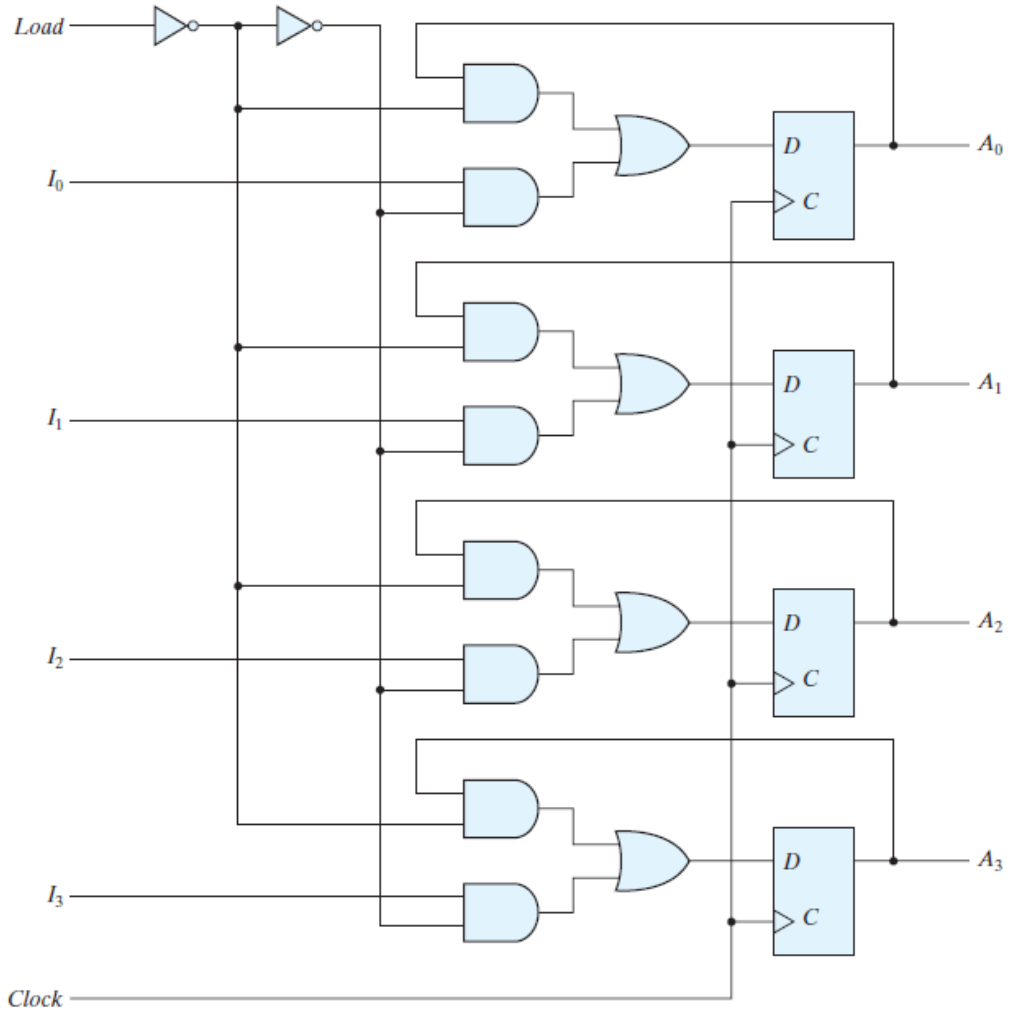
How to keep the contents of the register unchanged (A_0, A_1 …)?

- ➢ Keep inputs (I_0, I_1 …) unchanged
- ➢ Disable clock
- ✓ Provide another signal that decides whether to change the content or not

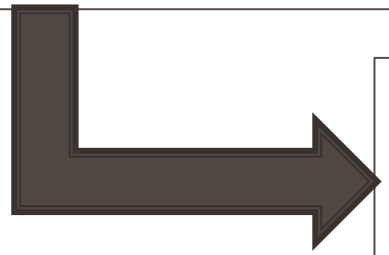
Register with parallel load

- The transfer of **new information** into a register is referred to as ***loading*** the register
- A separate control signal ***Load*** decides whether the register will be loaded or not

- $Load = 1$, Inputs (I_0, I_1 …) connected to D
- $Load = 0$, Outputs (A_0, A_1 …) connected to D



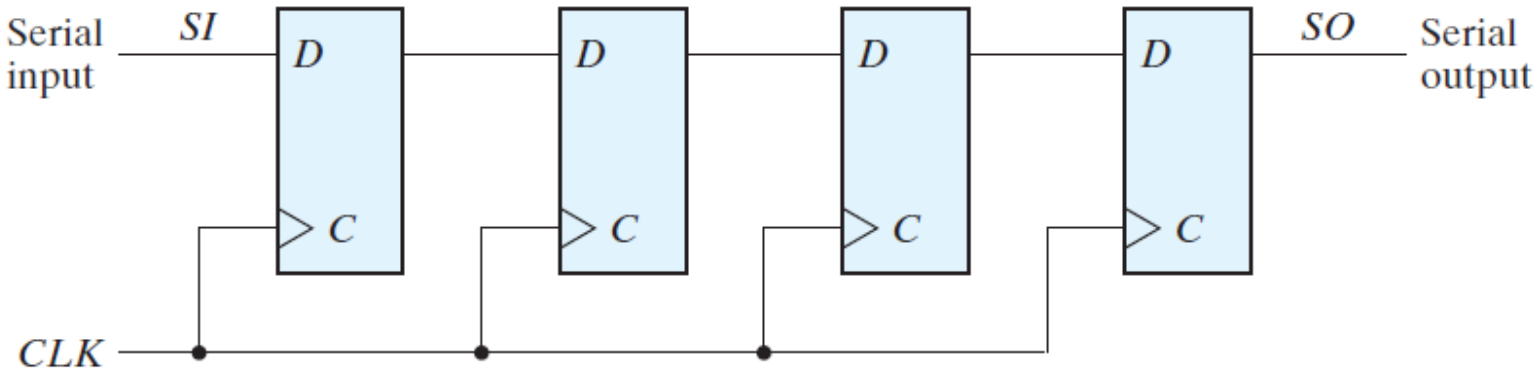
Sequential Circuits



Shift Registers

Shift Register

- **Shift Register**: A register capable of shifting the binary information held in each cell to its neighboring cell (in a particular direction)



- The output of a given flip-flop is connected to the D input of the flip-flop at its right
- This shift register is unidirectional (left-to-right)

- *SI* decides what goes into left-most bit
- The outputs appear serially on the port *SO*

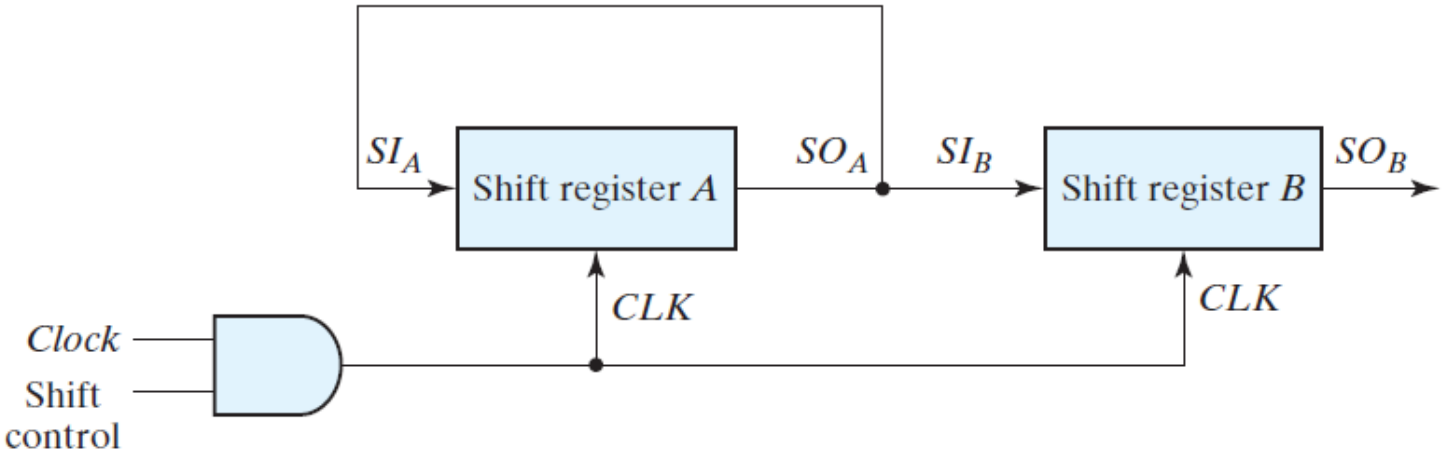
Shift Register: Serial vs. Parallel Mode

Two modes of data transfer

1. **Serial Mode**: Information is transferred and manipulated **one bit at a time** by shifting the bits out of the source register and into the destination register

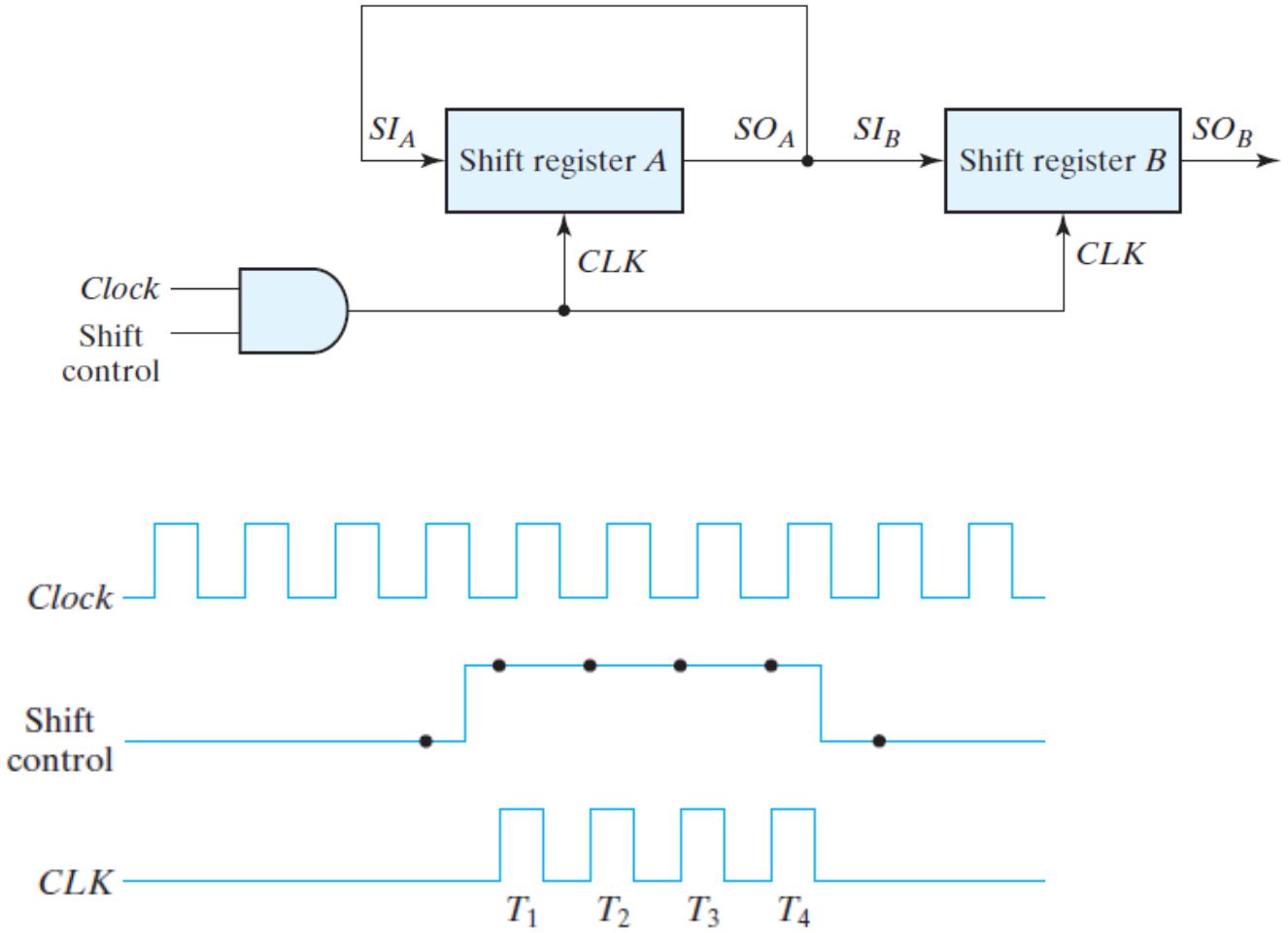
2. **Parallel Mode: All the bits** of the register are transferred at the same time

Shift Register: Serial Mode



- Serial Out (SO_A) of register A is connected to Serial In (SI_B) of register B
- To prevent data loss: Output of register A is recirculated (SO_A connected to SI_A)
- Shift controls when the clock signal ($Clock$) is applied

Serial Mode: Timing Diagram (Problem)



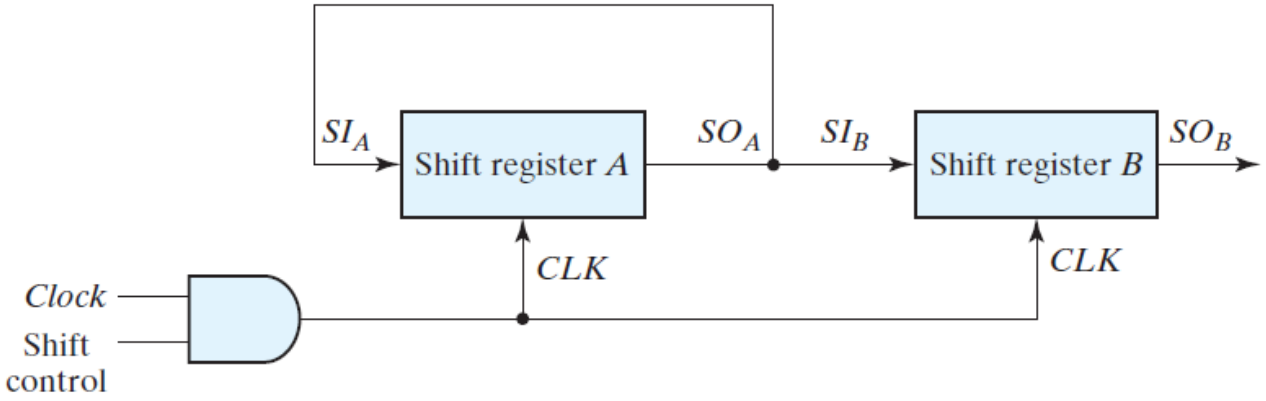
Problem:

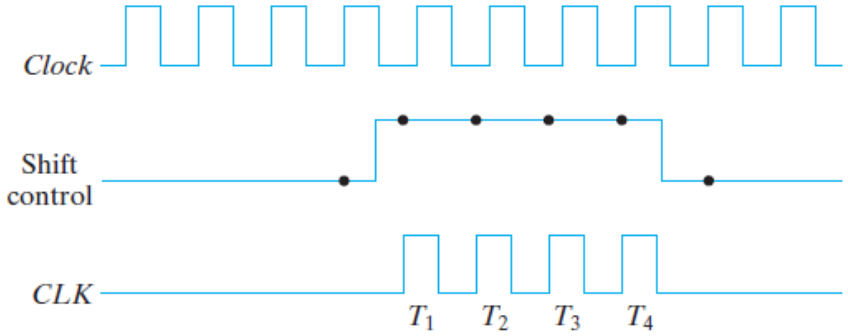
Assume that the shift registers consists of four bits.

Assume that initially Register A has bit pattern: 1011 and Register B has bit pattern: 0010.

Find out the bit pattern in Register A and B after Clock Pulse T_1, T_2, T_3 and T_4.

Serial Mode: Timing Diagram (Solution)



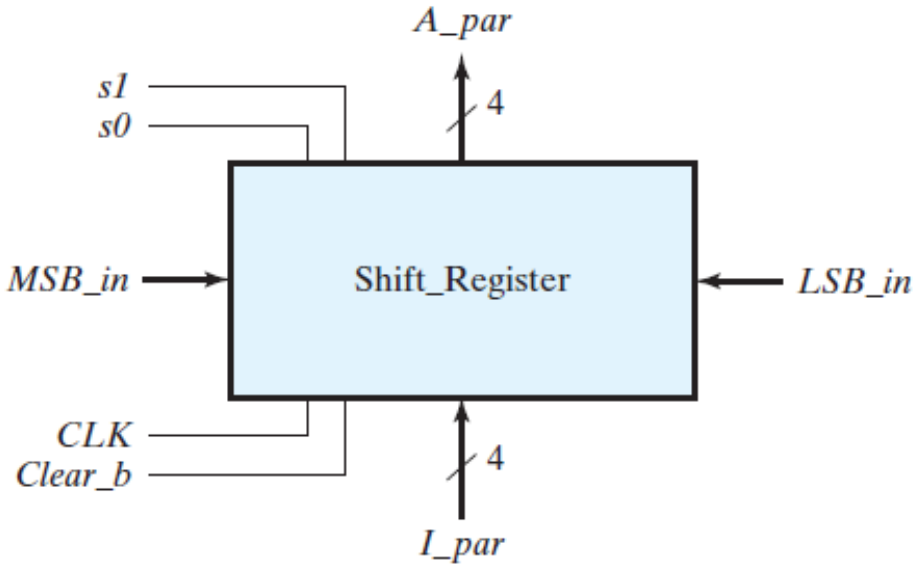


Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

Universal Shift Register: Functionality

- Unidirectional/Bi-directional shift registers:
  - A register capable of shifting in one direction only is a unidirectional shift register.
  - One that can shift in both directions is a bidirectional shift register.

- If the register has both shifts and parallel-load capabilities, it is referred to as a ***universal shift register***



Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Universal Shift Register: Implementation