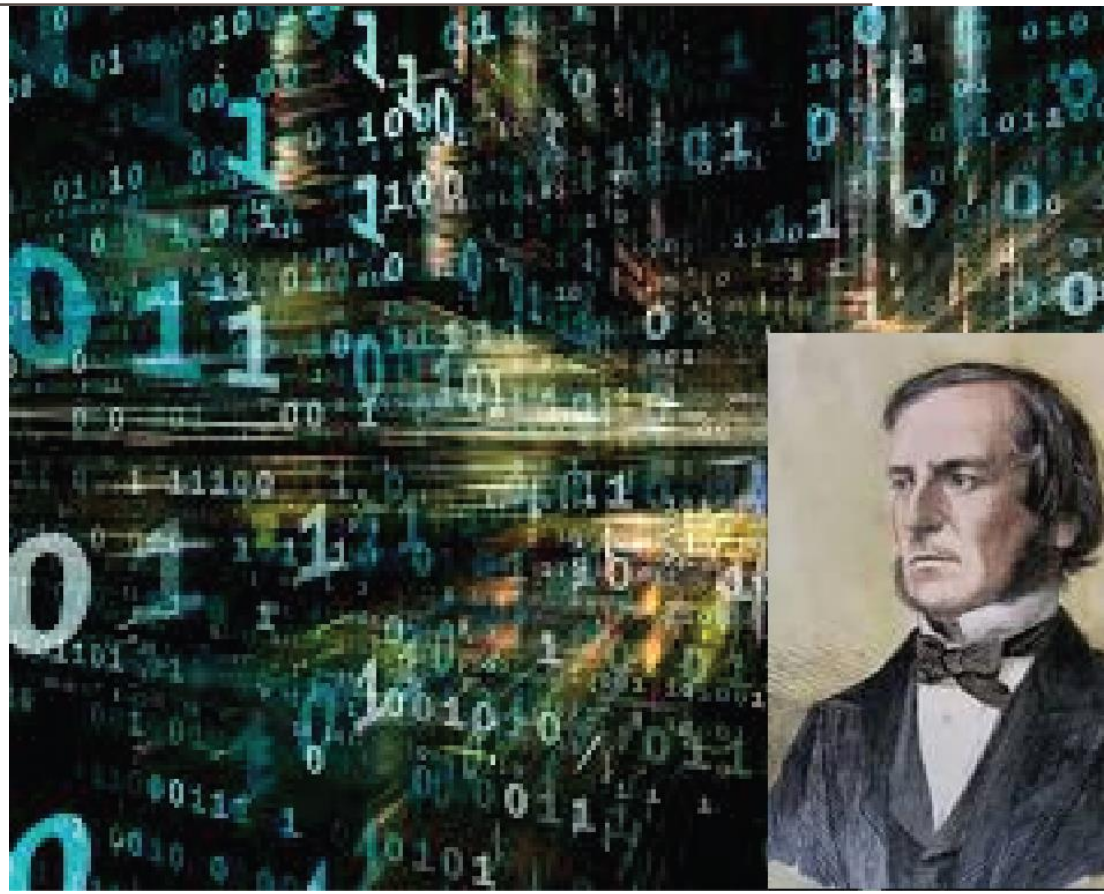
DIGITAL CIRCUITS

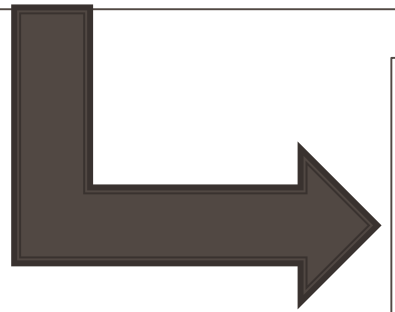
Week-10, Lecture-2
Sequential Circuits



Sneh Saurabh
10th October, 2018

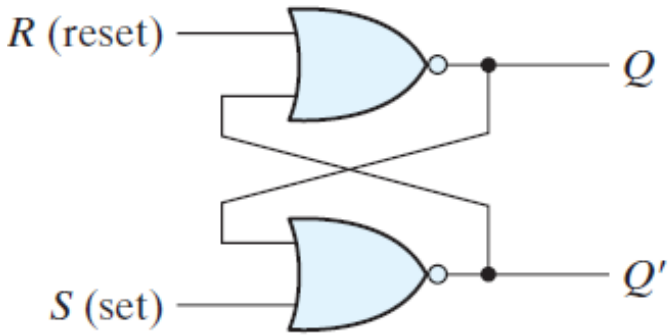
Digital Circuits: Announcements/Revision

Sequential Circuits



Latches

SR Latch: Basics

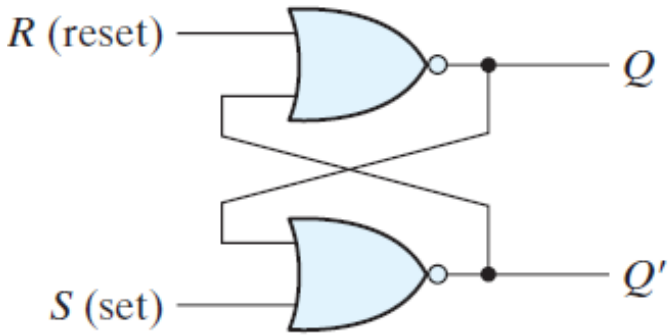


Can you derive function table for an SR Latch?

- **Set State**: When output $Q = 1$ and $Q' = 0$
- **Reset State**: When $Q = 0$ and $Q' = 1$
- Outputs Q and Q' are normally the ***complement*** of each other

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

SR Latch: Normal operation (Set State)



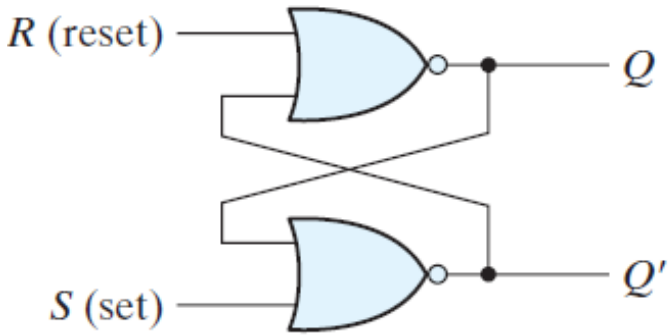
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

- Under normal conditions $S = R = 0$ unless the state has to be changed

Reaching Set State:

- The application of a momentary $S = 1$ causes the latch to go to the ***set state***
  - Then $S = 0$ is made before any other changes take place, to avoid forbidden input condition ($S = R = 1$)
  - When S goes back to 0, the latch still remains in the set state (**memory action**)

SR Latch: Normal operation (Reset State)



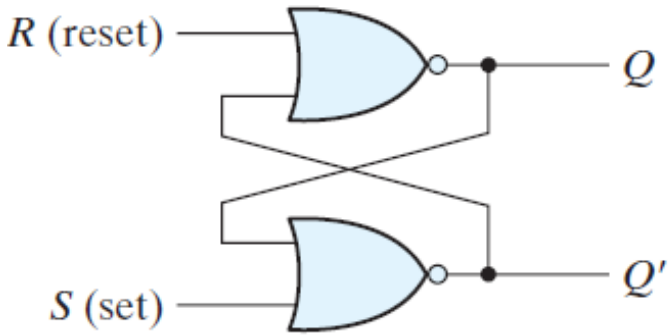
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

Reaching Reset State:

- After $S = R = 0$, it is possible to go to the ***reset state*** by momentarily applying a $R = 1$
- Then $R = 0$ is made, and the latch still remains in the reset state

- When $S = R = 0$, the latch can be in either the set or the reset state, depending on **which input was most recently a 1**

SR Latch: Forbidden State

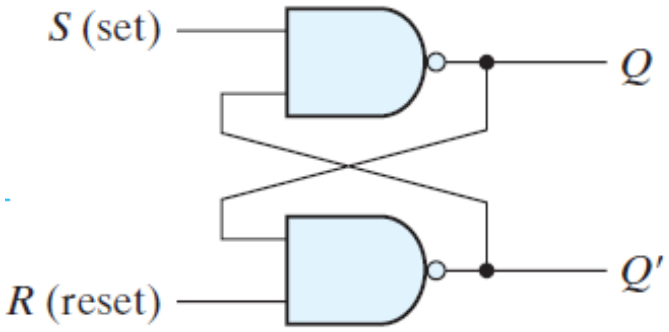


S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

Forbidden state:

- When $S = R = 1, Q = Q' = 0$
  - ➢ Both outputs are equal to 0 (rather than be mutually complementary)
- **Race condition**: In the forbidden state, if both inputs are switched to $S = R = 0$ simultaneously, the device will enter an unpredictable or undefined state
- In practical applications, setting both inputs to 1 is forbidden

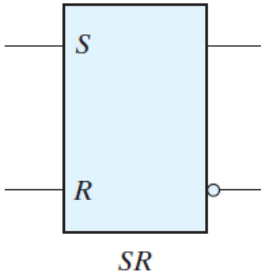
SR Latch: Active Low

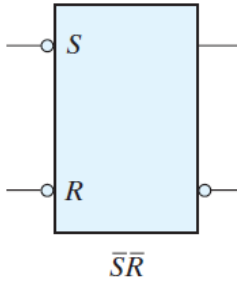


Can you derive function table for an NAND-based SR Latch?

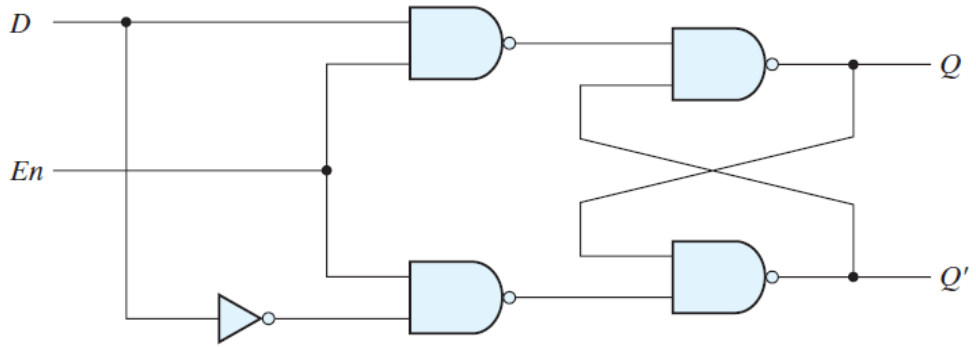
- Input signals for the NAND-based latch requires the complement of those values used for the NOR-based latch
- Because the NAND latch requires a 0 signal to change its state, it is sometimes referred to as an $S'R'$ latch or $\bar{S}\bar{R}$ latch (primes indicate active low)

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)





D Latch (Transparent Latch): Basics



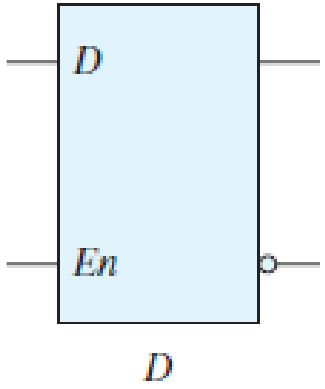
- Most widely used latch is D latch for circuit applications
- Eliminates reaching forbidden state in the SR latch by ensuring that inputs S and R are never equal to 1 at the same time

Can you derive function table for an SR Latch with Enable?

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

En	D	Next state of Q
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

D Latch (Transparent Latch): Functionality

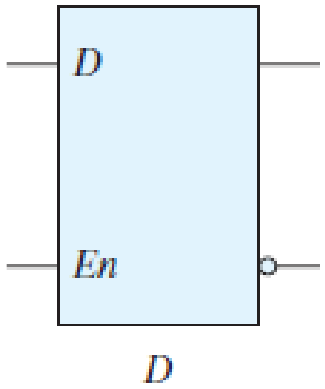


En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

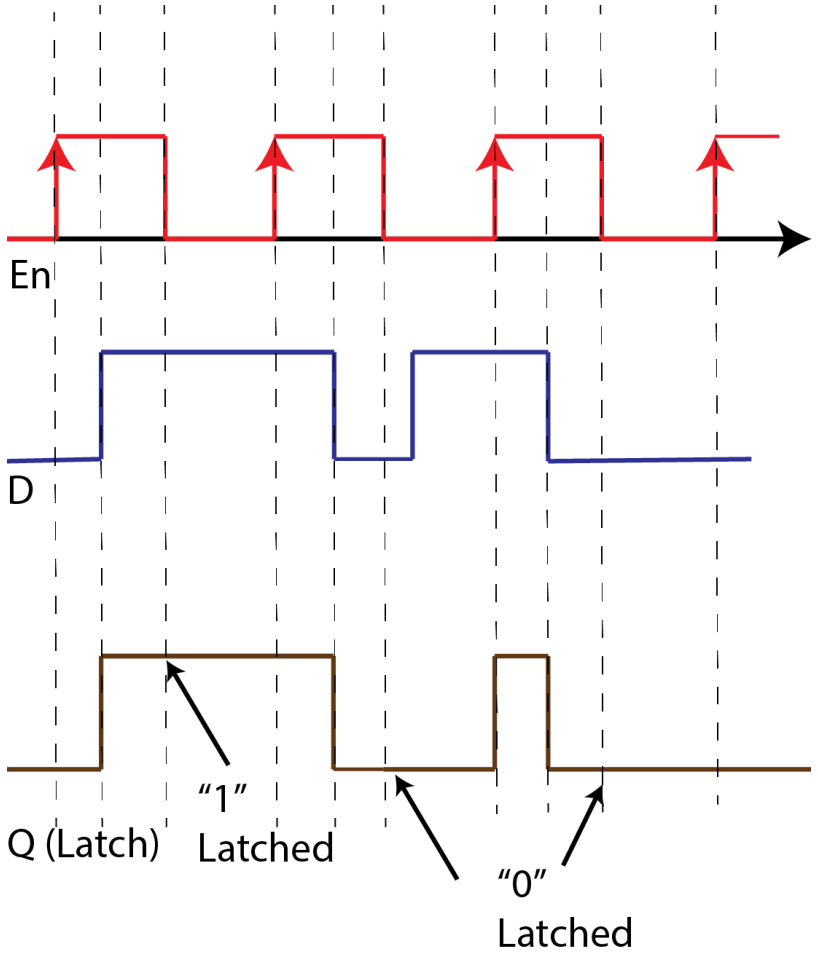
- The D latch holds data in its internal storage
- The binary information present at the data input of the D latch is transferred to the Q output when the enable input is asserted.
- **Transparent latch:** The output follows changes in the data input as long as the enable input is asserted

- When $En = 0$, the binary information that was present at the data input at the time the transition occurred is retained (i.e., stored) at the Q output [Memory Action]

D Latch (Transparent Latch): Illustration

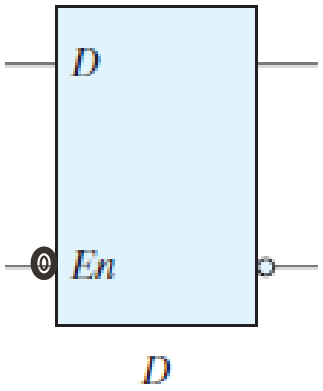


En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state



D Latch (Transparent Latch): Active Low Enable

- An inverter can be placed before the En pin
- D Latch is enabled when $En = 0$



Problem: Assuming that the latch is active low enabled, draw the waveform at the Q-pin of the D latch