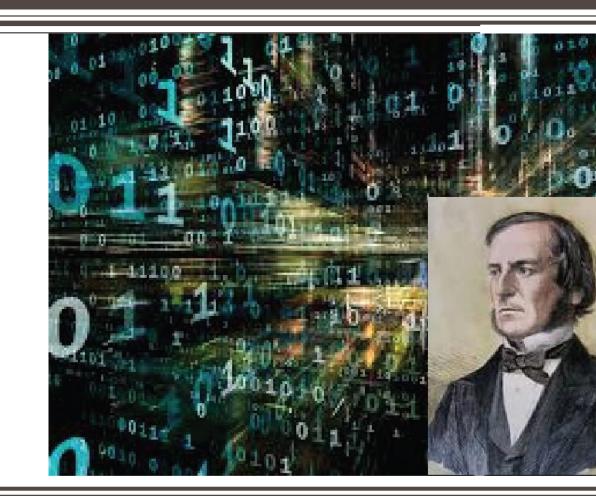
## DIGITAL CIRCUITS

Week-1, Lecture-1 Introduction

Sneh Saurabh 1<sup>st</sup> August, 2018

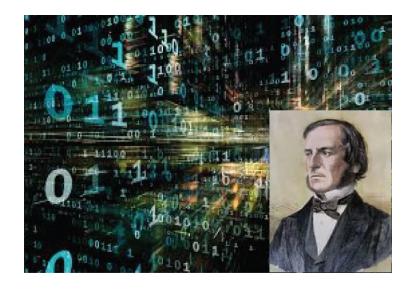


# About the Course

### Digital Circuits: Objectives

### **Learning Digital Logic Design**

- ➤ Get introduced to Signal Representation, Boolean Algebra, Logic Gates and Design with Logic Gates.
- ➤ Be familiar with designing Combinational and Sequential Circuits
- > Get introduced to the concept of Pipelining

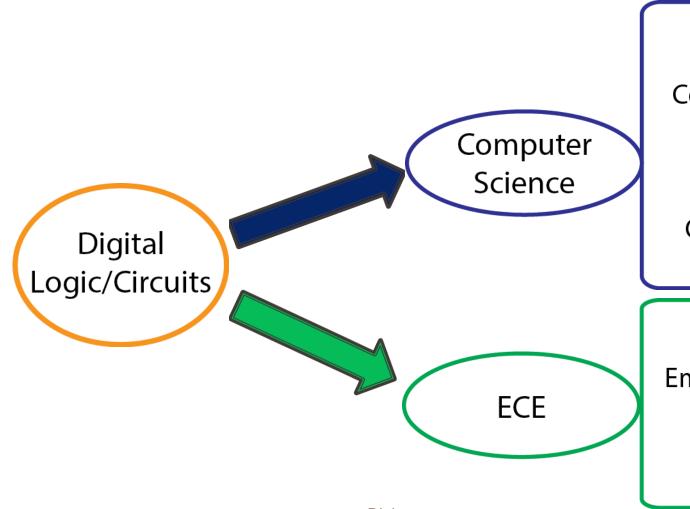


### Digital Circuits: Expected Outcome

- > Translate a decision-making process into digital logic
- Understand Number System and circuits realizing Arithmetic operations
- Design simple digital circuits based on combinational logic and sequential logic
- ➤ Design Asynchronous and Synchronous counters and Shift Registers.
- ➤ Understand the concept of State Machines.
- ➤ Understand the concept of Pipelining



## Digital Circuits: Where to apply the learning?



Programming
Machine Learning
Computer Organization
Networks
Artificial Intelligence
Verification
Quantum Computing
Compilers

VLSI Embedded Logic Design Signal and Systems Communications

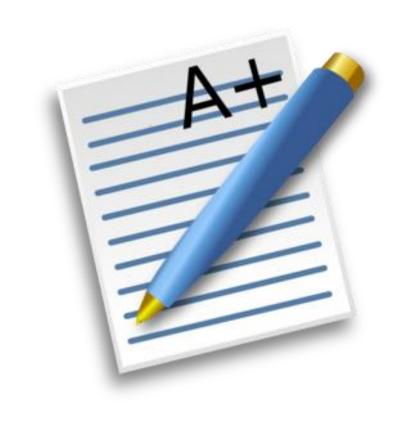
••••

# Digital Circuit: Course Content

Week No.	Topic
	Analog and Digital Representation of Information, Data vs. Signal, Information Processing Steps: Logic and Arithmetic (2hrs)
Week 1-2	Binary variables; Basic logic operations – AND, OR, NOT; Basic gates; Essentials of Boolean algebra; De Morgan's laws; Truth Table; Boolean functions; (4hrs)Transforming a logical problem statement into a Boolean expression.(4 hrs)
	Positional number systems – Binary, Decimal, Octal, Hexadecimal; Signed number representations; Arithmetic operations.(4 hrs)
Week 4, 5,	Realisation of Boolean functions using gates; Karnaugh map; Minimisation of Boolean functions; Multiplexer-based realisation of K-maps; Combinational circuit design using multiplexers and gates. ALU (11 hrs)
9 and 10	Latches and Flip-flops; Ripple counters; Sequence generator using flip-flops; State Table and State Diagram; Synchronous counters; Shift Registers; Ring and MLS counters.(10 hrs)
	Pipelining: Pipelining with Edge Triggered Flip Flop, Pulse Triggered Flip Flop and Latches. Introduce the concepts of Skew and Jitter (9 hrs)

# Digital Circuits: Evaluation Criteria

Type of Evaluation	Contribution in Grade
Mid-semester Exam	20 %
Final Exam	40 %
Assignments	10 %
Labs	15 %
Quiz (Best (N-1) out of N)	15 %



### Responsibilities

➤ Lecture: Instructor

➤ Tutorial: Instructor+Teaching Assistants (TAs)

➤ Quizzes/Theory Exams: Instructor

➤ Assignments: TAs

➤ Labs: Teaching Fellows (TFs)

### Plagiarism !!!

- Plagiarism: offence of taking undue credit for someone else's work.
- We follow Zero tolerance policy against plagiarism!
- https://www.iiitd.ac.in/sites/default/files/docs/education/Aca demicDishonesty.pdf
  - One grade reduction for first instance and report to academic department
  - 2) F grade for second instance





### Exam

### **Open Book**

- Only Book and notes written in their own handwriting (no XEROX, printouts)
- No sharing of book/notes allowed
- No laptop/mobiles/communication/storage devices allowed.



- ✓ Tutorials are for solving problems
- ✓ New problems with application of concepts are expected in exams



### **Evaluation**

Assignments: 10%

Quiz: 15% (Best N-1 out of N)

- If there is a large disparity in the marks obtained by a student in an Assignment and the Quiz following the Assignment submission, steps will be taken to check the understanding of the student with respect to the submitted assignment.
  - This may be done through a viva or another quiz (announced with a notice of less than a day) for students with large disparity in the marks obtained in an Assignment and the Quiz following the Assignment submission.
  - If such students continue to perform below par in the exploratory test, the marks in both the Assignment and the Quiz following will be made zero.
- Students with two such zeros in Assignment and Quiz will not be permitted to sit for the end-sem examination.



### Digital Circuits: Books

- Digital Design with an Introduction to the Verilog HDL M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).
- Fundamentals of Digital Logic with Verilog Design S. Brown, Z. Vranesic, Ed-3, McGraw-Hill
- References will be provided during lectures also.

### Online Resources

- 1. <a href="https://www.youtube.com/playlist?list=PLDFF5A99731ECFC6C">https://www.youtube.com/playlist?list=PLDFF5A99731ECFC6C</a>
- 2. <a href="https://www.youtube.com/playlist?list=PLB52B8F4E464CEEF7">https://www.youtube.com/playlist?list=PLB52B8F4E464CEEF7</a>
- 3. <a href="https://www.youtube.com/playlist?list=PL803563859BF7ED8C">https://www.youtube.com/playlist?list=PL803563859BF7ED8C</a>
- 4. <a href="https://www.youtube.com/channel/UCbl7mdq1mJidoe8pcRAnTbw/videos">https://www.youtube.com/channel/UCbl7mdq1mJidoe8pcRAnTbw/videos</a>.

## Usebackpack

### Register yourself on https://www.usebackpack.com/

- Lecture will be shared
- Homework/Tutorials/Grade
- Announcements

**-** . . .

# **Policies**

### Digital Circuits: Policies (1)

- Be punctual to class
- Come to the class before the scheduled time
- Up to 5 minutes late is tolerated, beyond that please do not come

 Food, Cell phones, Laptops, IPODs, MP3 players or other portable electronic devices of any kind NOT allowed in classroom







### Digital Circuits: Expectations

- Revise last day lecture before coming
  - Revision will be done at the start of every lecture for 5 minutes
  - One student at random will be asked to revise the topics covered in the last lecture
  - You are allowed to use your own notes in the revision
  - A good review (preferably without notes)
     from the student will be AWARDED !!!

- Ask questions and be active participants
- Give feedback



### Digital Circuits: Attendance Policy

Lectures: Attendance not mandatory

#### • Tutorials:

- If attendance before mid-sem is less than 75%, you will get zero marks in one of the quizzes and it will be considered as compulsory quiz.
- If attendance after mid-sem is less than 75%, you will get zero marks in one of the quizzes and it will be considered as compulsory quiz.
- Labs: All experiments must be completed before each labexam. Otherwise, you will not be allowed to appear for lab exams.



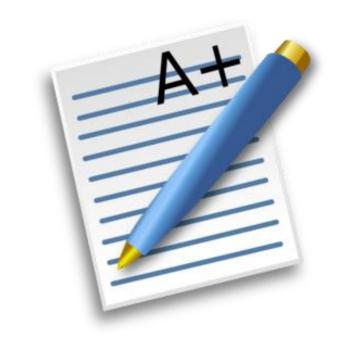
### Digital Circuits: Questions/Doubt/Office Hours

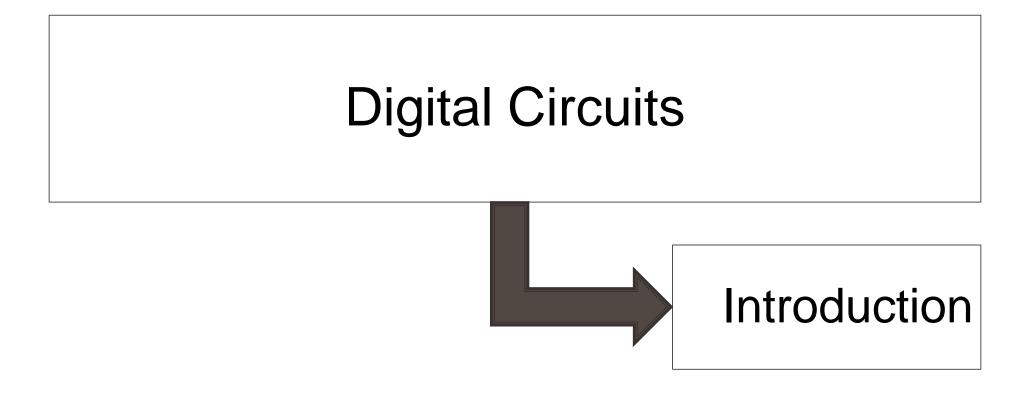
- Class: Many may have the same questions
- Just After Class
  - Will be available for some time after the class
- Before the start of the next lecture
- Office-hours
  - Monday 2:30-3:30 pm, B-608 (New Academic Building)



### Digital Circuits: Why grades are important?

- For branch change
- For good internship, placements in "good" companies, good research project, scholarship/TA'ship during BTech
- For recommendation letters: admission and scholarship for MS/PhD





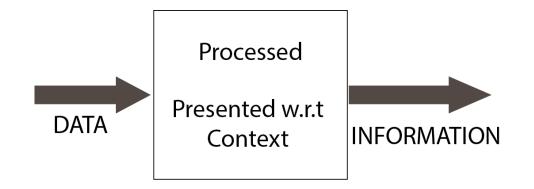
### Information

#### What is *information*?

- Data that has been processed and made meaningful or useful
- Information can be used to take decision
- Information is related to data

#### What is *data*?

Data are simply raw facts



DATA	INFORMATION
Temperature all over the world for last 100 years	Global Temperature is rising
{4, 6, 10, 5}	Runs given in 4 different overs by some player: {4, 6, 10, 5}