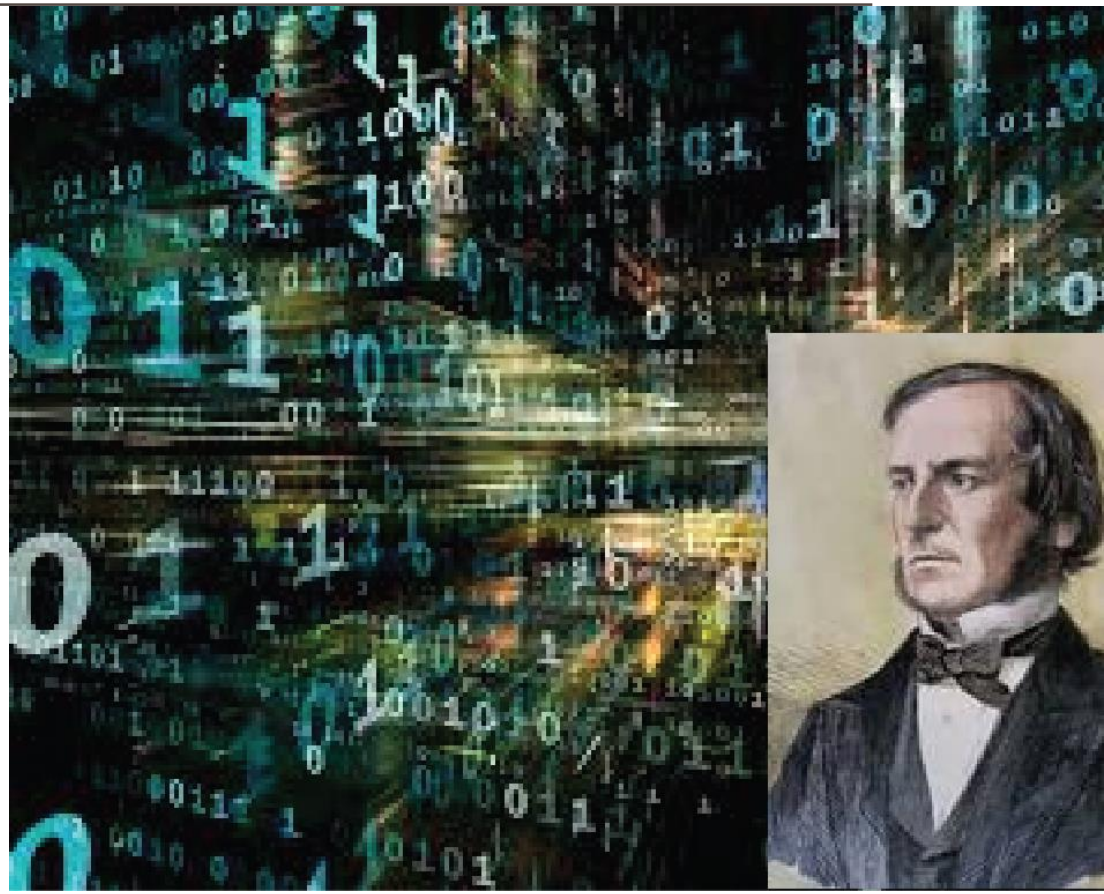
DIGITAL CIRCUITS

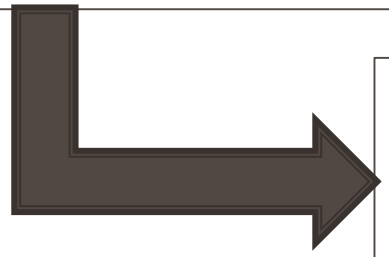
Week-12, Lecture-1
Sequential Circuits



Sneh Saurabh
30th October, 2018

Digital Circuits: Announcements/Revision

Sequential Circuits

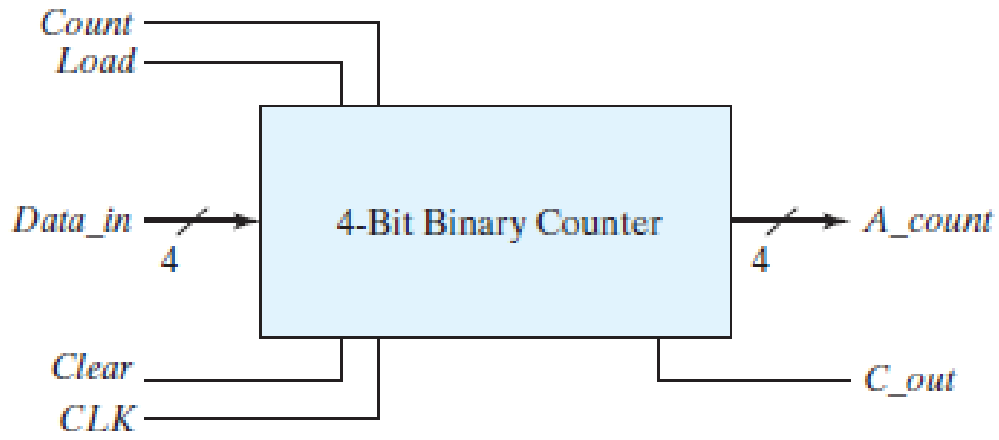


Registers and Counters

Binary Counter with Parallel Load: Operation

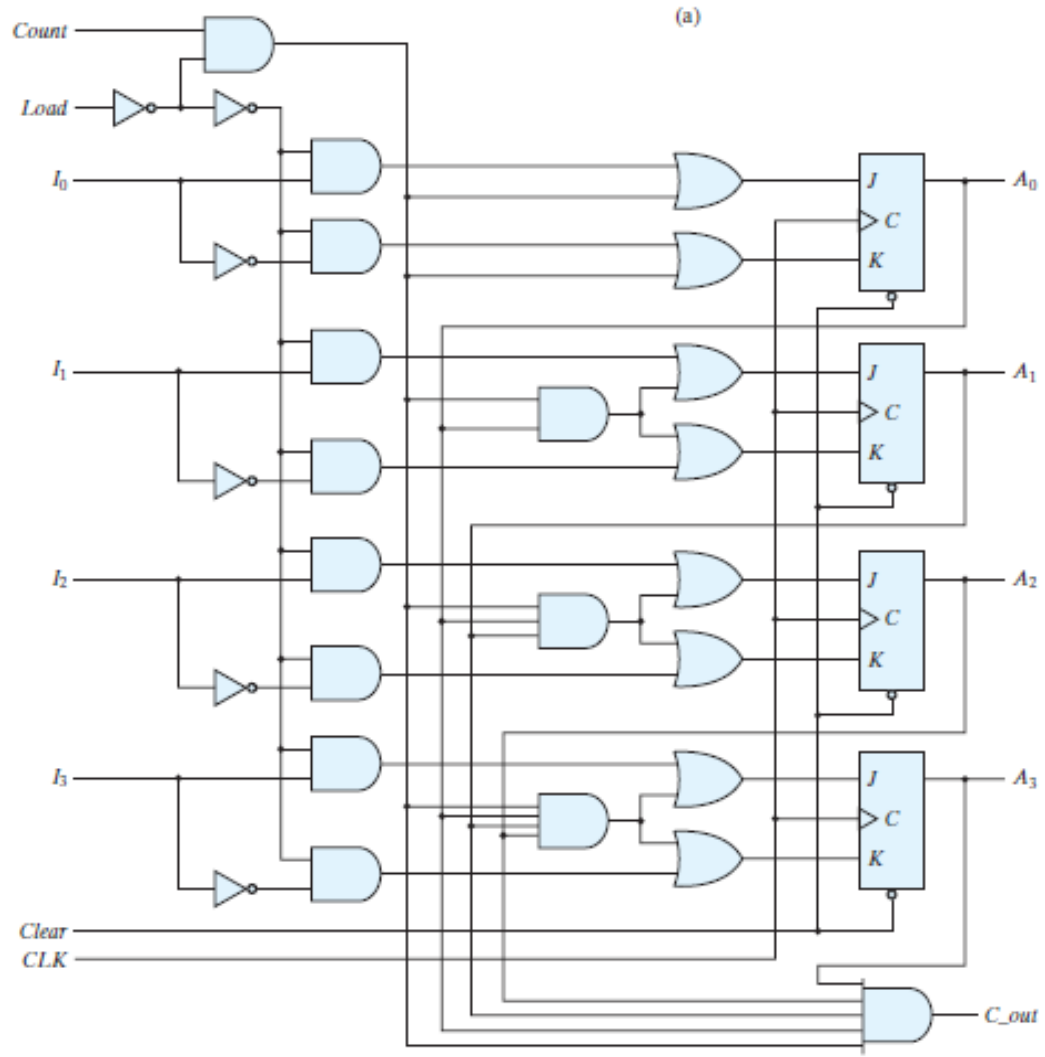
- **Parallel Load**: used for transferring an initial binary number into the counter prior to the count operation.

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



- When $Clear = 0$, the counter is cleared regardless of the presence other inputs (it is asynchronous)
- When $Load = 1$, data from $Data\_in$ is transferred to A_count
- When $Count = 1$, circuit behaves as counter
- If both control inputs are 0, clock pulses do not change the state of the register.

Binary Counter with Parallel Load: Implementation



Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

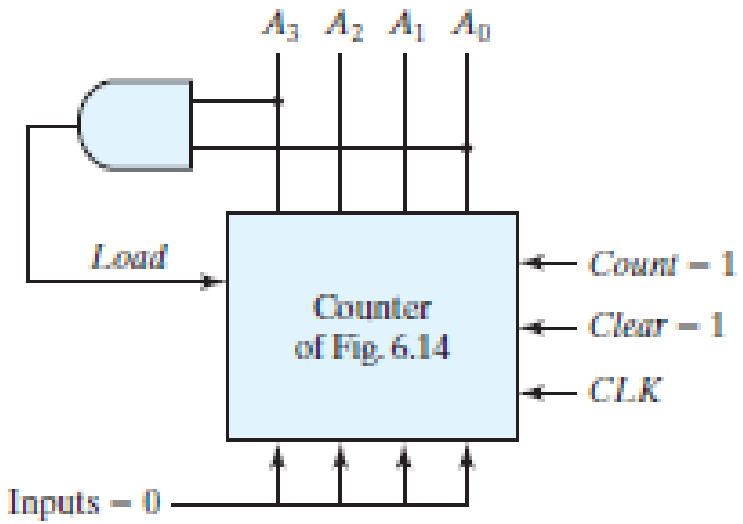
- The carry output becomes a 1 if all the flip-flops are equal to 1 while the count input is enabled.
- This is the condition for complementing the flip-flop that holds the next significant bit.
- The carry output is useful for expanding the counter to more than four bits.

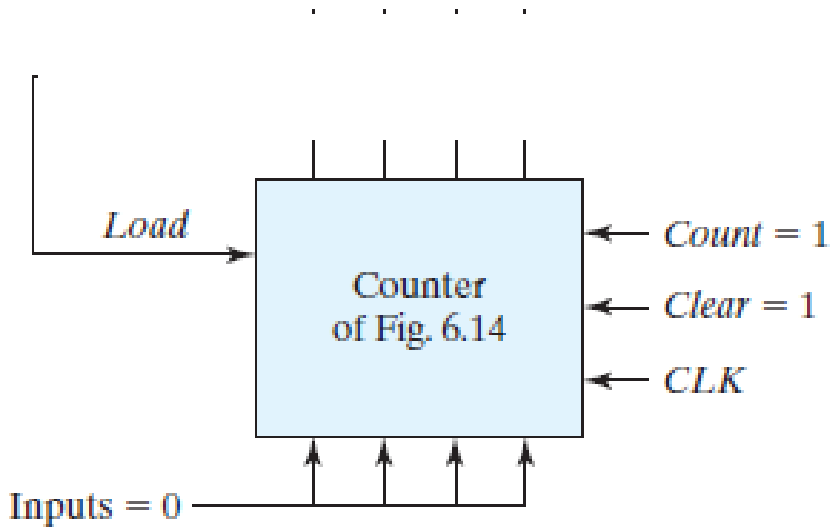
Binary Counter with Parallel Load: Application

Problem:

Implement a ***BCD counter*** by modifying the counter with a parallel load shown alongside.

BCD Counter: counts from 0000 to 1001 and then back to 0000.



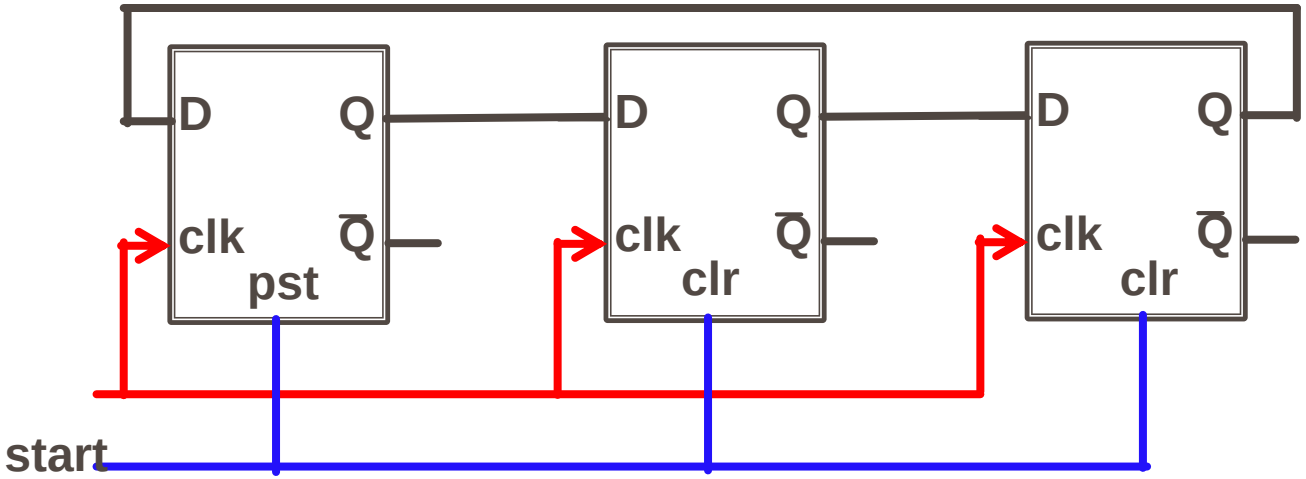


- When the output reaches the count of 1001, both A0 and A3 become 1, making the output of the AND gate equal to 1.
- This condition activates loads 0000 on the next clock edge

Ring Counter: Functionality

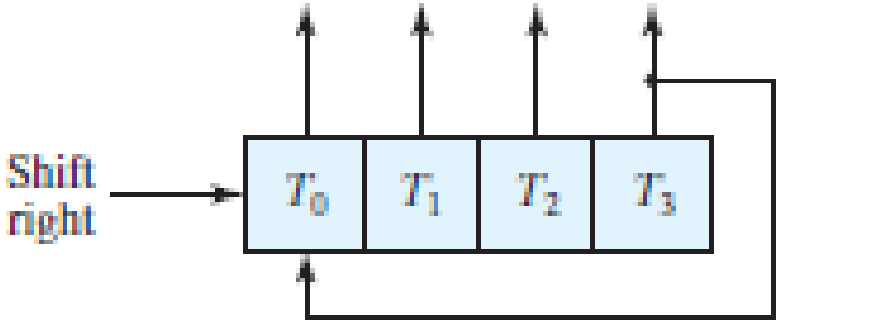
- A ring counter is a circular shift register with only one flip-flop being set at any particular time; all others are cleared.
- The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals.

- For a four-bit ring counter, the states would be 1000, 0100, 0010 and 0001.

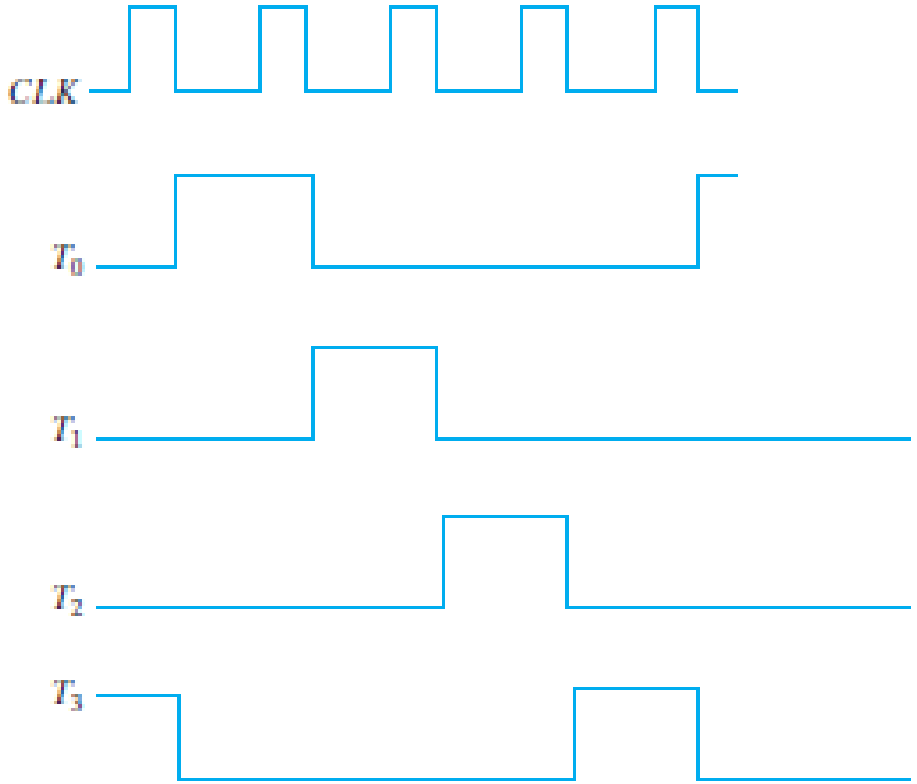


A	B	C
1	0	0
0	1	0
0	0	1
1	0	0
0	1	0
0	0	1

Ring Counter: Four bit



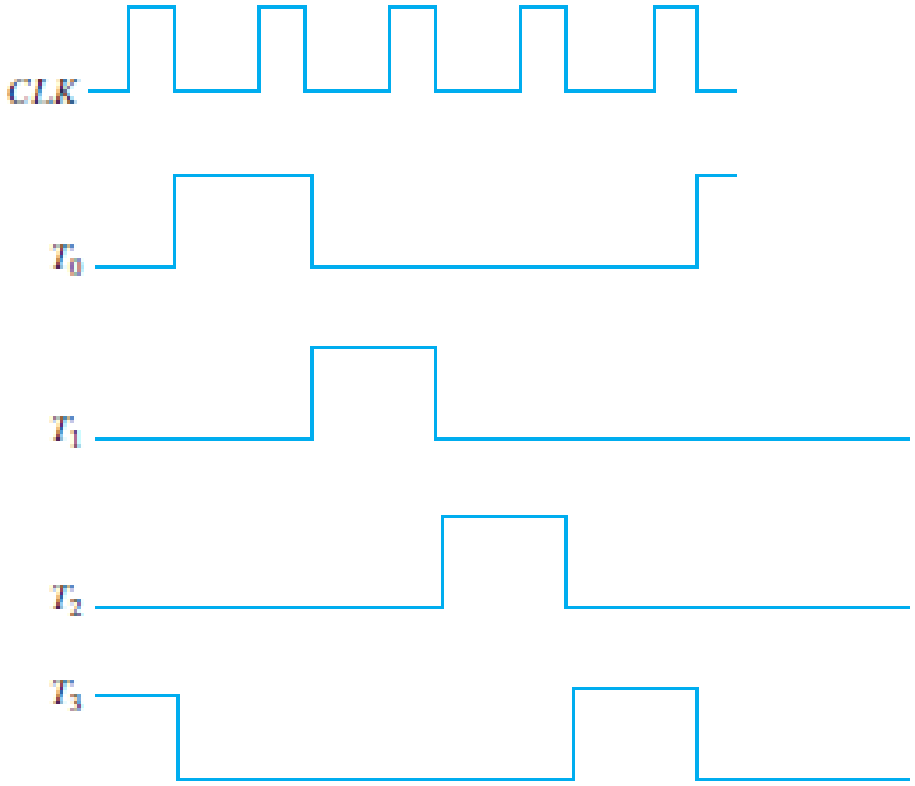
(a) Ring-counter (initial value = 1000)

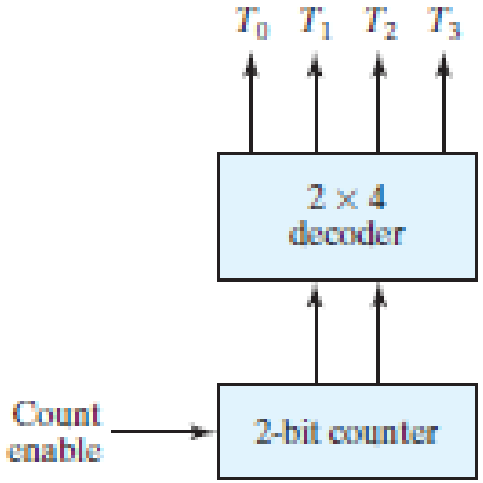


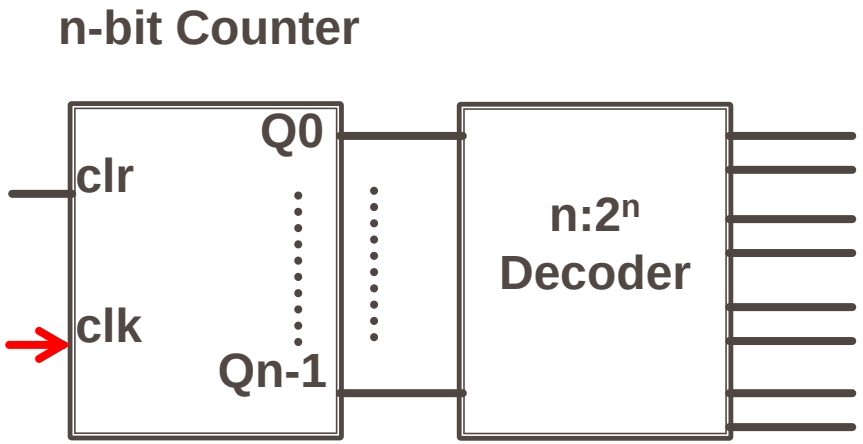
- **Modulus of a counter**: Number of the states that the counter counts before repeating itself

- **Ring counter**: Can be used to implement counter of any modulus

Ring Counter: Using decoder







Johnson Counter: Functionality

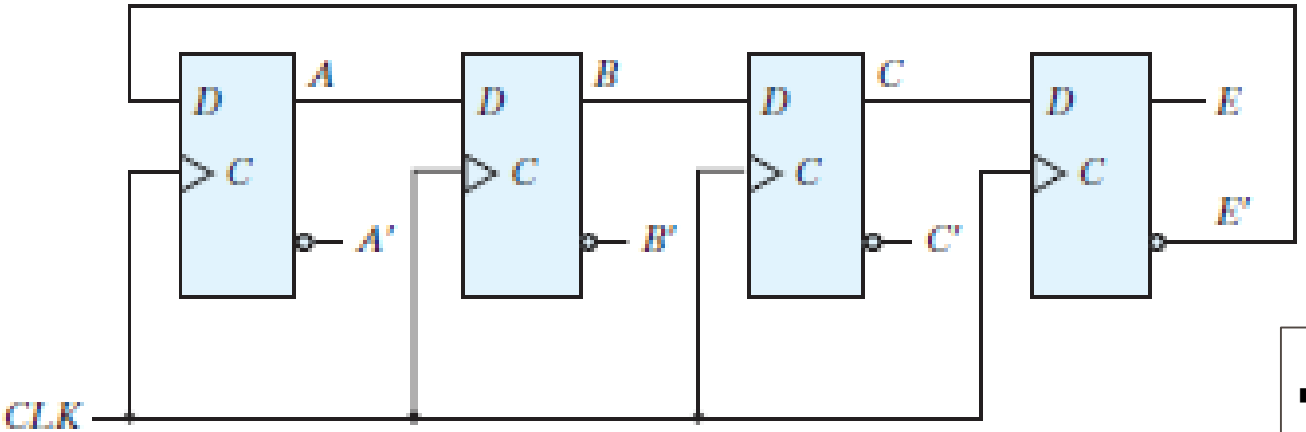
Ring Counter:

- N-flip flops have N states (mod N counter)
- For a four-bit ring counter, the states would be 1000, 0100, 0010 and 0001.

Johnson Counter:

- N-flip flops have 2N states (mod 2N counter)
- Obtained by switch-tail ring counter configuration
- Shift register with the complemented output of the last flip-flop connected to the input of the first flip-flop
- For four flip-flop Johnson counter there will be eight states

Johnson Counter: Four bits

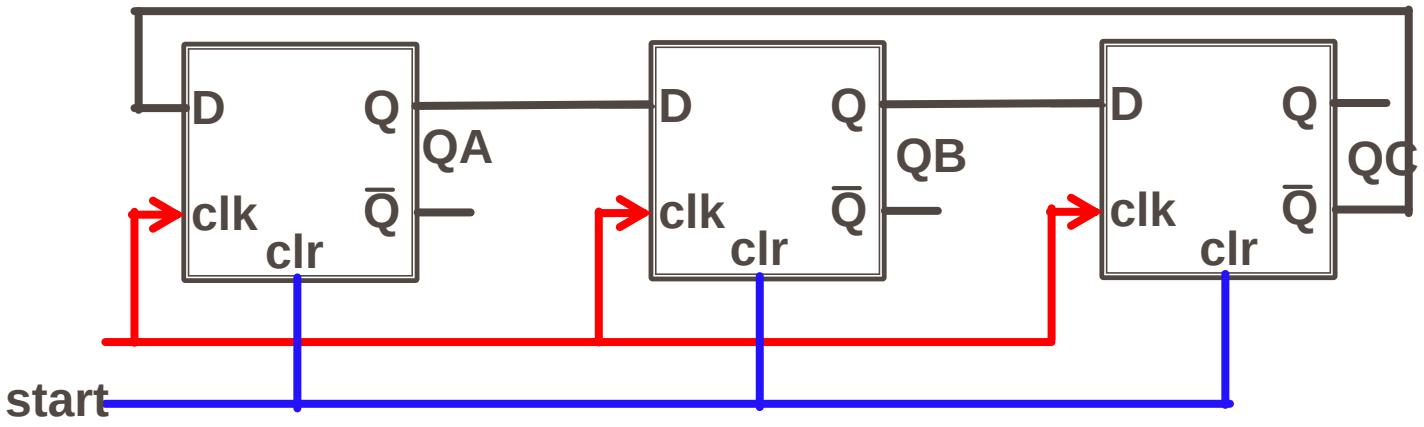


Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

- Each gate is enabled during one particular state sequence

- An N-bit Johnson counter can be used to provide outputs for 2N timing signal (using 2N decoding gates)

Johnson Counter: Problem-1

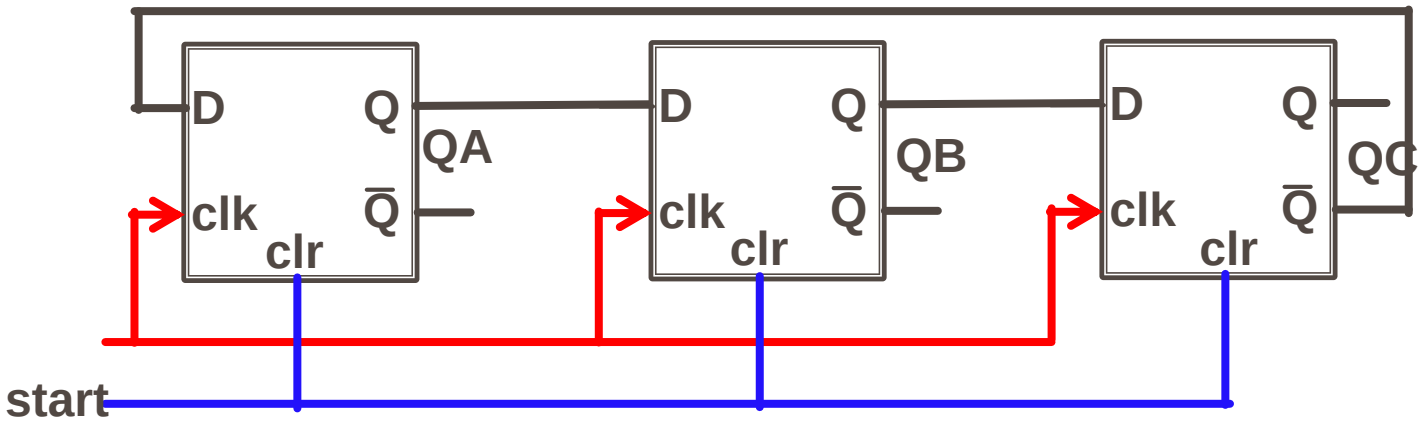


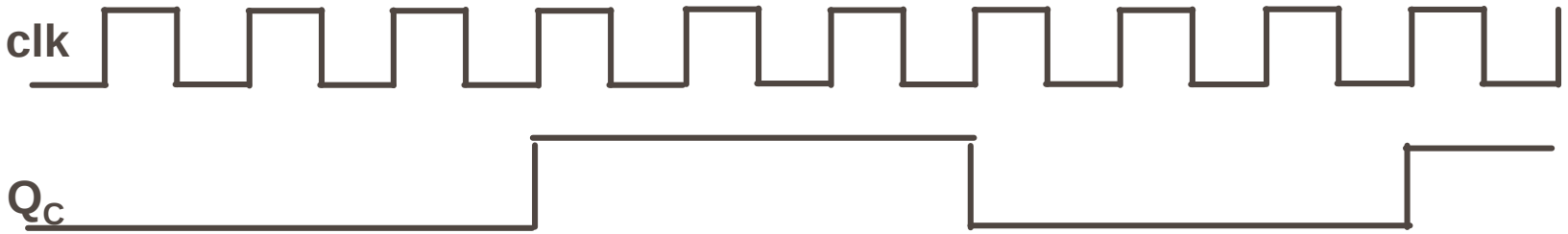
Problem:

Starting with the state {0,0,0} at 0^{th} clock cycle, find the states in subsequent clock cycles.

QA	QB	QC
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0

Johnson Counter: Frequency divider





$$F0 = Fclk/6$$

QA	QB	QC
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0