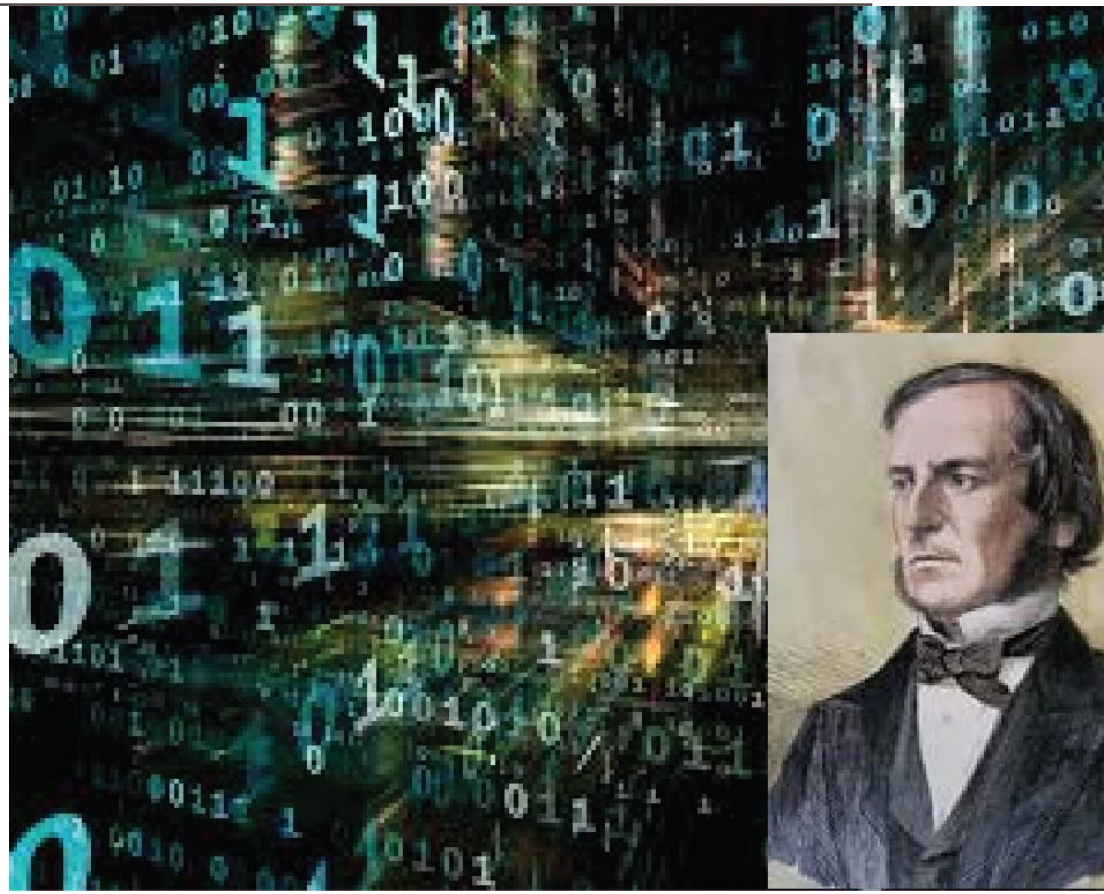
DIGITAL CIRCUITS

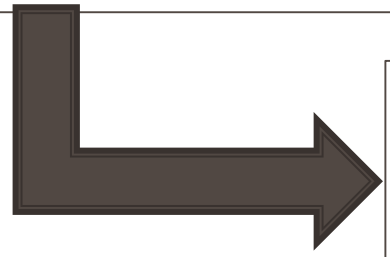
Week-14, Lecture-1
Sequential Circuits



Sneh Saurabh
13th November, 2018

Digital Circuits: Announcements/Revision

Sequential Circuits



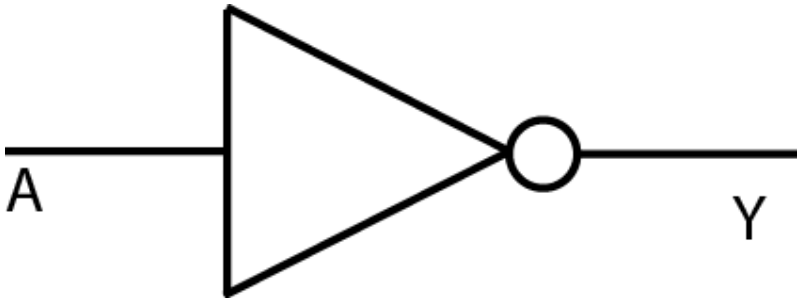
Pipelining

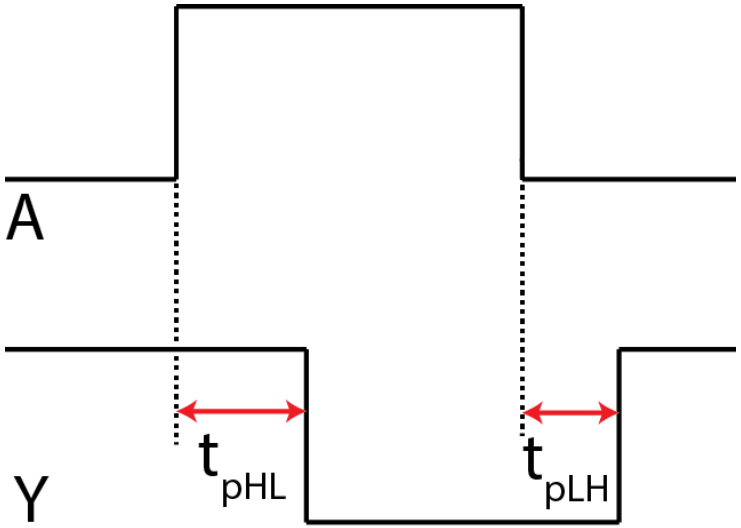
Concept of Delay

Delay: Basic concept

- When the input to a logic gate is changed, the output **does not change instantaneously**
- The ***transistors*** or other switching elements within the gate take a finite time to react to a change in input
  - ➢ Time to react depends on electrical characteristics such as ***capacitance*** and ***resistance***
  - ➢ The change in the gate output is **delayed** with respect to the input change

Delay: Inverter (Simple model)





- For a transition from 1 (High) to 0 (Low), the change in output is delayed by t_{pHL}
  - t_{pHL} is called High to Low ***Propagation delay***

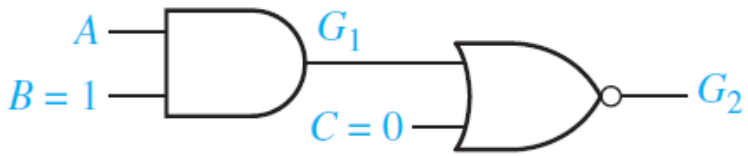
- For a transition from 0 (Low) to 1 (High), the change in output is delayed by t_{pLH}
  - t_{pLH} is called Low to High ***Propagation delay***

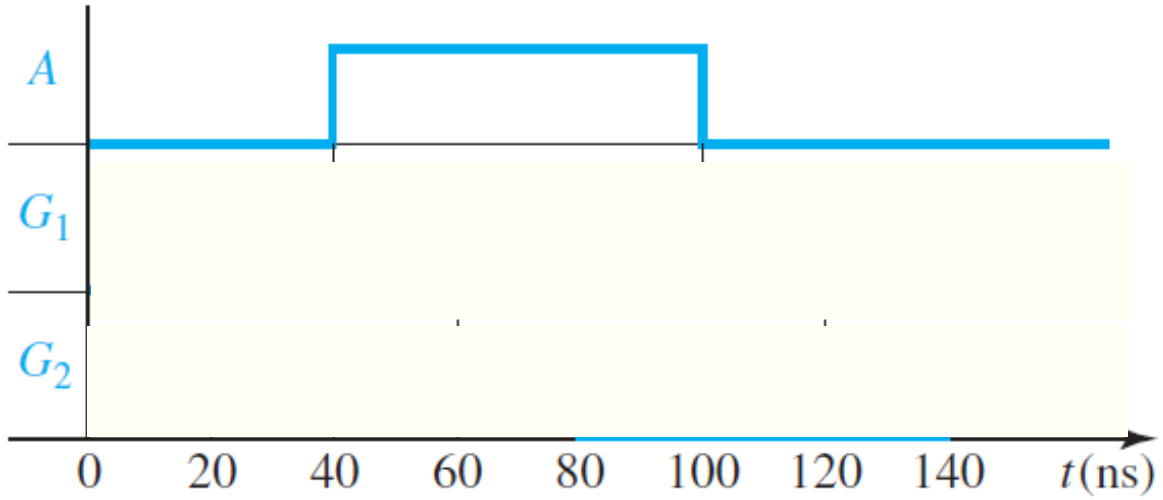
- In general, $t_{pHL} \neq t_{pLH}$
- Sometime average of t_{pHL} and t_{pLH} is specified as propagation delay t_p
- $t_p = \frac{t_{pHL}+t_{pLH}}{2}$
- During analysis of a circuit, in this case for both transitions the same propagation delay t_p can be taken

Delay: Timing Diagram

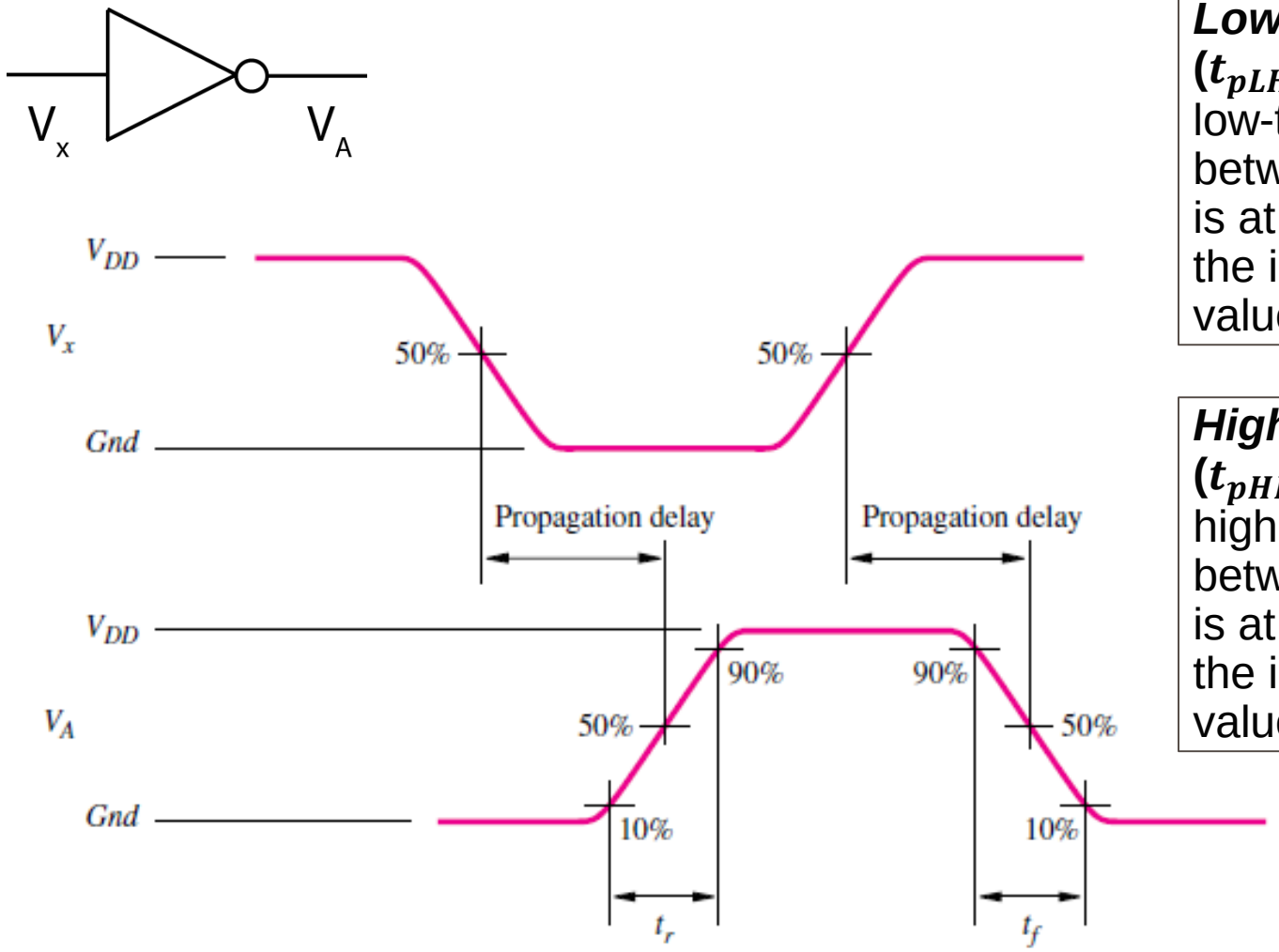
For the circuit shown below, complete the timing diagram.

Assume that each gate has a propagation delay of 20 ns.





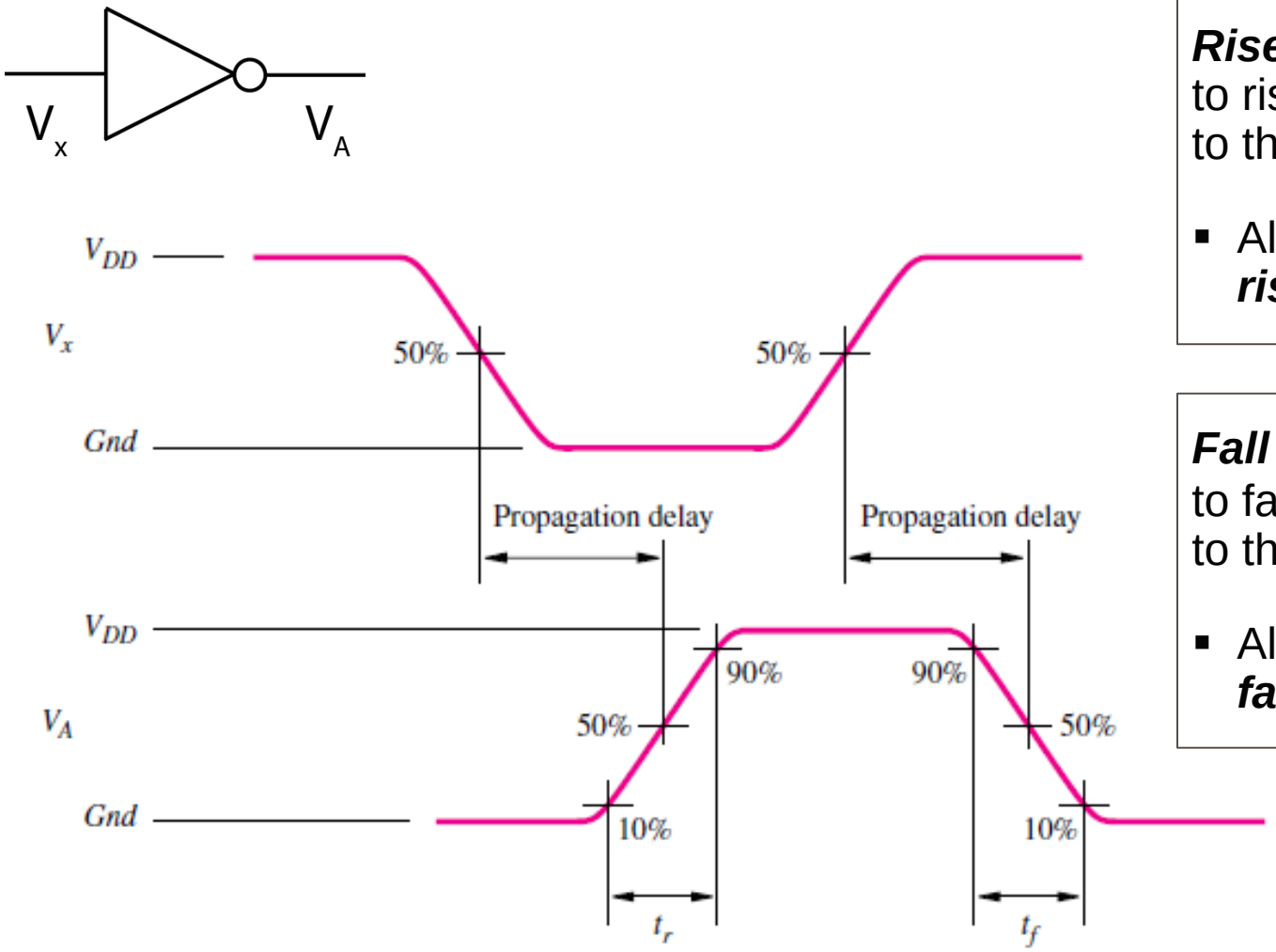
Timing Model: Propagation Delay



Low-to-high propagation delay **(t_{pLH}):** When the output switches from low-to-high, the time difference between the instant when the output is at 50% of its maximum value and the input is at 50% of its maximum value

High-to-Low propagation delay **(t_{pHL}):** When the output switches from high-to-low, the time difference between the instant when the output is at 50% of its maximum value and the input is at 50% of its maximum value

Timing Model: Rise/Fall Time



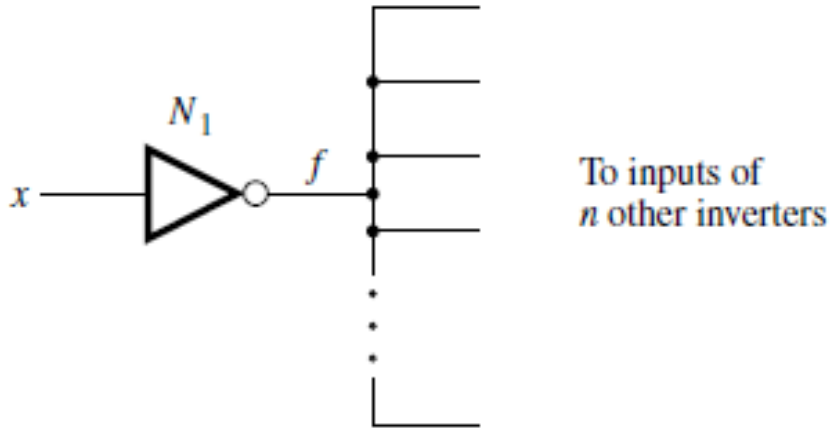
Rise time **(t_r):** Time taken by a signal to rise from 10% of its maximum value to the 90% of its maximum value.

- Also called ***rise transition time***, ***rising slew***

Fall time **(t_f):** Time taken by a signal to fall from 90% of its maximum value to the 10% of its maximum value.

- Also called ***fall transition time***, ***falling slew***

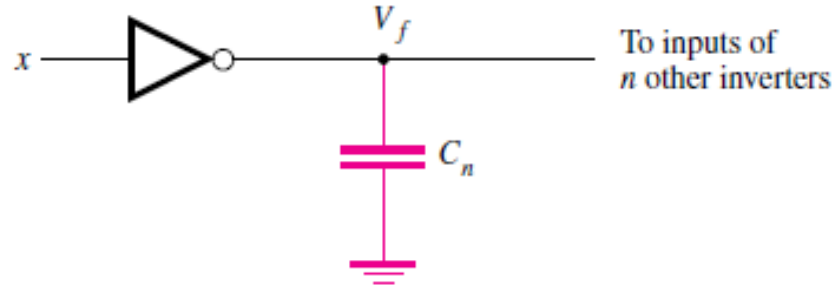
Timing Model: Factors affecting delay

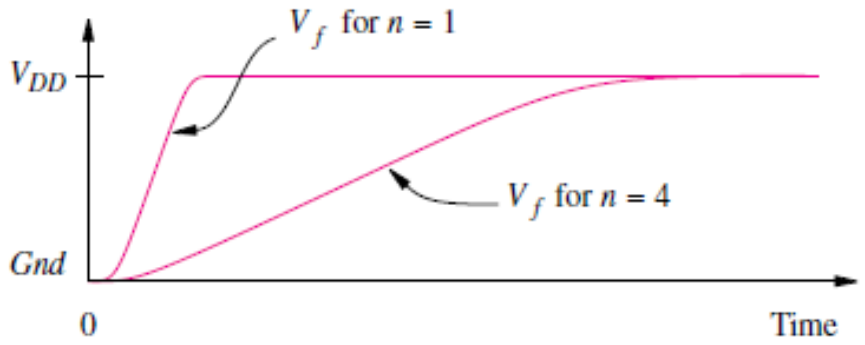


***Fanout (n)*:** Number of other pins driven by the inverter output or output of any other logic gate

***Load at the output*:** If more gates are connected at the output of an inverter or any other logic gate, then the effective capacitance increases.

- As a result, propagation delay will increase





Delay in a path in a combinational circuit

Delay in a path in a combinational circuit is computed as a sum of delay in the individual gates.

***Problem*:**

For the circuit shown alongside, it is given that:

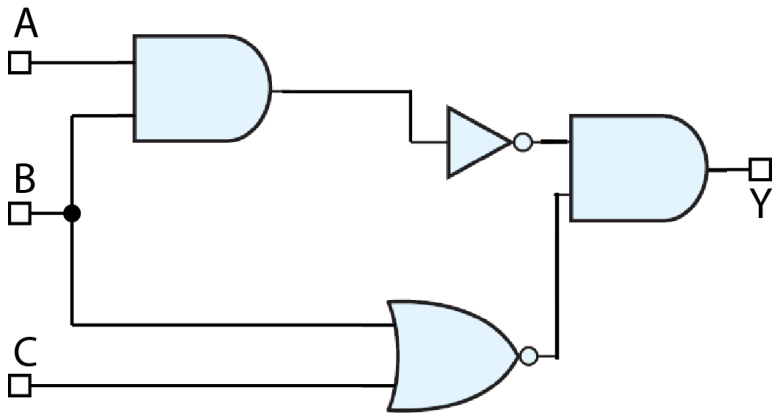
Propagation delay of NOT, AND, NOR gates are 1 ns, 6 ns, 3 ns respectively.

Compute the minimum and the maximum delay between the following ports:

a) From A to Y

b) From B to Y

c) From C to Y



***Answer*:**

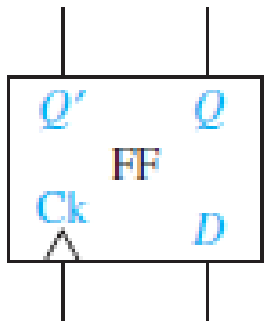
a) From A to Y: min = max = 13 ns

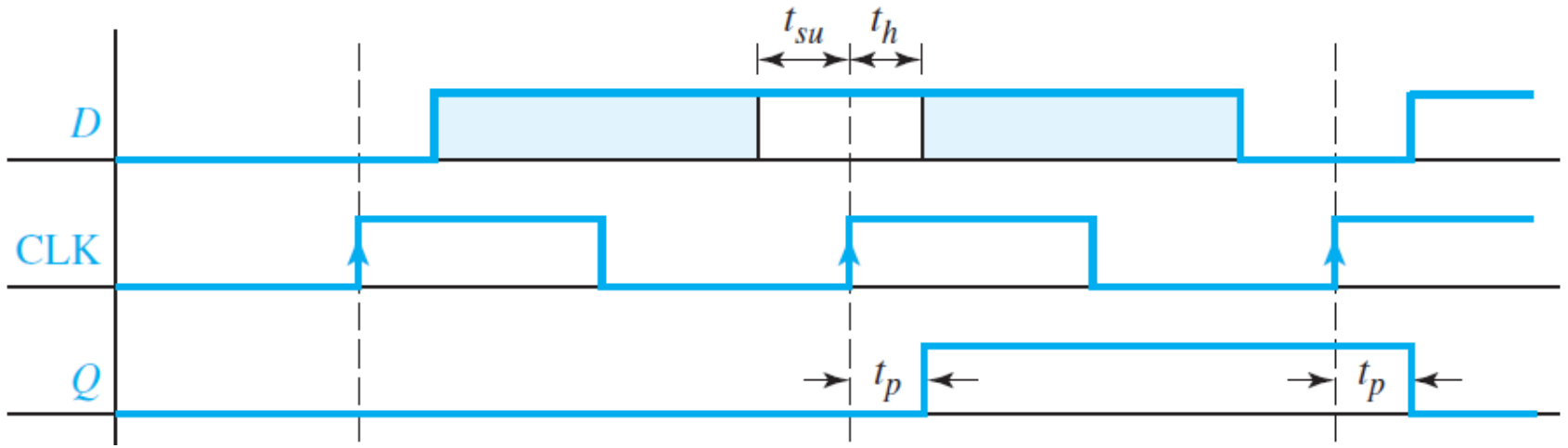
b) From B to Y: min=9 ns, max=13 ns

c) From C to Y: min=max=9 ns

Timing constraints on Flip-flops due to delay

Flip-flop: Constraints





Constraints:

a) **Setup Time (t_{su}):** amount of time that D must be stable before the active edge.

b) **Hold Time (t_h):** amount of time that D must hold the same value after the active edge

Delay:

Clock-to-Q propagation delay (t_p): the amount of time elapsed between the clock changes until the Q output changes.