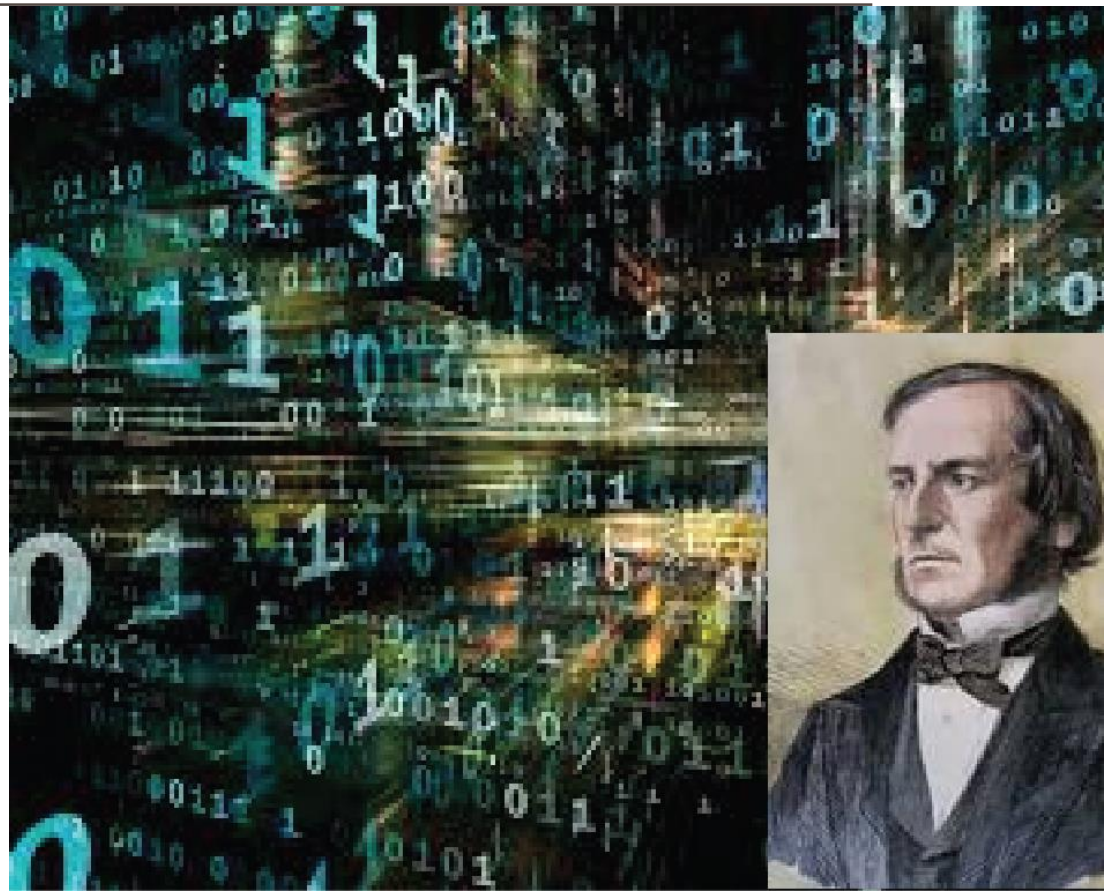
DIGITAL CIRCUITS

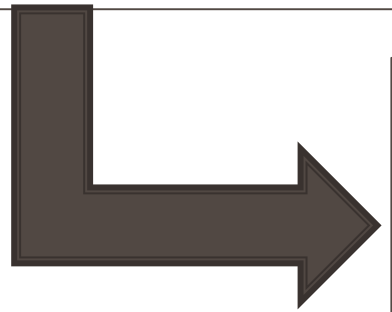
Week-10, Lecture-3
Sequential Circuits



Sneh Saurabh
12th October, 2018

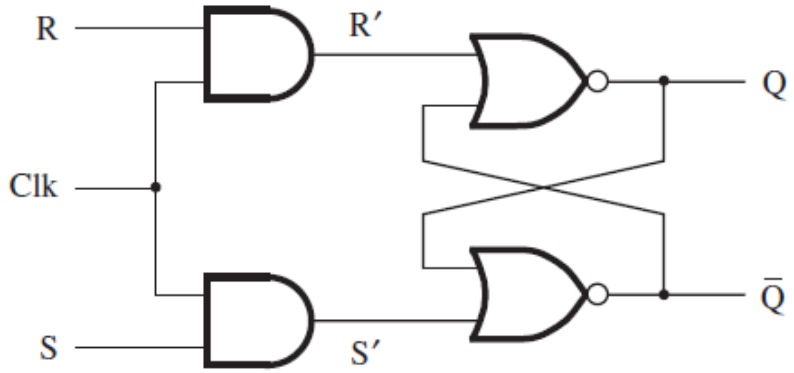
Digital Circuits: Announcements/Revision

Sequential Circuits

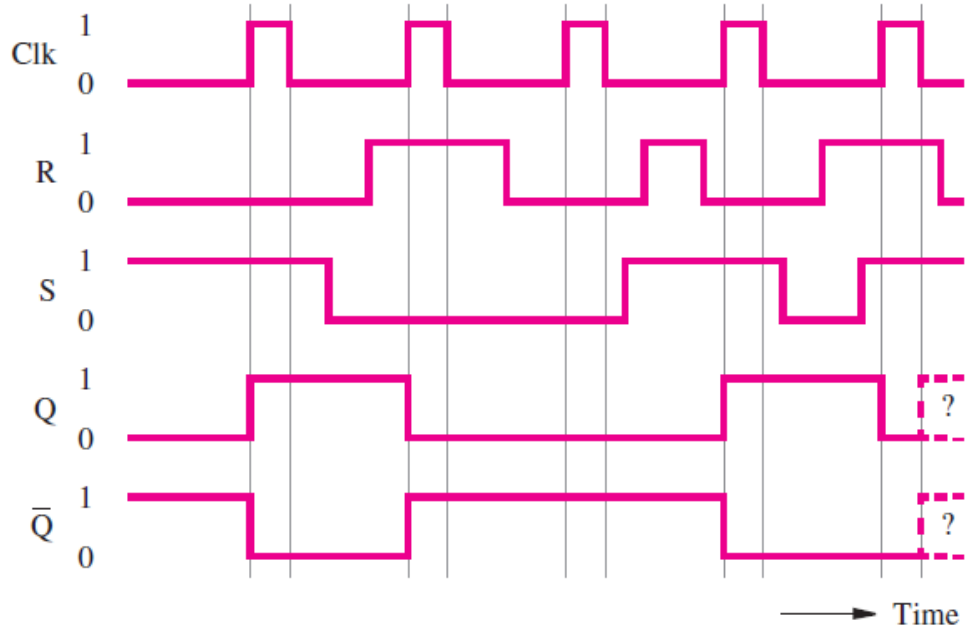


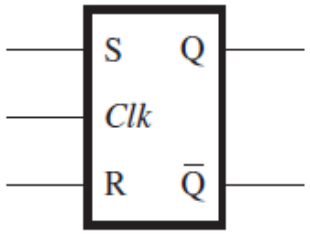
Latches

Gated SR Latch (Revision)

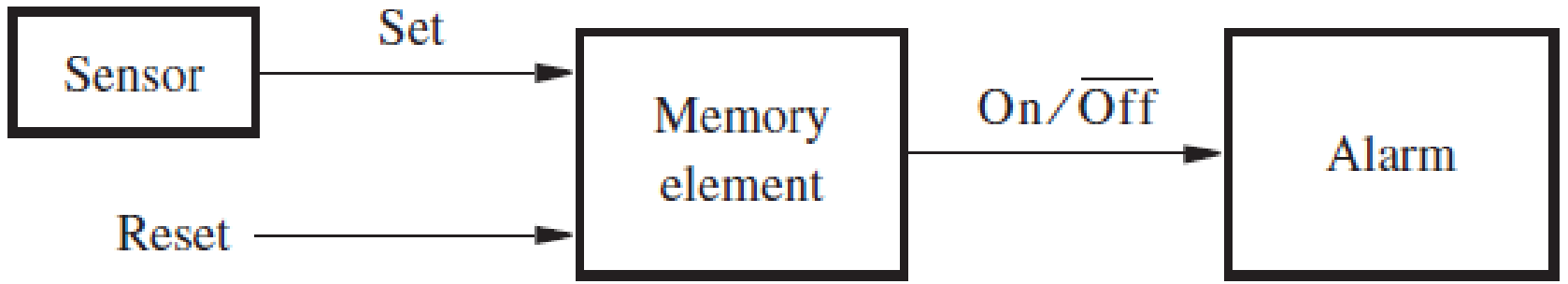


Clk	S	R	Q(t + 1)
0	x	x	Q(t) (No change)
1	0	0	Q(t) (No change)
1	0	1	0
1	1	0	1
1	1	1	x





Latch: Application



- Alarm turns-on by a signal "1" from the memory element
- Once the alarm is triggered, it must remain active even if the sensor output goes back to zero (Memory action)
- The alarm is turned off manually by means of a Reset input.

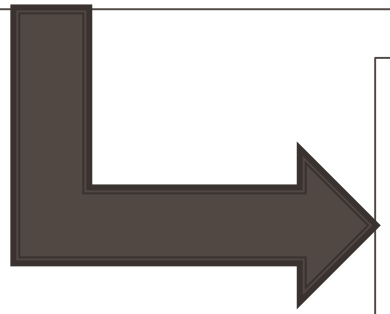
- An SR Latch can be used as a memory element in this alarm system

Latch: Review

Problem:

Can a D Latch be realized using a 2-to-1 multiplexer?

Sequential Circuits



Synchronous/Asynchronous Circuits

Types of Sequential Circuits

Two types:

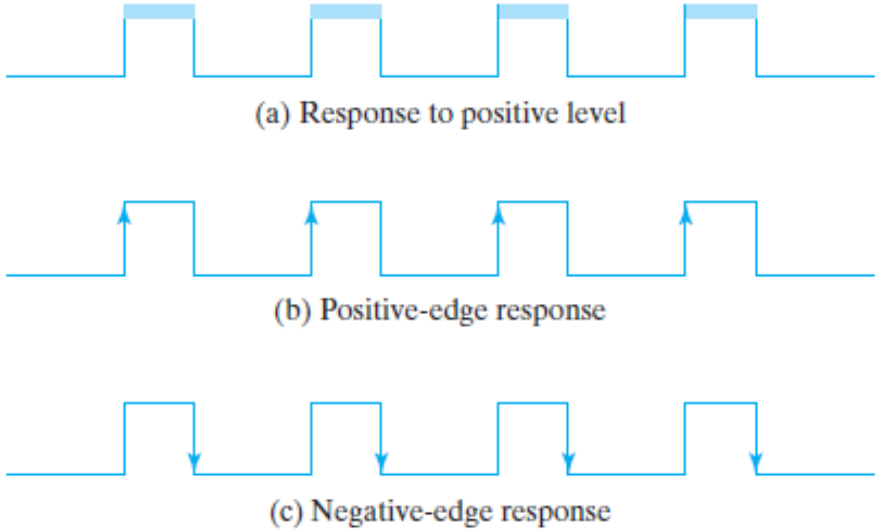
- **Synchronous circuit**: employs signals (clock) that affect the storage elements at only discrete instants of time (state changes at discrete time)
- **Asynchronous circuit**: behavior depends upon the input signals at any instant of time (state can change at any time)

In practice:

- Most of the designs are Synchronous circuits
- Synchronous circuits are easier to design and verify

Clock Signal

Synchronous circuits use clock signals

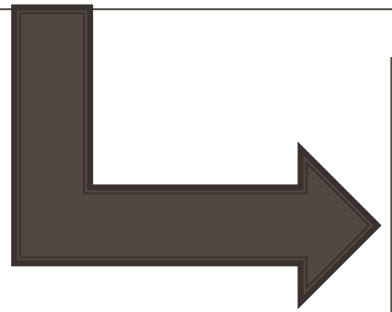


- Clock signals have the form of a periodic train of pulses
- The clock signal is commonly denoted by the identifiers ***clock*** and ***clk***

- Distributed throughout the system to all memory elements

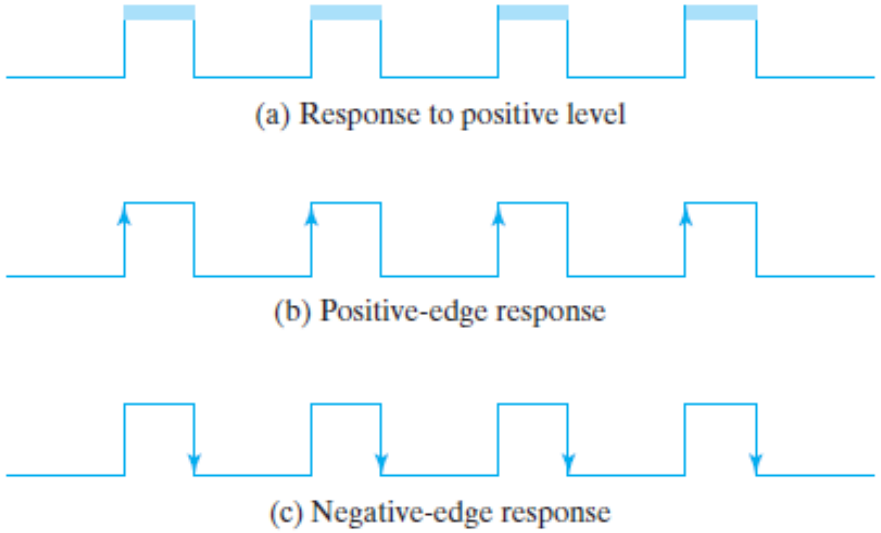
- A clock pulse goes through two transitions: from 0 to 1 and then return from 1 to 0
- The positive transition is defined as the ***positive edge*** and the negative transition as the ***negative edge***.

Sequential Circuits



Flip-flops

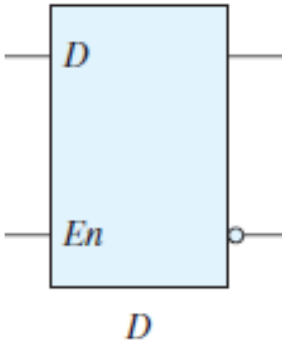
Flip-flops: Basics



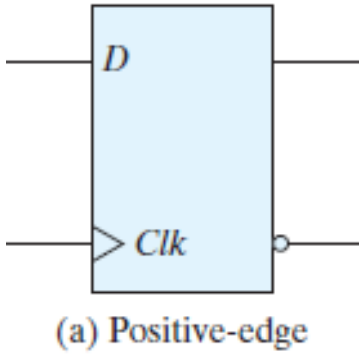
- D Latch is a level triggered device
  - ➢ When En is high, whatever is in D is passed to Q/QN

- In contrast, Flip-flops are edge triggered devices
  - ➢ Output changes only at the point in time when the clock changes from one value to the other

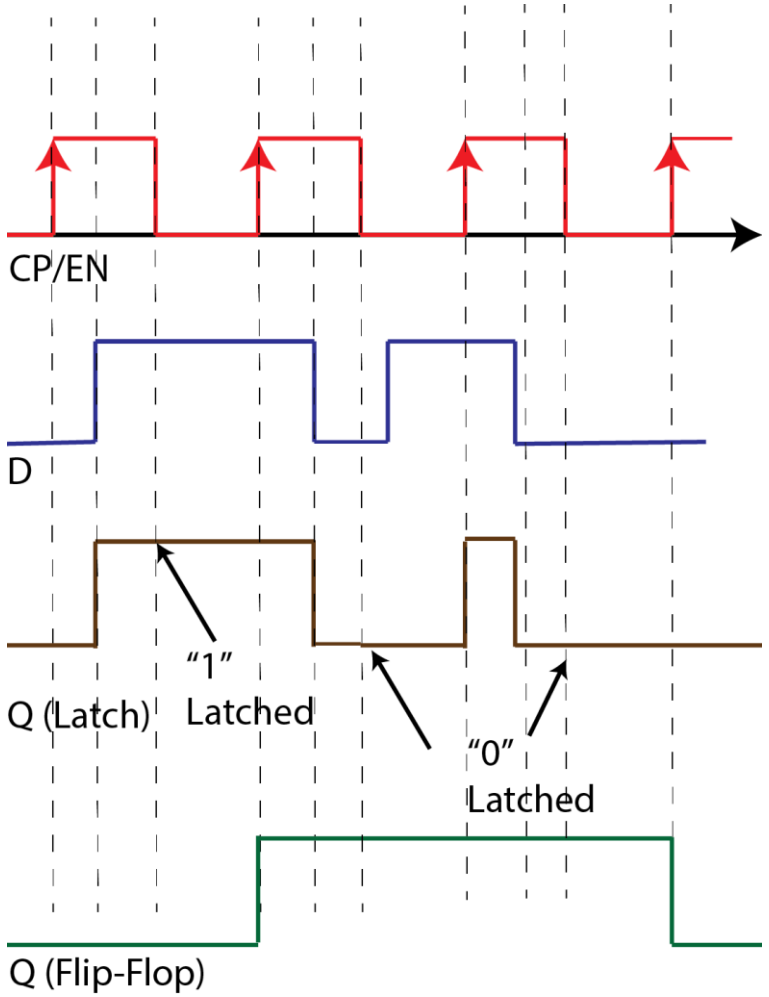
Flip-flops vs. Latch



D Latch



Flip-flop

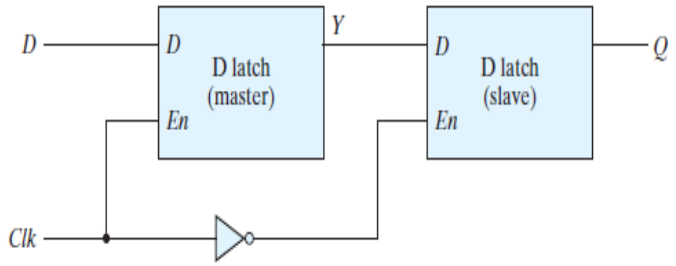


Flip-flop Implementation

Two implementations:

- Master-slave configuration
- Edge-triggered configuration

Flip-flop Implementation: Master-Slave



Can you derive the functionality?

Two latches:

- Master: Triggered when $Clk = 1$
- Slave: Triggered when $Clk = 0$

When $Clk = 1$

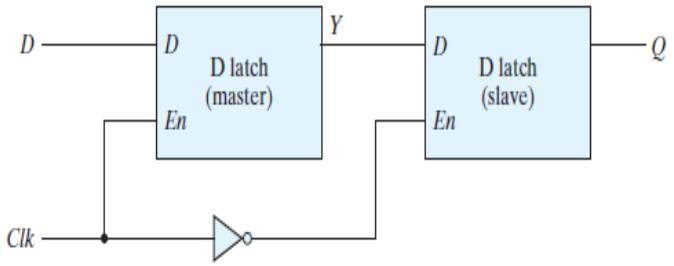
- The slave is disabled, because its enable input is equal to 0
- Any change in the input changes the master output at Y, but cannot affect the slave output.

When $Clk = 0$

- The master is disabled and is isolated from the D input.
- At the same time, the slave is enabled and the value of Y is transferred to the output of the flip-flop at Q

- Thus, a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

Flip-flop Implementation: Master-Slave



Can it be converted to a positive edge triggered flip-flop?

- Connecting the slave stage directly to the clock and the master stage to the complement of the clock.

- Another way: use 3 SR latches

Digital Circuits: Practice Problems

Problem 5.1

from “Digital Design”– M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).

Problems 7.1 – 7.5

from Fundamentals of Digital Logic with Verilog Design - S. Brown, Z. Vranesic