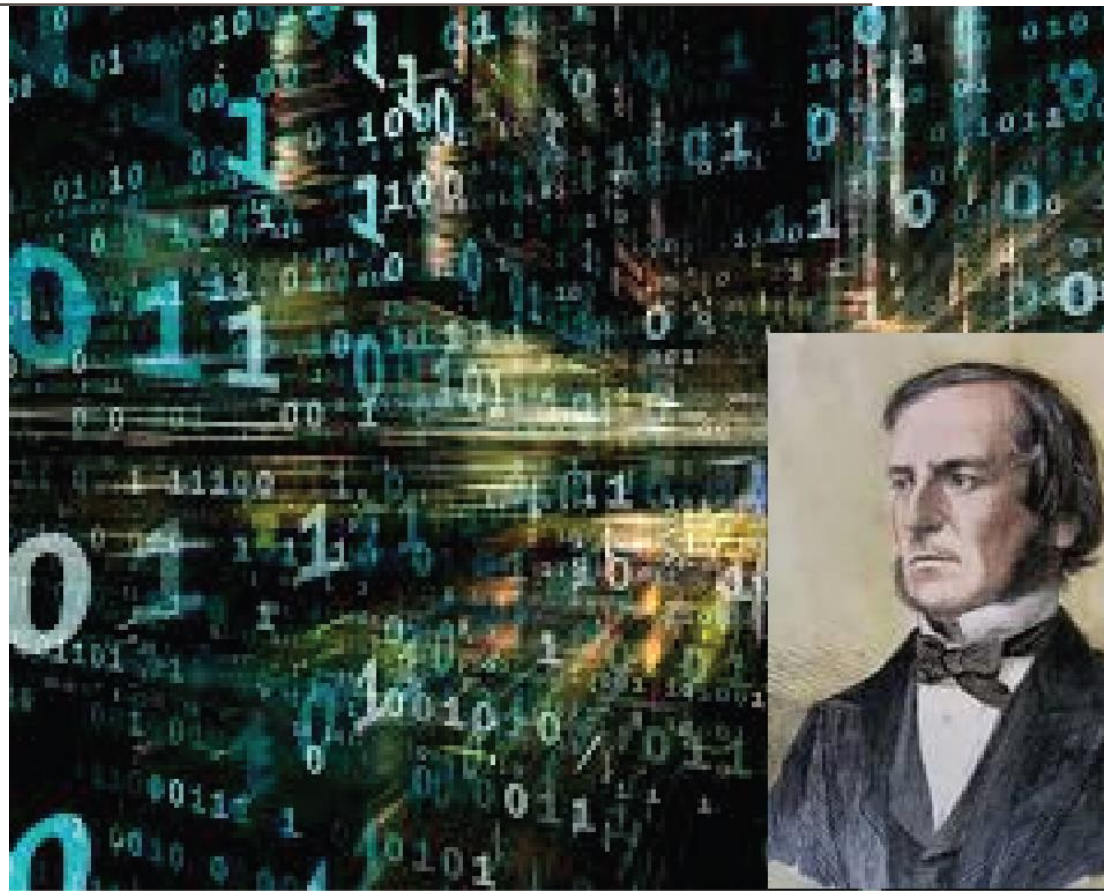
DIGITAL CIRCUITS

Week-8, Lecture-2
Decoders

Sneh Saurabh
26th September, 2018



Digital Circuits: Announcements/Revision

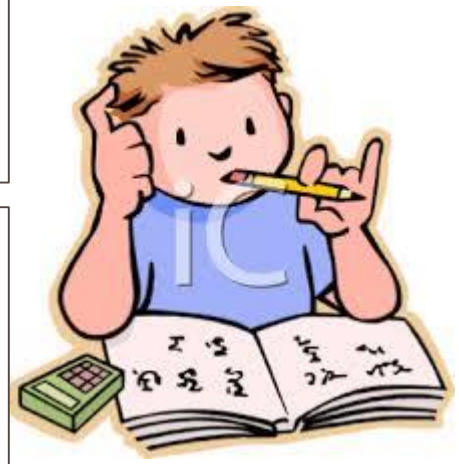
Digital Circuits: Practice Problems

Problems 4.31-4.35

from “Digital Design”– M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).

Problems 6.3-6.10

from Fundamentals of Digital Logic with Verilog Design - S. Brown, Z. Vranesic



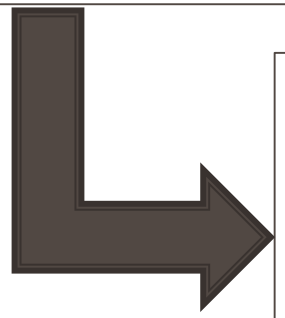
Problem: Design XNOR gate using 4:1 multiplexer

Problem: Design XNOR gate using 2:1 multiplexers

Problem: Implement the function $f(w,x,y,z) = \Sigma m(1,4,5,7,9,12,13)$ using a 8-to-1 MUX and minimum number of 2-to-1 MUX only.

Problem: Implement the function $f(w,x,y,z) = \Sigma m(1,4,5,7,9,12,13)$ using a 8-to-1 MUX and minimum number of logic-gates only.

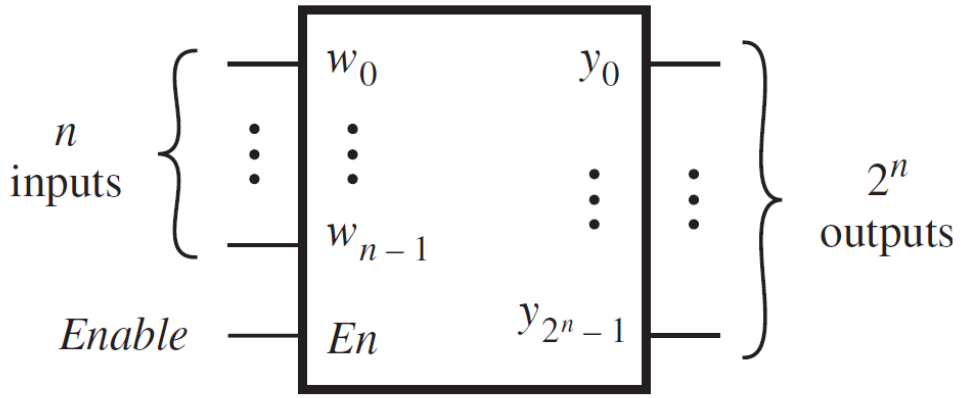
Digital Circuits



Decoders

Decoder: Basics

- A binary decoder is a combinational circuit with:
  - n inputs: $w_0, w_1, \ldots, w_{n-1}$
  - 2^n outputs: $y_0, y_1, \ldots, y_{2^n-1}$
  - A pin named En or $Enable$



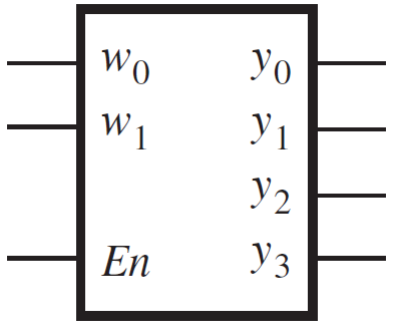
- Only one of the outputs is asserted "1" and rest of the outputs are "0"
- Which of the outputs is asserted "1" depends on the binary number at the inputs corresponding to: $w_{n-1} \ldots w_1 w_0$

- A decoder also has an input named "En" or "$Enable$"
  - When "$En = 0$", all the outputs are "0"
  - When "$En = 1$", one of the outputs gets a value of "1"

Decoder: 2-to-4 decoder

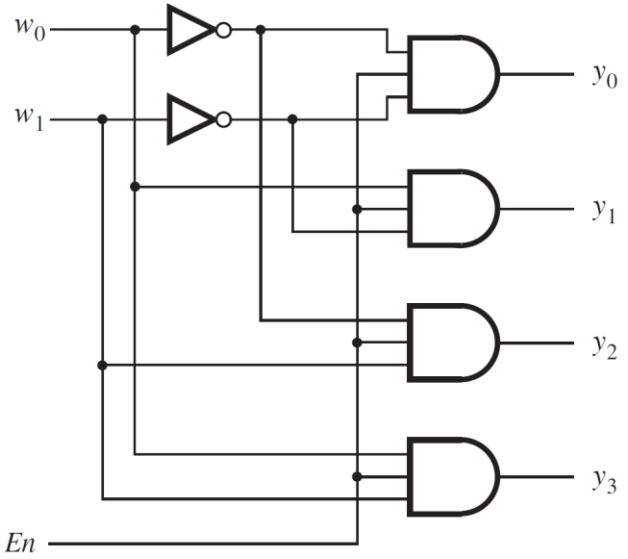
2-to-4 decoder:

- Two data inputs w_0,w_1, one En input and four outputs y_0,y_1, y_2 and y_3
- One of the outputs gets a value “1” depending on the binary number represented by w_1w_0



En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

- Can you write the expression for each output y_0,y_1, y_2 and y_3?
- Each output correspond to a minterms of the 2 variable function $f(w_0,w_1)$

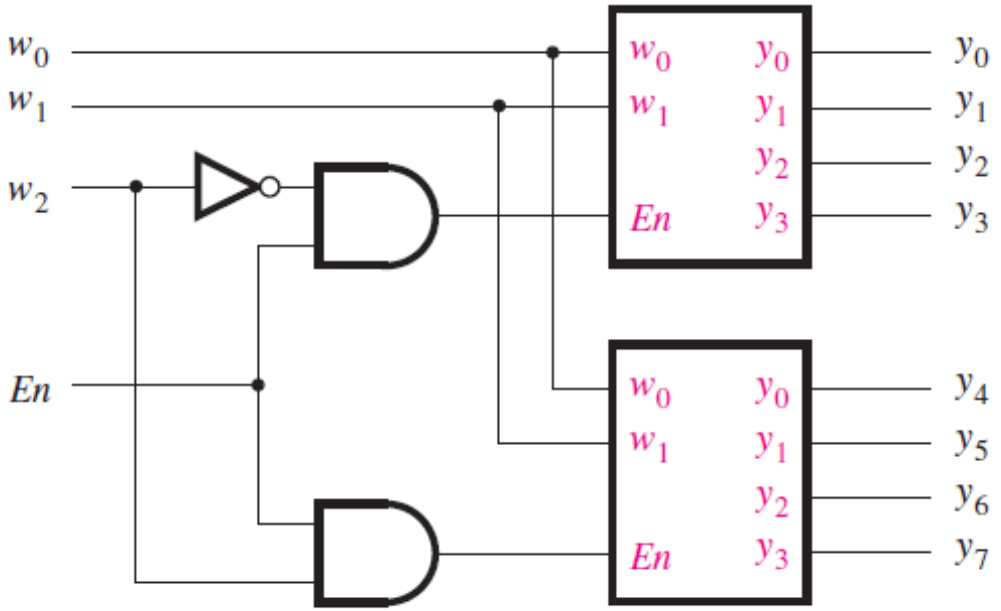


Decoder: Large decoder from small decoder

- Larger decoders can be built using smaller decoders

- Build a 3-to-8 decoder using two 2-to-4 decoders and some other gates.

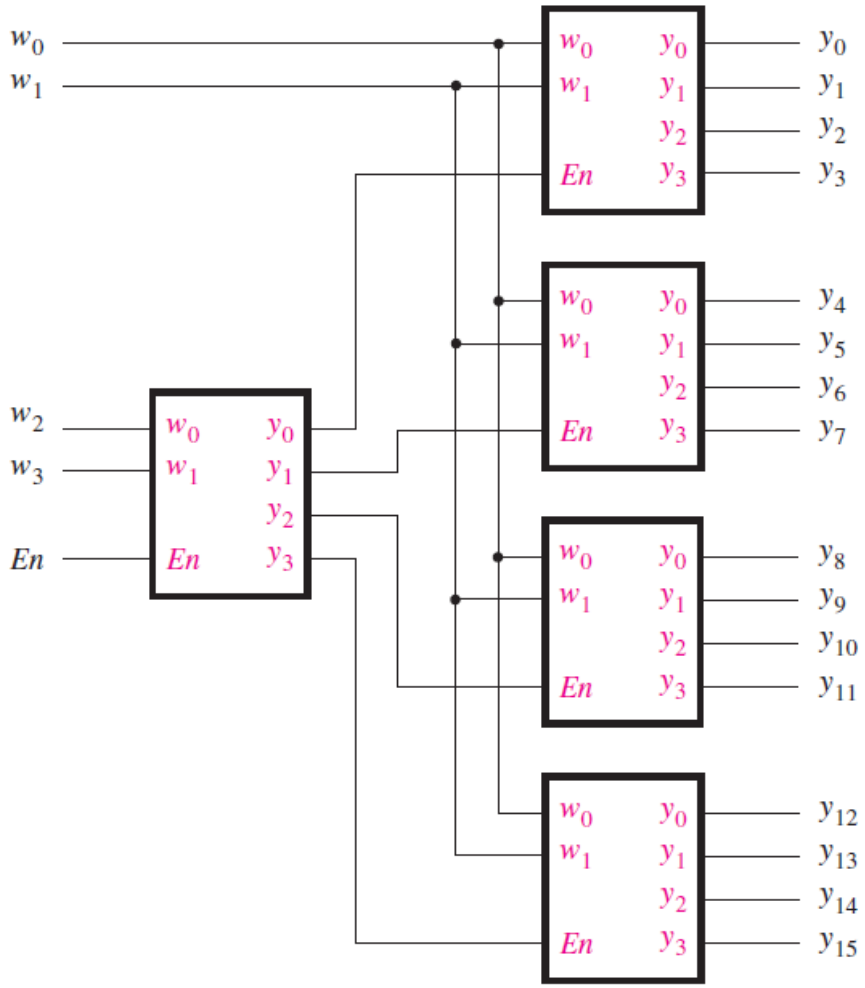
- The w_2 input drives the enable inputs of the two decoders
- The top decoder is enabled if $w_2 = 0$, and the bottom decoder is enabled if $w_2 = 1$



Decoder: Large decoder from small decoder

- Build a 4-to-16 decoder using only five 2-to-4 decoders

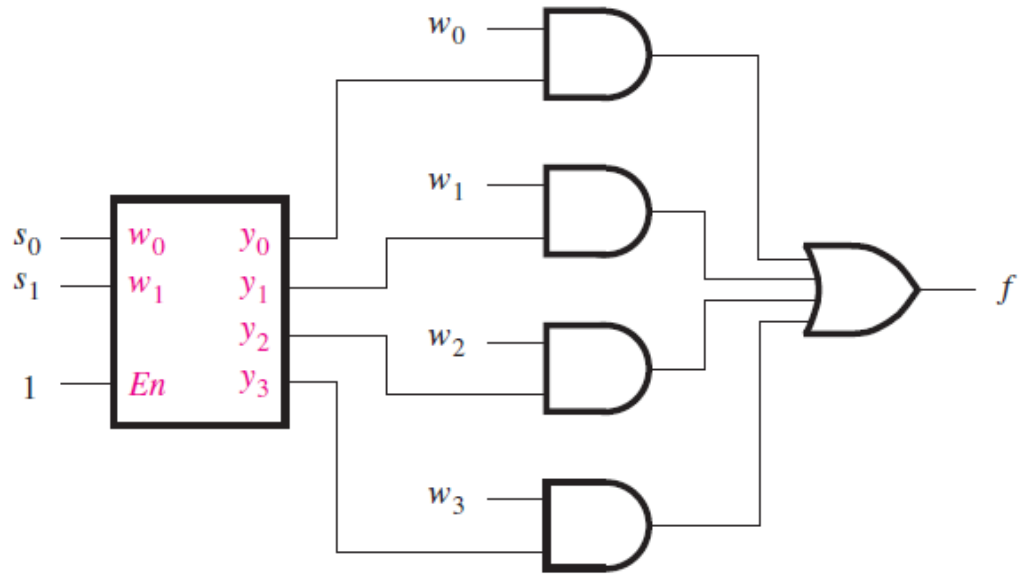
- The w_2w_3 input drives the enable inputs of the four decoders
- The top decoder is enabled if $w_2w_3 = 00$, and the bottom decoder is enabled if $w_2w_3 = 11$



Decoder: To multiplexer

- Build a 4-to-1 multiplexer using a 2-to-4 decoder and AND/OR gates

- En pin is set to 1
- The output of the decoder generates 1 on one of the four lines, based on the binary number represented by the select lines $s_1 s_0$
- The output of the decoder selects one of the inputs w_0, w_1, w_2, w_3 of the multiplexer

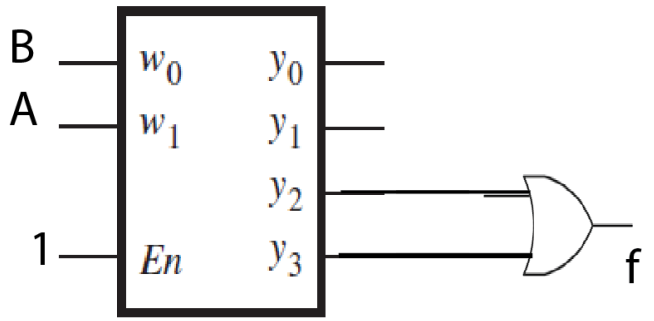


Decoder: Realizing a given function

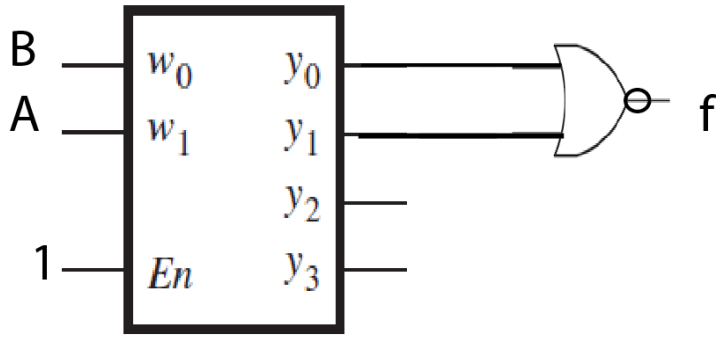
Implement the function:

$f(A, B) = \Sigma m(2,3)$

using a 2-to-4 decoder and an OR gate.



- If a function F has many minterms then the OR gate will have a large number of inputs
  - Implementing F' and taking the complement will be more efficient



- Depending on the number of minterms in a given function, implementing using either OR gate or using NOR gate may be more efficient.

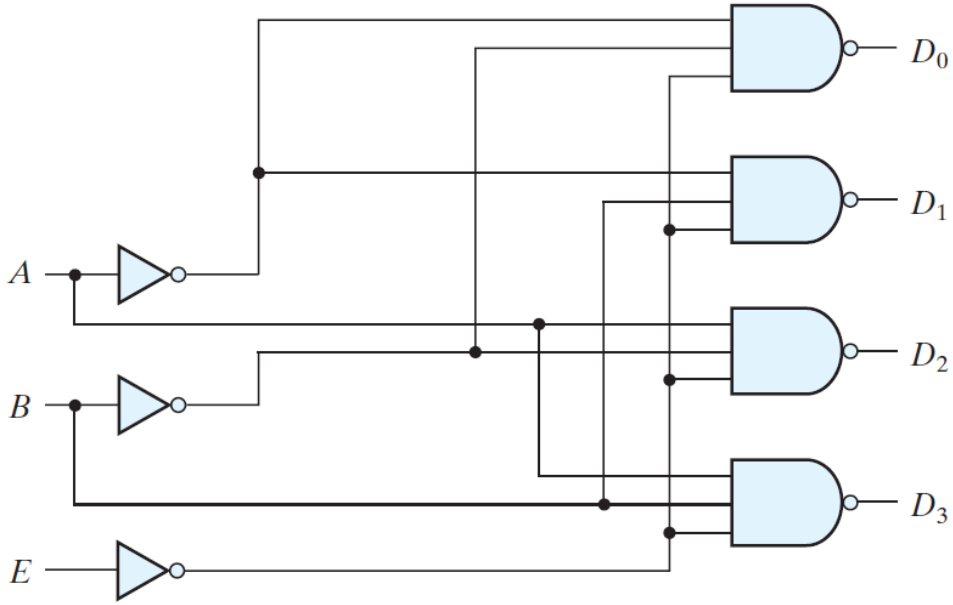
Decoder: Realized using NAND gates

- A decoder can be built using NAND gates

- $Enable$ is active low (Decoder is enabled when $E = 0$)
- Outputs are active low (output is complement of normal decoder): complement of the minterms
- Only one of the outputs is 0, rest are 1

- Since outputs are complement of minterms, realizing a function will require using NAND gates, rather than OR gates

Implement the function: $f(A, B) = \Sigma m(2,3)$ using the decoder that is realized using NAND gates



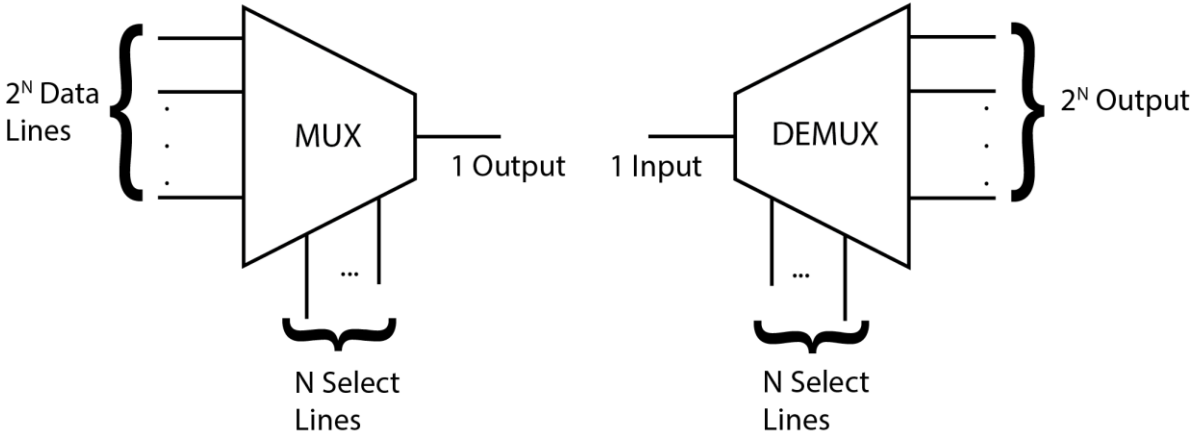
E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Decoder: To demultiplexer

- Decoder with enable input can work as a ***demultiplexer***

Demultiplexer

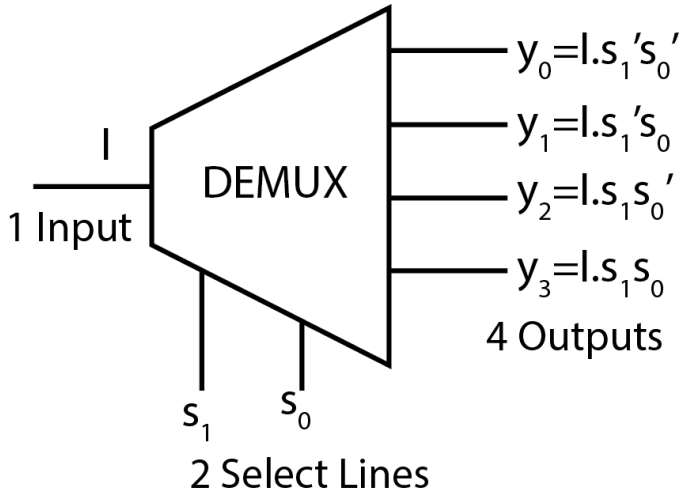
- Demultiplexer is a combinational circuit that function opposite to that of a multiplexer



Function of a Demultiplexer

- The output a circuit that receives information from a single line and directs it to one of the 2^N possible output lines
- The selection of a specific output is controlled by the bit combination of N selection lines

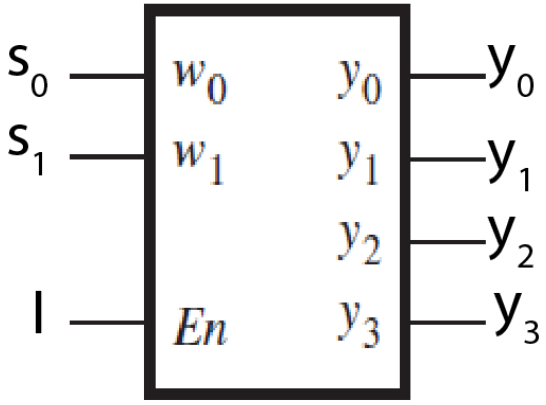
Decoder: To demultiplexer



s_1	s_0	y_0	y_1	y_2	y_3
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

1-to-4 Demultiplexer

- Build a 1-to-4 Demultiplexer using a decoder



Digital Circuits: Practice Problems

Problems 4.22-4.28

from “Digital Design”– M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).