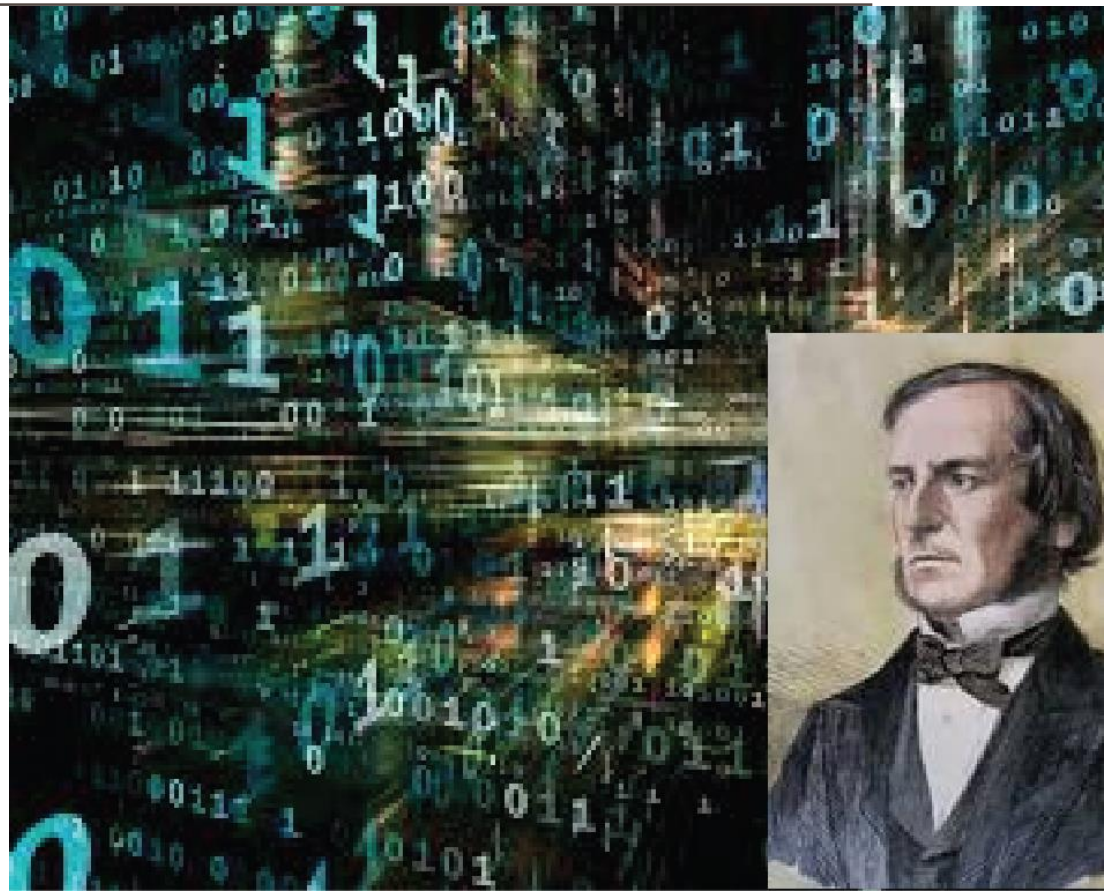
DIGITAL CIRCUITS

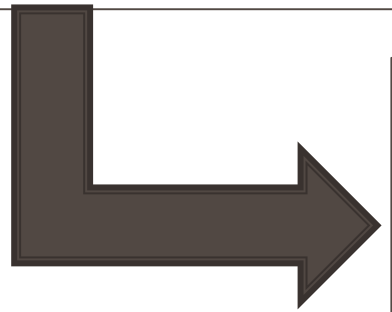
Week-11, Lecture-2
Sequential Circuits



Sneh Saurabh
24th October, 2018

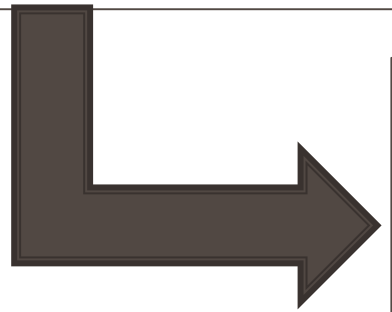
Digital Circuits: Announcements/Revision

Sequential Circuits



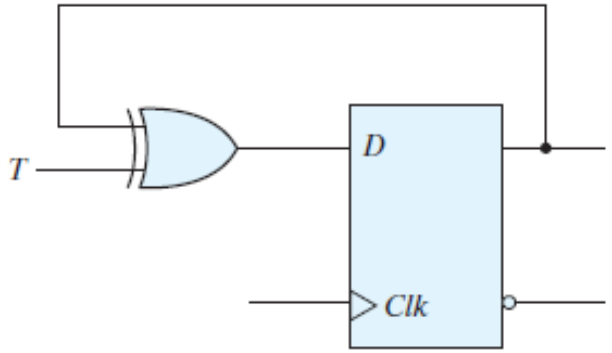
Flip-flops

Sequential Circuits



Other types of Flip-flops

T Flip-Flop using D flip-flop



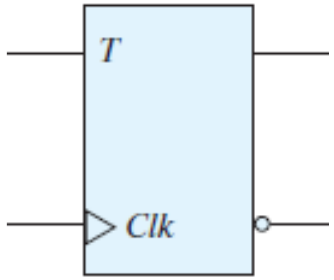
Problem:

A T flip-flop is realized using a D flip-flop using the circuit shown alongside.

Obtain the functionality of the T flip-flop in a form of ***characteristics table*** and ***characteristics equation***

T	$Q(t+1)$
0	
1	

T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$



$$Q(t+1) = T \oplus Q$$

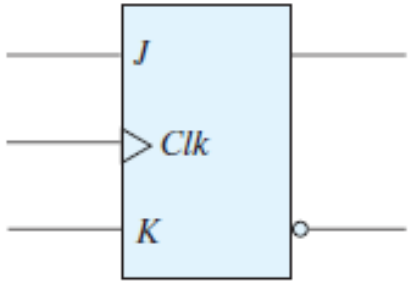
T Flip-Flop using JK Flip-flop

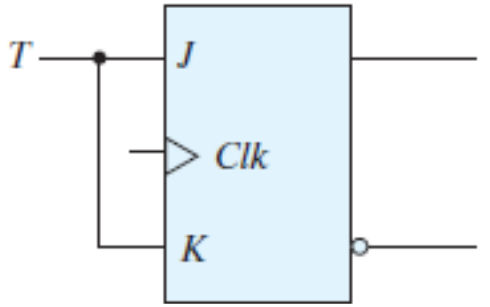
Problem:

A T flip-flop needs to be realized using a JK flip-flop. Find the implementation.

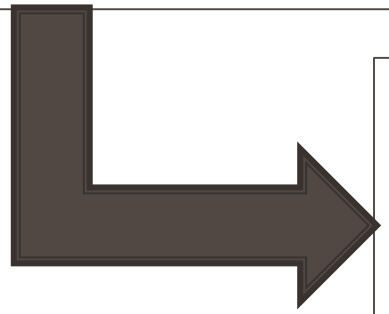
J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$



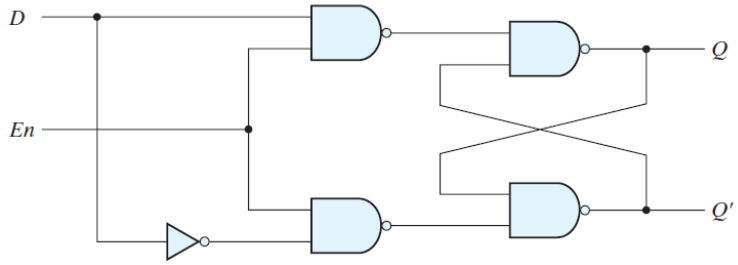


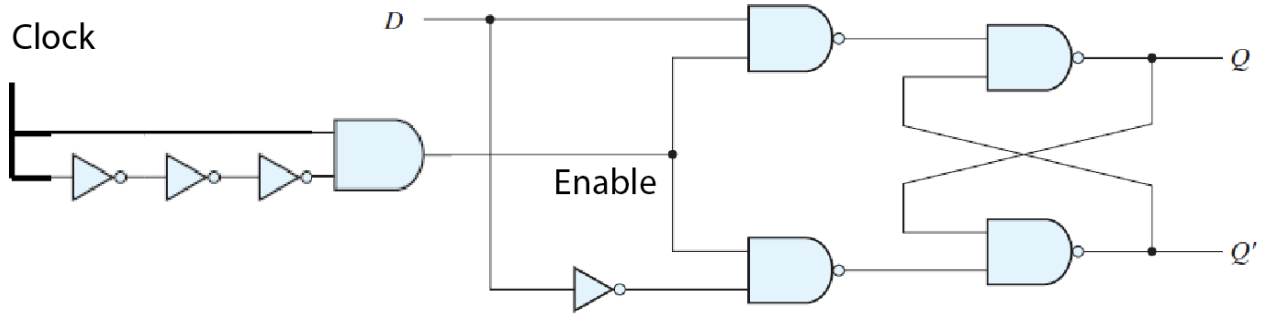
Sequential Circuits



Problems on Latches/Flip-flops

Pulse-triggered Flip-flop (1)



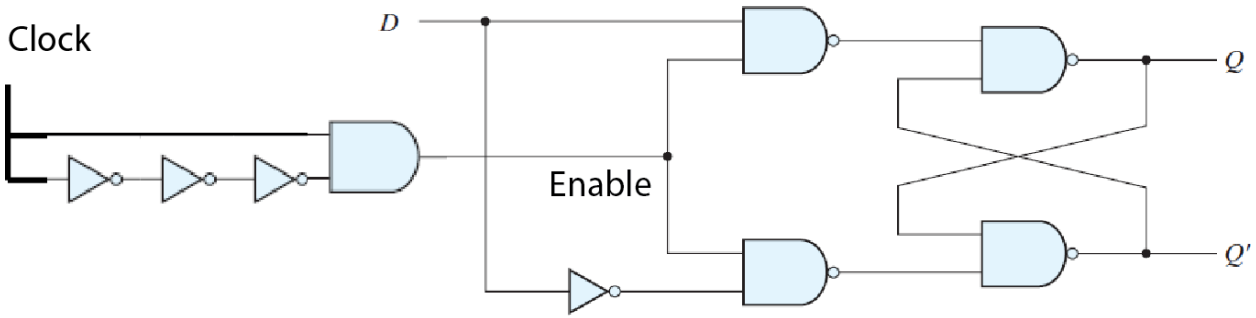


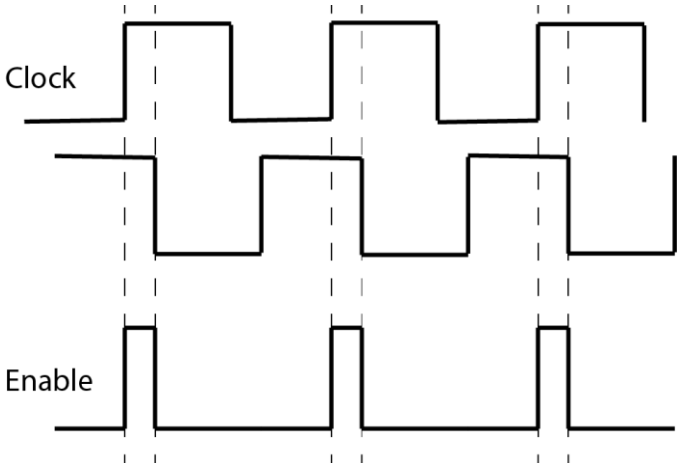
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

Problem-1

Analyze the behavior of the circuit shown above.

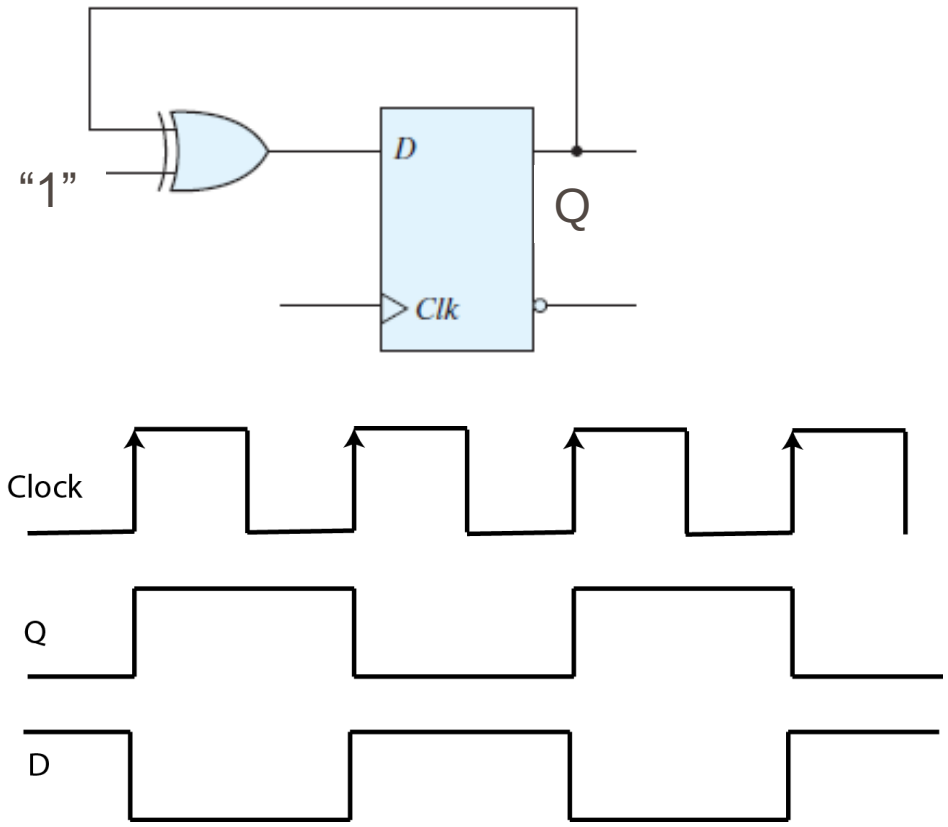
Pulse-triggered Flip-flop (2)





- Positive edge detector at enable pin
- Latch enabled for a short duration after the arrival of positive edge of the clock
- When latch is enabled D passes to Q
- Works as pulse-triggered Flip-flop
- Pulse width needs to be kept small

Flip-flop: Unstable state (Toggle)

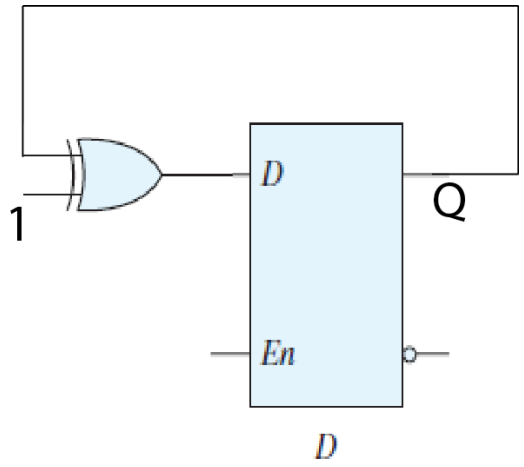


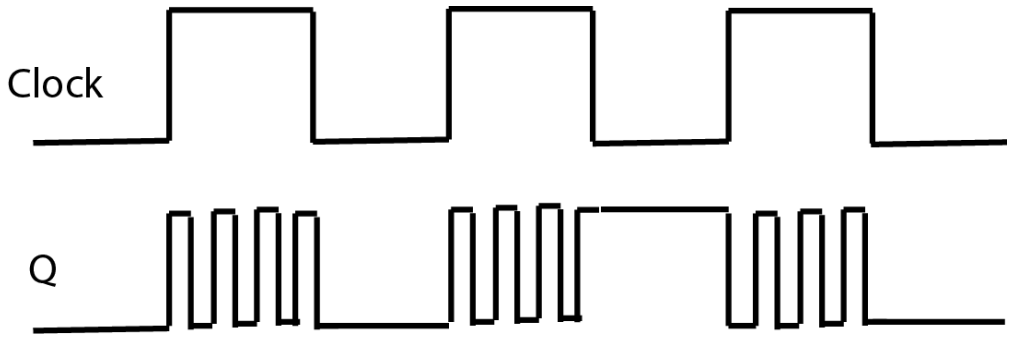
Problem-2

Analyze the behavior of the circuit shown.

- D and Q are complement of each other
- The state of the flip-flop is unstable (toggle state)
- Frequency Divider circuit

D Latch: Race Condition





Problem-3

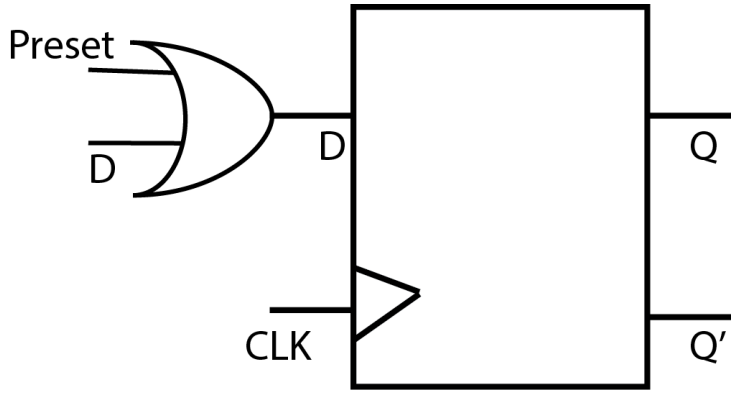
Analyze the behavior of the circuit.

- D and Q are complement of each other
- When $En = 1$, state changes rapidly between 0 and 1
- When $En = 0$, state can be either 0 or 1, difficult to predict
- This is a **race condition**
- The behavior is unpredictable and this circuit should be avoided

Flip-flop with Synchronous Preset

Problem-4

Implement a flip-flop with synchronous preset that is active high.



Digital Circuits: Practice Problems

Problems 5.1-5.4

from “Digital Design”– M. Morris Mano & Michael D. Ciletti, Ed-5, Pearson (Prentice-Hall).

Problems 7.1-7.9

from Fundamentals of Digital Logic with Verilog Design - S. Brown, Z. Vranesic