

國立中山大學電機工程系
實用數位系統設計

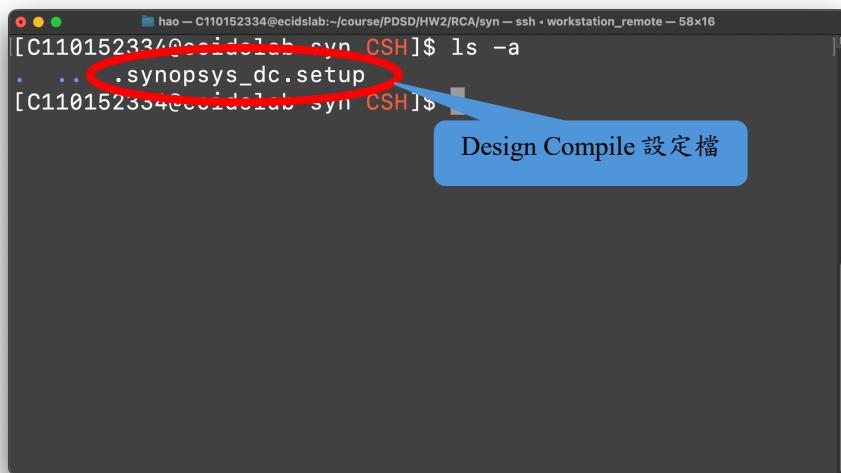
Homework 2

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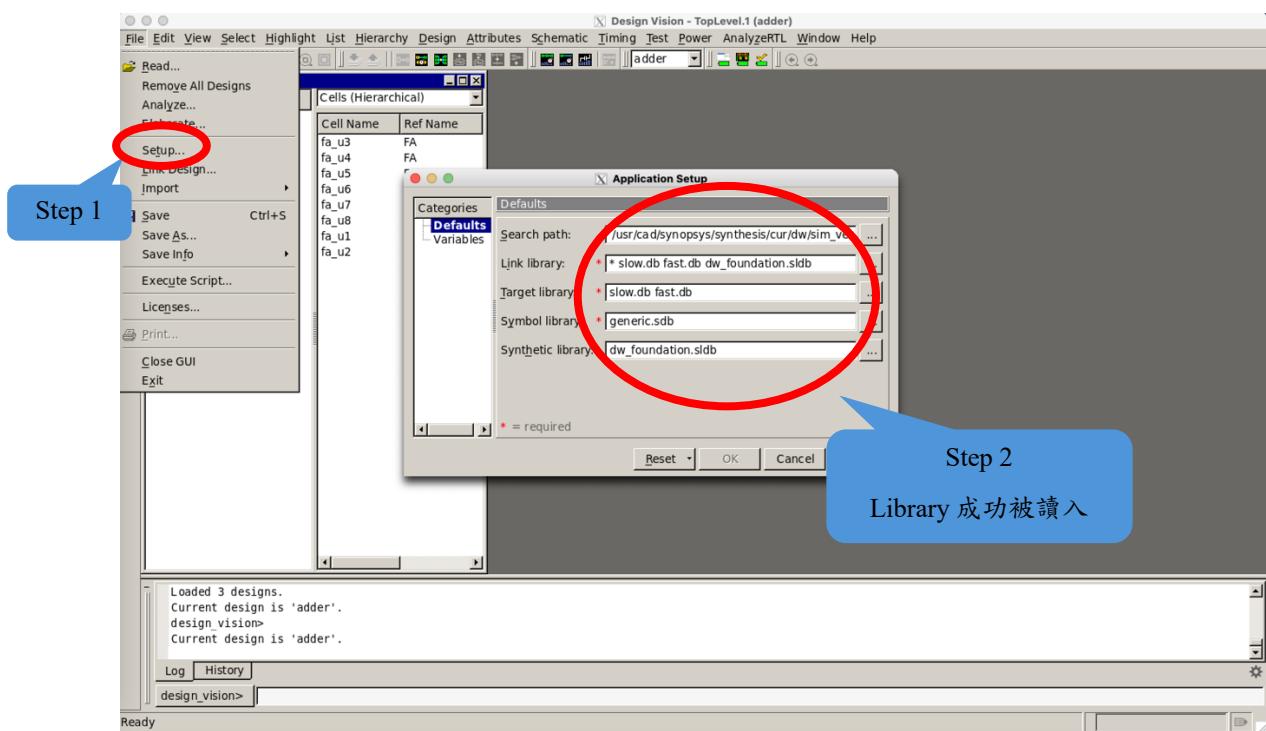
一、 Ripple Carry Adder (RCA)

1. 合成

- i. 加入 Design Compile 設定檔：
加入 .synopsys_dc.setup 檔案，並確定 Library 是否被引入。



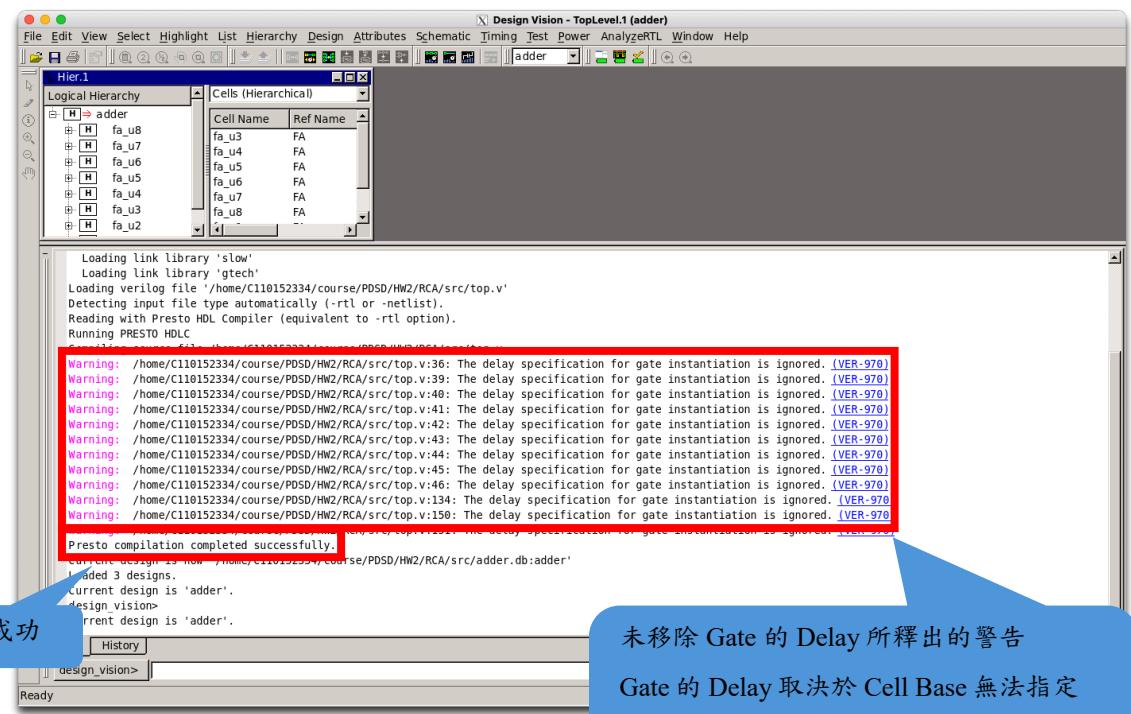
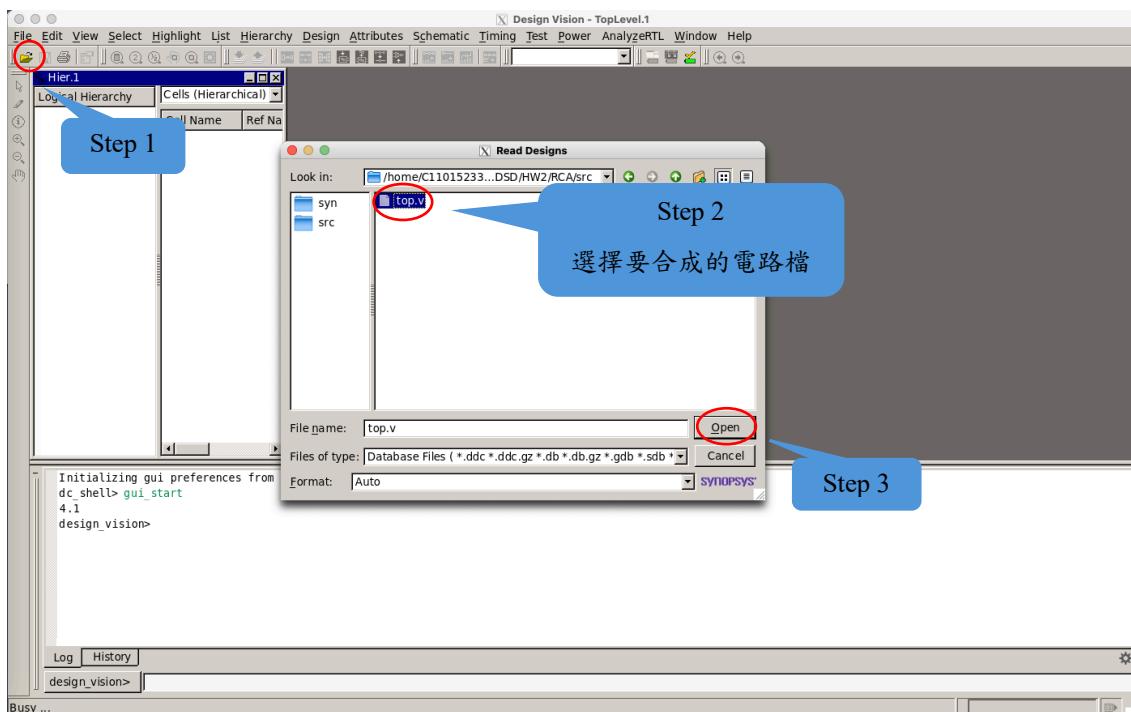
```
[C11015233@ecidslab syn CSH]$ ls -a
.  .. .synopsys_dc.setup
[C11015233@ecidslab syn CSH]$
```



ii. Read File :

讀取電路檔(.v)。

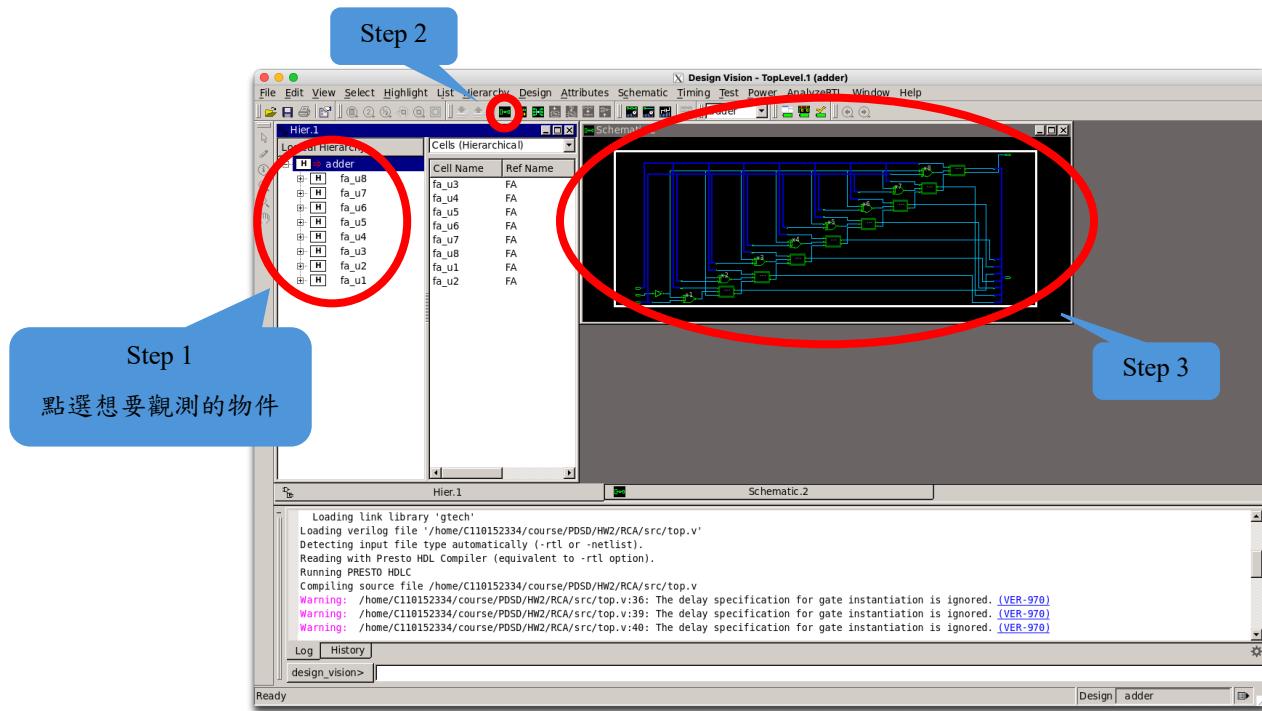
Command: read_file -format verilog {"File Path" }



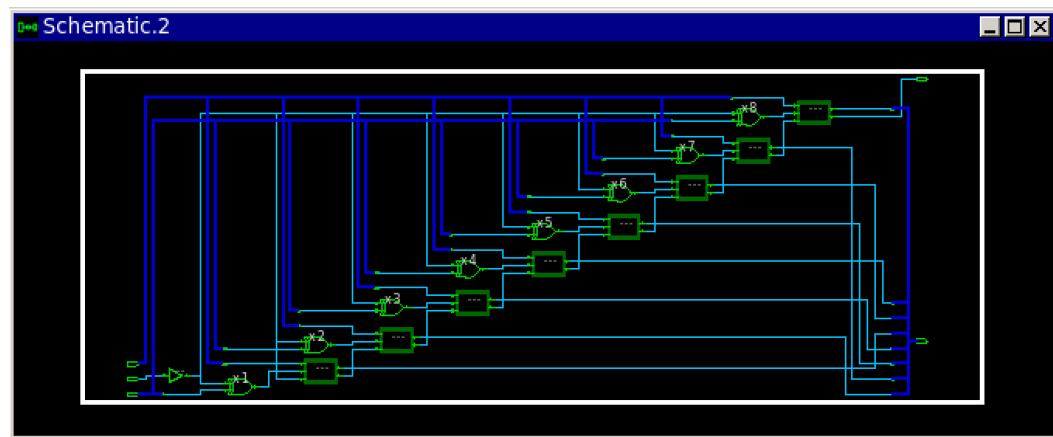
iii. Schematic View:

確認合成前結構是否與設計吻合

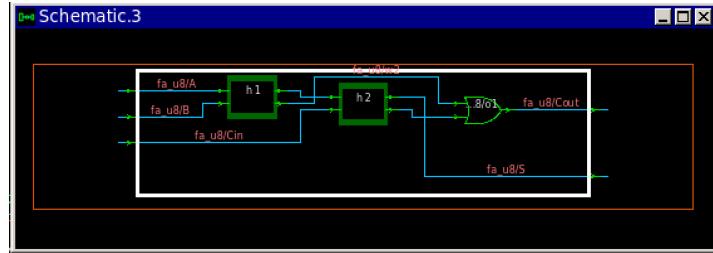
(邏輯閘非製成所提供的 Cell Library，而是 Gtech Library)



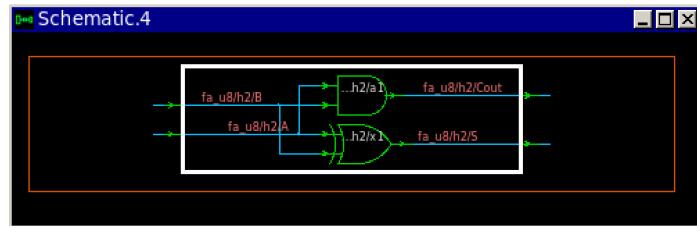
(1.) Adder(Top module)



(2.) Full Adder



(3.) Half Adder



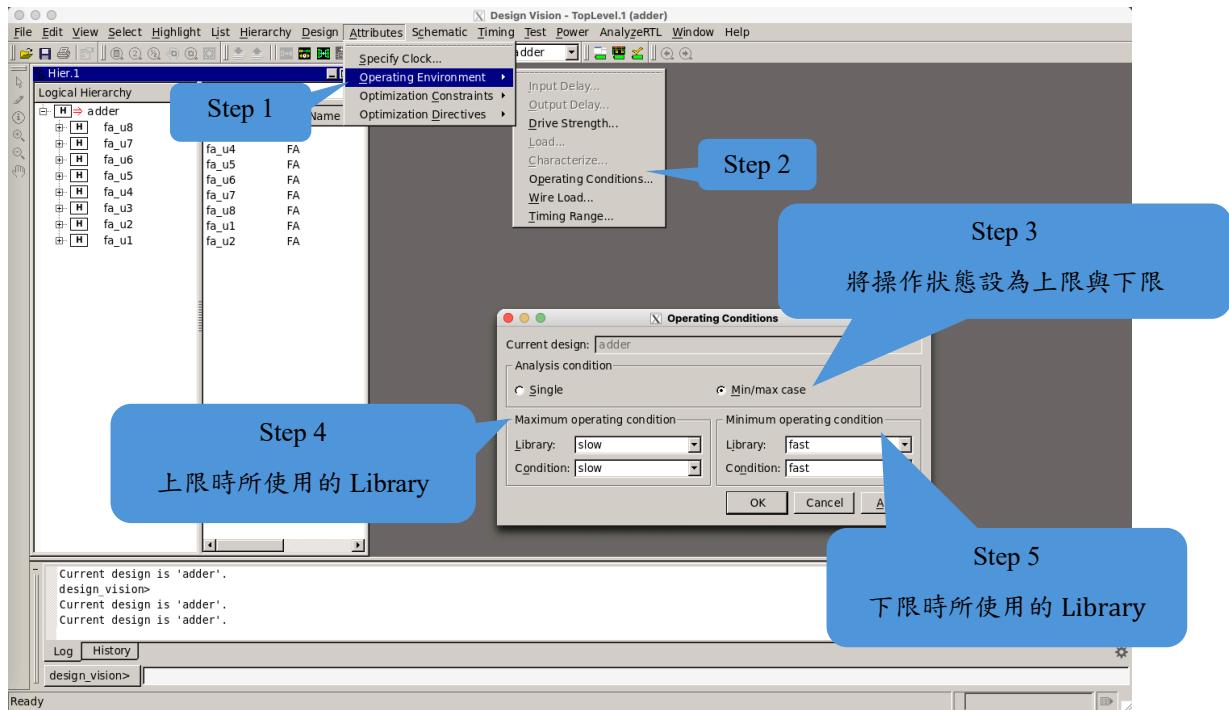
iv. 插入 Buffer

為了防止訊號未經任何處理就直接輸出，輸入下面指令幫直接輸出的訊號插入 Buffer。

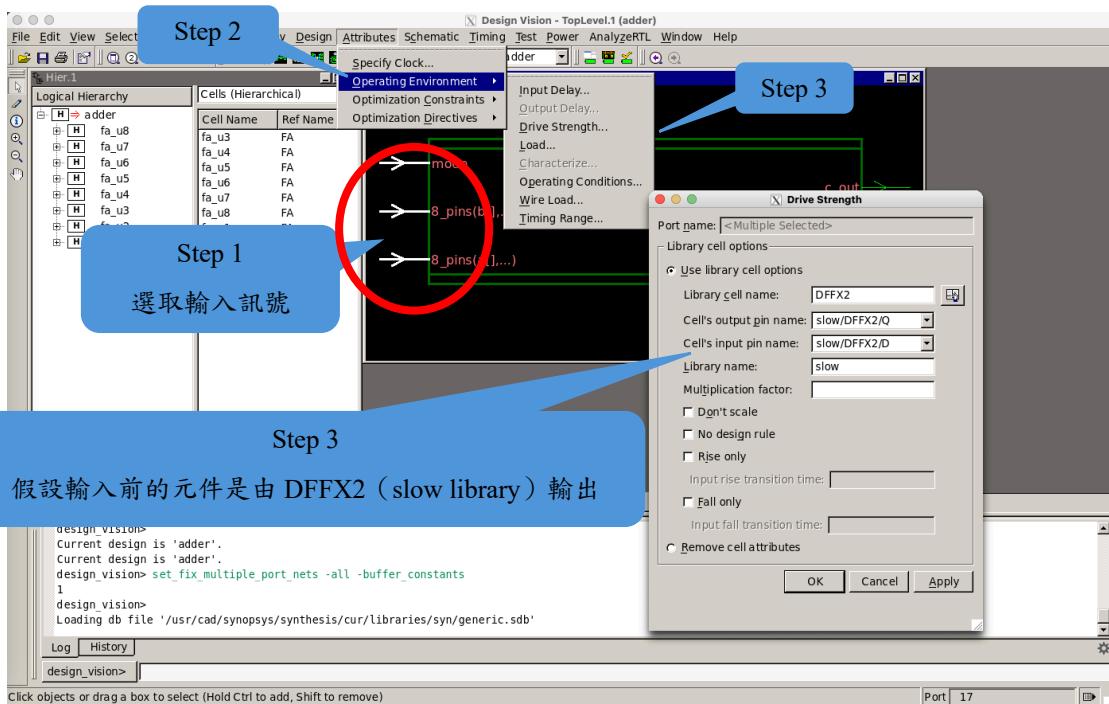
Command : set_fix_multiple_port_nets -all -buffer_constants

```
Current design is 'adder'.
design_vision>
Current design is 'adder'.
Current design is 'adder'.
design_vision> set_fix_multiple_port_nets -all -buffer_constants
1
design_vision>
```

v. Operating Condition
讓合成時可以考慮電壓與溫度的狀態



vi. Input Driving Strength
設定後可以得到更真實的 Translation 時間（預設為 0）。

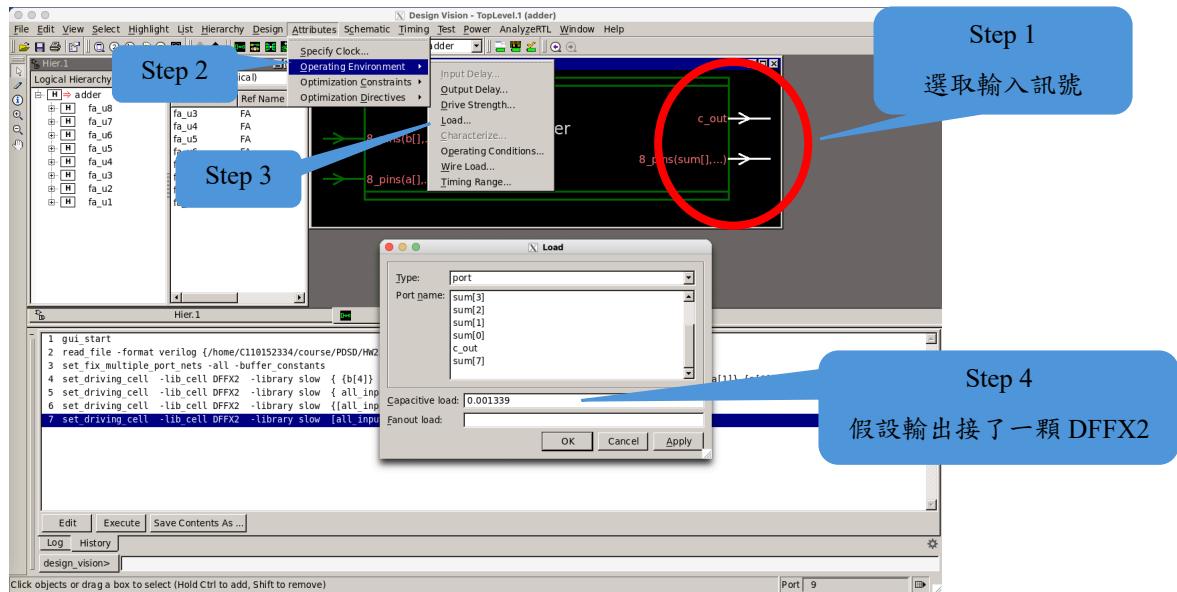


vii. Output Loading

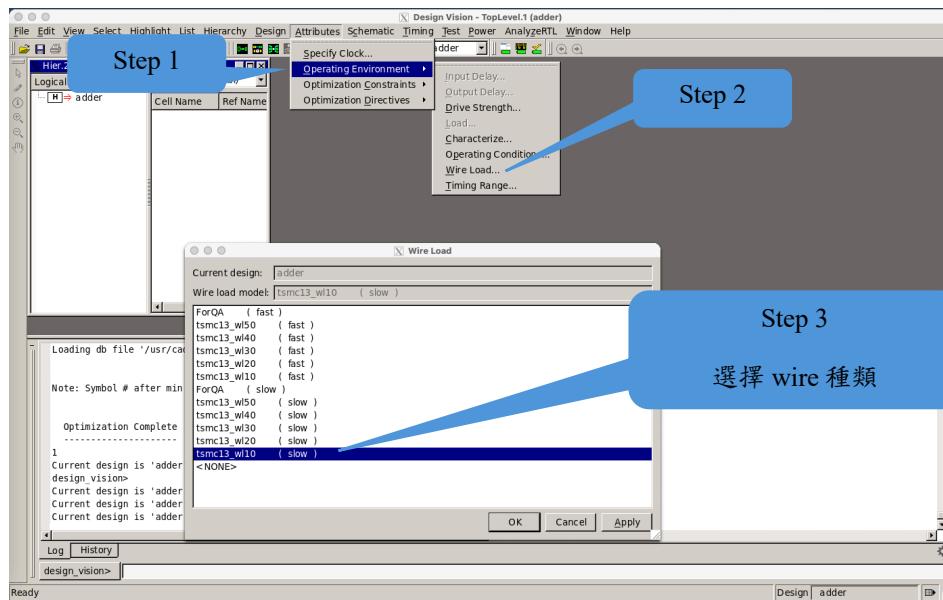
(1.) DFFX2 角位 D 的 Load

```
design_vision> load_of "slow/DFFX2/D"
0.001339
```

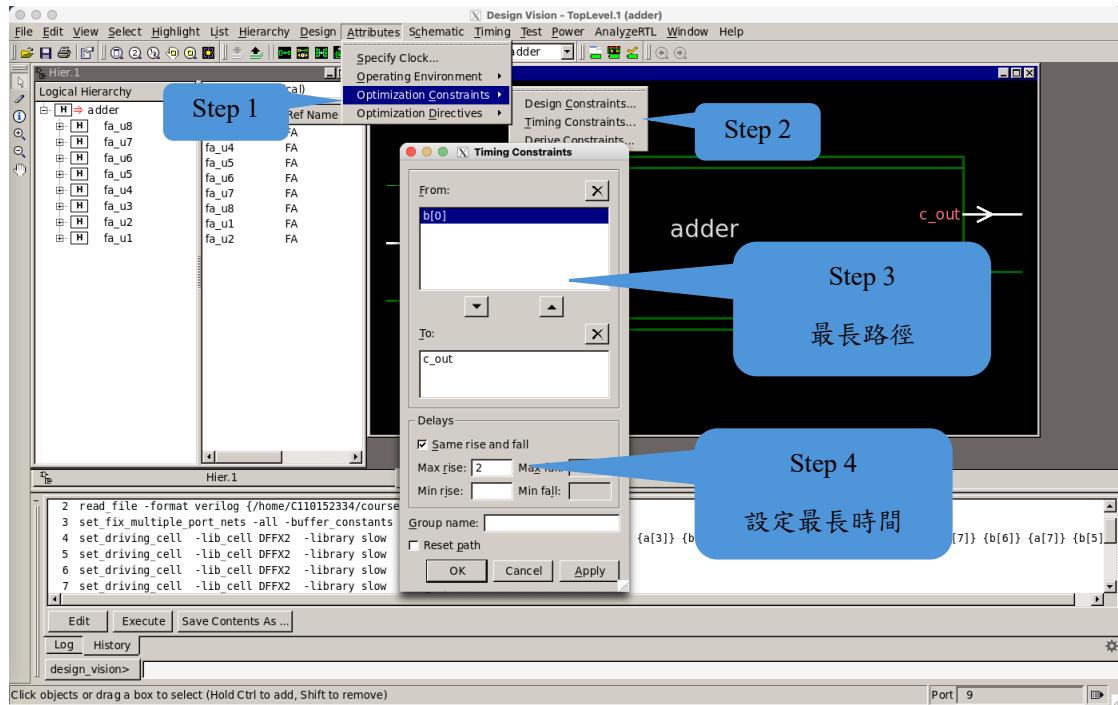
(2.) 設定輸出 Load



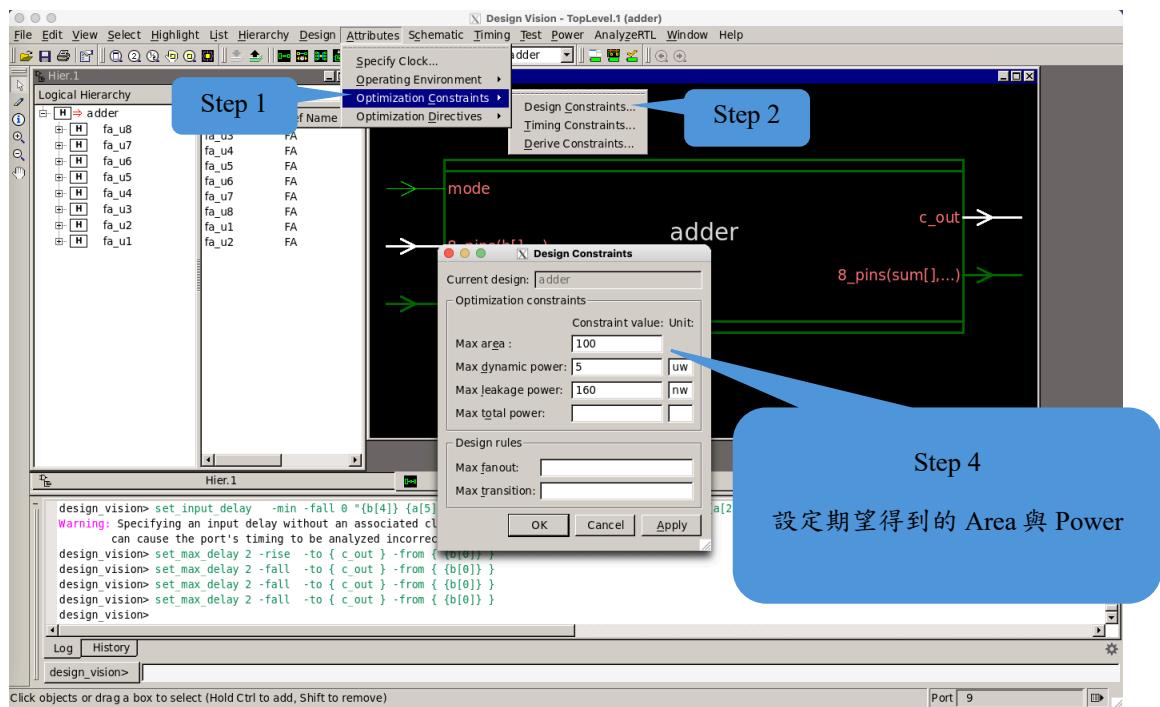
viii. Set Wire Load Model



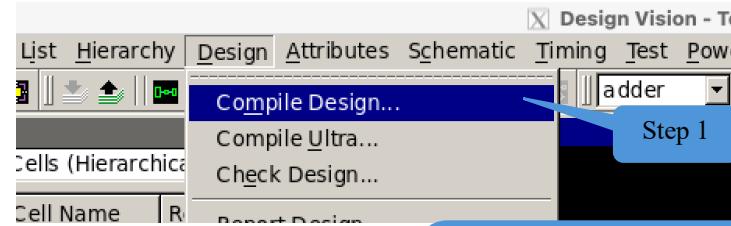
ix. Timing Constraints



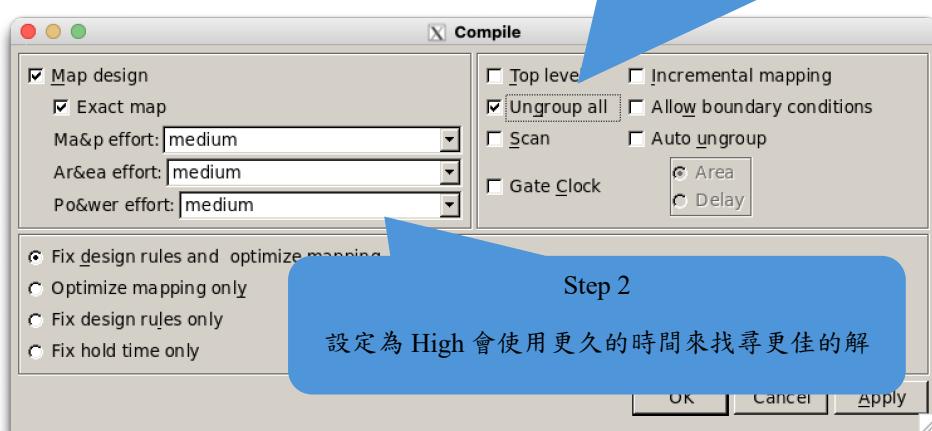
x. Area & Power Constraints



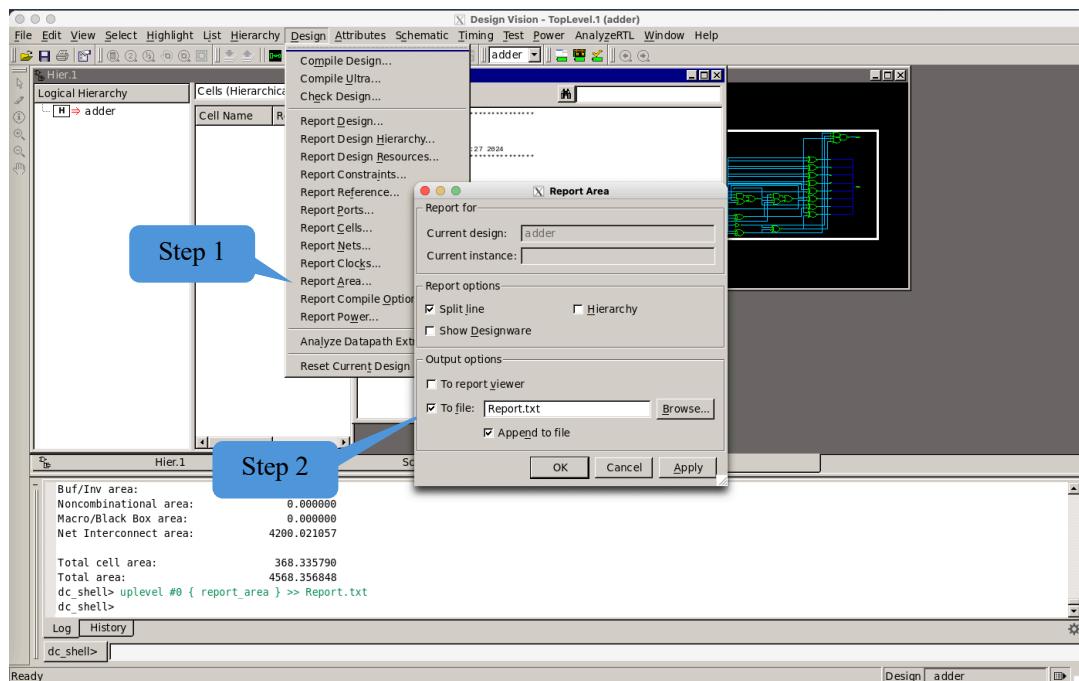
xi. Compile

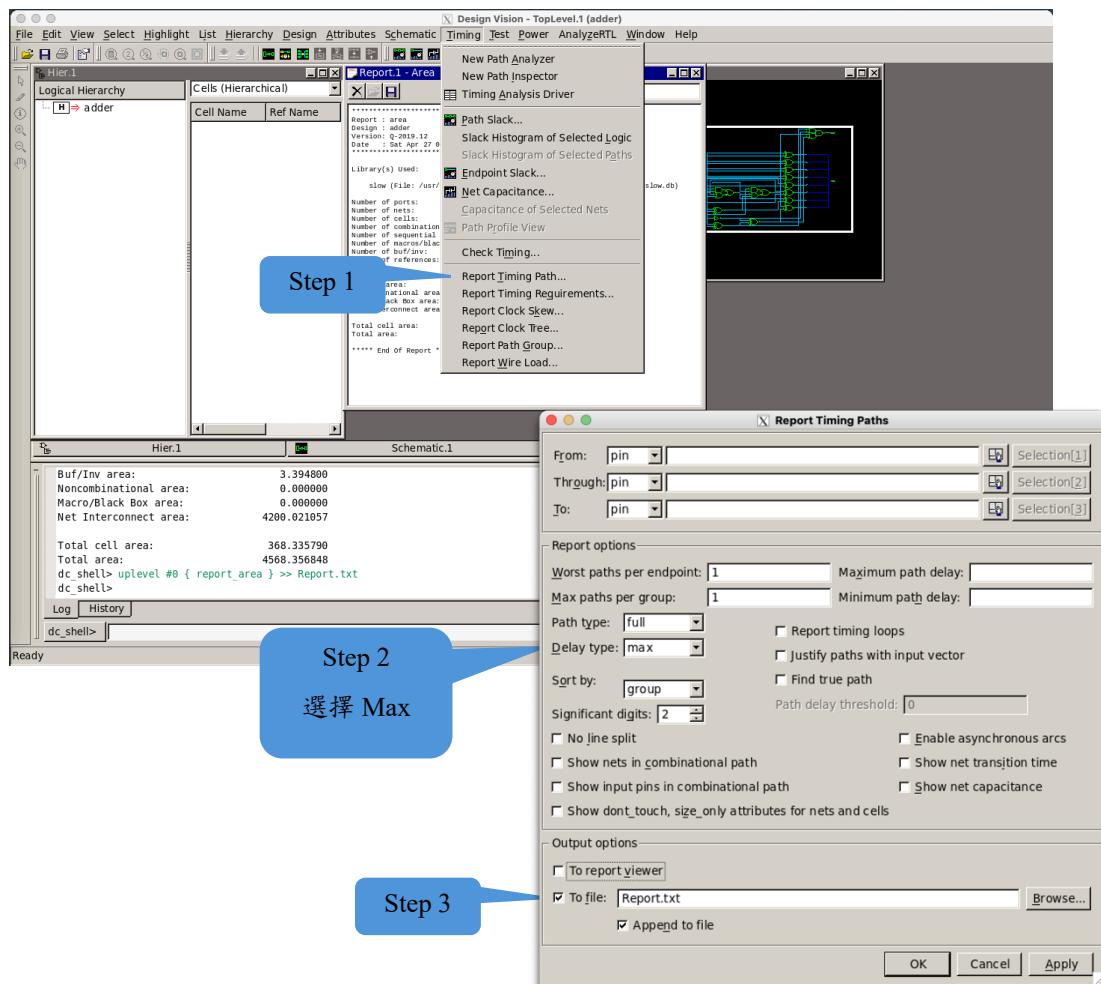


使用 Ungroup all 會打開 module 的界線，可以使結果更優化，
可是會喪失原本樣子會變得難以辨識電路。

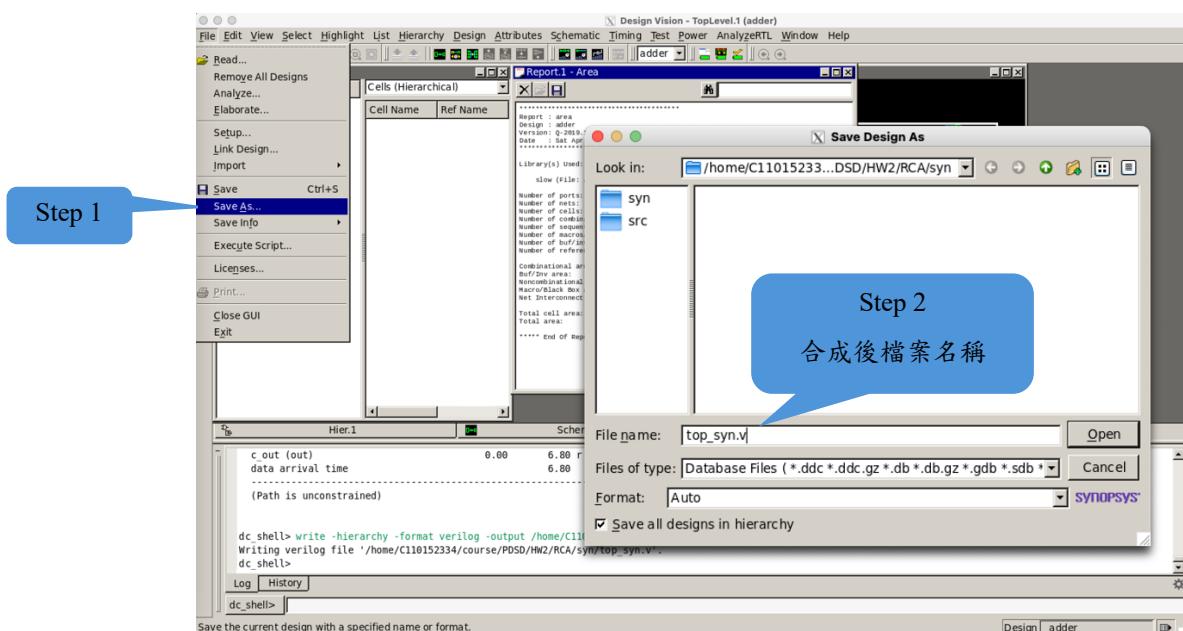


xii. Save Report Area & Timing & Power





xiii. Write Netlist



xiv. Write SDF

輸入 write_sdf -version 1.0 -context verilog top_syn.sdf

```
dc_shell> write_sdf -version 1.0 -context verilog top_syn.sdf
Information: Annotated 'cell' delays are assumed to include load delay. (UID-282)
Information: Writing timing information to file '/home/C110152334/course/PDSD/HW2/RCA/syn/top_syn.sdf'. (WT-3)
1
```

2. 電路分析

a. Area

Total Area : 412.4681 NAND2 : 5.0922

Gate Count : 80

```
*****
Report : area
Design : adder
Version: Q-2019.12
Date   : Sat Apr 27 11:17:37 2024
*****
Library(s) Used:
    slow (file: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Number of ports:          26
Number of nets:           66
Number of cells:          49
Number of combinational cells: 49
Number of sequential cells: 0
Number of macros/black boxes: 0
Number of buf/inv:         1
Number of references:      3

Combinational area:        412.468188
Buf/Inv area:              5.092200
Noncombinational area:     0.000000
Macro/Black Box area:      0.000000
Net Interconnect area:    4946.691467

Total cell area:          412.468188
Total area:                5555.159055
```

b. Max Delay : 5.51 ns

```
Startpoint: mode (input port)
Endpoint: c_out (output port)
Path Group: default
Path Type: max

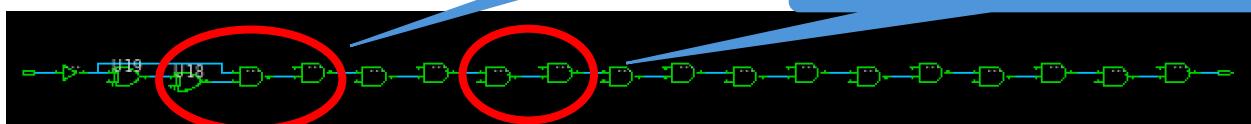
Des/Clust/Port      Wire Load Model      Library
-----              tsmc13_w110          slow

Point             Incr      Path
-----
input external delay      0.00    0.00 +
mode (in)            0.06    0.06 +
U20/Y (INX3)          0.35    0.41 +
U19/Y (XOR2X1)        0.44    0.85 +
U18/Y (XOR2X1)        0.46    1.31 +
U23/Y (NAND2X1)       0.19    1.50 +
U21/Y (NAND2X1)       0.31    1.81 +
U26/Y (NAND2X1)       0.18    1.99 +
U24/Y (NAND2X1)       0.31    2.30 +
U29/Y (NAND2X1)       0.18    2.48 +
U27/Y (NAND2X1)       0.31    2.79 +
U32/Y (NAND2X1)       0.18    2.97 +
U30/Y (NAND2X1)       0.31    3.28 +
U35/Y (NAND2X1)       0.18    3.46 +
U33/Y (NAND2X1)       0.31    3.77 +
U38/Y (NAND2X1)       0.18    3.95 +
U36/Y (NAND2X1)       0.31    4.25 +
U41/Y (NAND2X1)       0.18    4.44 +
U39/Y (NAND2X1)       0.31    4.74 +
U44/Y (NAND2X1)       0.18    4.93 +
U42/Y (NAND2X1)       0.18    5.11 +
c_out (out)           0.00    5.11 +
data arrival time     5.11
```

第一個 FA 的 Delay

c. 最長路徑

第一個 FA 之後的計算進位的 delay



d. Power

Dynamic Power : 176.8242 uW

Static Power : 458.8810 nW

```
*****
Report : power
          -analysis_effort low
Design : adder
Version: Q-2019.12
Date  : Sat Apr 27 11:19:09 2024
*****


Library(s) Used:

slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow Library: slow
Wire Load Model: top

Design      Wire Load Model      Library
-----
adder        tsmc13_wl10        slow

Global Operating Voltage = 1.08
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW   (derived from V,C,T units)
  Leakage Power Units = 1pW

  Cell Internal Power = 56.0633 uW (32%)
  Net Switching Power = 120.7609 uW (68%)
  -----
  Total Dynamic Power = 176.8242 uW (100%)

  Cell Leakage Power = 458.8810 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

      Internal      Switching      Leakage      Total
Power Group    Power       Power       Power     Power ( % ) Attrs
-----
io_pad         0.0000      0.0000      0.0000      0.0000 ( 0.00%)
memory         0.0000      0.0000      0.0000      0.0000 ( 0.00%)
black_box       0.0000      0.0000      0.0000      0.0000 ( 0.00%)
clock_network   0.0000      0.0000      0.0000      0.0000 ( 0.00%)
register        0.0000      0.0000      0.0000      0.0000 ( 0.00%)
sequential       0.0000      0.0000      0.0000      0.0000 ( 0.00%)
combinational   5.6063e-02    0.1208     4.5888e+05 pW      0.1773 ( 100.00%)
-----
Total          5.6063e-02 mW      0.1208 mW      4.5888e+05 pW      0.1773 mW
```

二、Carry Lookahead Adder (CLA)

1. 電路分析

a. Area

Total Area : 706.1184 NAND2 : 5.0922

Gate Count : 138

Startpoint: mode (input port)	Endpoint: c_out (output port)	Path Group: default
Des/Clust/Port	Wire Load Model	Library
adder	tsmc13_wl10	slow
Point	Incr	Path
input external delay	0.00	0.00 r
mode (in)	0.20	0.20 r
U10/Y (INVX8)	0.17	0.37 f
U39/Y (XOR2X1)	0.23	0.60 f
U16/Y (BUFX8)	0.18	0.78 f
U57/Y (AND2X2)	0.23	1.01 f
U55/Y (NOR2X6)	0.13	1.14 r
U71/Y (A021X4)	0.17	1.31 r
U67/Y (NAND3BX4)	0.13	1.44 f
U18/Y (AND4X4)	0.19	1.63 f
U72/Y (OA1Z21X2)	0.25	1.88 r
U68/Y (OA1ZBB1X2)	0.11	1.99 f
c_out (out)	0.00	1.99 r
data arrival time		1.99
max_delay	2.00	2.00
output external delay	0.00	2.00
data required time		2.00
data required time	2.00	
data arrival time		-1.99

b. Max Delay: 1.99 ns

Report : area	
Design : adder	
Version: Q-2019.12	
Date : Sat Apr 27 11:33:03 2024	

Library(s) Used:	
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)	
Number of ports:	26
Number of nets:	80
Number of cells:	63
Number of combinational cells:	63
Number of sequential cells:	0
Number of macros/black boxes:	0
Number of buf/inv:	20
Number of references:	30
Combinational area:	706.118400
Buf/Inv area:	86.567398
Noncombinational area:	0.000000
Macro/Black Box area:	0.000000
Net Interconnect area:	6533.366089
Total cell area:	706.118400
Total area:	7239.000000

c. 最長路徑



d. Power

Dynamic Power : 229.4575 uW
Static Power : 676.9463 nW

```
*****
Report : power
    -analysis_effort low
Design : adder
Version: Q-2019.12
Date   : Sat Apr 27 11:35:36 2024
*****


Library(s) Used:
    slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----
adder          tsmc13_wl10        slow

Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW      (derived from V,C,T units)
    Leakage Power Units = 1pW

Cell Internal Power = 88.3840 uW (39%)
Net Switching Power = 141.0755 uW (61%)
-----
Total Dynamic Power = 229.4575 uW (100%)
Cell Leakage Power = 696.9463 nW

Information: Report power power group summary does not include estimated clock tree power. (PWR-789)

      Internal      Switching      Leakage      Total
Power Group    Power       Power       Power     Power ( % ) Attrs
-----
io_pad         0.0000      0.0000      0.0000      0.0000 ( 0.00%)
memory         0.0000      0.0000      0.0000      0.0000 ( 0.00%)
black_box       0.0000      0.0000      0.0000      0.0000 ( 0.00%)
clock_network   0.0000      0.0000      0.0000      0.0000 ( 0.00%)
register        0.0000      0.0000      0.0000      0.0000 ( 0.00%)
sequential       0.0000      0.0000      0.0000      0.0000 ( 0.00%)
combinational  8.8384e-02  0.1411    6.9695e+05  0.2302 ( 100.00%)
-----
Total        8.8384e-02 mW    0.1411 mW    6.9695e+05 pW    0.2302 mW
```

三、Carry Select Adder (CSEA)

1. 電路分析

a. Area :

Total Area : 1050.6905 NAND2 : 5.0922

Gate Count : 206

```
*****
Report : area
Design : adder
Version: Q-2019.12
Date  : Sat Apr 27 11:10:53 2024
*****  
Library(s) Used:  
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)  
Number of ports: 26  
Number of nets: 90  
Number of cells: 89  
Number of combinational cells: 57  
Number of sequential cells: 32  
Number of macros/black boxes: 0  
Number of buf/inv: 16  
Number of references: 30  
Combinational area: 573.721191  
Buf/Inv area: 101.843998  
Noncombinational area: 476.969400  
Macro/Black Box area: 0.000000  
Net Interconnect area: 8726.710449  
Total cell area: 1050.690591  
Total area: 8727.401044
```

b. Max Delay : 2.99 ns

```
*****
Report : timing
-path full
-delay max
-max_paths 1
Design : adder
Version: Q-2019.12
Date  : Sat Apr 27 11:12:48 2024
*****  
Operating Conditions: slow Library: slow
Wire Load Model Mode: top  
Startpoint: mode (input port)
Endpoint: c.out (output port)
Path Group: default
Path Type: max  
Des/Clust/Port      Wire Load Model      Library
adder              tsmc13_wl10      slow  
Point           Incr     Path
-----  
input external delay    0.00   0.00 r
mode (in)            0.17   0.17 r
U0/Y (INX12)          0.15   0.33 f
U20/Y (XNOR2X4)       0.16   0.49 r
U19/Y (NAND2X4)       0.08   0.58 f
fu.u/m2/_tmp301/Y (TBUFX3) 0.34   0.92 f
U12/Y (CLKINX8)        0.08   1.00 r
fu.u/m2/_tmp300/Y (TBUFX6) 0.23   1.23 f
U13/Y (CLKINX3)        0.10   1.34 r
fu.u/m2/_tmp300/Y (TBUFX16) 0.17   1.51 f
U37/Y (INX4)            0.11   1.63 r
fu.u/m2/_tmp300/Y (TBUFX16) 0.18   1.81 f
U22/Y (INX3)            0.11   1.92 r
fu.u/m2/_tmp300/Y (TBUFX16) 0.18   2.11 f
U38/Y (INX3)            0.10   2.21 r
fu.u/m2/_tmp301/Y (TBUFX6) 0.16   2.37 r
fu.u/m2/_tmp300/Y (TBUFX6) 0.28   2.65 f
U41/Y (INX1)             0.12   2.77 r
fu.u/m2/_tmp300/Y (TBUFX3) 0.22   2.99 f
c.out (out)            0.00   2.99  
data arrival time      2.99  
max_delay            3.00   3.00
output external delay  0.00   3.00
data required time     3.00  
-----  
data required time     3.00
data arrival time      -2.99
-----  
slack (MET)           0.01
```

c. 最長路徑

第一個級的 Multiplexer

第一個級後的 Multiplexer



d. Power

Dynamic Power : 121.9634 uW

Static Power : 232.9054 nW

```
*****
Report : power
    -analysis_effort low
Design : adder
Version: Q-2019.12
Date  : Sat Apr 27 11:22:50 2024
*****


Library(s) Used:

    slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----
adder        tsmc13_wl10        slow

Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW   (derived from V,C,T units)
    Leakage Power Units = 1pW

    Cell Internal Power = 131.9634 uW (36%)
    Net Switching Power = 232.9054 nW (64%)
    -----
    Total Dynamic Power = 364.8689 uW (100%)
    Cell Leakage Power = 1.3561 uW

Information: Report_Power_Group summary does not include estimated clock tree power. (PWR-789)

          Internal      Switching      Leakage      Total
Power Group     Power       Power       Power      Power ( % ) Attrs
-----
io_pad         0.0000      0.0000      0.0000      0.0000 ( 0.00% )
memory         0.0000      0.0000      0.0000      0.0000 ( 0.00% )
black_box       0.0000      0.0000      0.0000      0.0000 ( 0.00% )
clock_network   0.0000      0.0000      0.0000      0.0000 ( 0.00% )
register        0.0000      0.0000      0.0000      0.0000 ( 0.00% )
sequential       0.0000      0.0000      0.0000      0.0000 ( 0.00% )
combinational   0.1320      0.2329      1.3561e+06 pW      0.3662 mW
-----
Total          0.1320 mW      0.2329 mW      1.3561e+06 pW      0.3662 mW
```

四、Adder 模擬

1. 在 tb 中加入 SDF 檔案

```
`ifdef SDF
    initial $sdf_annotation("../syn/adder_syn.sdf", adder_u1);
`endif
```

SDF 檔路徑

2. 開始執行 (+define+SDF)

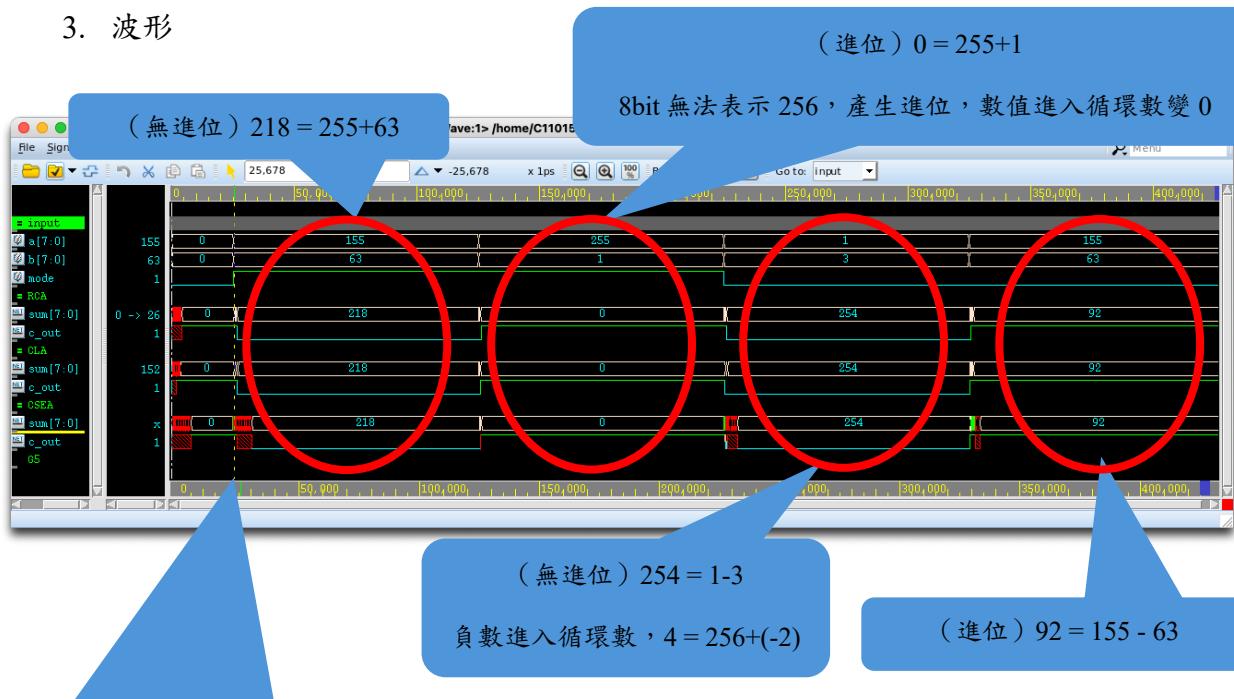
```
Reading SDF file from location "../syn/adder_syn.sdf"
Annotating SDF timing data:
    Compiled SDF file:      adder_syn.sdf.X
    Log file:
    Backannotation scope:  testfixture.adder_u1
    Configuration file:
    MTM control:
    Scale factors:
    Scale type:
Annotation completed successfully...
SDF statistics: No. of Pathdelays = 212 Annotated = 100.00% -- No. of Tchecks = 0 Annotated = 0.00%
```

SDF 成功讀入

```
=====
Mode | A | B | Sum | C_out | t_sum
=====
Pattern | 1 Success | 1 | 155 | 63 | 218 | 0 | 218 |
Pattern | 2 Success | 1 | 255 | 1 | 0 | 1 | 0 |
Pattern | 3 Success | 0 | 1 | 3 | 254 | 0 | 254 |
Pattern | 4 Success | 0 | 155 | 63 | 92 | 1 | 92 |
=====
Test Result: 4 Success, 0 Error
=====
Simulation complete via $finish(1) at time 425 NS + v
./testfixture.v:100          $finish;
ncsim> exit
```

模擬成功

3. 波形



可以發現合成後加入延遲，輸入訊號更改後會先進入轉換的狀態
之後才會進入穩態，轉換的最大時間為 Max Delay

五、 Voting

1. 電路分析

a. Area

Total Area : 398.88899 NAND2 : 5.0922

Gate Count : 78

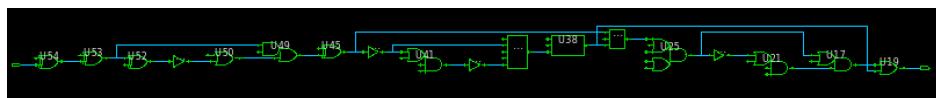
```
*****
Report : area
Design : voting
Version: Q-2019.12
Date   : Sat Apr 27 11:47:58 2024
*****  
*****  
Library(s) Used:  
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)  
  
Number of ports: 18  
Number of nets: 62  
Number of cells: 47  
Number of combinational cells: 47  
Number of sequential cells: 0  
Number of macros/black boxes: 0  
Number of buf/inv: 9  
Number of references: 18  
  
Combinational area: 398.888995  
Buf/Inv area: 30.553200  
Noncombinational area: 0.000000  
Macro/Black Box area: 0.000000  
Net Interconnect area: 5413.360474  
  
Total cell area: 398.888995  
Total area: 5413.360474
```

b. Max Delay : 6.89ns

```
Startpoint: a1[1] (input port)
Endpoint: out[1] (output port)
Path Group: (none)
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----  
voting          tsmc13_wl10      slow  
  
Point           Incr     Path
-----  
input external delay  0.00    0.00 r  
a1[1] (in)       0.09    0.09 r  
U54/Y (XOR2X1)   0.35    0.44 r  
U53/Y (XOR2X1)   0.47    0.91 r  
U52/Y (XOR2X1)   0.55    1.47 r  
U51/Y (CLKINVX1) 0.25    1.72 f  
U50/Y (NOR2BX1)  0.38    2.10 r  
U49/Y (A021X1)   0.37    2.47 r  
U45/Y (XOR2X1)   0.52    2.99 r  
U44/Y (CLKINVX1) 0.36    3.35 f  
U41/Y (OAI211X1) 0.35    3.69 r  
U40/Y (CLKINVX1) 0.19    3.88 f  
U39/Y (A0I221XL) 0.51    4.39 r  
U38/Y (A0I2B1X1) 0.47    4.86 f  
U37/Y (MXI2X1)   0.34    5.20 f  
U25/Y (OAI32X1)   0.54    5.73 r  
U23/Y (CLKINVX1) 0.25    5.98 f  
U21/Y (OAI211X1) 0.32    6.30 r  
U17/Y (OAI21X1)   0.33    6.63 f  
U19/Y (NOR2X1)   0.26    6.89 r  
out[1] (out)      0.00    6.89 r  
data arrival time 6.89
```

c. 最長路徑



d. Power

Dynamic Power : 198.9326 uW

Static Power : 403.4597 nW

```
Library(s) Used:
    slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow  Library: slow
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----
voting          tsmc13_wl10        slow

Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW   (derived from V,C,T units)
    Leakage Power Units = 1pW

    Cell Internal Power = 52.7316 uW (27%)
    Net Switching Power = 146.1509 uW (77%)
    -----
    Total Dynamic Power = 198.9326 uW (100%)
    Cell Leakage Power = 403.4597 nW

Information: report_power power_group summary does not include estimated clock tree power. (PWR-789)

          Internal      Switching      Leakage      Total
Power Group    Power       Power       Power     Power  ( % )  Attrs
-----
io_pad        0.0000      0.0000      0.0000      0.0000 ( 0.00%)
memory        0.0000      0.0000      0.0000      0.0000 ( 0.00%)
black_box     0.0000      0.0000      0.0000      0.0000 ( 0.00%)
clock_network 0.0000      0.0000      0.0000      0.0000 ( 0.00%)
register      0.0000      0.0000      0.0000      0.0000 ( 0.00%)
sequential     0.0000      0.0000      0.0000      0.0000 ( 0.00%)
combinational 5.2782e-02    0.1462    4.0346e+05    0.1993 ( 100.00%)
-----
Total        5.2782e-02 mW      0.1462 mW      4.0346e+05 pW      0.1993 mW
```

六、Voting 模擬

1. 在 tb 中加入 SDF 檔案

```
`ifdef SDF  
    initial $sdf_annotate("../syn/median_syn.sdf",dut);  
`endif
```

SDF 檔路徑

2. 開始執行 (+define+SDF)

```
Reading SDF file from location "../syn/voting_syn.sdf"  
Annotating SDF timing data:  
    Compiled SDF file: voting_syn.sdf.X  
    Log file:  
    Backannotation scope: tb.dut  
    Configuration file:  
    MTM control:  
    Scale factors:  
    Scale type:  
Annotation completed successfully...  
SDF statistics: No. of Pathdelays = 143 Annotated = 100.00% -- No. of Tchecks = 0 Annotated = 0.00%  
Build time: 0.000 seconds
```

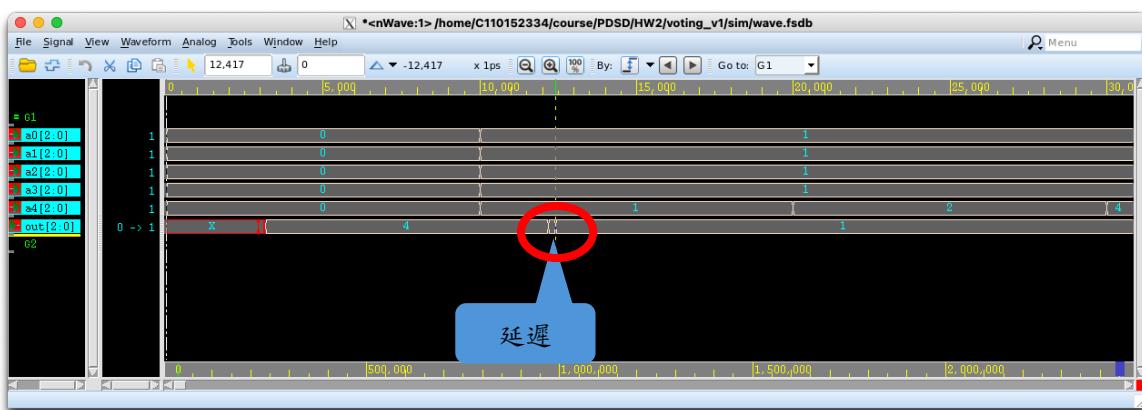
SDF 成功讀入

驗證方法：由於此電路輸入狀態僅有 243 種，所以使用窮舉的方式驗證此電路。

```
235 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:001 a4:010  
236 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:001 a4:100  
237 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:010 a4:001  
238 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:010 a4:010  
239 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:010 a4:100  
240 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:100 a4:001  
241 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:100 a4:010  
242 Success Target answer:100 Your answer:100 a0:100 a1:100 a2:100 a3:100 a4:100  
All Success  
Simulation complete via $finish(1)  
./tb_voting.v:122  
ncsim> exit
```

模擬成功

3. 波形



七、Median_v1

1. 電路分析

a. Area

Total Area : 745.1585 NAND2 : 5.0922

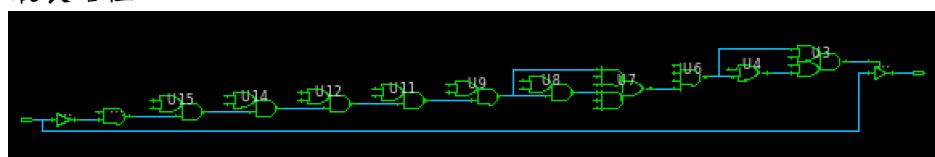
Gate Count : 146

```
Library(s) Used:  
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)  
  
Number of ports: 32  
Number of nets: 94  
Number of cells: 86  
Number of combinational cells: 62  
Number of sequential cells: 24  
Number of macros/black boxes: 0  
Number of buf/inv: 17  
Number of references: 10  
  
Combinational area: 500.733008  
Buf/Inv area: 57.711599  
Noncombinational area: 244.425591  
Macro/Black Box area: 0.000000  
Net Interconnect area: 11993.393463  
  
Total cell area: 745.158598  
Total area: 1238.552061
```

b. Max Delay : 6.62 ns

```
Startpoint: a1[7] (input port)  
Endpoint: out[7] (output port)  
Path Group: (none)  
Path Type: max  
  
Des/Clust/Port      Wire Load Model      Library  
-----  
median              tsmc13_wl10          slow  
  
Point                Incr      Path  
-----  
input external delay 0.00      0.00 r  
a1[7] (in)           0.18      0.18 r  
U46/Y (CLKINVX1)    0.25      0.43 f  
U17/Y (NAND2X1)    0.32      0.75 r  
U15/Y (OA21XL)     0.54      1.29 r  
U14/Y (OA21XL)     0.56      1.84 r  
U12/Y (OA21XL)     0.56      2.40 r  
U11/Y (OA21XL)     0.56      2.95 r  
U9/Y (OA21XL)      0.56      3.51 r  
U8/Y (OA21XL)      0.56      4.07 r  
U7/Y (AOI33X1)      0.28      4.35 f  
U6/Y (NAND4X1)      0.56      4.91 r  
U4/Y (NOR2BX1)      0.36      5.27 f  
U2/Y (OAI22X2)      0.72      5.99 r  
u5_Selecter/out_tri[7]/Y (TBUFXL) 0.63      6.62 r  
out[7] (out)         0.00      6.62 r  
data arrival time   6.62  
-----  
(Path is unconstrained)
```

c. 最長路徑



d. Power

Dynamic Power : 241.3855 uW
Static Power : 685.3362 nW

```
*****
Report : power
-analyses_effort low
Design : median
Version: Q-2019.12
Date : Sat Apr 27 13:26:07 2024
*****


Library(s) Used:
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----      -----      -----
median        tsmc13_wl10      slow

Global Operating Voltage = 1.08
Power-specific unit information :
  Voltage Units = IV
  Capacitance Units = 1.000000pF
  Time Units = 1ns
  Dynamic Power Units = 1mW      (derived from V,C,T units)
  Leakage Power Units = 1pW

Cell Internal Power = 47.1952 uW (20%)
Net Switching Power = 194.1903 uW (80%)
-----
Total Dynamic Power = 241.3855 uW (100%)
Cell Leakage Power = 685.3362 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

      Internal          Switching          Leakage          Total
Power Group    Power       Power       Power       Power ( % ) Attrs
-----      -----      -----      -----      -----
io_pad        0.0000     0.0000     0.0000     0.0000 ( 0.00% )
memory        0.0000     0.0000     0.0000     0.0000 ( 0.00% )
black_box     0.0000     0.0000     0.0000     0.0000 ( 0.00% )
clock_network 0.0000     0.0000     0.0000     0.0000 ( 0.00% )
register      0.0000     0.0000     0.0000     0.0000 ( 0.00% )
sequential     0.0000     0.0000     0.0000     0.0000 ( 0.00% )
combinational 4.7195e-02   0.1942    6.8534e+05 pW   0.2421 mW
-----
Total        4.7195e-02 mW    0.1942 mW    6.8534e+05 pW   0.2421 mW
```

八、Median_v2

1. 電路分析

a. Area

Total Area : 329.295596 NAND2 : 5.0922

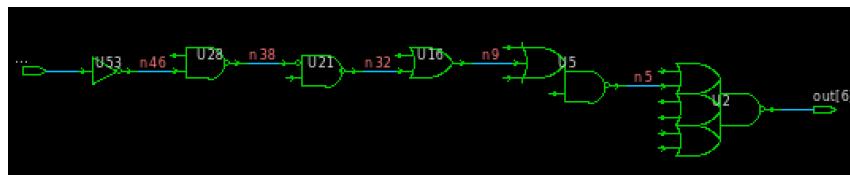
Gate Count : 65

```
Library(s) Used:  
slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)  
  
Number of ports: 32  
Number of nets: 78  
Number of cells: 54  
Number of combinational cells: 54  
Number of sequential cells: 0  
Number of macros/black boxes: 0  
Number of buf/inv: 19  
Number of references: 12  
  
Combinational area: 329.295596  
Buf/Inv area: 64.501199  
Noncombinational area: 0.000000  
Macro/Black Box area: 0.000000  
Net Interconnect area: 6206.697784  
  
Total cell area: 329.295596  
Total area: 6555.002150
```

b. Max Delay : 2.63 ns

```
Operating Conditions: slow Library: slow  
Wire Load Model Mode: top  
  
Startpoint: a0[1] (input port)  
Endpoint: out[6] (output port)  
Path Group: (none)  
Path Type: max  
  
Des/Clust/Port      Wire Load Model      Library  
-----  
median             tsmc13_wl10      slow  
  
Point           Incr      Path  
-----  
input external delay 0.00  0.00 f  
a0[1] (in)        0.09  0.09 f  
U51/Y (NOR2X1)    0.34  0.43 r  
U49/Y (NOR2BX1)   0.45  0.88 r  
U21/Y (NAND2BX1)  0.27  1.14 f  
U16/Y (OR2X1)     0.53  1.67 f  
U5/Y (OAI31XL)    0.58  2.25 r  
U2/Y (OAI222XL)   0.37  2.63 f  
out[6] (out)       0.00  2.63 f  
data arrival time 2.63
```

c. 最長路徑



d. Power

Dynamic Power : 59.1517 uW

Static Power : 172.1662 nW

```
*****
Report : power
    -analysis_effort low
Design : median
Version: Q-2019.12
Date   : Sat Apr 27 14:38:00 2024
*****
```

Library(s) Used:

slow (File: /usr/cad/designkit/CBDK_IC_Contest_v2.1/SynopsysDC/db/slow.db)

Operating Conditions: slow Library: slow
Wire Load Model Mode: top

Design	Wire Load Model	Library
median	tsmc13_wl10	slow

Global Operating Voltage = 1.08

Power-specific unit information :

Voltage Units	= 1V
Capacitance Units	= 1.000000pf
Time Units	= 1ns
Dynamic Power Units	= 1mW (derived from V,C,T units)
Leakage Power Units	= 1pW

Cell Internal Power = 11.0477 uW (19%)
Net Switching Power = 48.1040 uW (81%)

Total Dynamic Power = 59.1517 uW (100%)

Cell Leakage Power = 172.1662 nW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	0.0000	0.0000	0.0000	0.0000	(0.00%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	1.1048e-02	4.8104e-02	1.7217e+05	5.9324e-02	(100.00%)	
Total	1.1048e-02 mW	4.8104e-02 mW	1.7217e+05 pW	5.9324e-02 mW		

九、Median 模擬

- 在 tb 中加入 SDF 檔案

```
`ifdef SDF  
    initial $sdf_annotate("../syn/median_syn.sdf",dut);  
`endif
```

SDF 檔路徑

- 開始執行 (+define+SDF)

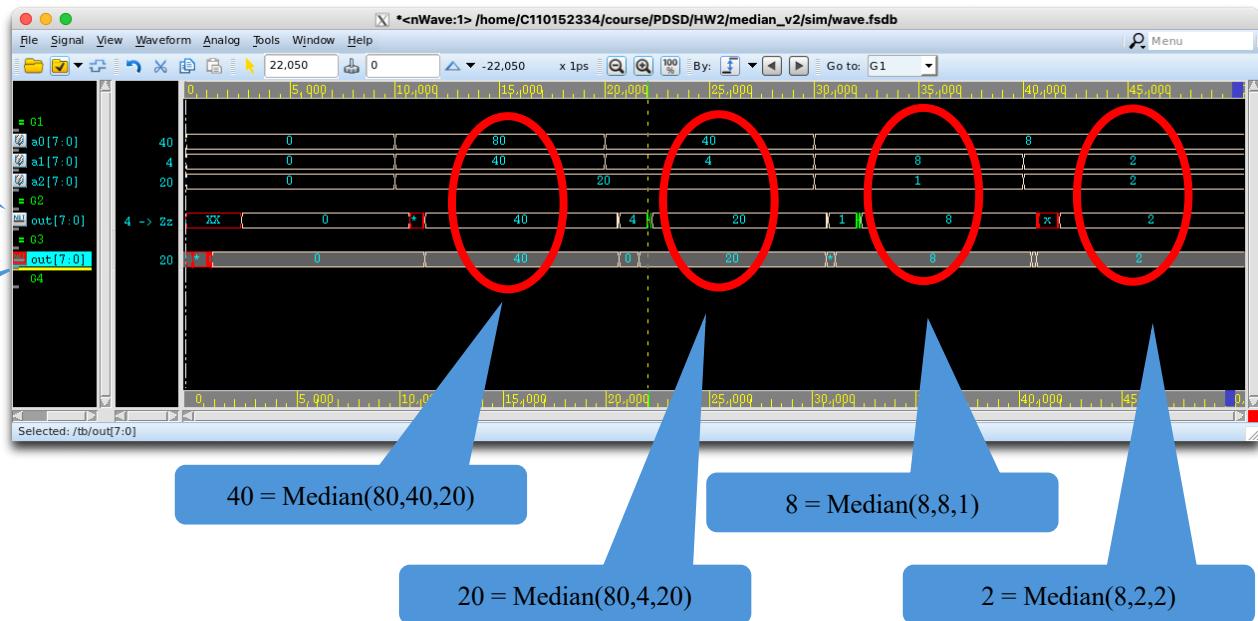
```
Annotating SDF timing data:  
Compiled SDF file: median_syn.sdf.X  
Log file:  
Backannotation scope: tb.dut  
Configuration file:  
MTM control:  
Scale factors:  
Scale type:  
Annotation completed successfully...  
SDF statistics: No. of Pathdelays = 233 Annotated = 100.00% -- No. of Tchecks = 0 Annotated = 0.00%
```

SDF 成功讀入

```
Success Target answer:01000000 Your answer:01000000 a0:10000000 a1:01000000 a2:00100000  
Success Target answer:00100000 Your answer:00100000 a0:01000000 a1:00000100 a2:00100000  
Success Target answer:00001000 Your answer:00001000 a0:00001000 a1:00001000 a2:00000001  
Success Target answer:00000010 Your answer:00000010 a0:00001000 a1:00000010 a2:00000010  
Simulation complete via $finish(1) at time 50 NS + 0  
./tb_median.v:76 $finish();  
ncsim> exit
```

模擬成功

- 波形



十、比較

1. Adder

	Area	Delay
RCA	412.4681	5.51
CSEA	706.1184	1.99
CLA	1050.6905	2.99

Area : RCA < CSEA < CLA

Speed : CSEA < CLA < RCA

2. Median

	Area	Delay
V1	745.1585	6.62
V2	329.295596	2.63

Area : V1 < V2

Speed : V1 > V2

十一、心得

這次作業中最具挑戰性的部分是撰寫 TCL 腳本來執行。由於使用圖形界面雖然方便，但不盡適用，因此我決定自行編寫 TCL 腳本。我參考了首次執行圖形界面所生成的指令，並結合實驗室資源以及之前參加的 IC 設計競賽所提供的腳本，最終成功打造出一份相對通用的腳本，以提高後續項目的合成效率。

在某些合成過程中，我遭遇了不少問題。例如，在合成 CLA 電路時，發現 Lookahead 結構與預期不符，從平行計算轉為串級的方式。為解決此問題，我嘗試了各種調整合成參數的方法，經過多次嘗試後，最後才成功合成出符合預期的電路結構。

這是我第一次使用圖形界面來使用 Design Compile。我發現與文字界面相比，最大的差異在於使用者體驗。圖形界面提供了更直觀的操作介面，方便用戶查找相關設定。相反，文字界面下需要熟悉指令才能完成操作，對於不熟悉的人來說可能較為困難。然而，我相信一旦熟悉後，文字界面的效率將優於圖形界面。