Midterm Report

ECE 437 : Computer Design and Prototyping

Name: Chongjin Chua

Michael Malachowski

TAs: Mengchi Zhang

Noah Chesnut

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4.2 Overview

The performance of each design is determined by analyzing the maximum frequency, average IPC, latency, performance in MIPS, and FPGA resources. These parameters are obtained from various log files which are detailed in the results sections. The benefits of the single cycle design are that it has a lower instruction latency, higher performance, and is a simpler design. The benefits of the pipelined design are that it can run at a higher frequency than the single cycle design, with a higher throughput. While the pipelined design has a higher clock frequency, it still has lower performance (measured in MIPS) than the single cycle design. In addition, the pipelined design has a higher instruction latency and requires more FPGA resources.

In order to test the designs, the program Mergesort.asm is used because it not only covers a wide variety of MIPS instructions, but also contains a fair amount of dependencies between R-type and I-type instructions. This program structure turns out to be a good test program in validating the functionality of hazard unit and forwarding unit of the pipeline design. As a conclusion, pipelining the processor improves its throughput, allowing a higher number of instructions to be executed at a time. This would result in a shorter duration needed to execute a test program. Besides, multiple pipeline stages reduces the length of critical path, which in turn increases the clock speed of the design.

4.3 Processor Design

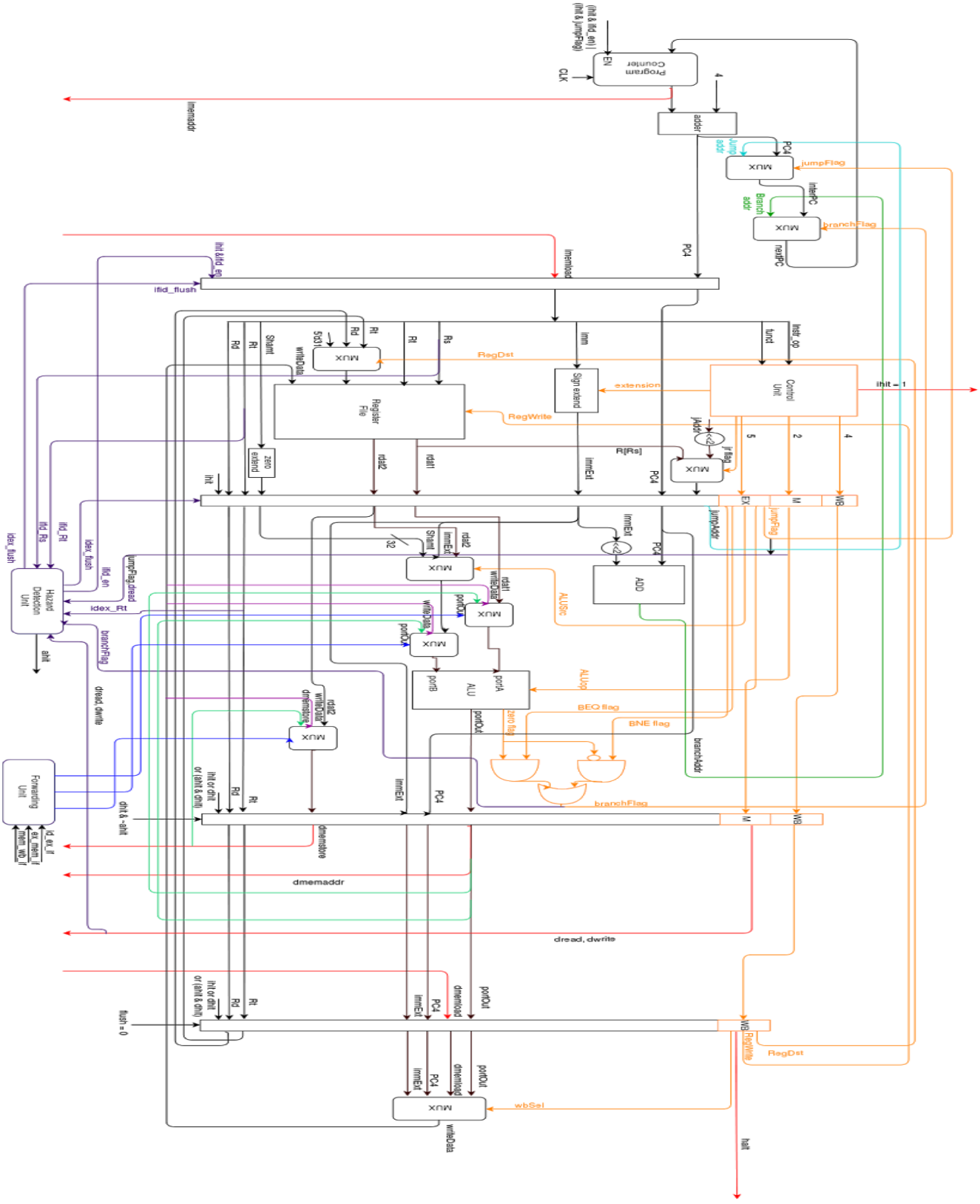


Figure 1: Pipeline design

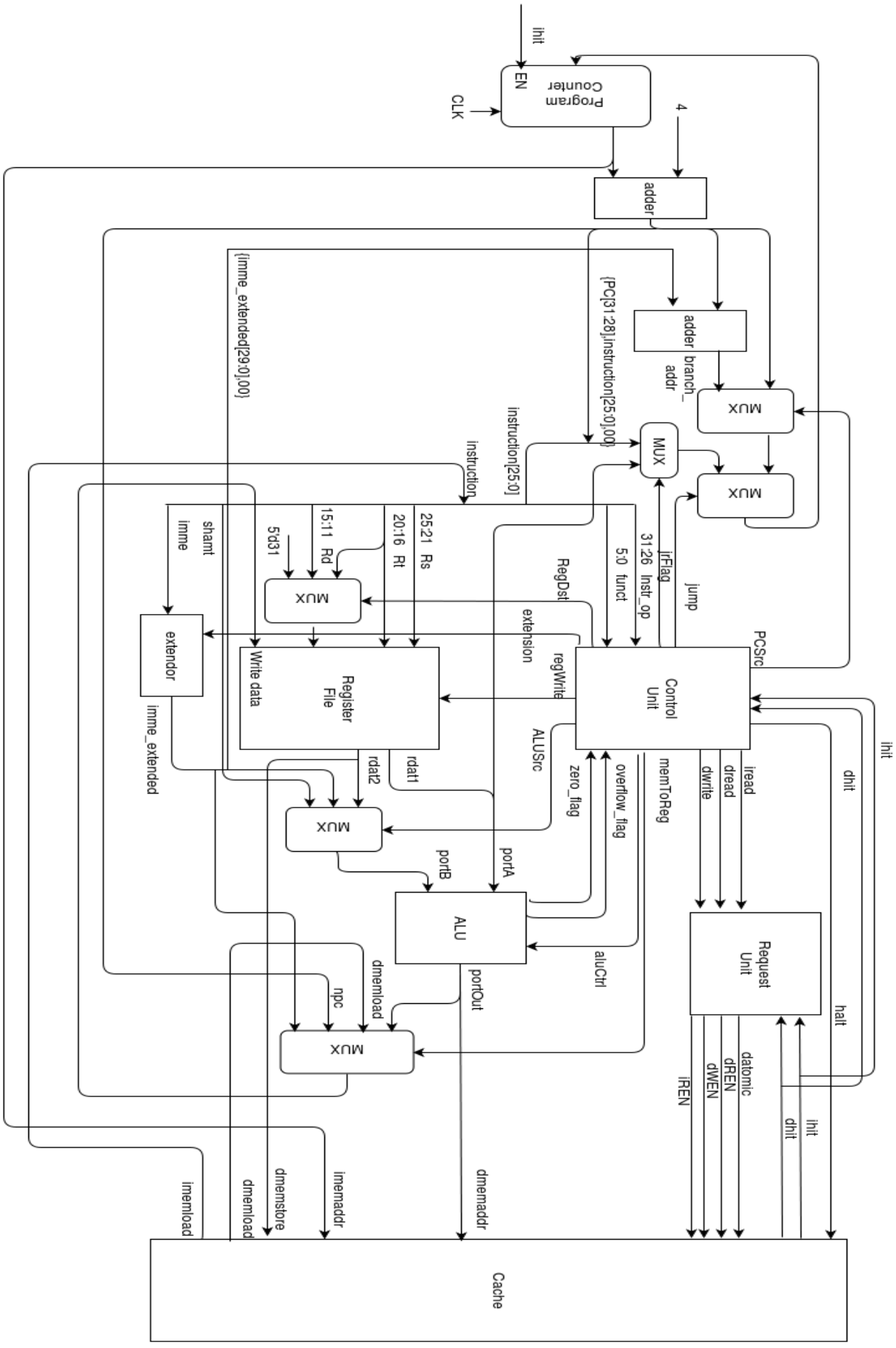


Figure 2: Single Cycle design

4.4 Results

The following results are obtained by running both designs on ‘mergesort.asm’ test program with a RAM latency of 0. The total number of instructions executed are obtained from the assembler; The time to run the test program is obtained from the simulator; and the FPGA resources used are obtained from Fitter Report. Both designs are run at their full capacity, which is a clock period of 20ns for single cycle and 10ns for pipeline design.

Formula for Instruction Latency:

$$Instruction\ Latency\ =\ \frac{Number\ of\ Stages}{Maximum\ Frequency}$$

Formula for Average Instructions Per Cycle:

$$Average\ Instructions\ Per\ Cycle\ =\ \frac{Number\ of\ Instructions\ in\ Program}{Number\ of\ CPU\ Clock\ Cycles}$$

Maximum Theoretical CPUCLK Frequency (MHz)	34.665
Maximum Testbench CPUCLK (MHz)	25
Instruction Latency (ns)	40
Average Instructions Per CPUCLK Clock Cycle	.7828
MIPS	19.750
Total Logic Elements	3187/114480
Total Combinational Functions	2923/114480
Logic Registers	1279/114480
Total Registers	1279
Memory Bits	524288

Figure 3: Single Cycle Table

Maximum Theoretical CPUCLK Frequency (MHz)	50.32
Maximum Testbench CPUCLK (MHz)	50
Instruction Latency (ns)	20
Average Instructions Per CPUCLK Clock Cycle	.3462
MIPS	17.309
Total Logic Elements	3643/114480
Total Combinational Functions	3316/114480
Logic Registers	1788/114480
Total Registers	1789
Memory Bits	524288

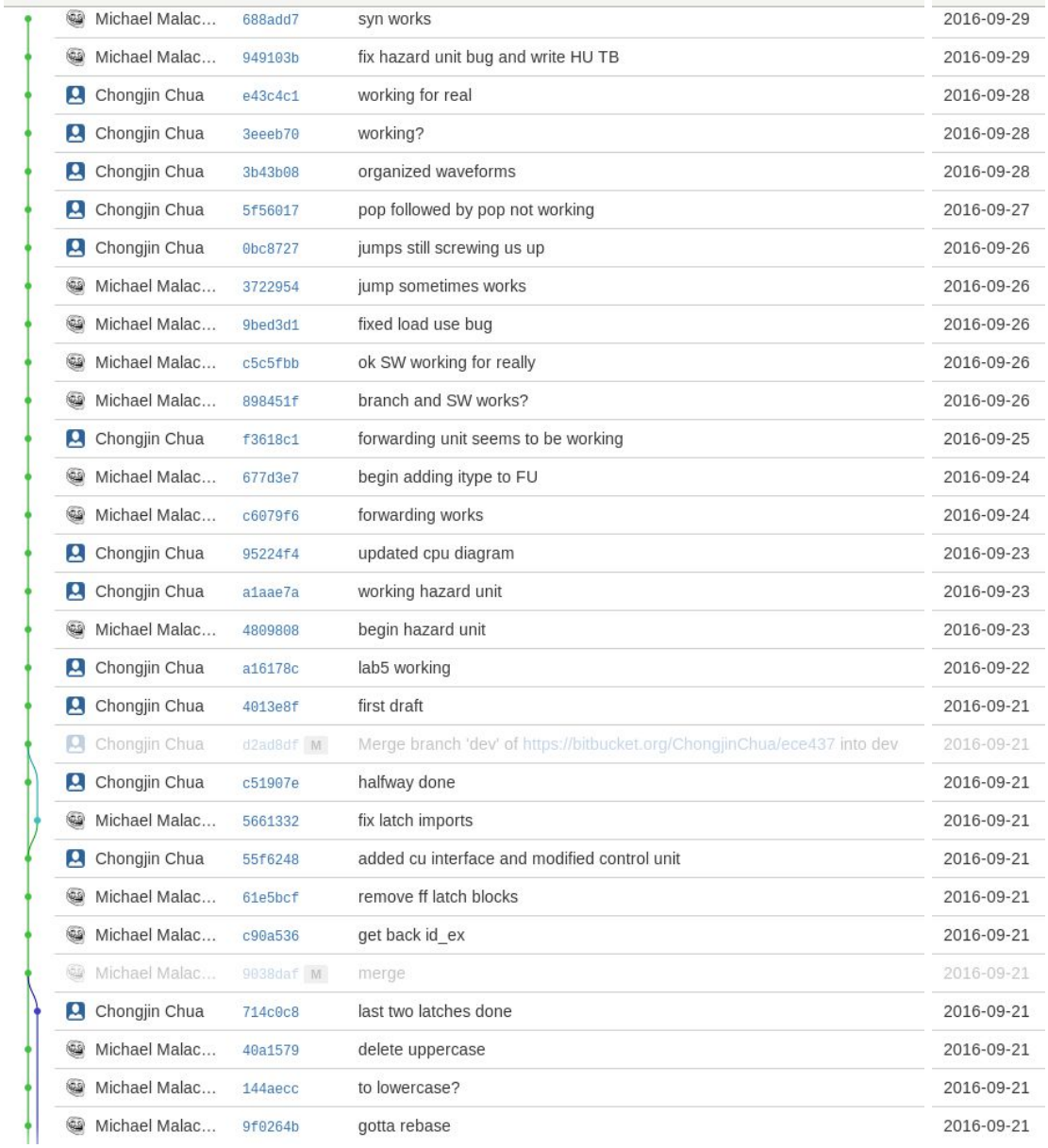
Figure 4: Pipeline Table

4.5 Conclusions

Many of the metrics of the pipeline design show an improvement over those of the single cycle design's. However, the pipelined design has lower performance than the latter design. Due to the fact that the pipelined design is broken up into several stages, the critical path is shorter, and thus, it can be run at a higher frequency. However, the instruction latency of the pipeline design is longer, owing to the fact that it takes five clock cycles for an instruction to traverse through the entire pipeline, but the frequency of the pipeline design is not at least five times faster. In addition, the pipeline design requires slightly more FPGA resources due to the additional logic required for the stage latches, forwarding unit, hazard unit, and additional logic that is not present in the single cycle design.

As far as performance, the pipelined design processes fewer MIPS than the single cycle design. Ideally, splitting the critical path into five identical length stages in the pipelined design would allow for about a five-fold increase in clock speed and MIPS. However, the critical path in our pipelined design is not evenly split, and pipeline stalls due to hazards introduce increases in CPI, which together lower the MIPS of our pipelined design below that of the single cycle. In order to increase the MIPS of our pipelined design, it would be necessary to further decrease the length of the critical path.

4.6 Contributions



Michael Malac...	688add7	syn works	2016-09-29
Michael Malac...	949103b	fix hazard unit bug and write HU TB	2016-09-29
Chongjin Chua	e43c4c1	working for real	2016-09-28
Chongjin Chua	3eeeb70	working?	2016-09-28
Chongjin Chua	3b43b08	organized waveforms	2016-09-28
Chongjin Chua	5f56017	pop followed by pop not working	2016-09-27
Chongjin Chua	0bc8727	jumps still screwing us up	2016-09-26
Michael Malac...	3722954	jump sometimes works	2016-09-26
Michael Malac...	9bed3d1	fixed load use bug	2016-09-26
Michael Malac...	c5c5fbb	ok SW working for really	2016-09-26
Michael Malac...	898451f	branch and SW works?	2016-09-26
Chongjin Chua	f3618c1	forwarding unit seems to be working	2016-09-25
Michael Malac...	677d3e7	begin adding itype to FU	2016-09-24
Michael Malac...	c6079f6	forwarding works	2016-09-24
Chongjin Chua	95224f4	updated cpu diagram	2016-09-23
Chongjin Chua	a1aae7a	working hazard unit	2016-09-23
Michael Malac...	4809808	begin hazard unit	2016-09-23
Chongjin Chua	a16178c	lab5 working	2016-09-22
Chongjin Chua	4013e8f	first draft	2016-09-21
Chongjin Chua	d2ad8df M	Merge branch 'dev' of https://bitbucket.org/ChongjinChua/ece437 into dev	2016-09-21
Chongjin Chua	c51907e	halfway done	2016-09-21
Michael Malac...	5661332	fix latch imports	2016-09-21
Chongjin Chua	55f6248	added cu interface and modified control unit	2016-09-21
Michael Malac...	61e5bcf	remove ff latch blocks	2016-09-21
Michael Malac...	c90a536	get back id_ex	2016-09-21
Michael Malac...	9038daf M	merge	2016-09-21
Chongjin Chua	714c0c8	last two latches done	2016-09-21
Michael Malac...	40a1579	delete uppercase	2016-09-21
Michael Malac...	144aecc	to lowercase?	2016-09-21
Michael Malac...	9f0264b	gotta rebase	2016-09-21

Fig 5: Partial List of git commit history

Both team members contributed starting from 2016-9-21 to 2016-9-29. 45 git commits were made throughout this period. Some of the commits consist of contributions from both team members.