CSD19506KCS 80 V N-Channel NexFET™ Power MOSFET

1 Features

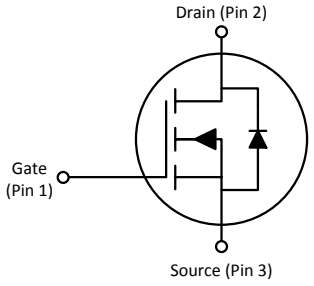
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 80 V, 2.0 mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	80		V
Q_g	Gate Charge Total (10 V)	120		nC
Q_{gd}	Gate Charge Gate to Drain	20		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V	2.2	mΩ
		V_{GS} = 10 V	2.0	mΩ
$V_{GS(th)}$	Threshold Voltage	2.5		V

Ordering Information(1)

Device	Package	Media	Qty	Ship
CSD19506KCS	TO-220 Plastic Package	Tube	50	Tube

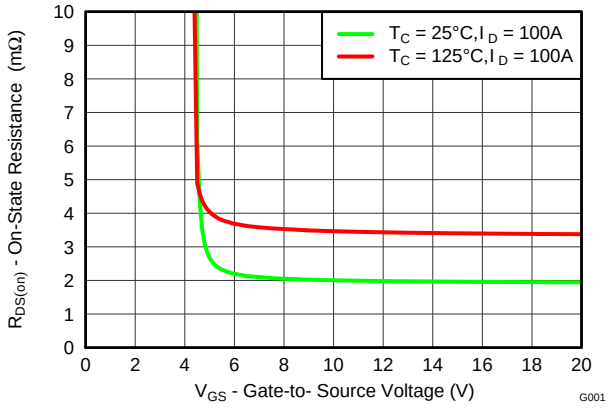
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

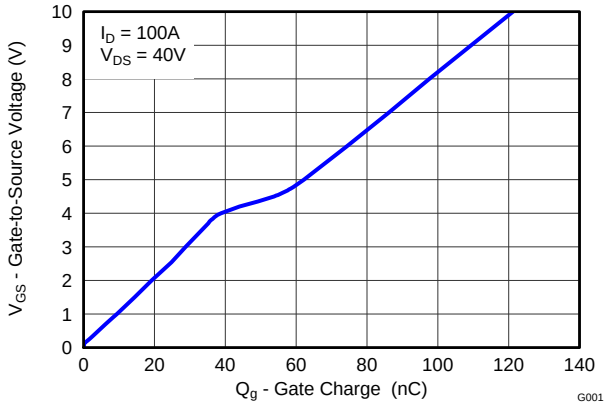
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	150	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	273	
	Continuous Drain Current (Silicon limited), T_C = 100°C	193	
I_{DM}	Pulsed Drain Current (1)	400	A
P_D	Power Dissipation	375	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 175	°C
E_{AS}	Avalanche Energy, single pulse I_D = 129 A, L = 0.1 mH, R_G = 25 Ω	832	mJ

(1) Max $R_{\theta JC}$ = 0.4°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B **Page**

- Changed Pulsed Drain Current Conditions ... 1
- Updated the SOA in Figure 10 ... 6

Changes from Original (December 2013) to Revision A **Page**

- Increased Package Current Limit to 150 A ... 1
- Increased Pulsed Drain Current to 400 A ... 1
- Updated SOA Curve ... 5

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	80			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 64 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.1	2.5	3.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 6 V, I_D = 100 A		2.2	2.8	mΩ
		V_{GS} = 10 V, I_D = 100 A		2.0	2.3	mΩ
g_{fs}	Transconductance	V_{DS} = 8 V, I_D = 100 A		297		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		9380	12200	pF
C_{oss}	Output Capacitance			2260	2940	pF
C_{rss}	Reverse Transfer Capacitance			42	55	pF
R_G	Series Gate Resistance			1.3	2.6	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 40 V, I_D = 100 A		120	156	nC
Q_{gd}	Gate Charge Gate to Drain			20		nC
Q_{gs}	Gate Charge Gate to Source			37		nC
$Q_{g(th)}$	Gate Charge at V_{th}			25		nC
Q_{oss}	Output Charge	V_{DS} = 40 V, V_{GS} = 0 V		345		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 40 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		19		ns
t_r	Rise Time			11		ns
$t_{d(off)}$	Turn Off Delay Time			30		ns
t_f	Fall Time			10		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 40 V, I_F = 100 A, di/dt = 300 A/µs		525		nC
t_{rr}	Reverse Recovery Time			107		ns

5.2 Thermal Information(1)

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

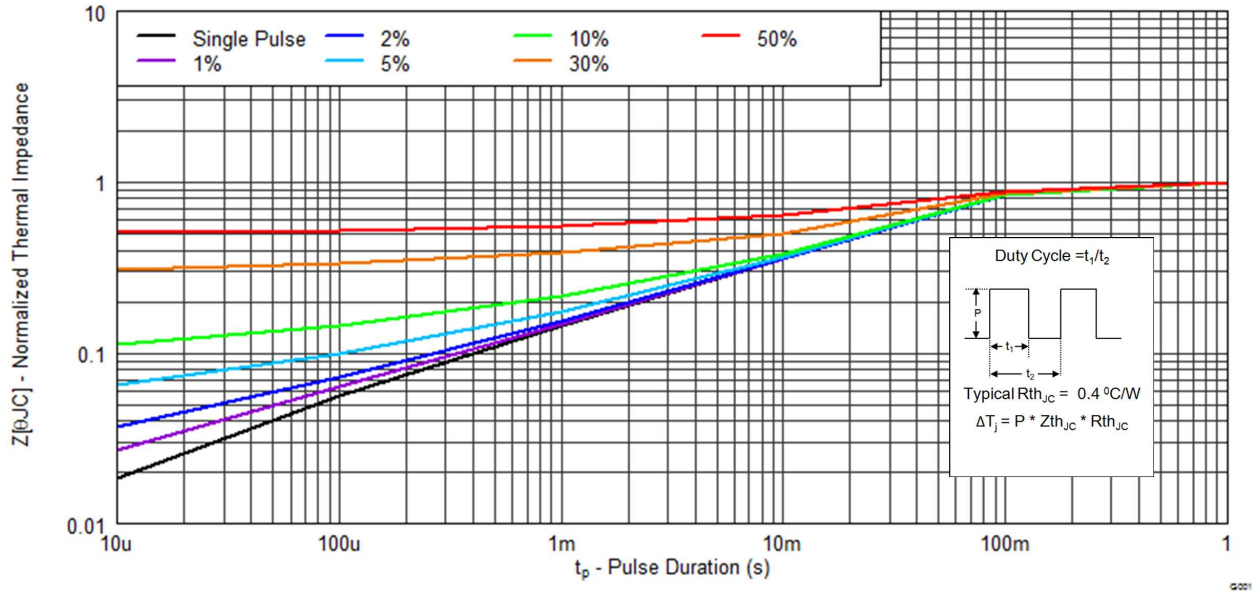


Figure 1. Transient Thermal Impedance

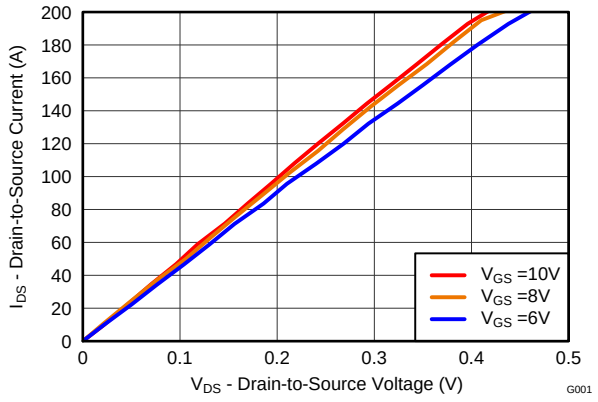


Figure 2. Saturation Characteristics

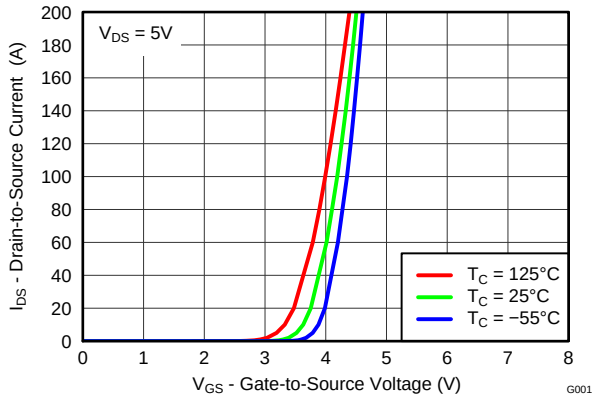


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

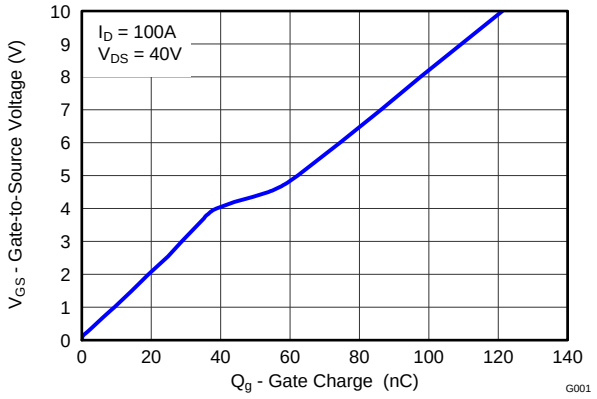


Figure 4. Gate Charge

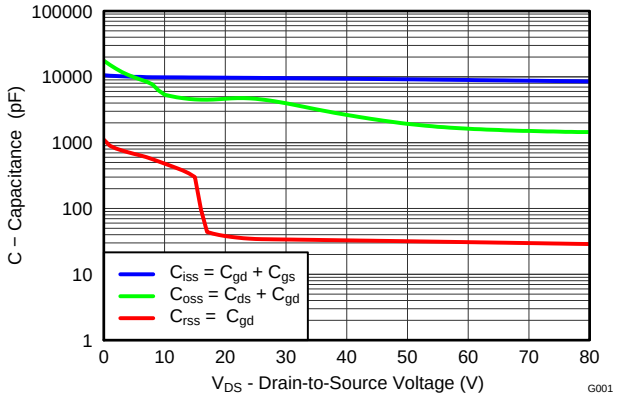


Figure 5. Capacitance

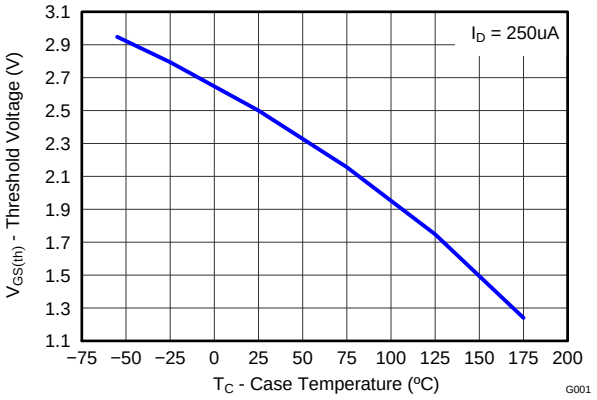


Figure 6. Threshold Voltage vs Temperature

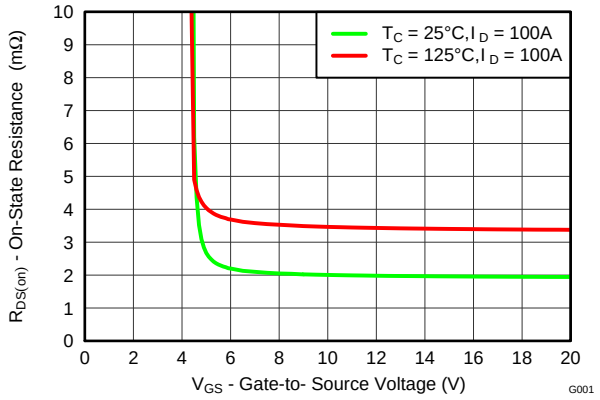


Figure 7. On-State Resistance vs Gate-To-Source Voltage

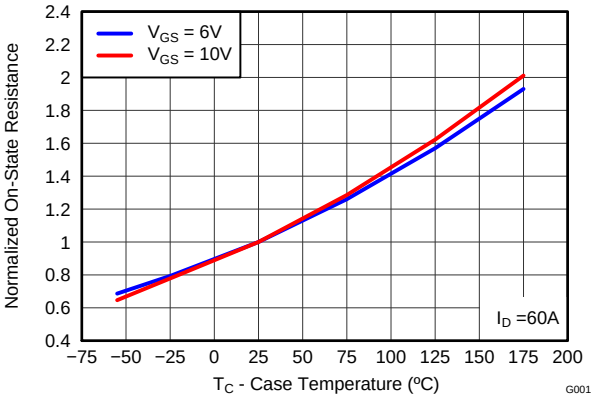


Figure 8. Normalized On-State Resistance vs Temperature

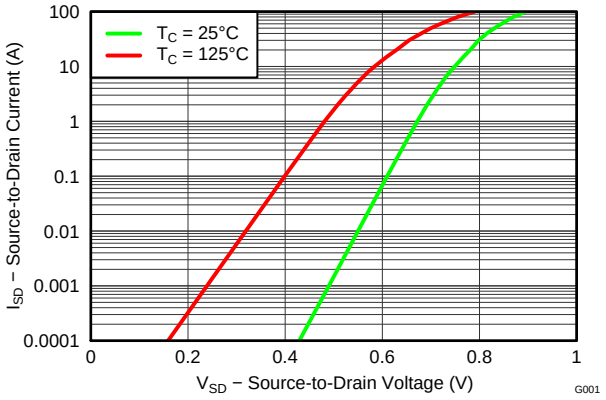


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

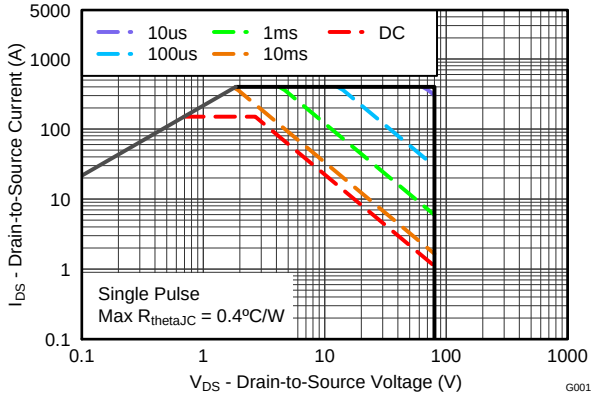


Figure 10. Maximum Safe Operating Area

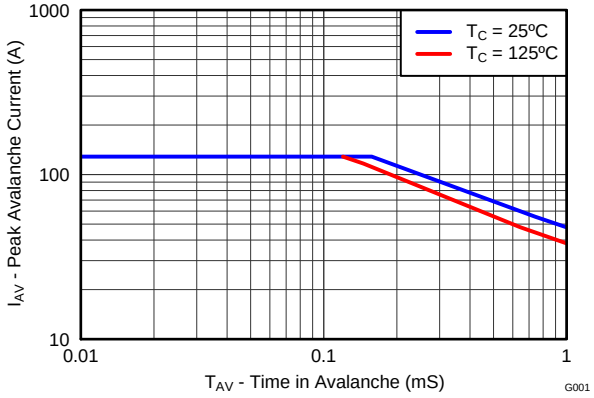


Figure 11. Single Pulse Unclamped Inductive Switching

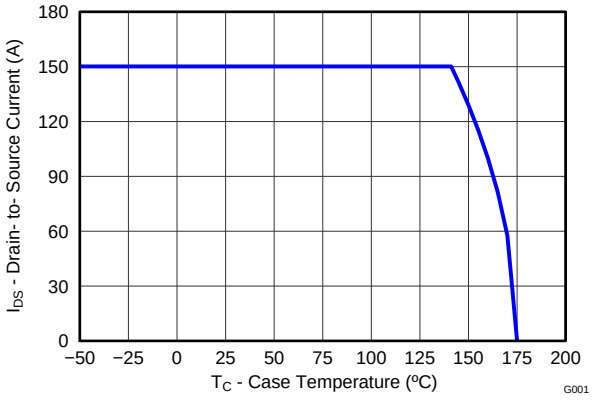


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

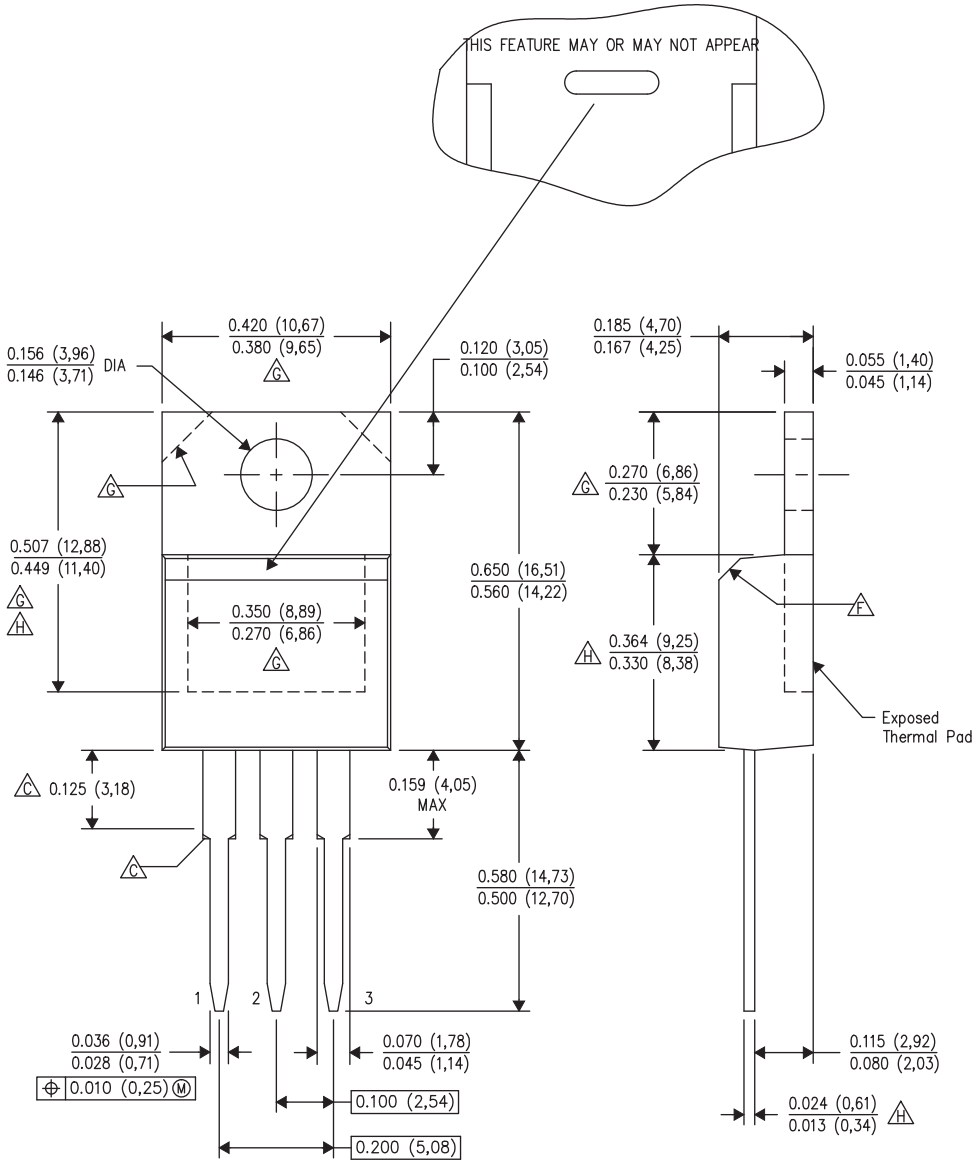
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions

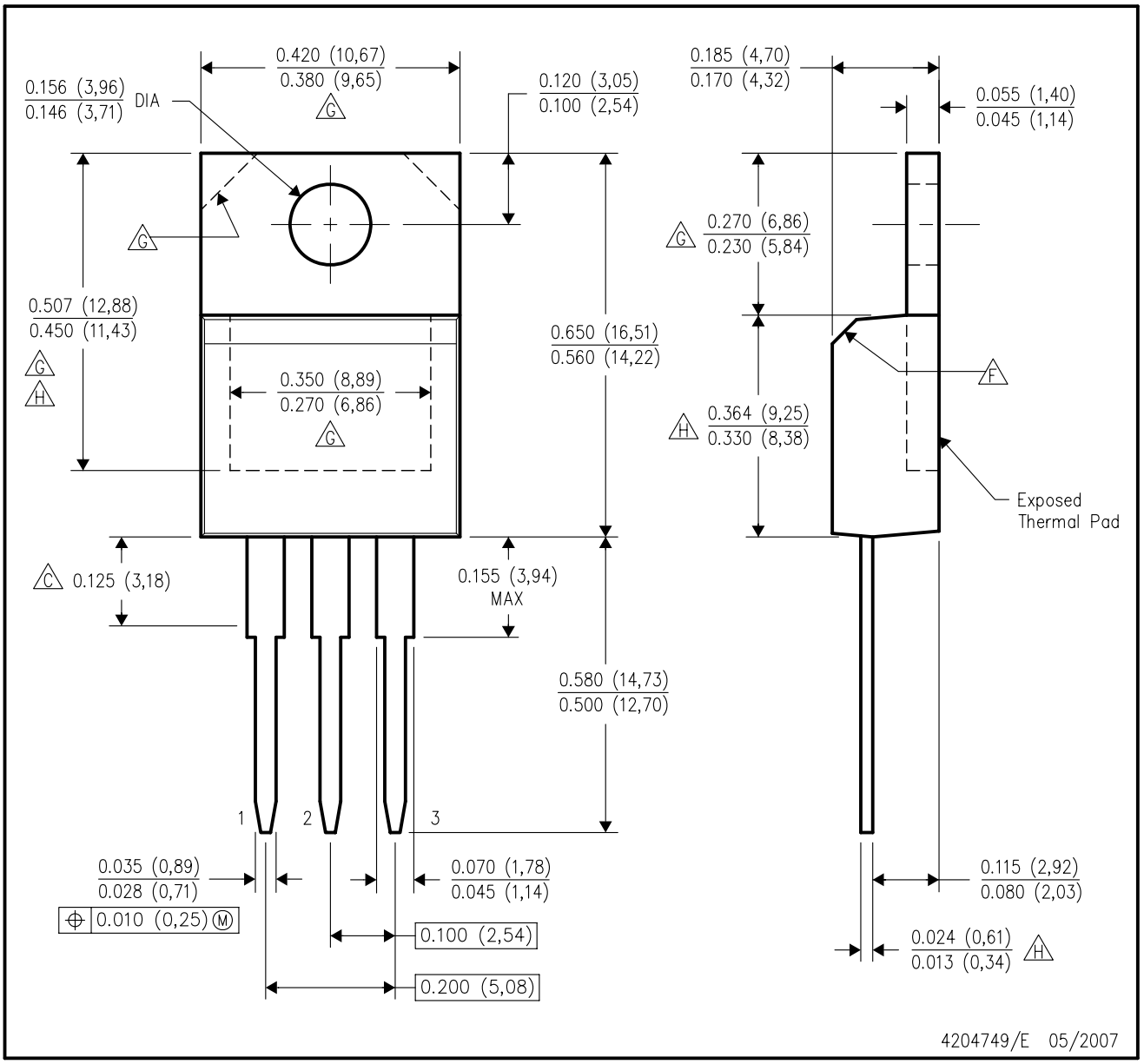


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



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H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

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