Name:	

CS/CoE 0447 – Spring 2017 Lab 6: Subtraction and Multiplication

Released: Thursday 16 February 2017 **Due: Monday 27 February 2017, 11.59 pm**

Each of you should submit your own solution. If you choose to work with a neighbor/partner, put your partner's name on your submitted copy of the lab. Late submissions will not be accepted.

To help your practice for the exam, consider working each problem in pen or pencil on a hard copy of this document. Then, **enter your answers into CourseWeb.**

- 1. For each of the following subtractions, convert the numbers into 8-bit two's-complement, add those and convert the resultant binary two's-complement number into decimal form. Practice by **showing all your work.**
 - a. 45 57

b. 75 - 15

c. -21 - 62

2. Show the steps for multiplying the 8-bit multiplicand 0001 0110 (unsigned) and the 8-bit multiplier 1100 0101 (unsigned) using the Slow Shift Algorithm, which is Hardware Design 1 from http://people.cs.pitt.edu/~childers/CS0447/lectures/multiplication.pdf.

Populate the cells of the following table. Do each addition operation within the table.

			Slow-Shift Algorithm		
It.	Multiplicand (16 bits)	Multiplier	Step	Product Register (16 bits)	
0					
1					
2					
3					
4					
5					
6					
7					
8					

FINAL PRODUCT:	0001 0110 × 1100 0101 (unsig	ned) =
----------------	--	--------

3. Show the steps for multiplying the 8-bit multiplicand 0001 0110 (unsigned) and the 8-bit multiplier 1100 0101 (unsigned) using the Fast Shift Algorithm, which is Hardware Design 3 from http://people.cs.pitt.edu/~childers/CS0447/lectures/multiplication.pdf

Populate the cells of the following table. Do each addition operation within the table.

		Fast-Shift Algorithm			
Iteration	Multiplicand	Step	Product Register (16 bits)		
0					
1					
2					
3					
4					
5					
6					
7					
8					

THIRD TROUBLE CONTROL AND A TITUS OF THE CONTROL	FINAL PRODUCT:	0001 0110 × 1100 0101 (unsigned) =
--	----------------	------------------------------------

¹ For Step 2 shown on slide 51, shift in the carry out bit of Step 1a. If Step 1a is bypassed, shift in 0.