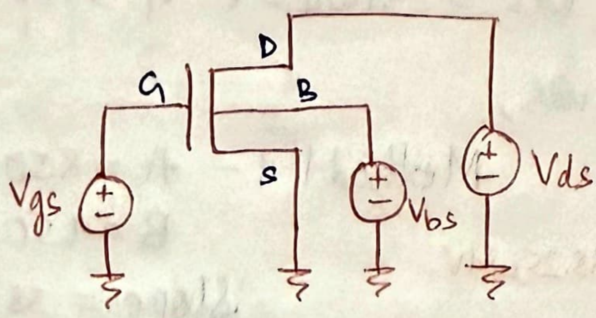
AICD - Exp 1

1) Rig up the circuit as shown.

NMOS → $W = 2\mu m$
$L = 180nm$



For Vgs, Vbs, Vds → Select DC voltage (Vdc) & assign values as Vgs, Vbs & Vds

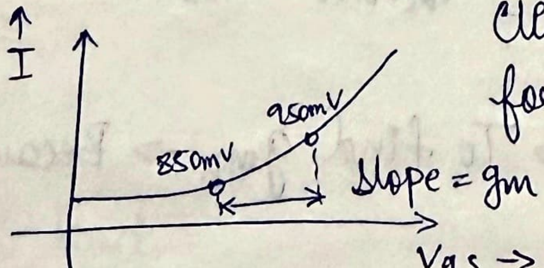
2) Find I_D vs V_{gs} → To find g_m → Because $g_m = \partial I_D / \partial V_{gs}$

Now, ADEL → Under Design variables column → Right click → Copy from cellview. $V_{bs} = 0$ $V_{ds} = 0.9V$ $V_{gs} = 0.9V$ $\left[\because \frac{V_{dd}}{2} = \frac{1.8}{2} = 0.9\right]$

Now, DC analysis → Save DC operating point → Component parameter → Select component → Select Vgs → Start = 0 Stop = 1.8

Outputs → Select the drain terminal of NMOS → Run

We get a graph as,



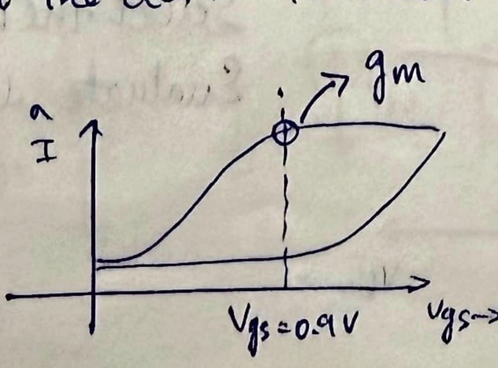
Click A for 1st pt & B for 2nd pt, A = 850mV & B = 950mV

↳ Method 1

Method 2 :-

Tools → Calculator → Select the wave option → Click on the above waveform → Select the deriv function → Evaluate the expression

We get the graph as,

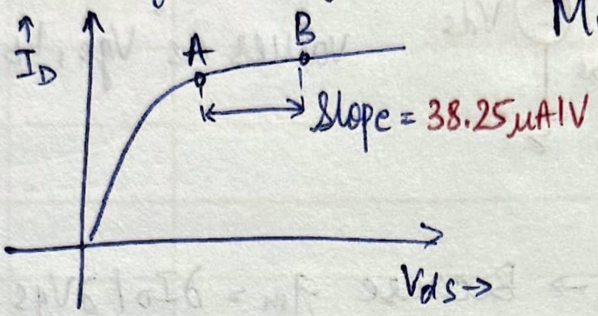


Now → Press V → Place at Vgs = 0.9V

$\therefore g_m = 906.95 \mu A/V$

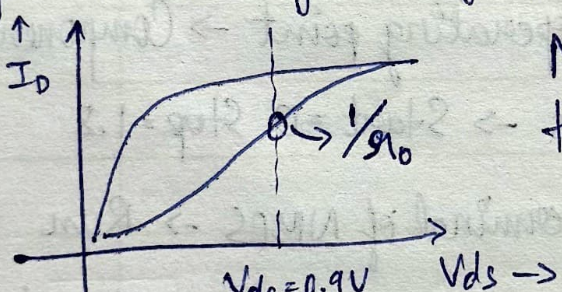
3) Find I_D vs V_{ds} → To find r_o → Because $r_o = \frac{1}{\lambda I_D} = \frac{\partial V_{ds}}{\partial I_D} = \frac{1}{\text{slope}}$

Now, DC analysis → Select V_{ds} → Start = 0 & Stop = 1.8 V and run, we get the graph as,



Method 1 :- A = 850 mV
B = 950 mV
Slope = 38.25 µA/V
1/slope = r_o = 26.14 kΩ

Method 2 :-
Select the wave → Apply deriv function → Now apply 1/x for the deriv function, we get the graph as,

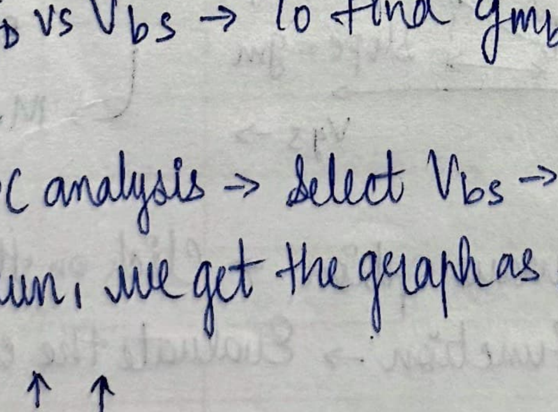


Now, Press V, at 0.9 V, see the value of r_o

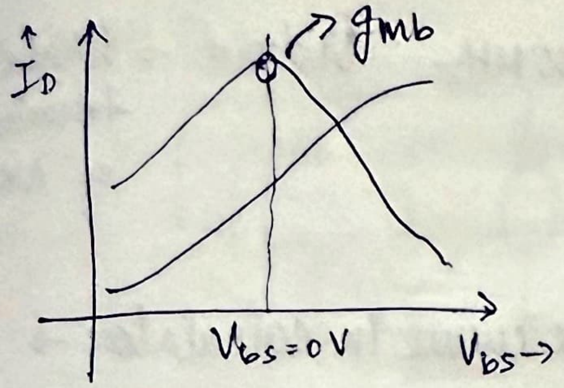
∴ r_o = 25.781 kΩ

4) Find I_D vs V_{bs} → To find g_{mb} → Because $g_{mb} = \frac{\partial I_D}{\partial V_{bs}}$

Now, DC analysis → Select V_{bs} → Start = −1V & Stop = +1V and run, we get the graph as,



Select the wave → Apply deriv → Evaluate, we get the graph as,



Now, Press V, at 0 V, see the value of g_{mb}.

$\therefore g_{mb} = 271.5002 \mu A/V$

5) Dummy DC analysis

Just run DC analysis → Save DC operating points → OK
Outputs → Select the drain-terminal of NMOS → Run

Now, ADEL window → Results → Print → DC operating points → click on the NMOS. Now, from the results window,

$g_m = 917.516 \mu A/V$

$g_{mb} = 276.508 \mu A/V$

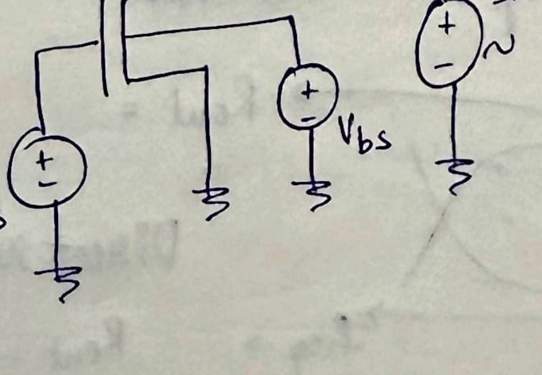
$r_o = r_{out} = 26.186 K\Omega$

$i_d = 247.222 \mu A$

6) AC analysis → To get Rout

i) Figure 1:-

$V_{bs} = 0V$
$V_{gs} = 0.9V$



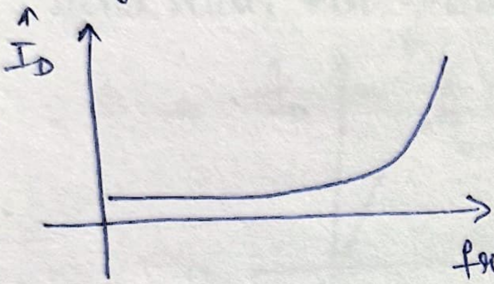
Vsin → DC voltage = 0.9V
AC mag = 1V

V_{bs} & V_{gs} → Vdc

Note :- Remember to remove the Vds variable in ADEL window

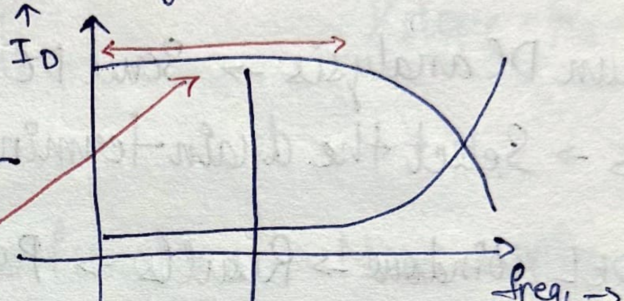
Now, AC analysis → Frequency → 1 to 100MHz Output → Drain terminal of NMOS

We get the curve as,



Now, Select the curve in calculator → Apply the $1/x$ function → Evaluate

Now, we get the curve as,

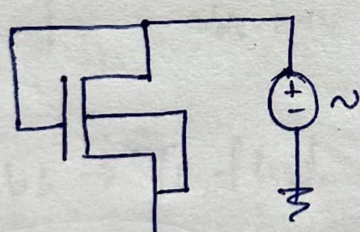


Simply place the cursor on the top most curve, anywhere on the straight line

∴ Rout =

ii) Figure 2 :-

W = 2u
L = 180n

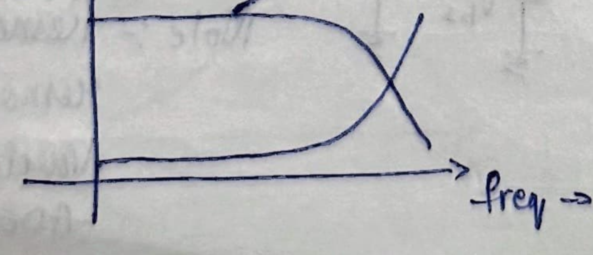


Vsin → DC voltage = 0.9V
AC mag = 1V

Outputs → Drain of NMOS

AC analysis → Freq = 1 to 100MHz

We get a curve → Apply $1/x$ → Evaluate

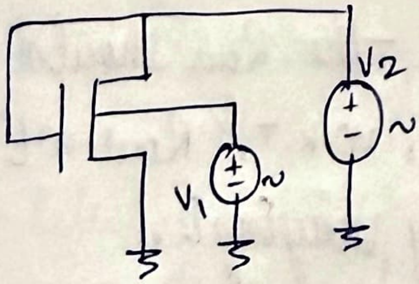


Rout =

Direct result,

$$R_{out} = \frac{1}{g_m} \parallel r_o$$

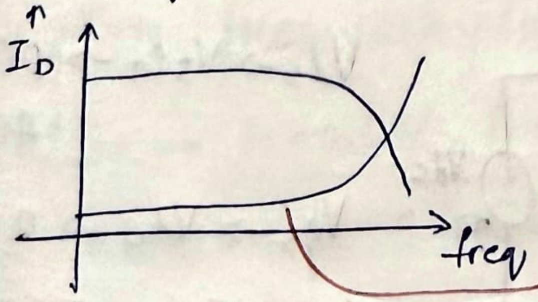
iii) Figure 3 :-



$V_1 \rightarrow V_{sin} \rightarrow$ DC voltage = 0V
AC mag = 1V

$V_2 \rightarrow V_{sin} \rightarrow$ DC voltage = 0.9 V
AC mag = 1V

AC analysis $\rightarrow$ Freq = 1 to 100MHz $\rightarrow$ Select the curve $\rightarrow$ Apply 1/x



Now, in this figure, select the bottom curve and find Rout.

Rout =

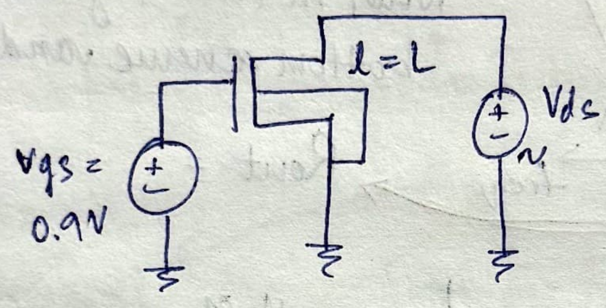
Now, Direct result, Rout = $\frac{1}{g_m + g_{mb}} \parallel r_o$

AICD - Exp2

Theoretically, for a current mirror, the Rout should be ideally ∞ and practically as high as possible. W.K.T, Rout ∝ L, therefore we need to determine the Rout value by varying L.

1) Rig up circuit as below,

$\boxed{W = 10\mu}$



V_{ds} -> Vsin -> DC voltage = 0.9V
AC mag = 1V

V_{gs} -> Vdc -> DC voltage = 0.9V

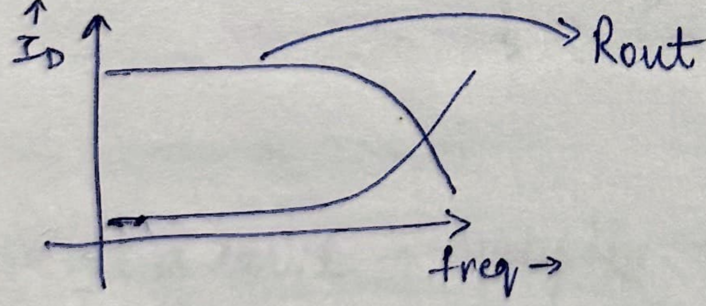
L = 180nm, 590nm, 1µm
(vary the length)

W.K.T, to get Rout, we do AC analysis with f = 1 to 1GHz.

In ADEL window -> Design variables -> Right click -> Copy from cellview

Perform three trials with L = 180nm, 590nm, 1µm

Run AC analysis -> Select the curve -> Apply 1/x function -> Evaluate



	Rout
180nm	5.72KΩ
590nm	52.54KΩ
1µm	118.28KΩ

We select the value of L for which Rout is ↑.

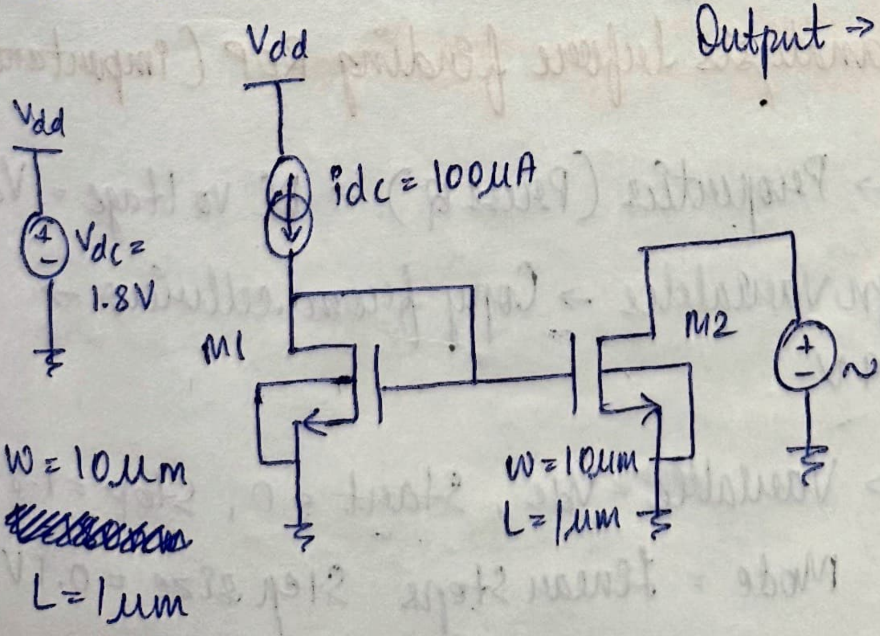
∴ L = 1µm

Now,
Analyses → DC → Save DC operating points ☑ → Component parameter → Select component → Select Vds → DC voltage → Start = 0 , Stop = 1.8
Outputs → Select the NMOS drain terminal
Now, run parametric analysis → Variable = L , Start = 180 nm, Stop = 1um , Mode = Auto , Steps = 3 → Run
we get three plots, from each plot we get Id variation & Ro
For ID variation → A = 0.5V , B = 1.8V , check the dy value
For Ro → A = 850mV , B = 950mV , get the slope value &
$R_o = 1/\text{slope}$

Now,

L	dy = ID variation	Ro
180 nm	220.98 μA	5.714 KΩ
590nm	24.943μA	52.33KΩ
1 um	11.886μA	117.7KΩ

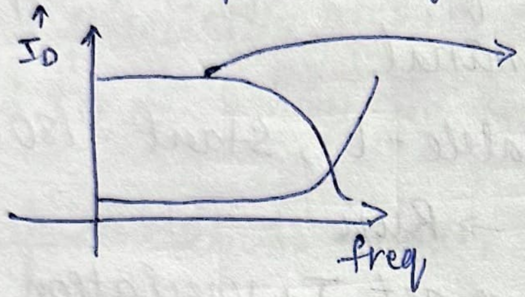
2) Basic current mirror



Output → Select drain terminal of M2 transistor

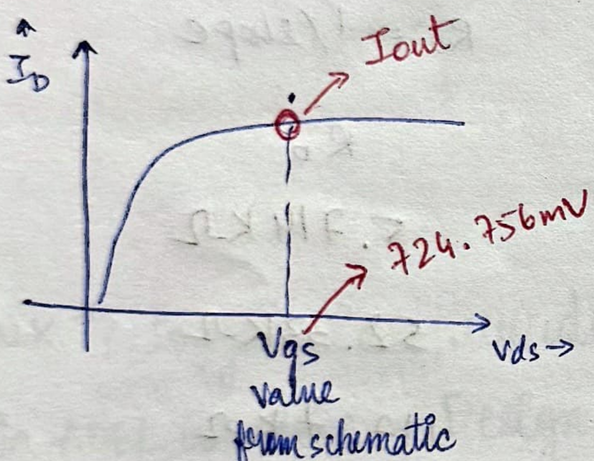
Vsin → DC voltage = 0.9V
AC mag = 1V

a) AC analysis → Freq = 1 to 1GHz → Run → Select the curve in calculator by enabling wave option → Apply 1/x function → Evaluate



R_{out} = 301.75kΩ

b) DC analysis → Select component → Select Vds → Start = 0
Stop = 1.8



Now in the schematic, check what is the value of Vgs for M2 transistor. So for that Vgs value, check what is the I_D value in DC analysis.

∴ Iout = 99.9996µA

c) Finding the region of operation of M2 to determine $V_{out,min}$

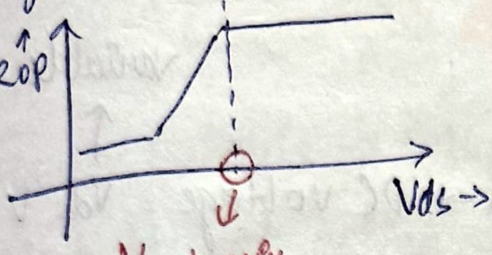
Note :- Need to run DC analysis before finding ROP (Important)

In schematic, select Vds → Properties (Press Q) → DC voltage = Vds

In ADEL window → Design variables → Copy from cellview → Give value for Vds as 0.9V

Now, Parametric analysis → Variable = Vds, Start = 0, Stop = 1.8,
Mode = Linear steps Step size = 0.1V

We get the graph as,



Implies min voltage required for M2 to get into saturation

Get the value for Vout, min where the value of Rop = 2.

∴ Vout, min = 0.3V

Now, for the value of Vout, min = 0.3V check what is the current value in the DC curve.

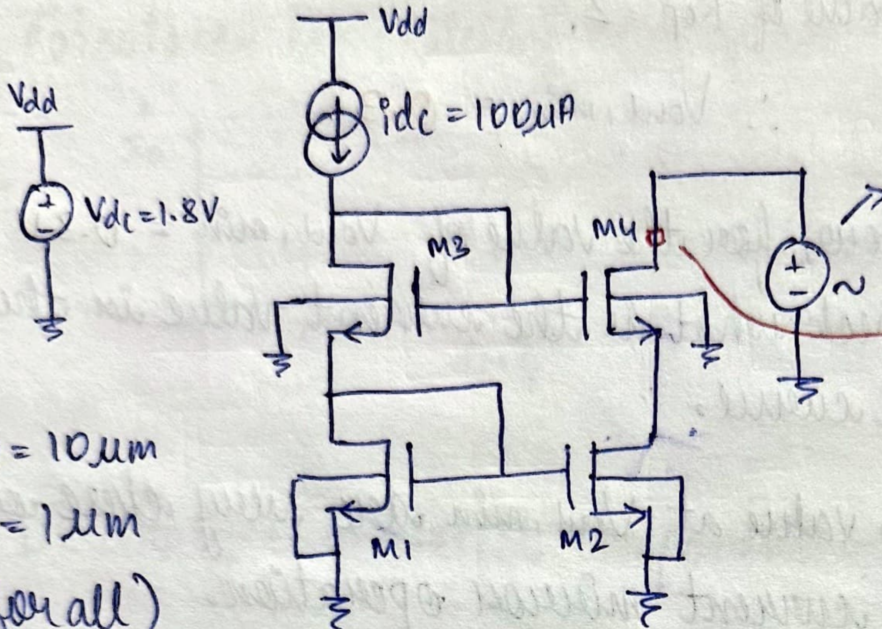
Check if both Iout & ID value at Vout, min are very close or similar which justifies the current mirror operation.

Note :- Before parametric analysis, do the following (mandatory)

Outputs -> Setup -> Name = ROP -> Calculator Open -> Select the ⊙opt option -> In schematic select M2 -> In the dialogue box -> Click on list -> Select region -> Now, go back to the setup window -> Select Get expression -> OK

I_D at Vout, min = 95.7005 µA

3) Cascode current mirror



→ Vsin → DC voltage = Vds V ← Variable

AC mag = 1V

Output → Drain terminal of M4

W = 10um

L = 1um

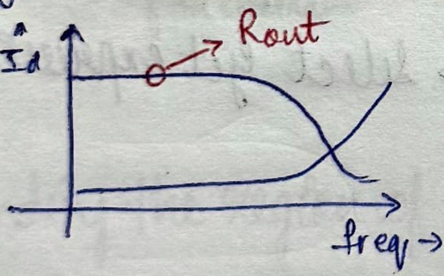
(for all)

a) AC analysis → Freq = 1 to 1GHz → OK

Output → Drain of M4

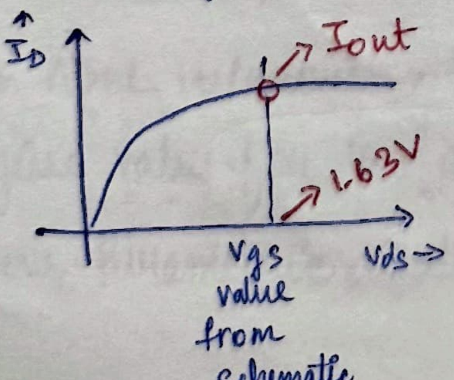
ADEL → Design variables → Right click → Copy from cellview →

Give V_{ds} = 0.9V → Run → Select the curve → Apply 1/x function →



∴ Rout = 848.32KΩ

b) DC analysis → Select Vds → Start = 0, Stop = 1.8V → Run



Now, in schematic, check the V_{gs} value of M4 transistor. For that value, check what is I_D in DC curve.

∴ Iout = 99.99992uA

c) Finding ROP of M2 & M4 transistor, to get $V_{out,min}$

Note :- DC analysis should have been done before determing ROP.

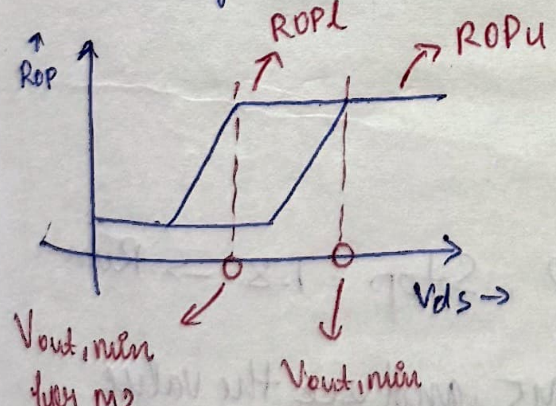
ADEL -> Outputs -> Setup -> Name = ROPu -> Open Calculator -> select the opt option -> In schematic, select M4 -> Under the list, select region option -> Now, go back to setup window -> click on Get expression -> OK

Do the same as above for M2 transistor -> Name = ROPl

Now, Parametric analysis -> Variable = Vds , Start = 0, Stop = 1.8, Mode = Linear steps Step size = 0.1

Note :- Before running parametric analysis, see to that the ROPu & ROPl under the Outputs window is enabled & the drain of M4 is disabled.

Run -> We get a curve as,

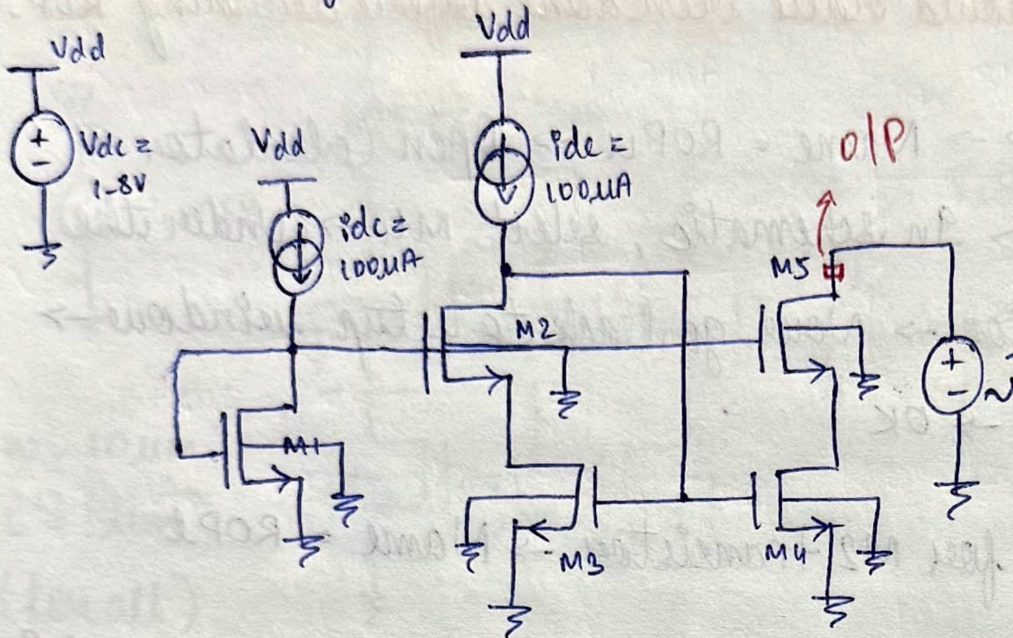


$V_{out,min}$ (M4) = 1V

Now, for the above value, check the value of I_D in DC analysis curve & verify if this value & the Iout value is similar / very close.

I_D at $V_{out,min}$ = 99.97075 μA

4) Low voltage cascode current mirror



$L = 1\mu m$

$W_{M2,M3,M4,M5} = 12\mu m$

$W_{M_1} = 3\mu m$ [$1/4^{th}$ of 12μ]

→ Vsin → DC voltage = V_{ds}

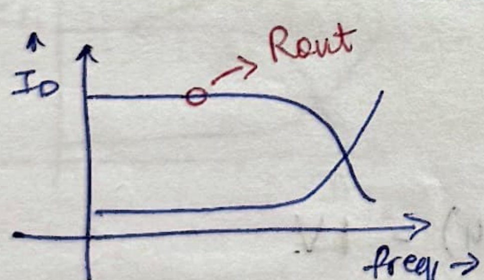
AC mag = 1V

a) AC analysis → f = 1 to 1GHz

Output → Drain terminal of M5

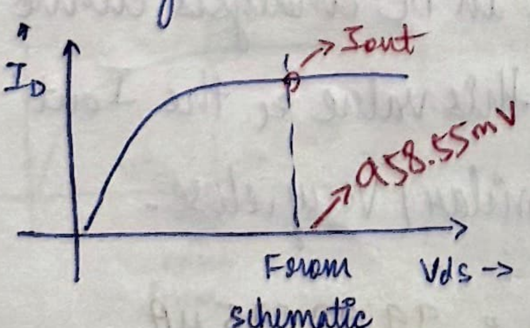
ADEL → Design variables → Copy from cellview → $V_{ds} = 0.9V$ → Run

Select the curve → Apply $1/x$ function → Evaluate



∴ $R_{out} = 3.523 M\Omega$

b) DC analysis → Select V_{ds} → Start = 0, Stop = 1.8 → Run



Check V_{gs} of M5 and see the value of I_{ds}

∴ $I_{out} = 100.102\mu A$

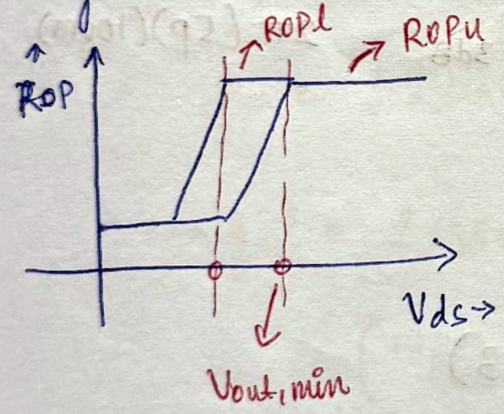
c) Finding ROP of M5 & M4

ADEL → Outputs → Setup → Name = ROPu → Open Calculator → Select opt → Click on M5 → Select region → From the setup window → Click on Get Expression → OK

Do the same for transistor M4 → Name = ROPl

Run parametric analysis → Variable = Vds , Start = 0, Stop = 1.8,
Mode = Linear steps Step size = 0.1

We get the curve as,

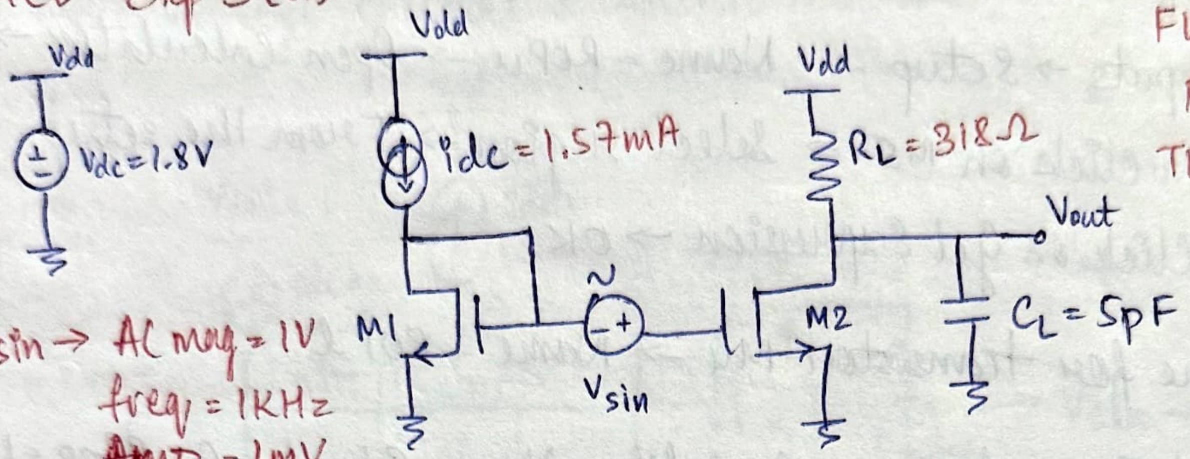


$\therefore V_{out,min}(M5) = 0.5V$

Check Iout value vs the value of I_D at Vout,min in the DC curve.

I_D at $V_{out,min} = 99.8037\mu A$

AICD - Exp 3 (a)



FW = 40.45 μm
F = 5
TW = 202.25 μm
L = 1 μm

Vsin → AC mag = 1V
freq = 1KHz
Amp = 1mV

Let $V_{DD} = 1.8V$, $|A_v| = 5$, $f_{3dB} = 100MHz$, $C_L = 5pF$

W.K.T,

$$f_{3dB} = \frac{1}{2\pi R_L C_L} \Rightarrow R_L = \frac{1}{2\pi C_L f_{3dB}} = \frac{1}{2\pi (5p)(100m)}$$

$$\boxed{\therefore R_L = 318.3\,\Omega}$$

W.K.T,

$$|A_v| = g_m R_L \Rightarrow 5 = g_m (318.3)$$

$$\therefore g_m = \frac{5}{318.3} = 15.7 mA/V$$

To find operation region of T^r, run a dummy DC analysis, keep the default values of T^r & idc = 100μA, $R_L = 318.3\,\Omega$, $C_L = 5pF$

Default T^r ⇒ W = 1μ L = 180nm, F = 1, M = 1. Now, from the Point results → DC operating points, get values of V_{gs} & V_{th}

$\therefore V_{gs} = 730.753m \simeq 0.8V$

$V_{th} = 542.767m \simeq 0.6V$

$\therefore V_{ov} = V_{gs} - V_{th} = 0.8 - 0.6 = 0.2V$

Now, $I_D = \frac{1}{2}\mu_n C_{ox}(W/L)(V_{gs}-V_{Tn})^2 = \underbrace{\frac{1}{2}\mu_n C_{ox}(W/L)(V_{gs}-V_{Tn})}_{g_m}\underbrace{(V_{gs}-V_{Tn})}_{V_{ov}}$

$\therefore I_D = \frac{1}{2} g_m V_{ov} = \frac{1}{2}(15.7m)(0.2) = 1.57mA$

$\boxed{\therefore i_{dc} = 1.57mA}$

Now, to find W/L

For 180nm → $\mu_n C_{ox} = 388.125\,\mu A/V^2$

W.K.T,

$g_m = \sqrt{2\mu_n C_{ox}(W/L) I_D}$

$\Rightarrow g_m^2 = 2\mu_n C_{ox}(W/L) I_D$

$\therefore (W/L) = \frac{g_m^2}{2\mu_n C_{ox} \cdot I_D} = \frac{(15.7m)^2}{2(388.125\mu)(1.57m)}$

$\therefore \frac{W}{L} = \frac{(15.7m)(15.7m)}{2(1.57m)(388.125\mu)} = 0.20225\frac{m}{\mu}$

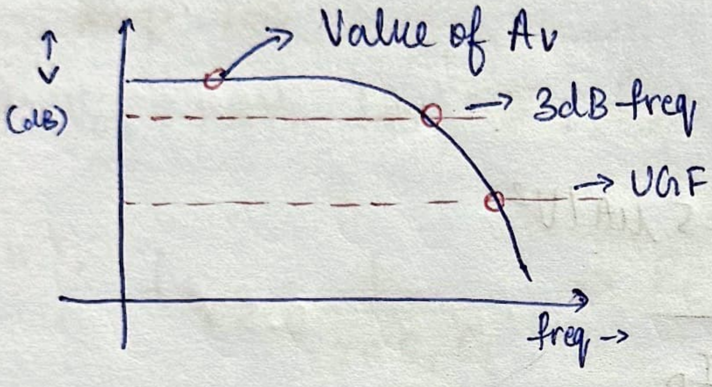
$\therefore \frac{W}{L} = \frac{202.25\mu}{1\mu} \Rightarrow \boxed{\begin{array}{l} W = 202.25\,\mu m \\ L = 1\,\mu m \end{array}}$

Make Fingers, F = 5 $\therefore TW = 202.25\,\mu m$

$FW = \frac{TW}{F} = \frac{202.25\mu}{5}$

$\boxed{\therefore FW = 40.45\,\mu m}$

1) AC analysis → freq = 1 to 1GHz → Just run without any o/P → Now in ADEL window → Results → Direct plot → Main form → In the Direct Plot Form window → Analysis = ac, Function = voltage, Select = Net, Modifier = dB20 → Select the o/P net (Dont press on OK) → We get the waveform.



For 3dB freq → Check the value of Av, then at Av − 3, place a horizontal line (Press H) → Check the freq. value

For UGF → Place a horizontal line at 0dB → Check the freq. value

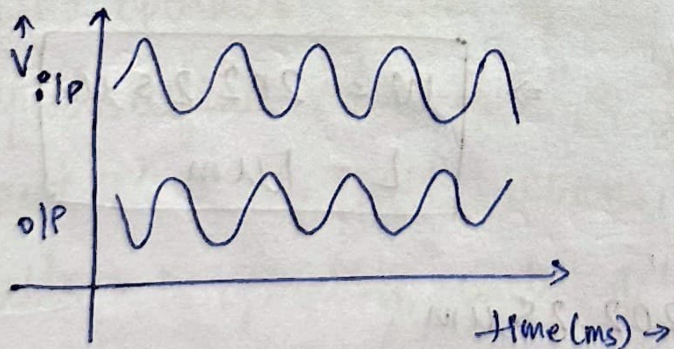
∴ Av (in dB) = 13.12

3dB freq = 95.385MHz at 10.12dB

UGF = 397.49 MHz

2) Transient analysis → Stop time = 10m

Outputs → Select the o/P net & the i/P net (For M2) — in b/w Gate of M2 & +ve terminal of Vsin



Now, Calculator → Select the wave option → Select the o/P curve → apply Peak to Peak function → Evaluate

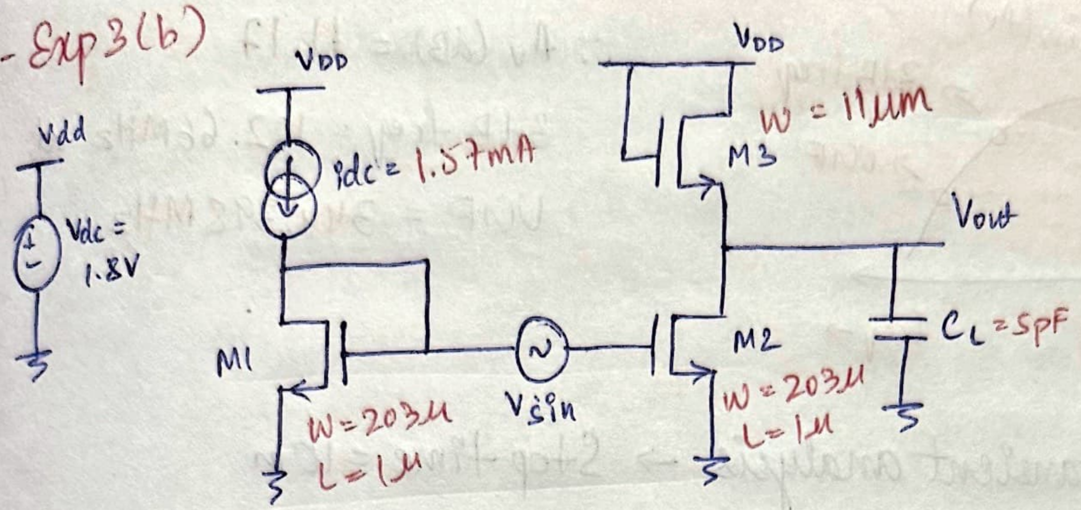
Do the same for i/P curve

∴ $V_{o(P-P)}$ = 9mV

$V_{i(P-P)}$ = 2mV

$A_v = \frac{V_{o(P-P)}}{V_{i(P-P)}} = \frac{9m}{2m} = 4.5$

AICD - Exp 3(b)



V_{DD} = 1.8V

$|A_v|$ = 5

f_{3dB} = 100MHz

C_L = 5pF

Vsin → AC mag = 1V
Amp = 1mV
freq = 1KHz

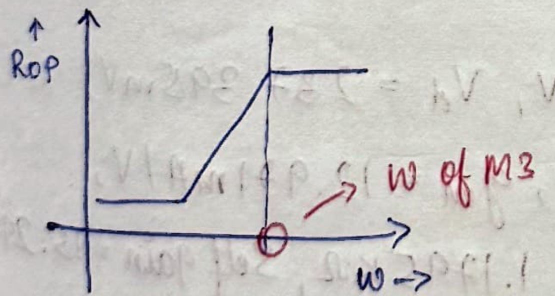
Now, M1 & M2 → W/L = 203µ/1µ   Initially keep i_{dc} = 1.57mA

Now, run dummy DC analysis & find g_m & g_{mb} of M3 transistor

Now, for M3, L = 1µm & W = W [We need to find W of M3 such that M2 remains in saturation].

Now, find ROP of M2 as → ADEL → Outputs → Setup → Name = ROP → Open Calculator → Select opt option → Click on T^r M2 → Under list, select region → Go to Setup window → Click on get expression → OK

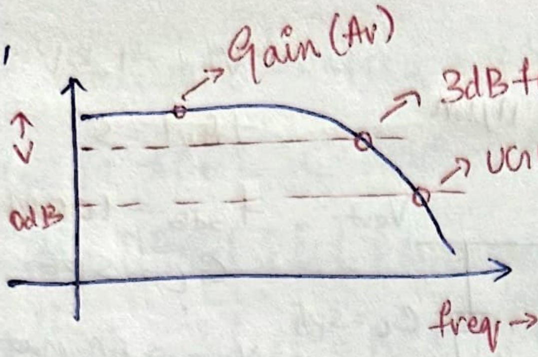
Now, run parametric analysis → Variable = W, From = 2µ, To = 15µ,
Step mode = Linear steps Size = 1µ



∴ W of M3 = 11µm

Now, change W of M3 and perform AC analysis → freq = 1 to 1GHz
Outputs → Vout net → Run the analysis → Click on the waveform → Right-click → Dependent modifier → dB20

Now,



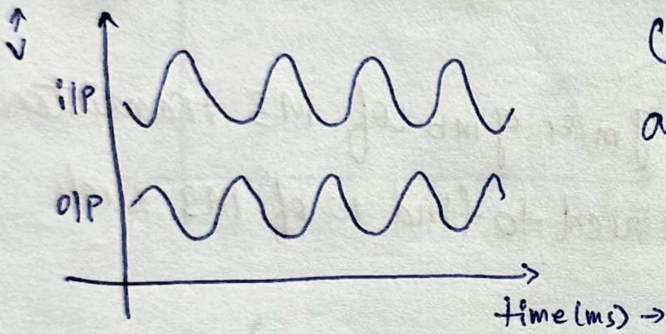
∴ A_v (dB) = 11.17

3dB freq = 102.66MHz at 8.17

UGF = 344.398 MHz

Now, perform transient analysis → Stop time = 10m

Outputs → Vout net & i/p net of M2



Calculator → Select the i/p / o/p waveform → apply PeaktoPeak function → Evaluate

$V_{o(p-p)} = 7.2mV$

$V_{i(p-p)} = 2mV$

$$A_v = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{7.2m}{2m} = 3.6$$

Exp 3a → M2 → V_g = 655.503mV, V_s = 0V, V_d = 1.28956V,
V_b = 0V, I_D = 1.606mA, g_m = 14.462mA/V,
g_{ds} = 48.4256µA/V, r_o = 20.65kΩ, Self gain = 298.64

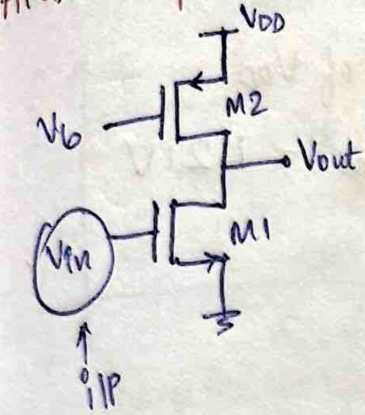
Exp 3b → M2 → V_g = 655.447mV, V_s = 0V, V_d = 237.395mV,
V_b = 0V, I_D = 1.4895mA, g_m = 12.971mA/V,
g_{ds} = 847.829µA/V, r_o = 1.1795kΩ, Self gain = 15.299

M3 → V_g = 1.8V, V_d = 1.8V, V_s = 237.395mV, V_b = 0V,
I_D = 1.4895mA, g_m = 2.071mA/V, g_{ds} = 25.375µA/V,
r_o = 39.41kΩ, Self gain = 81.6007

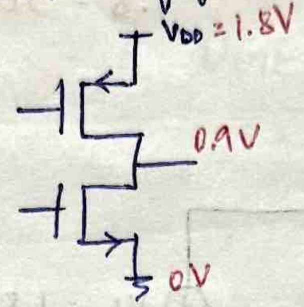
AICD - Exp 4a

The transistors M1 & M2 need to be sized.

$L = 3$ times $180nm \simeq 500nm$



Consider the figure below

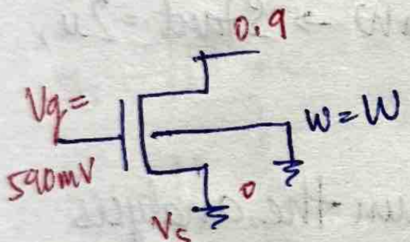


Using the Potential Divider Method (PDM), we estimate the voltage at drain of each transistor, here

$V_{DD} = 1.8V$ No. of $T^r = 2$

$\therefore$ V at each node $= \frac{V_{DD}}{n} = \frac{1.8}{2} = 0.9$

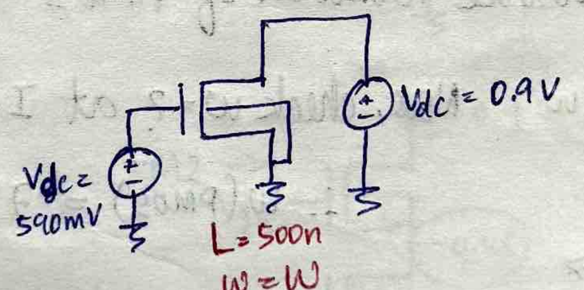
Now, consider the NMOS,



Now, W.K.T, $V_g = V_B + V_{Tn} + 5\%$ of V_{DD}

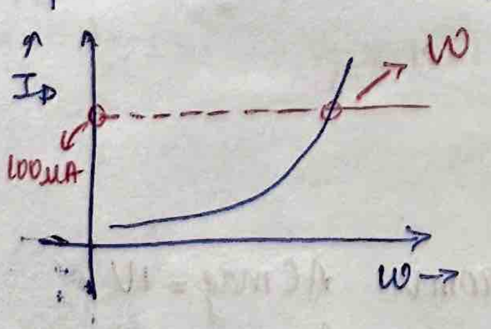
$V_g = 0 + 500m + 90m = 590mV$

Now, connect the ckt as,



Now, DC analysis → Save DC operating point → Component parameter → Select component → Select the NMOS → Select simW (Simulation width) → Start = 2u, Stop = 50u → OK

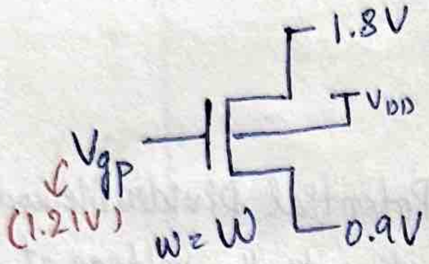
Output → Select drain of NMOS → Run the analysis



Now, place a horizontal line (Press H) at $I_D = 100\mu A$. Now see the value of W.

$\therefore W = 14.373\mu m$ (NMOS)

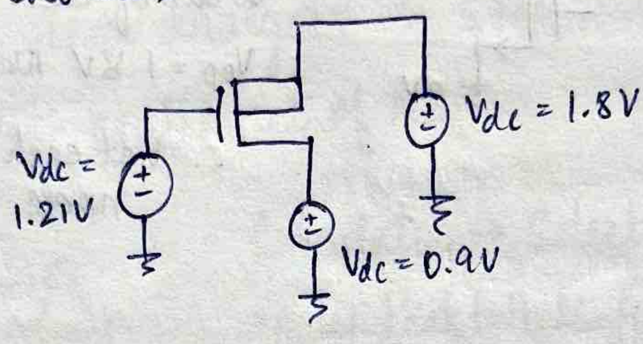
Now, consider the PMOS.



Now, W.K.T,

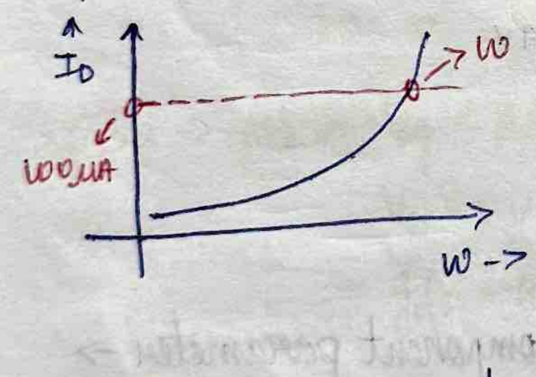
$$V_{gp} = V_s - |V_{thp}| - 5\% \text{ of } V_{DD}$$
$$= 1.8 - 500m - 90m = 1.21V$$

Now, connect the ckt. as,



Now, DC analysis → Select component → PMOS → sinW → Start = 2u, Stop = 100u → OK

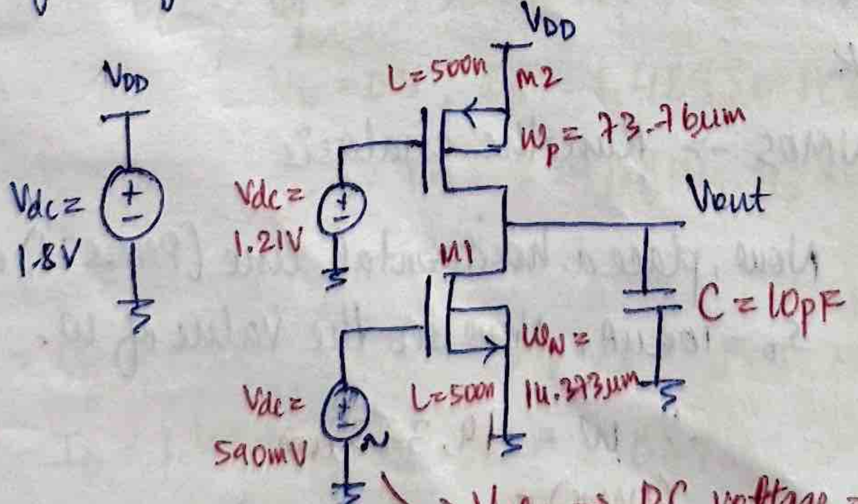
Output → Select the source terminal of PMOS → Run the analysis



Now, check w = ? at I = 100uA

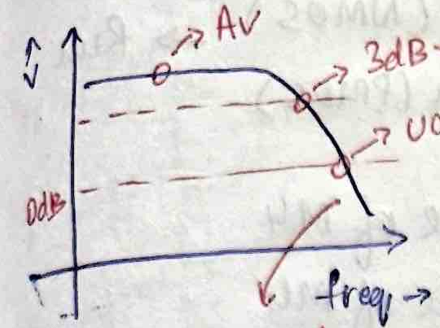
$\therefore$ w (PMOS) = 73.76um

Now, finally connect the ckt. as,



→ Vsin → DC voltage = 590mV AC mag = 1V,
freq = 1KHz Amp = 1mV

Now, AC analysis → freq = 1 to 1 GHz   Output → Vout net



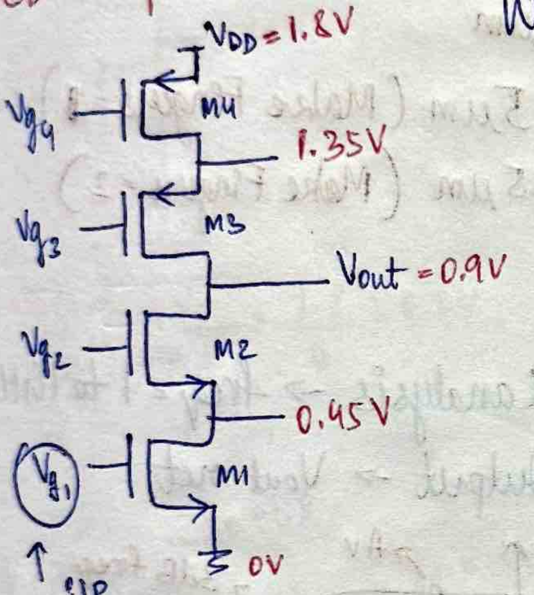
Change the waveform to dB20

∴ Av (dB) = 37.84

3dB freq = 252.51 KHz at 34.84 dB

UGF = 20.153 MHz

AICD - Exp 4 b

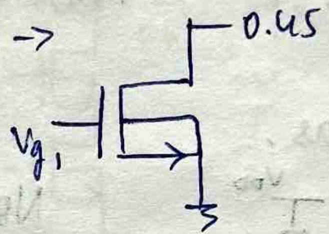


V at each node = $\frac{V_{DD}}{n} = \frac{1.8}{4} = 0.45V$

We get the node voltages using PDM,

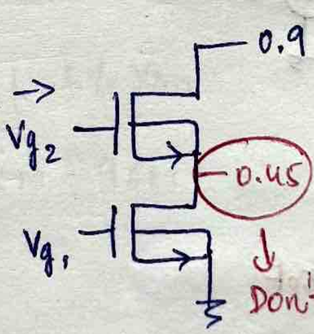
Now perform transistor sizing,

M1 →



$V_{g_1} = V_S + V_{TN} + 5\% \, V_{DD}$
$= 0 + 500m + 90m$
$\therefore V_{g_1} = 590 mV$

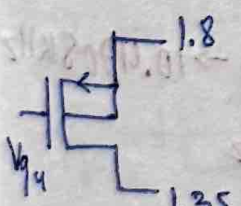
M2 →



Don't connect during schematic

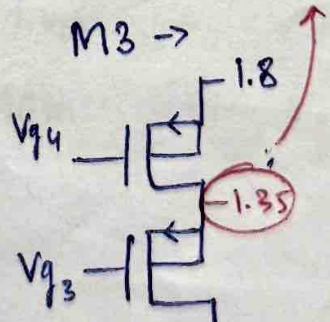
$V_{g_2} = V_S + V_{TN} + 5\% \, V_{DD}$
$= 0.45 + 500m + 90m$
$\therefore V_{g_2} = 1.04V$

M4 →



$V_{g_4} = V_S - |V_{TH}| - 5\% \, V_{DD}$
$= 1.8 - 500m - 90m$
$\therefore V_{g_4} = 1.21V$

M3 →

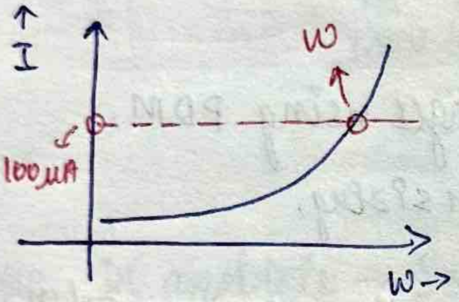


$V_{g_3} = V_S - |V_{TH}| - 5\% \, V_{DD}$
$= 1.35 - 500m - 90m$
$\therefore V_{g_3} = 0.76V$

Perform DC analysis → Select the respective T^n → Select simW →
Start = 2µ, Stop = 50µ (NMOS) → Run
Stop = 100µ (PMOS)

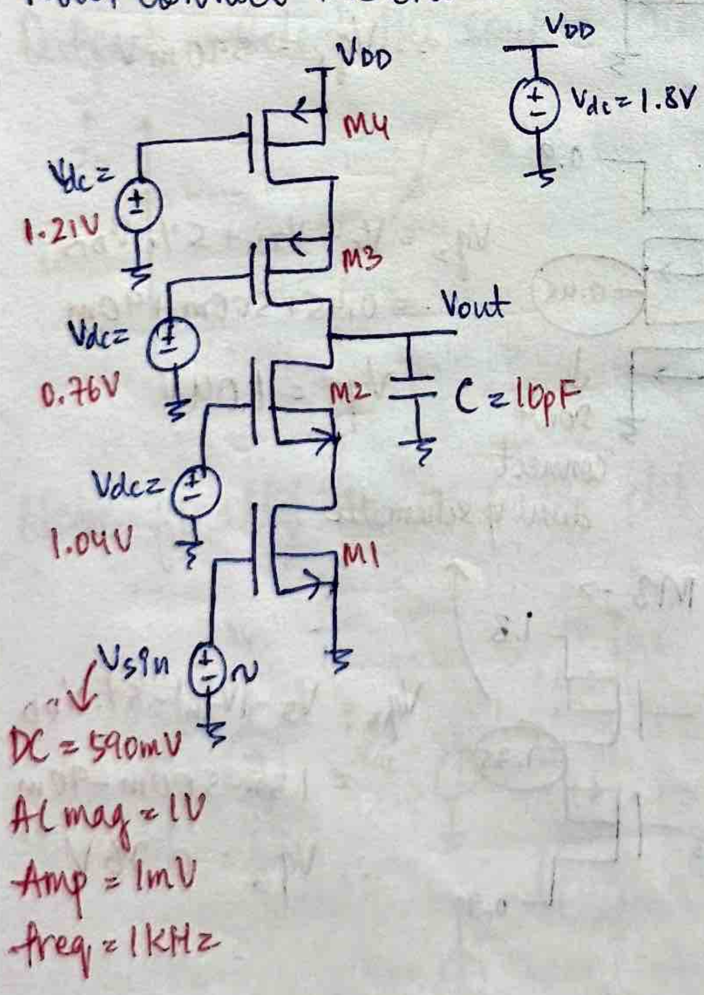
Outputs → M1 → Drain of M1 M3 → Source of M4
M2 → Drain of M1 M4 → Source of M4

Now, check W at I = 100µA

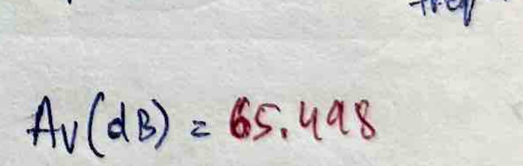


M1 = 14.946 µm
M2 = 16.65 µm
M3 = 41.475 µm (Make Fingers = 1)
M4 = 77.345 µm (Make Fingers = 2)

Now, connect the ckt. as,



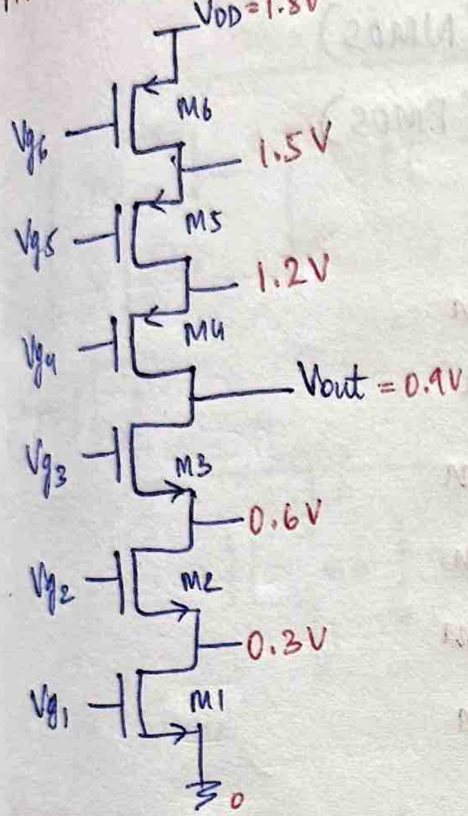
Now, AC analysis → freq = 1 to 1GHz
Output → Vout net



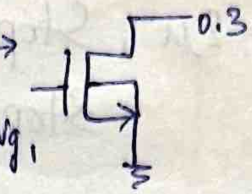
∴ Av(dB) = 65.498
3dB freq = 62.498 → 10.4708KHz
UGF = 20.165MHz

AICD - Exp 4c

Transistor sizing :-



M1 →

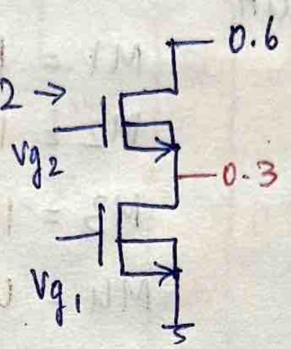


$V_{g_1} = V_s + V_{Tn} + 5\%\ V_{DD}$

$= 0 + 500m + 90m$

$= 590mV$

M2 →

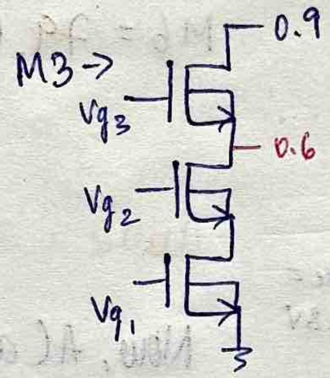


$V_{g_2} = V_s + V_{Tn} + 5\%\ V_{DD}$

$= 0.3 + 500m + 90m$

$= 890mV$

M3 →



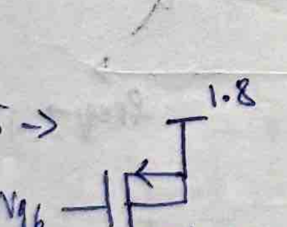
$V_{g_3} = V_s + V_{Tn} + 5\%\ V_{DD}$

$= 0.6 + 500m + 90m$

$= 1.19V$

V at each node $= \frac{V_{DD}}{n} = \frac{1.8}{6} = 0.3V$

M6 →

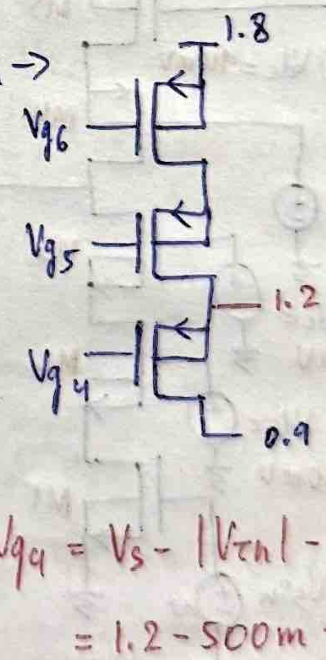


$V_{g_6} = V_s - |V_{Tn}| - 5\%\ V_{DD}$

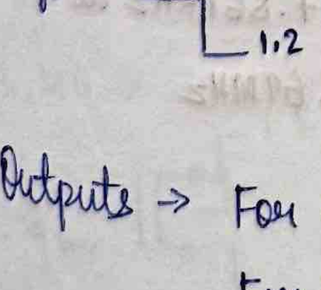
$= 1.8 - 500m - 90m$

$= 1.21V$

M4 →



M5 →



$V_{g_5} = V_s - |V_{Tn}| - 5\%.V_{DD}$

$= 1.5 - 500m - 90m$

$= 910mV$

$V_{g_4} = V_s - |V_{Tn}| - 5\%.V_{DD}$

$= 1.2 - 500m - 90m$

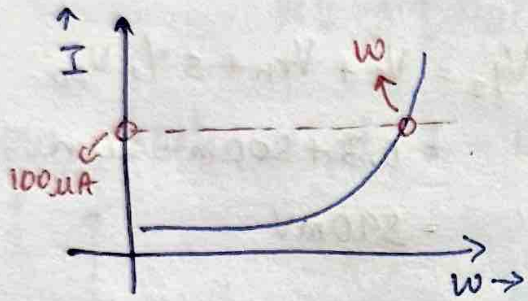
$= 610mV$

Outputs → For M1, M2, M3 → Drain of M1

For M4, M5, M6 → Source of M6

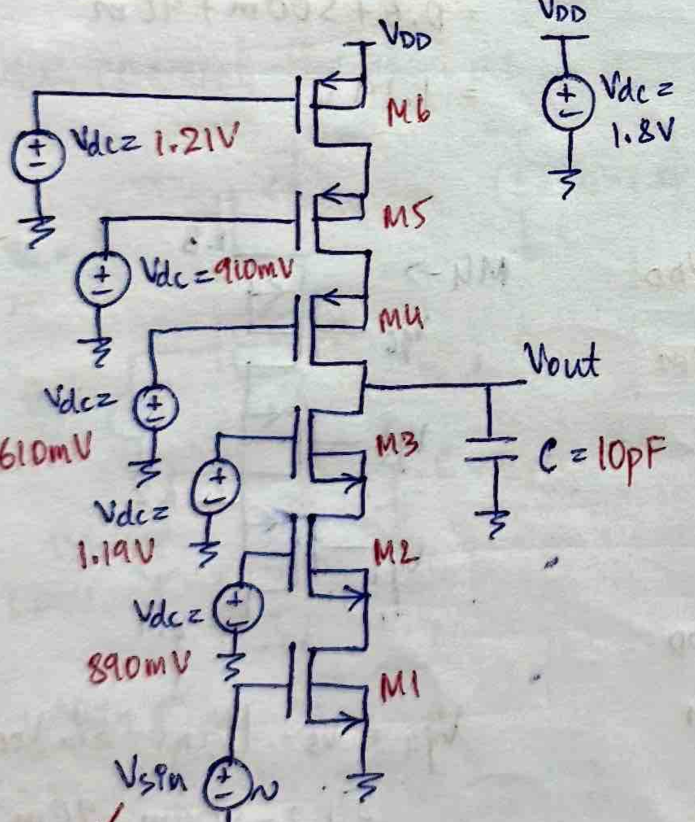
For DC analysis → Select the Tr → Select simW (width) →
Start = 2μ, Stop = 50μ (NMOS)
Stop = 100μ (PMOS)

Now, check w at I = 100μA



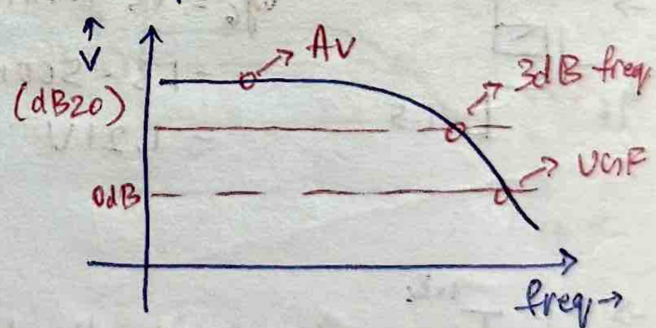
M1 = 15.31 μm
M2 = 15.4 μm
M3 = 14.87 μm
M4 = 45.36 μm
M5 = 52.94 μm
M6 = 79.18 μm

Now, connect the ckt. as,



DC voltage = 590mV
AC mag = 1V
Amp = 1mV
freq = 1KHz

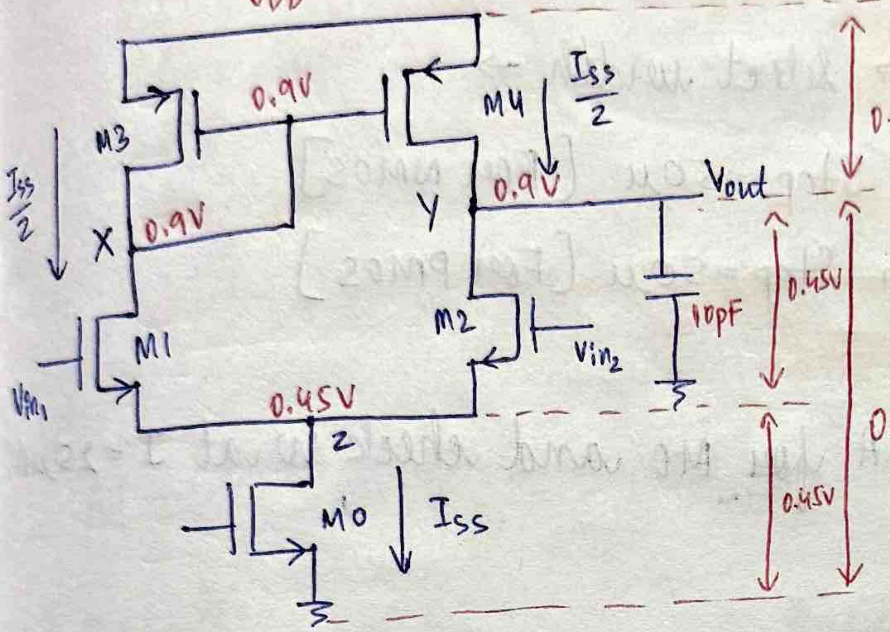
Now, AC analysis → freq = 1 to 1GHz
Output → Vout net



∴ Av (dB) = 67.77
3dB freq = 7.861 KHz at 64.77dB
UGF = 19.69 MHz

AICD - Exp 5

Using PDM,



1) $V_{DD} = 1.8V$

2) $V_X = V_Y = V_{out} = 0.9V$

$V_{g3} = V_{g4} = V_X = 0.9V$

3) $V_Z = 0.45V$

Length = 3 times 180nm

$\simeq$ 500nm

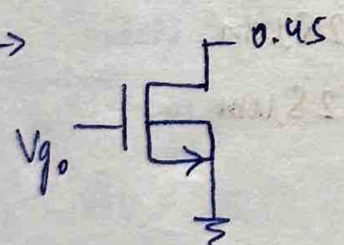
Now, I_{ss} = Slew rate $\times C_L$

$= 5V/\mu sec \times 10pF = 50\mu A$

$\therefore \frac{I_{ss}}{2} = \frac{50\mu}{2} = 25\mu A$

Transistor sizing :-

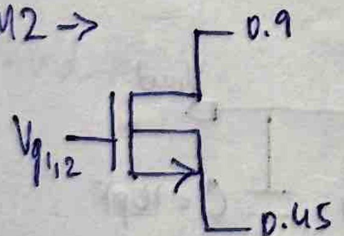
M0 ->



Now, $V_{g0} = V_s + V_{TN} + 5\% \; V_{DD}$

$= 0 + 500m + 90m = 590mV$

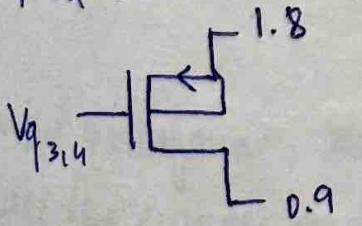
M1, M2 ->



Now, $V_{g1,2} = V_s + V_{TN} + 5\% \; V_{DD}$

$= 0.45 + 500m + 90m = 1.04V$

M3, M4 ->



Now, $V_{g3,4} = 0.9V$ [Because both PMOS are connected to node X & $V_X = 0.9V$]

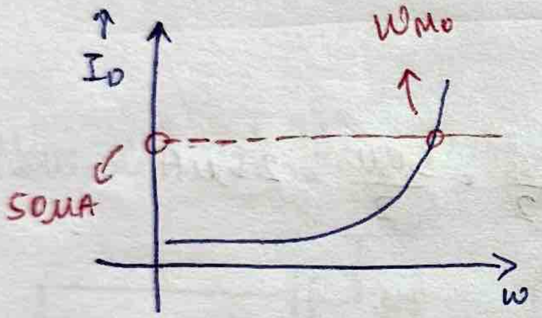
W.K.T, $I_{ss} = 50\mu A$ & $I_{ss}/2 = 25\mu A$

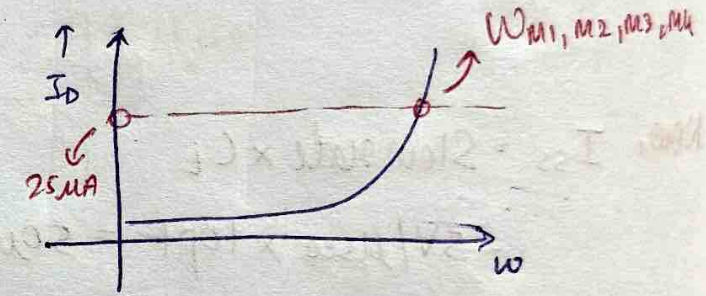
DC analysis → Select T^{r} → Select width →

Start = 2μ Stop = 50μ [For NMOS]

Start = 400n Stop = 50μ [For PMOS]

Now, check w at I = $50\mu A$ for M0 and check W at I = $25\mu A$ for M1, M2, M3, M4





$W_0 = 9.68\mu m$

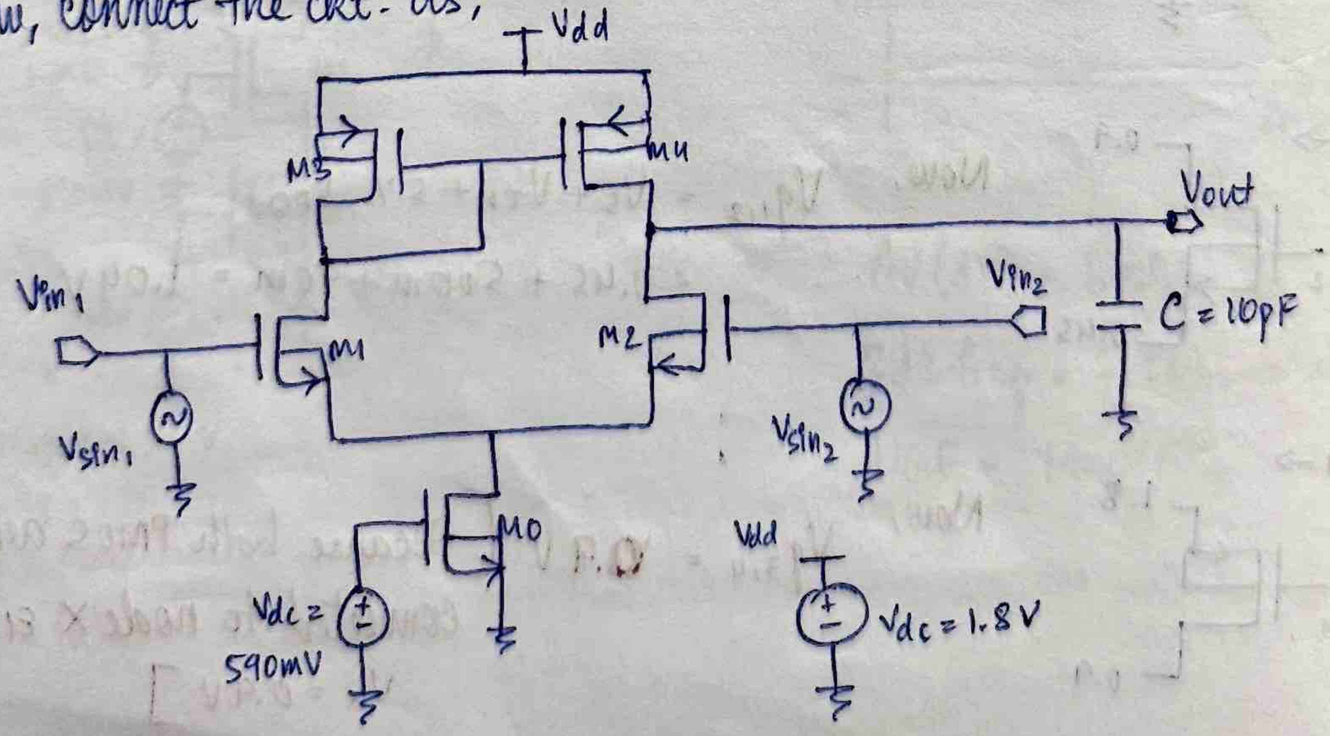
$W_1 = 5.04\mu m$

$W_2 = 5.04\mu m$

$W_3 = 2.28\mu m$

$W_4 = 2.28\mu m$

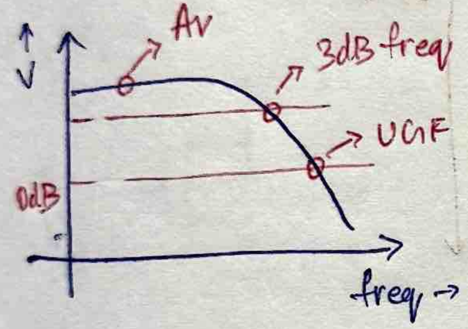
Now, connect the ckt. as,



$V_{sin_1} \rightarrow$ DC voltage = 1.04V
AC mag = 1V
Amp = 1mV
f = 1KHz
AC phase = 0
Initial sinusoidal phase = 0

$V_{sin_2} \rightarrow$ DC voltage = 1.04V
AC mag = 1V
Amp. = 1m V
f = 1KHz
AC phase = 180
Initial sinusoidal phase = 180

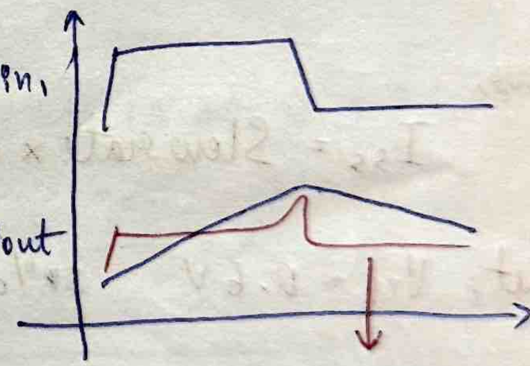
Now,
AC analysis → freq = 1 to 10GHz   Outputs → Vout net



∴ Av (dB) = 42.83
3dB freq = 71.83 KHz at 39.83dB
UGF = 9.966 MHz

Transient → Stop time = 10m
$V_{o(p-p)}$ = 264.6 mV
$V_{i(p-p)}$ = 1.965 mV

$$A_v = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{264.6m}{1.965m} = 134.7$$

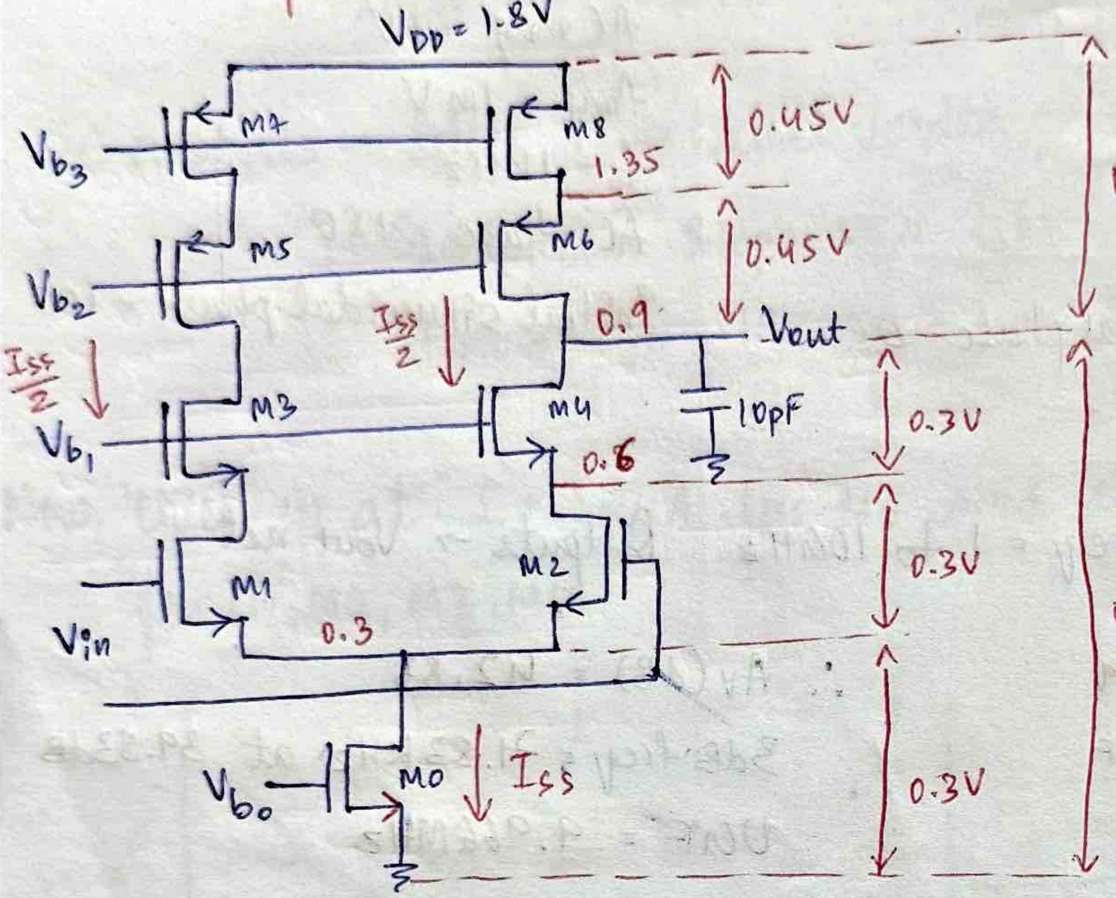


Slew = 5.87V/μs

To find slew :- Transient → Stop time = 20n
Now replace Vsin with Vpulse → DC voltage = 1.04V,
Period = 20n , Pulse width = 10n
V_{sin_1} → V1 = 0 V & V2 = 1.8 V
V_{sin_2} → V1 = 1.8 V & V2 = 0 V

In the waveform, select the Vout wave → Apply deriv function → Now place the cursor on the new wave to get slew value.

AICD - Exp 6



Now,

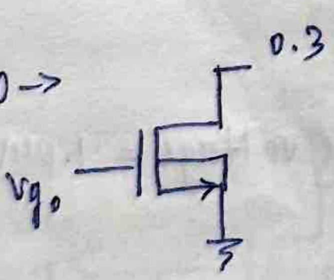
I_{ss} = Slew rate $\times C_L$ = $5V/\mu s \times 10pF = 50\mu A$

Let, $V_{Th} = 0.6V$ 5% V_{DD} = 90mV   L = 3 times 180 n ≃ 500nm

$\frac{I_{ss}}{2} = 25\mu A$

Transistor sizing:-

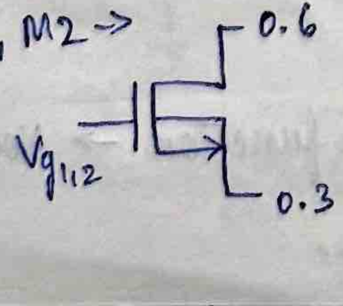
M0 ->



$V_{g_0} = V_s + V_{Th} + 5\% \, V_{DD}$

$= 0 + 600m + 90m = 690mV$

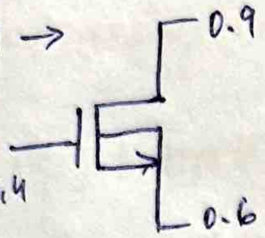
M1, M2 ->



$V_{g_{1,2}} = V_s + V_{Th} + 5\% \, V_{DD}$

$= 0.3 + 600m + 90m = 990mV$

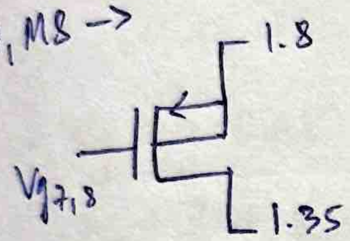
M3, M4 →



$V_{g_{3,4}} = V_s + V_{Tn} + 5\%\cdot V_{DD}$

$= 0.6 + 600m + 90m = 1.29V$

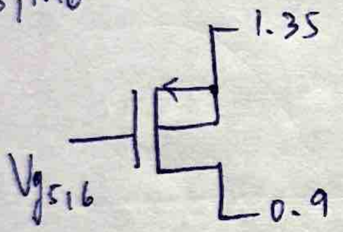
M7, M8 →



$V_{g_{7,8}} = V_s - |V_{Tn}| - 5\% \text{ of } V_{DD}$

$= 1.8 - 600m - 90m = 1.11V$

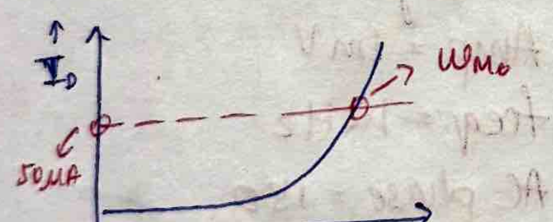
M5, M6 →



$V_{g_{5,6}} = V_s - |V_{Tn}| - 5\%\cdot V_{DD}$

$= 1.35 - 600m - 90m = 660mV$

For M0 → w at I = 50μA



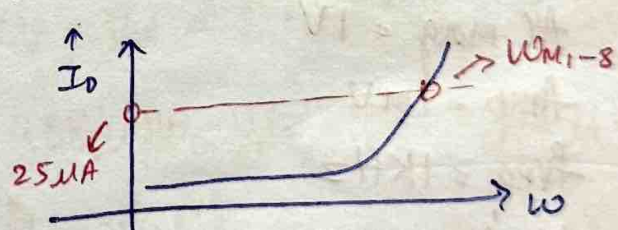
$\therefore W_{M_0} = 3.54\mu m$

DC analysis →

Start = 2μ Stop = 50μ (NMOS)

Start = 400n Stop = 50μ (PMOS)

For M1-8 → w at I = 25μA



$W_{M_1} = 1.699\mu m \simeq 1.7\mu m$

$W_{M_2} = 1.699\mu m \simeq 1.7\mu m$

$W_{M_3} = 1.7\mu m$

$W_{M_4} = 1.7\mu m$

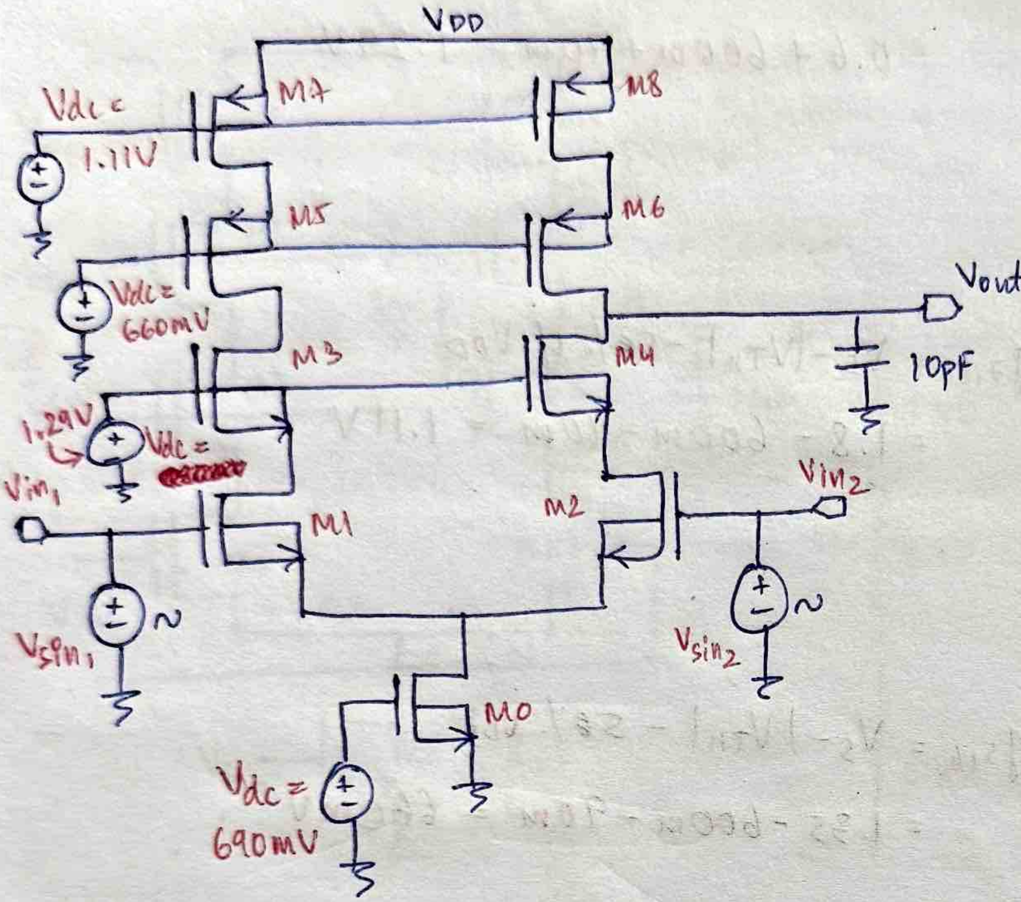
$W_{M_5} = 7.288\mu m \simeq 7.3\mu m$

$W_{M_6} = 7.3\mu m$

$W_{M_7} = 7.3\mu m$

$W_{M_8} = 7.3\mu m$

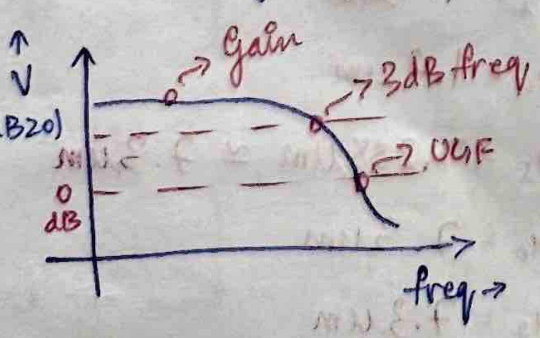
Now, connect the ckt. as,



V_{sin_1} → DC voltage = 990mV
AC mag = 1V
Amp = 1mV
freq = 1KHz
AC phase = 0
Initial sinusoidal phase = 0

V_{sin_2} → DC voltage = 990mV
AC mag = 1V
Amp = 1mV
freq = 1KHz
AC phase = 180
Initial sinusoidal phase = 180

Now, AC analysis → freq = 1 to 10GHz Output → Vout net



∴ A_V(dB) = 50.57
3dB freq = 8.39KHz at 47.57dB
UGF = 2.932MHz

Dummy DC analysis

M0 → $V_g = 690mV$, $V_s = 0V$, $V_d = 300.195mV$, $V_b = 0V$,
$I_D = 50.0054\mu A$, $g_m = 412.793\mu A/V$, $g_{ds} = 15.185\mu A/V$,
$r_o = 65.8544k\Omega$, Self gain $= g_m r_o = 27.18$

M1 → $V_g = 990mV$, $V_s = 300.195mV$, $V_d = 604.938mV$,
M2 $V_b = 300.195mV$, $I_D = 25.0025\mu A$, $g_m = 202.672\mu A/V$,
$g_{ds} = 7.65529\mu A/V$, $r_o = 130.629k\Omega$, Self gain $= 26.47$

M3 → $V_g = 1.29V$, $V_s = 604.938mV$, $V_d = 1.13557V$,
M4 $V_b = 604.938mV$, $I_D = 25.0059\mu A$, $g_m = 209.521\mu A/V$,
$g_{ds} = 2.75484\mu A/V$, $r_o = 362.998k\Omega$, Self gain $= 76.05$

M5 → $V_g = 660mV$, $V_s = 1.36037V$, $V_d = 1.13V$, $V_b = 1.36037V$,
M6 $I_D = 24.9992\mu A$, $g_m = 163.488\mu A/V$, $g_{ds} = 26.9048\mu A/V$,
$r_o = 37.1681k\Omega$, Self gain $= 6.07$

M7 → $V_g = 1.11V$, $V_s = 1.8V$, $V_d = 1.36037V$, $V_b = 1.8V$,
M8 $I_D = 25.0027\mu A$, $g_m = 184.681\mu A/V$, $g_{ds} = 3.47763\mu A/V$,
$r_o = 287.552k\Omega$, Self gain $= 53.10$

Transient → Stop time = 20 ns

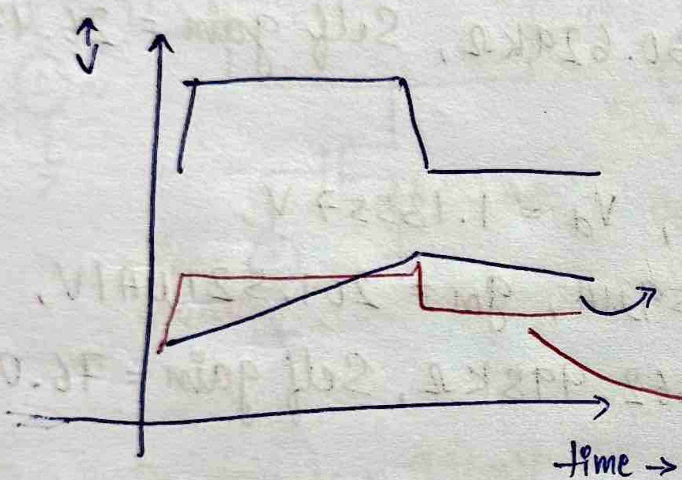
For, transient analysis, replace the V_{sin} with V_{pulse} →

DC voltage = 990 mV, Period = 20 ns, Pulse width = 10 ns,

for V_{sin1} → ~~V~~1 = 0V & V2 = 1.8V

for V_{sin2} → V1 = 1.8V & V2 = 0V

Outputs → Select Vout & Vin, → Run the analysis



In calculator, select the wave & apply the deriv function, we get a new wave, place cursor on that wave

∴ Slew = 2.5031 V/us

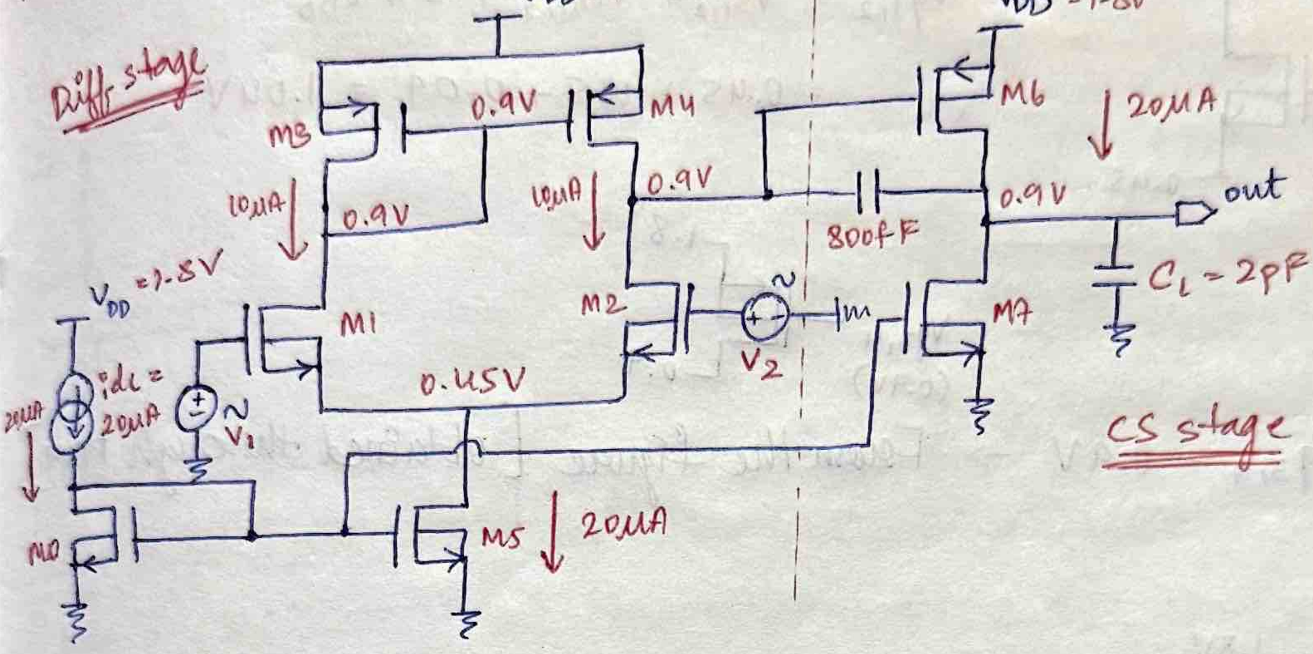
Transient → with V_{sin}

$V_{i(p-p)} = 2mV$

$V_{o(p-p)} = 489.5mV$

$A_V = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{489.5m}{2m} = 244.75$

AICD- Exp7



Given $V_{DD} = 1.8\,V$

Slew rate $= 20V/\mu s$

$C_L = 2pF$

$V_{Th} = 0.5\,V = 500mV$

Now, $I_{ss} = C_L \times$ Slew rate

$= 2p \times 20 \times 10^6 = 40\mu A$

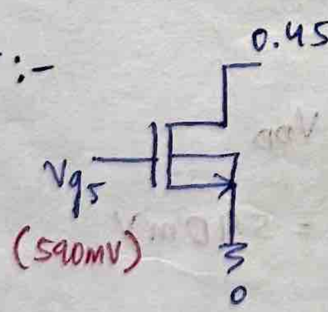
Here, we have two stages :-

1) Diff stage 2) CS stage

So, each stage carries $I = 20\mu A$

Transistor sizing :-

M5 :-

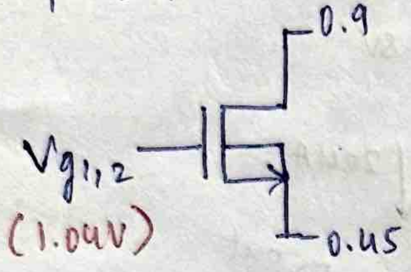


$V_{g5} = V_{s5} + V_{Th5} + 5\,\%\,V_{DD}$

$= 0 + 500m + 90m = 590mV$

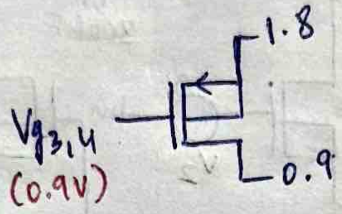
DC analysis -> Select NMOS -> Select w ->
Start = 400n, Stop = 50μ -> Outputs ->
Select drain of NMOS -> Run -> Check
w at I = 20μA

- M1, M2 :-



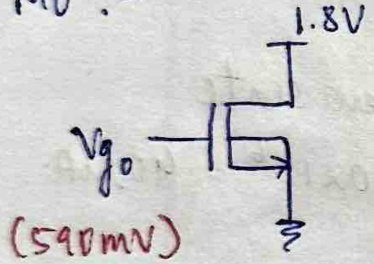
$$V_{g1,2} = V_{S1,2} + V_{Th1,2} + 5\% \, V_{DD}$$
$$= 0.45 + 0.5 + 0.09 = 1.04V$$

M3, M4 :-



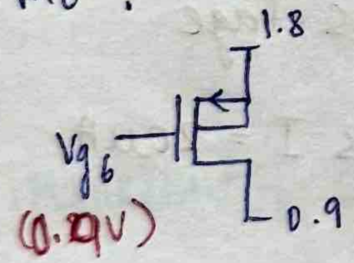
$V_{g3,4} = 0.9V \rightarrow$ From the figure [obtained through PDM]

M0 :-



$$V_{g0} = V_{s0} + V_{Th0} + 5\% \, V_{DD}$$
$$= 0 + 500m + 90m = 590mV$$

M6 :-

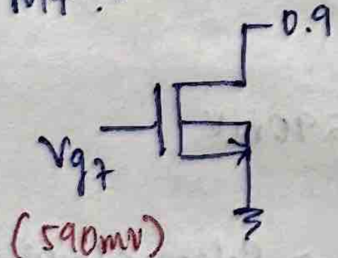


$\cancel{V_{g6} = V_{s6} + V_{Th6} + 5\% \, V_{DD}}$

$\cancel{= 1.8 + 500m + 90m = 2.39V}$

$V_{g6} = 0.9V$
↓
From the figure

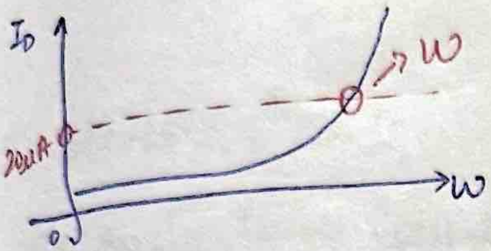
M7 :-



$$V_{g7} = V_{s7} + V_{Th7} + 5\% \, V_{DD}$$
$$= 0 + 500m + 90m = 590mV$$

Now, in DC curve,

$w = ?$ at $I = 20\mu A$



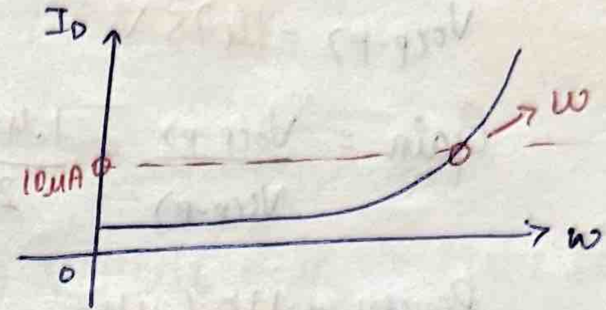
$w_0 = 3.56\mu m$

$w_5 = 3.99\mu m$

$w_6 = 1.83\mu m$

$w_7 = 3.81\mu m$

$w = ?$ at $I = 10\mu A$



$w_1 = 1.88\mu m$

$w_2 = 1.88\mu m$

$w_3 = 922.93nm \simeq 925nm$

$w_4 = 922.93nm \simeq 925nm$

Now,

V1 → DC voltage = 1.04V
AC mag = 1V
freq = 1KHz
Amp = 1mV
AC phase = 0
Initial sinusoidal phase = 0

V2 → DC voltage = 1.04V
AC mag = 1V
freq = 1KHz
Amp = 1mV
AC phase = 180
Initial sinusoidal phase = 180

Now,

AC analysis → freq = 1 to 1GHz   Output → out net

∴ Gain (dB) = 70.04

3dB freq = 14.863KHz at 67.04dB

UGF = 24.186MHz

Transient → Stop time = 10ms Outputs → V1, V2 & out net

$V_{i(p-p)} = 2mV$

$V_{o(p-p)} = 1.475 V$

$Gain = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{1.475}{2m} = 737.5$

Power = 110.6μW

M1, M2 → $V_g = 1.04V$, $V_s = 442.69mV$, $V_d = 877.386mV$, $V_b = 442.69mV$, $I_D = 10.946\mu A$, $g_m = 137.946\mu A/V$, $g_{ds} = 1.49687\mu A/V$, $r_o = 668.062k\Omega$, Self gain = 92.156

M3, M4 → $V_g = 877.386mV$, $V_s = 1.8V$, $V_d = 877.386mV$, $V_b = 1.8V$, $I_D = 10.946\mu A$, $g_m = 40.923\mu A/V$, $g_{ds} = 719.819nA/V$, $r_o = 1.389M\Omega$, Self gain = 56.85

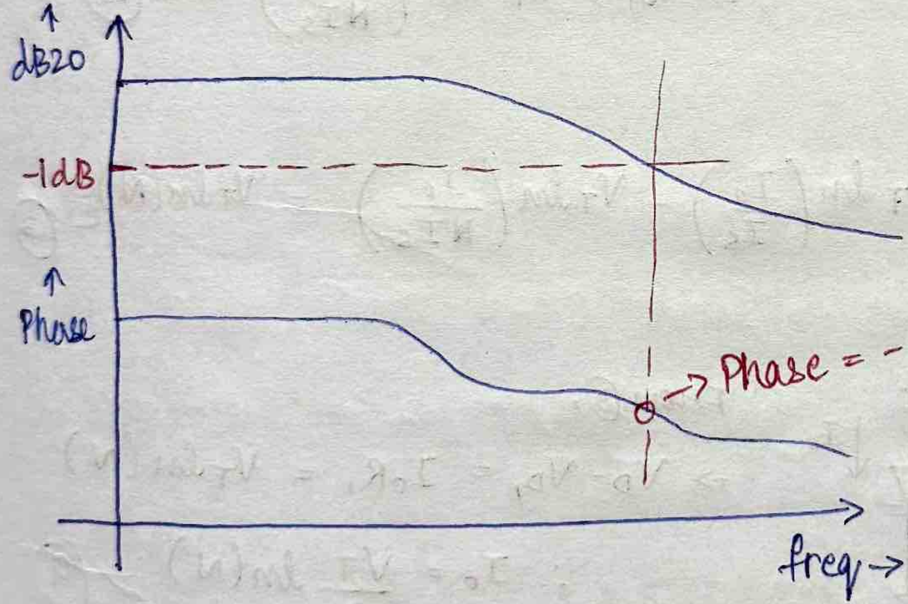
M5 → $V_g = 596.99mV$, $V_s = 0V$, $V_d = 442.69mV$, $V_b = 0V$, $I_D = 21.89\mu A$, $g_m = 281.595\mu A/V$, $g_{ds} = 2.86042\mu A/V$, $r_o = 349.599k\Omega$, Self gain = 98.44

M6 → $V_g = 877.386mV$, $V_s = 1.8V$, $V_d = 870.899mV$, $V_b = 1.8V$, $I_D = 21.847\mu A$, $g_m = 81.9952\mu A/V$, $g_{ds} = 1.4343\mu A/V$, $r_o = 697.201k\Omega$, Self gain = 57.167

M4 → $V_g = 596.991mV$, $V_s = 0V$, $V_d = 870.899mV$, $V_b = 0V$,
$I_D = 21.847\mu A$, $g_m = 278.97\mu A/V$, $g_{ds} = 1.748\mu A/V$,
$r_o = 572.066K\Omega$, Self gain $= 159.587$

To calculate phase :-

AC analysis → Copy the AC curve to seperate strip → Make one waveform to dB20 → Make the other to type "Phase" → Now in the dB20 plot place a horizontal line at -1dB. → Place a vertical line and at the intersection point, check value of phase in the Phase plot.



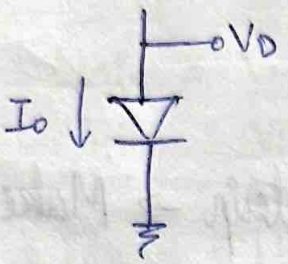
Now,

Phase Margin = $180 - 43.2049 = 136.79°$

AICD - Exp 8

$V_{DD} = 3.3V \quad I_{DC} = 5\mu A \quad N = 2$ (For PTAT)

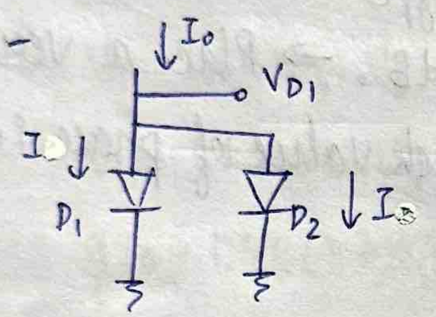
CTAT :-



$I_o = I_s e^{V_D/V_T}$

$\therefore V_D = V_T \cdot \ln\left(\frac{I_o}{I_s}\right)$ — ①

PTAT :-



$I_o = NI \quad$ W.K.T, $I = I_s e^{V_{D1}/V_T}$

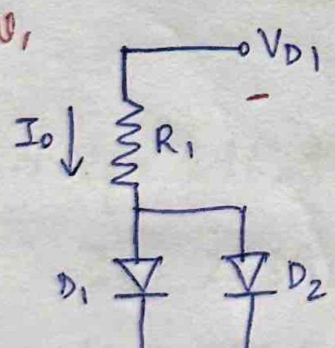
$\therefore I_o = N \cdot I_s e^{V_{D1}/V_T}$

$\Rightarrow V_{D1} = V_T \cdot \ln\left(\frac{I_o}{N I_s}\right)$ — ②

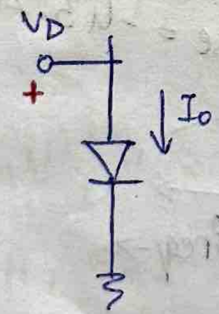
Now,

① - ② $\Rightarrow V_D - V_{D1} = V_T \ln\left(\frac{I_o}{I_s}\right) - V_T \ln\left(\frac{I_o}{N I_s}\right) = V_T \ln(N)$ — ③

Now,



PTAT



CTAT

From ③,

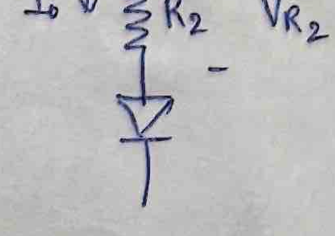
$\Rightarrow V_D - V_{D1} = I_o R_1 = V_T \ln(N)$

$\therefore I_o = \frac{V_T}{R_1} \ln(N)$ — ④

OR

$R_1 = \frac{V_T}{I_o} \ln(N)$

For getting PTAT, consider a seperate resistor, therefore



$\therefore V_{R_2} = I_o R_2 = V_T \ln(N) \frac{R_2}{R_1} \rightarrow$ From ④

$\therefore V_{R_2} = \alpha_1 V_T$ where, $\alpha_1 = \ln(N) \frac{R_2}{R_1}$

W.K.T, $V_{ref} = \alpha_1 PTAT + \alpha_2 CTAT$

$= \alpha_1 V_T + \alpha_2 V_D \quad - (5)$

Now, $\frac{\partial V_{ref}}{\partial T} = 0 \Rightarrow \alpha_1 \frac{\partial V_T}{\partial T} + \alpha_2 \frac{\partial V_D}{\partial T} = 0$

$\therefore \alpha_1 (0.086 mV/K) + \alpha_2 (-1.6 mV/K) = 0$

Assume, $\alpha_2 = 1$

$\therefore \alpha_1 = \frac{1.6m}{0.086m} = 18.60$

(5) $\Rightarrow \therefore V_{ref} = (18.6)(26m) + (1)(0.7) = 1.1836 \simeq 1.2V$

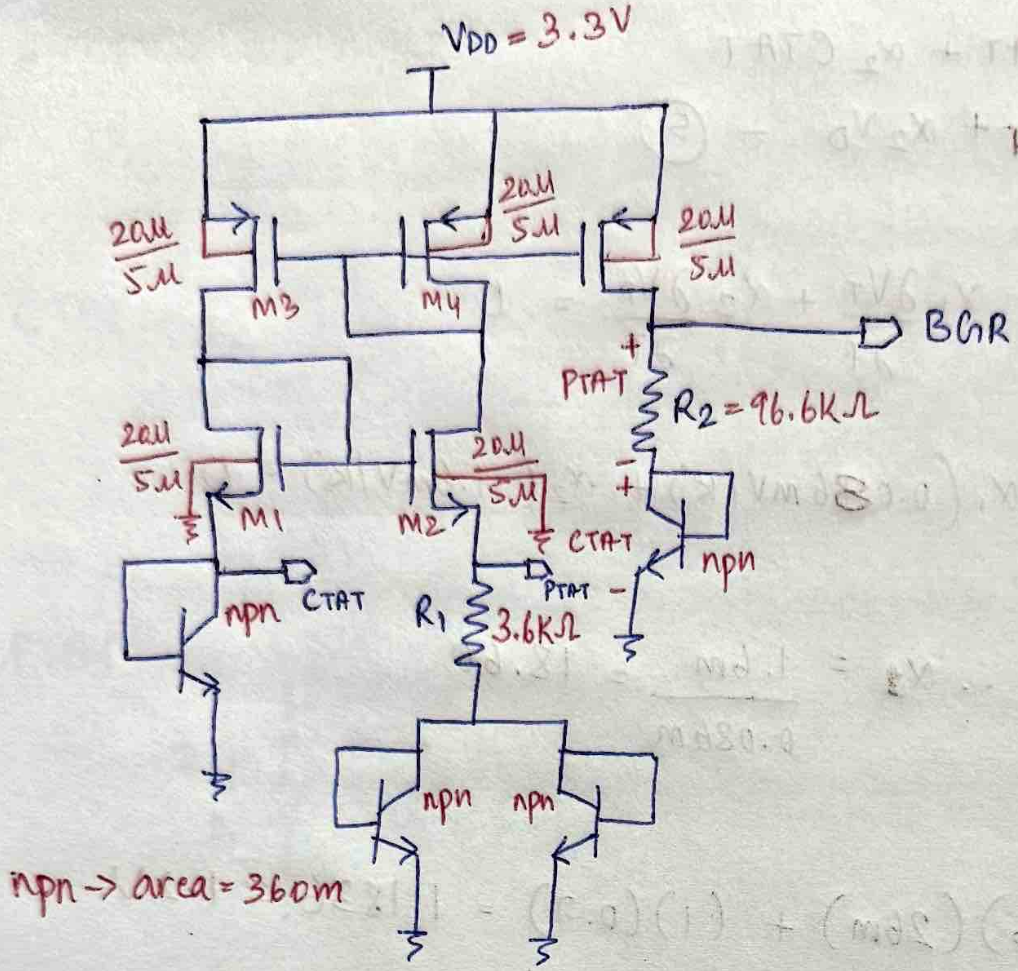
Now,

W.K.T, $R_1 = \frac{V_T \ln(N)}{I_0} = \frac{(26\times10^{-3})\ln(2)}{5\times10^{-6}} = 3.6K\Omega$

W.K.T, $\alpha_1 = \ln(N)\frac{R_2}{R_1} \Rightarrow R_2 = \frac{\alpha_1 R_1}{\ln(N)}$

$\therefore R_2 = \frac{(18.6)(3.6\times10^3)}{\ln(2)} = 96.6K\Omega$

Note :- Rig up the circuit in 90nm tech

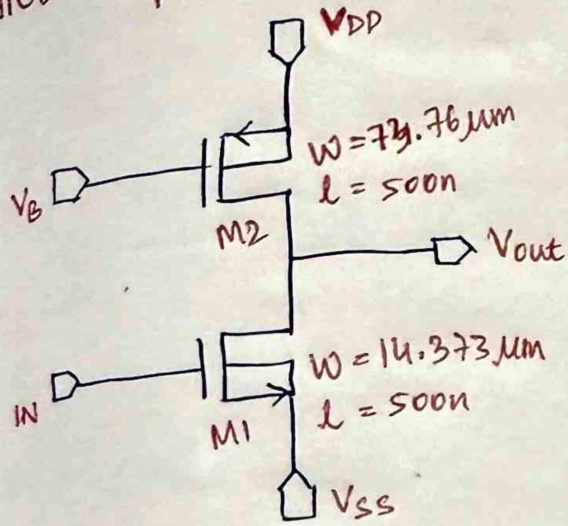


1) DC analysis :- Select Temperature -> Start = -50 Stop = 125

Outputs -> Select CTAT, PTAT, BGR

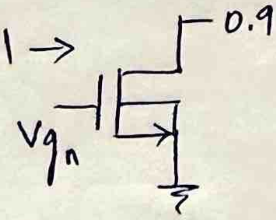
Extract graphs seperately & at last one graph will all three pins

AICD - Exp 9



Perform transistor sizing :-

M1 →

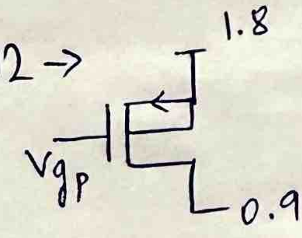


$V_{g_n} = V_S + V_{TN} + 5\% \, V_{DD}$

$= 0 + 500m + 90m$

$\therefore V_{g_n} = 590mV$

M2 →



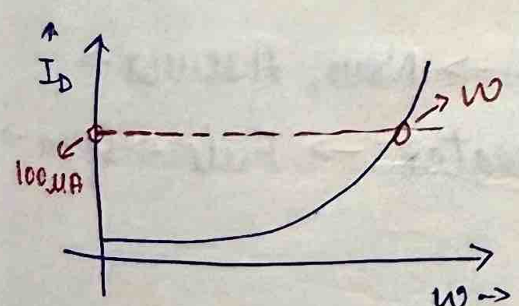
$V_{g_P} = V_S - |V_{TN}| - 5\% \, V_{DD}$

$= 1.8 - 500m - 90m$

$\therefore V_{g_P} = 1.21V$

DC analysis → Select component → Select PMOS / NMOS →
Select simW (Simulation width) → Start = 400n , Stop = 100µ → OK
Outputs → Drain of NMOS & Source of PMOS (Do seperately)
↳ For NMOS & PMOS

Now, W = ? at I = 100µA



$\therefore W_P = 73.76 \mu m$

$W_N = 14.373 \mu m$

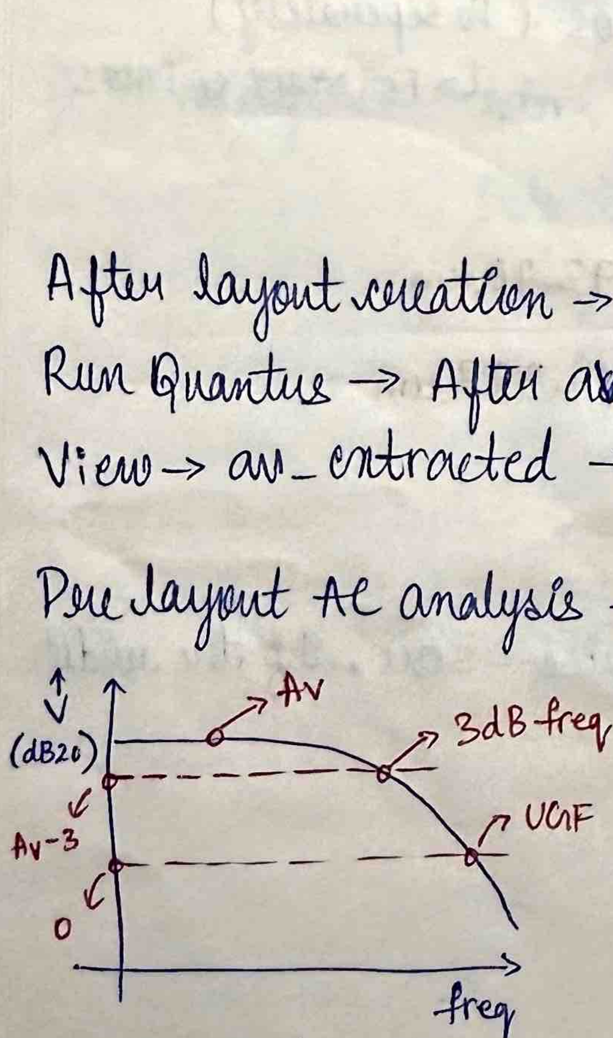
Note:- For 180nm tech, max width of device = 50µ. If the width exceeds 50µ, use fingers = 2.

∴ For PMOS → Fingers = 2
F.W = 36.88 µm
T.W = 73.76 µm

Dummy DC analysis → M2 & M1

After layout creation → Clear DRC & LVS → Now, Assura → Run Quantus → After av_extracted is created → File → Open → View → av_extracted → Click OK

Pre layout AC analysis → freq = 1 to 1 GHz Output → Vout



Gain(dB) = 37.84

3dB freq = 252.51KHz at 34.84dB

UGF = 20.153MHz

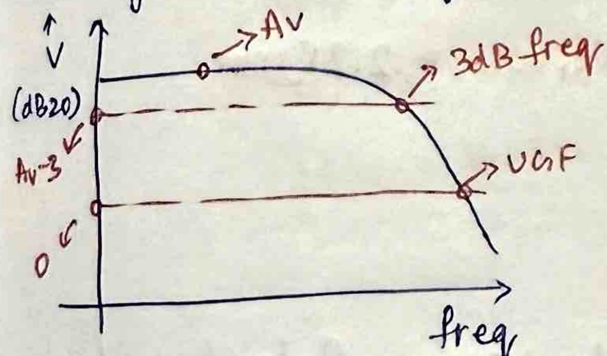
Transient → Stop time = 10m   Outputs → Vin & Vout

$V_{o(p-p)} = 155.6mV$

$V_{i(p-p)} = 2mV$

$$Gain = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{155.6m}{2m} = 77.8$$

Post layout AC analysis → freq = 1 to 1GHz   Output → Vout



Gain(dB) = 37.74

3dB freq = 246.856KHz at 34.74dB

UGF = 19.4827MHz

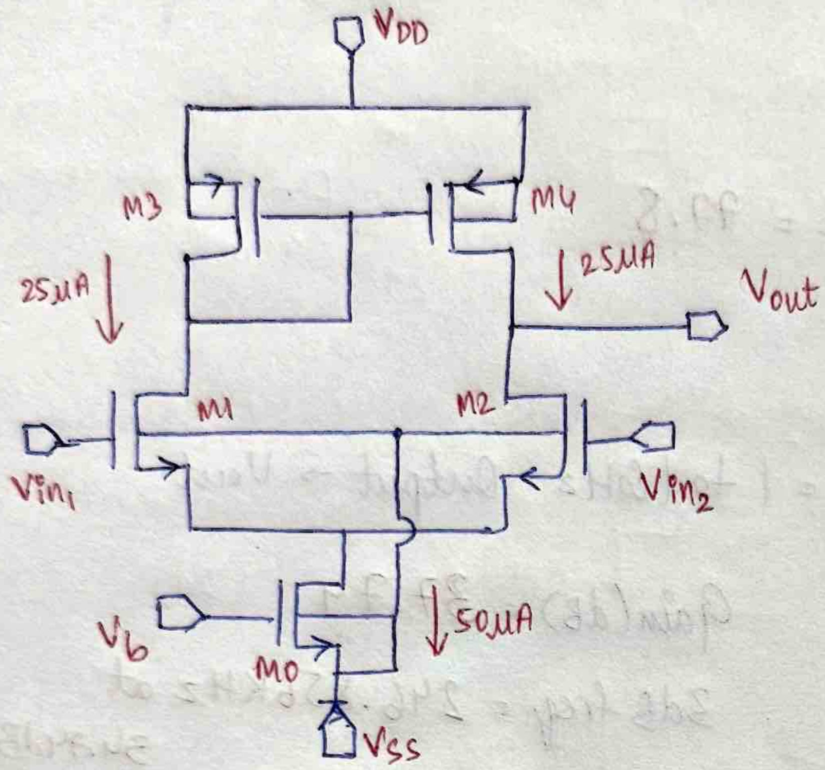
Post layout transient → Stop time = 10m   Outputs → Vin & Vout

$V_{o(p-p)} = 154mV$

$V_{i(p-p)} = 2mV$

$$Gain = \frac{V_{o(p-p)}}{V_{i(p-p)}} = \frac{154m}{2m} = 77$$

AICD - Exp 10



Perform Transistor sizing
(For simplicity, take the results of Exp-5)

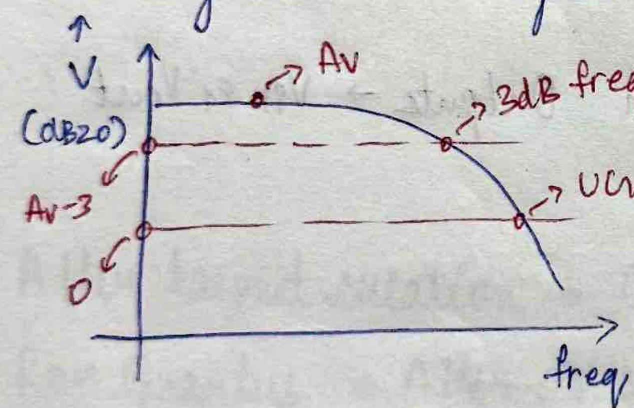
L = 500nm

W_0 = 9.68μm

W_1, W_2 = 5.04μm

$W_3; W_4$ = 2.28μm

Pre layout AC analysis :- freq = 1 to 1GHz   Output → Vout



Gain (dB) = 42.83

3dB freq = 71.83kHz at 39.83dB

UGF = 9.966MHz

Post layout AC analysis :-

Gain (dB) = 43.14

3dB freq = 66.943kHz at 40.14

UGF = 9.7597MHz

Pre layout transient → Stop time = 10m Output → Vin, & Vout

$V_{o(P-P)} = 264.6 mV$

$V_{i(P-P)} = 1.965 mV$

$$Gain = \frac{V_{o(P-P)}}{V_{i(P-P)}} = 134.7$$

Post layout transient →

$V_{o(P-P)} = 271.8 mV$

$V_{i(P-P)} = 1.946 mV$

$$Gain = \frac{V_{o(P-P)}}{V_{i(P-P)}} = 139.7$$

Dummy DC analysis → M0, M1 & M2, M3 & M4