

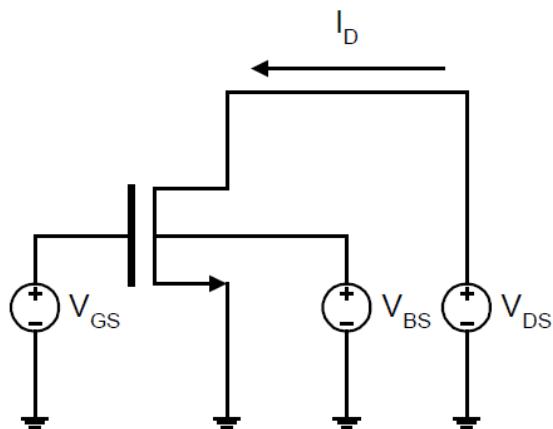
## EXPERIMENT 1

### STUDY OF MOS IV CHARACTERISTICS

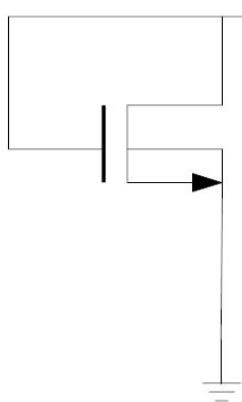
#### **OBJECTIVES:**

- i. To set up a MOS transistor to obtain  $I_D - V_{GS}$ ,  $I_D - V_{DS}$ ,  $I_D - V_{SB}$  characteristics
- ii. To estimate the small signal parameters  $g_m$ ,  $r_o$  and  $g_{mb}$  from IV characteristics.
- iii. Compare the small signal parameters obtained from graphical method and direct printing option from ADE L
- iv. To evaluate the small signal output resistance of MOSFETs in different configurations.

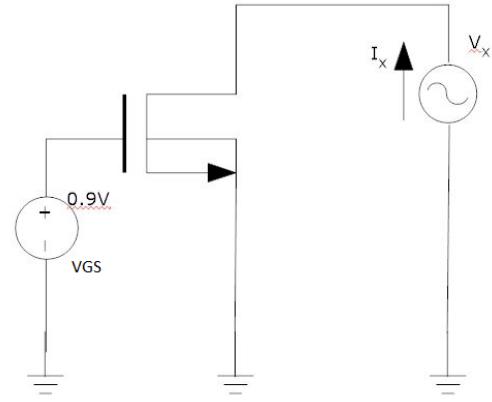
#### **CIRCUIT DIAGRAM:**



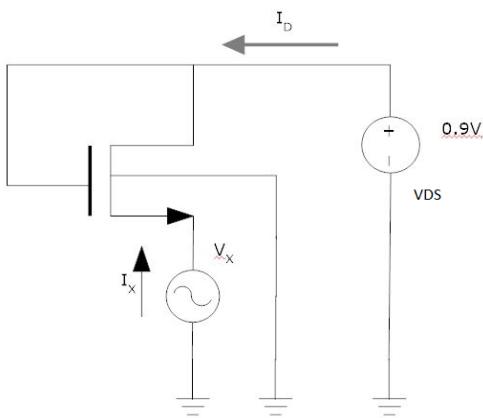
**Fig:1 MOSFET – SIMULATION SET UP**



**Fig:2 MOSFET Configuration**



**Fig:3 MOSFET Configuration**

**Fig:4 MOSFET Configuration**

## THEORY

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a type of field-effect transistor (FET), commonly fabricated by the controlled oxidation of silicon. It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. The traditional metal-oxide-semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO<sub>2</sub>) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a p-type semiconductor positive voltage V<sub>GB</sub> from gate to body creates a depletion layer by forcing the positively charged holes away from the gate-insulator or semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If V<sub>GB</sub> is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. The gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. When the voltage between transistor gate and source (V<sub>GS</sub>) exceeds the threshold voltage (V<sub>th</sub>), the difference is known as overdrive voltage.

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals.

**Cut off Region :** When V<sub>GS</sub> < V<sub>th</sub> where V<sub>GS</sub> is gate-to-source bias and V<sub>th</sub> is the threshold voltage of the device. The transistor is turned off, and there is no conduction between drain and source.

**Triode mode or linear region:** When V<sub>GS</sub> > V<sub>th</sub> and V<sub>DS</sub> < V<sub>GS</sub> – V<sub>th</sub>, the transistor is turned on, and a channel has been created which allows current between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current equation is as shown.

$$I_D = \frac{\mu_n C_{ox} W}{2} (V_{GS} - V_T)^2$$

**Saturation or active mode:** When  $V_{GS} > V_{th}$  and  $V_{DS} \geq (V_{GS} - V_{th})$ , the switch is turned on, and a channel has been created, which allows current between the drain and source. Since the drain voltage is higher than the source voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. Although the channel does not extend the full length of the device, the electric field between the drain and the channel is very high, and conduction continues. The current equation is as shown.

$$I_D = \frac{\mu_n C_{ox} W}{2} \frac{1}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{ds})$$

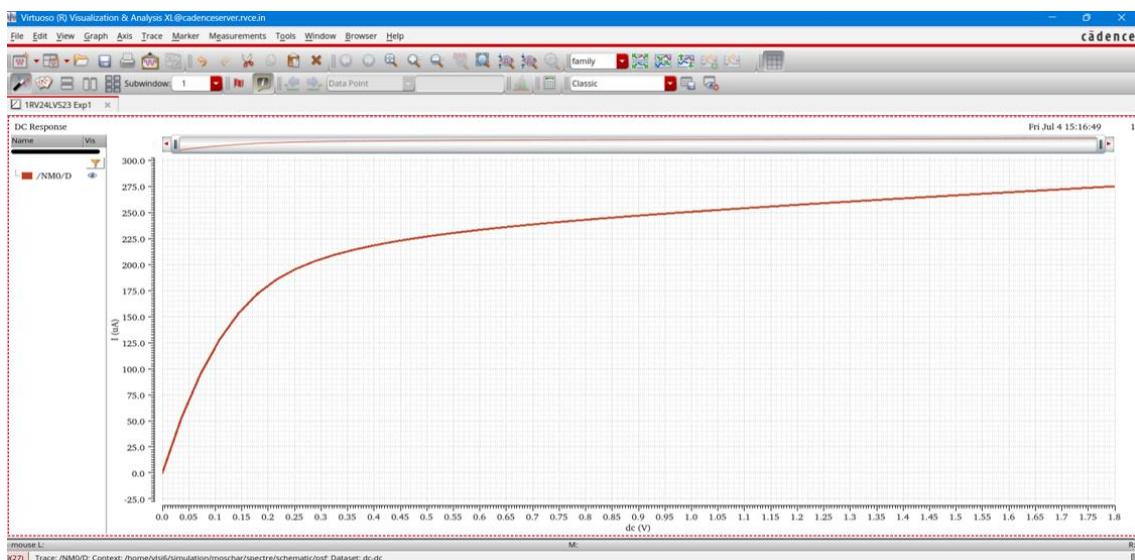
## EXPERIMENTAL PROCEDURE

1. Draw the circuit as shown in Fig1 with length of NMOS as 180nm and width 2um. Select Vdc voltage ( $v1 = V_{GS}$ ,  $V_{DS}$ ,  $V_{BS}$ ,  $v2=0$ ) at the input of gate, drain and body terminal of the NMOS respectively.
2. From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.
3. In the Analog Environment window select "Variables → Copy from Cell view". And give the values of  $V_{GS}$ ,  $V_{DS}$ ,  $V_{BS}$  as 0.9 V, 0.9V and 0V respectively.
4. Then in the window select “Analyses → Choose”. Select “dc” and then “Component Parameter”. Choose “Select Component” and then set start and stop voltages as 0 and 1.8 to sweep, for  $I_D - V_{SB}$  it is -1 to 1.8V.
5. Then select “Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic” to set the y-axis. Then run the simulation to see the results.
6.  $I_D - V_{GS}$  characteristics is obtained by choosing  $V_{GS}$  as the component in DC analysis.  $I_D - V_{DS}$  characteristics is obtained by choosing  $V_{DS}$  as the component in DC analysis. Similarly, by choosing  $V_{SB}$  for  $I_D - V_{SB}$ .
7. Press A and B keys to select two points on the graph and to measure the slope between the two points. In  $I_D - V_{GS}$  plot the points are chosen to be 850mv to 950mv. The slope gives the value of  $gm$ . Similarly,  $I_D - V_{DS}$  gives value of  $go$  (inverse gives  $ro$ ). Then plot of  $I_D - V_{SB}$  between points -50mv to 50mV gives  $gmb$  value.
8. Measure the  $I_D$  current by measuring the current value on y axis at voltage 0.9V on x axis in DC Analysis plot.
9. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS". This gives the values of all parameters of NMOS which can be used to compare with the graphically obtained values.
10. Draw the circuits shown in fig 2,3,4 and perform the dc analysis with  $V_{sin}$  voltage with name  $Vx$  (Dc voltage 900mV and Ac magnitude 1V). Then perform the ac analysis with frequency and range 1 to 100M Hz.
11. Plot the inverse of the graph using "Tools → Calculator" which gives the value of small signal output resistance of MOSFETs in different configurations. Verify the results "Results → Print → DC operating point and select NMOS". This gives the

values of all parameters of NMOS. Perform Parametric analysis by varying length L from 180nm to 1um in linear steps of 90nm for circuit 3 and 4 and view the plots.

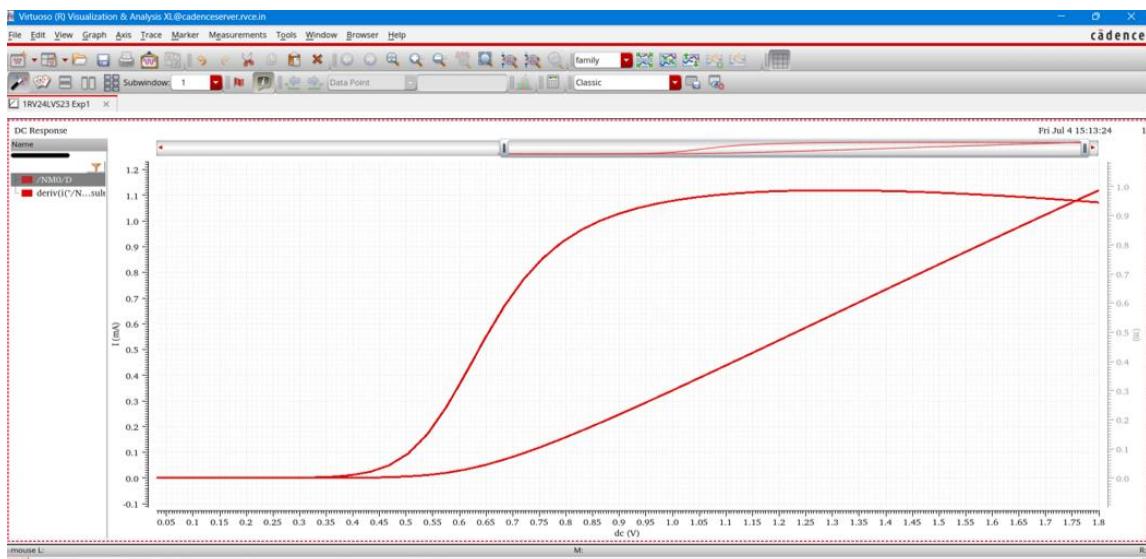
## DESIGN & ANALYSIS

The DC Analysis is performed for the Fig 1 basic circuit with  $V_{DS}$  as the component and the plot for  $I_D$  -  $V_{DS}$  characteristics is obtained as shown below. The slope is calculated which gives value of  $r_o$ . The slope is calculated at two points of 850mV and 950mV giving a difference of 100mV and the equation of  $R_{out} = 1/\lambda I_D$



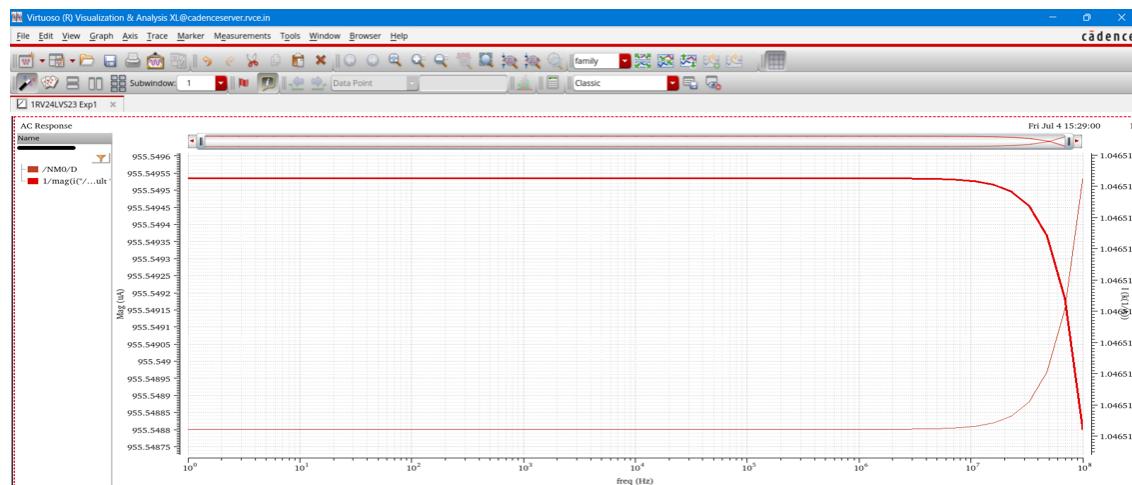
**Fig:5**  $I_D$  -  $V_{DS}$  characteristics

The DC Analysis is performed for the Fig 1 basic circuit with  $V_{GS}$  as the component and the plot for  $I_D$  -  $V_{GS}$  characteristics is obtained as shown below. The slope is calculated which gives value of  $g_m$ . The slope is calculated at two points of 850mV and 950mV giving a difference of 100mV and the equation of  $g_m = \partial I_D / \partial V_{GS} = 2I_D / (V_{GS} - V_{th})$



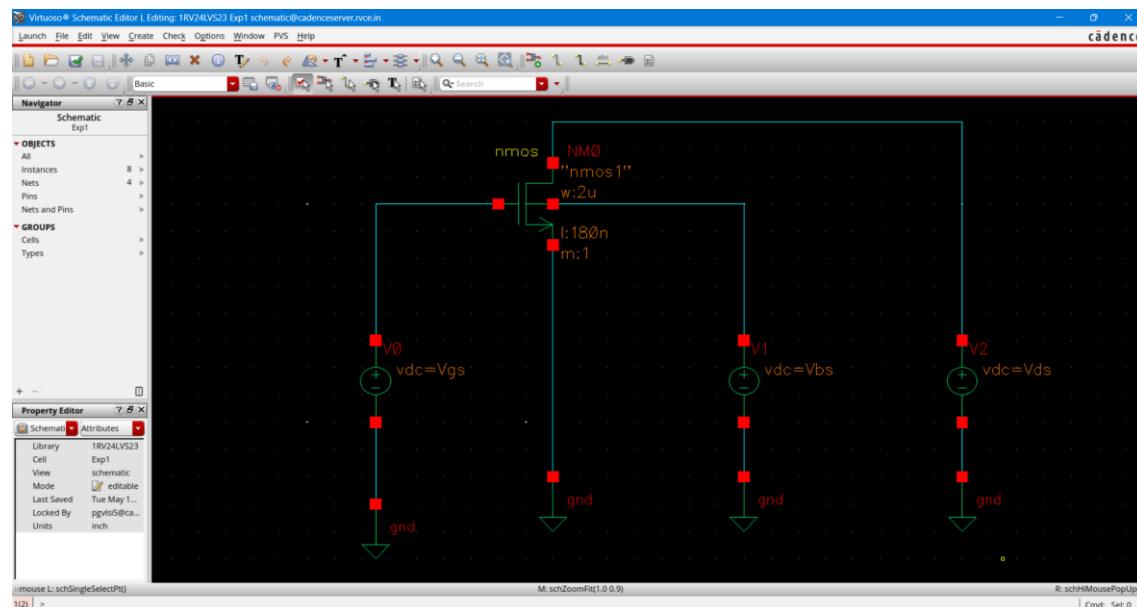
**Fig:6** Derivative of  $I_D$  -  $V_{GS}$  characteristics ( $g_m$  value)

The DC Analysis is performed for the Fig 1 basic circuit with  $V_{SB}$  as the component and the plot for  $I_D - V_{SB}$  characteristics is obtained as shown below. The slope is calculated which gives value of  $g_{mb}$ . The slope is calculated at two points of -50mV and +50mV giving a difference of 100mV and the equation of  $g_{mb} = \partial I_D / \partial V_{BS}$



**Fig:7**  $I_D - V_{SB}$  characteristics

The DC Analysis is performed for the Fig 1 basic circuit with  $V_{SB}$  as the component and the plot for  $I_D - V_{SB}$  characteristics is obtained as shown below. The slope is calculated which gives value of  $g_{mb}$ . The slope is calculated at two points of -50mV and +50mV giving a difference of 100mV and the equation of  $g_{mb} = \partial I_D / \partial V_{BS}$



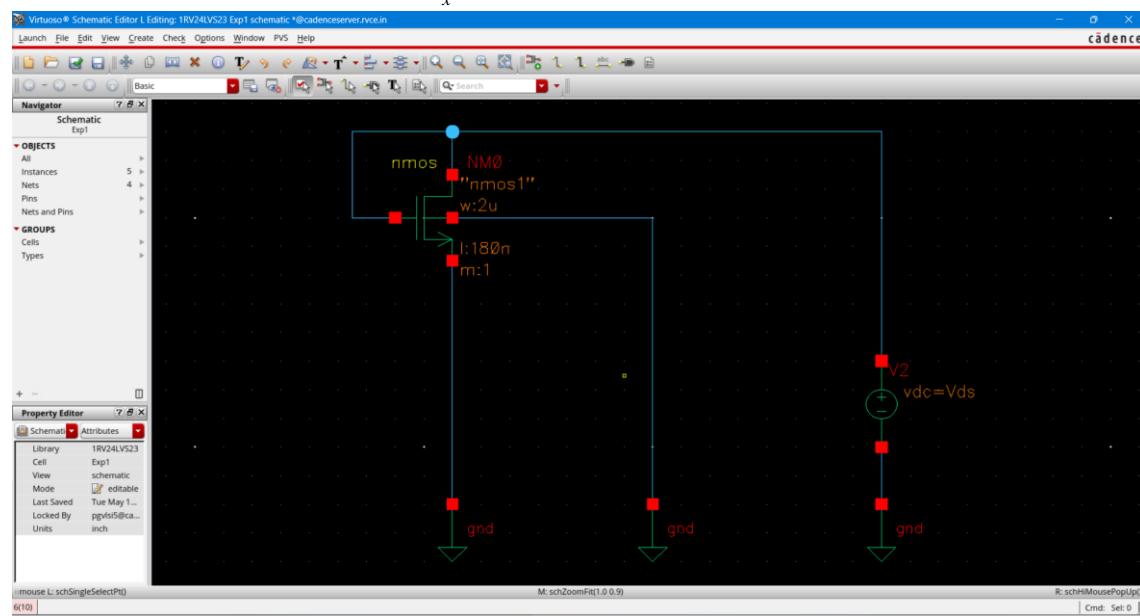
**Fig:8** MOSFET Configuration

The circuit shown below is Diode connected load circuit. From the small signal model of MOS transistor, the output resistance of the below circuit from the drain terminal is given by

$$R_{out} = \frac{1}{g_m} \parallel r_o$$

In the circuit test voltage is applied at drain end and current is driven through the NMOS. From the small signal model of MOS transistor, the output resistance of the

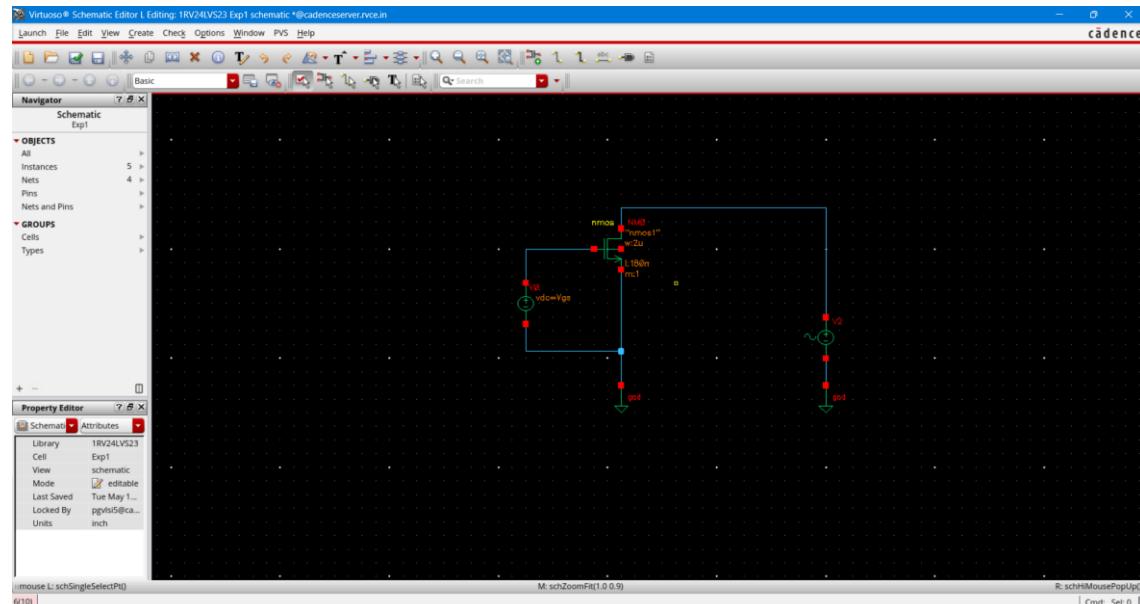
$$\text{below circuit is given by } R_{out} = \frac{V_x}{i_x}$$



**Fig:9 MOSFET Configuration**

In the circuit test voltage is applied at source end and current is driven through the NMOS. From the small signal model of MOS transistor, the output resistance of the

$$\text{below circuit is given by } R_{out} = \frac{1}{g_m + g_{mb}} \parallel r_o$$



**Fig:10 MOSFET Configuration**

## RESULTS

The DC Analysis for the Fig1 basic circuit is performed and the results are obtained graphically through  $I_D$  -  $V_{GS}$ ,  $I_D$  –  $V_{DS}$ ,  $I_D$  -  $V_{SB}$  characteristics. And they are compared with the direct results obtained from Print option.

NMOS (Fig 1)		Direct Results
$g_m$	<b>915.243u</b>	<b>917.516u</b>
$r_o$	<b>26.1910K</b>	<b>26.168K</b>
$g_{mb}$	<b>267.266u</b>	<b>276.508u</b>
$I_D$	<b>247.22u</b>	<b>247.2219u</b>

The AC analysis for Circuit in Fig 2 is performed and the final value of  $R_{out}$  is obtained graphically. Then from the direct results option  $g_m$  and  $r_o$  value are noted and  $R_{out}$  is calculated according to the equation.

NMOS (Fig 2)		Direct Results
$g_m$		<b>917.517u</b>
$r_o$		<b>26.1859K</b>
$R_{out}$	<b>1.0465K</b>	<b>1.0463K</b>

The AC analysis for Circuit in Fig 3 is performed and the final value of  $R_{out}$  is obtained graphically. Then from the direct results option  $r_o$  value is noted and  $R_{out}$  is calculated according to the equation.

NMOS (Fig 3)		Direct Results
$r_o$	<b>26.1910k</b>	<b>26.168K</b>

The AC analysis for Circuit in Fig 4 is performed and the final value of  $R_{out}$  is obtained graphically. Then from the direct results option  $r_o$ ,  $g_m$  and  $g_{mb}$  values are noted and  $R_{out}$  is calculated according to the equation.

NMOS (Fig 4)		Direct Results
$g_m$		<b>917.519U</b>
$r_o$		<b>26.185K</b>
$g_{mb}$		<b>276.50u</b>
$R_{out}$	<b>811.7</b>	

## DISCUSSIONS

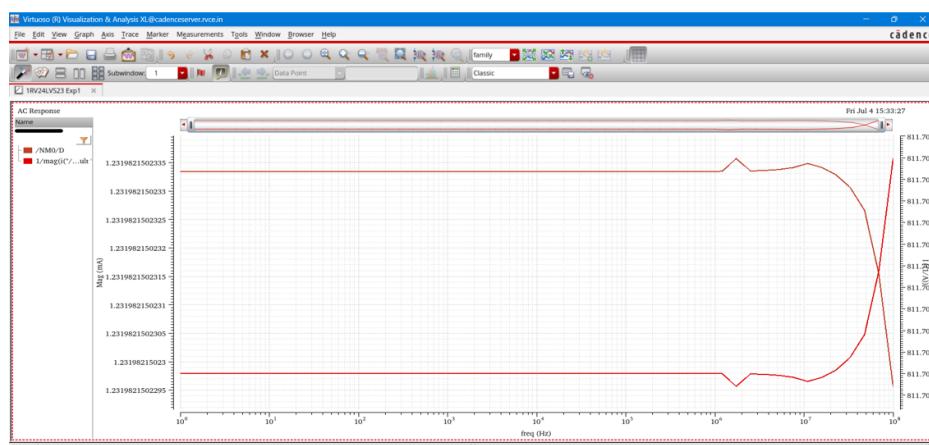
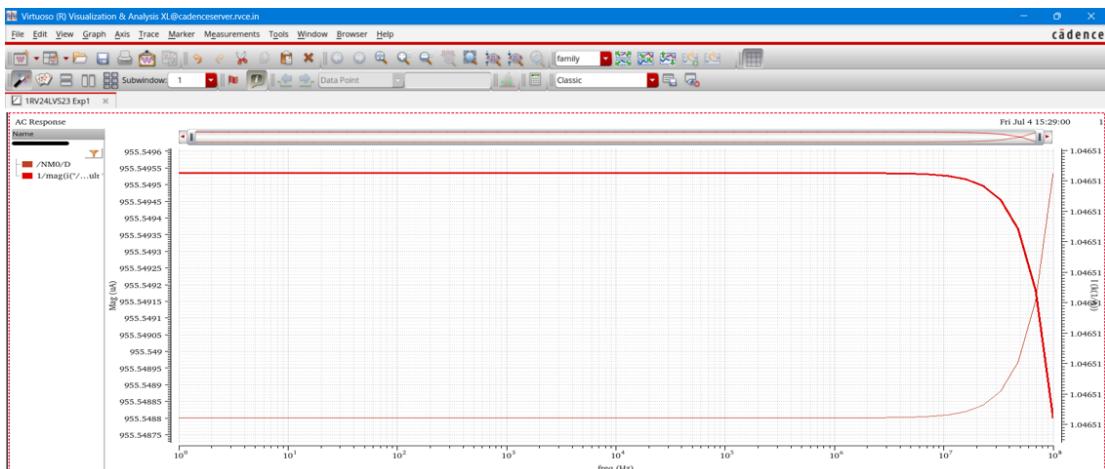


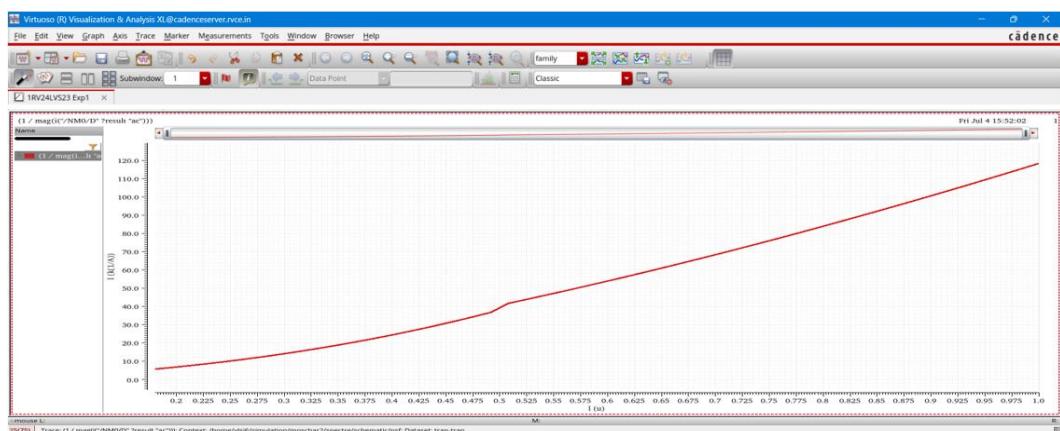
Fig:11 AC response of Fig 2 MOSFET Configuration

The AC response of diode connected load circuit is as shown in fig 11. The AC response is the plot of Id current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit.



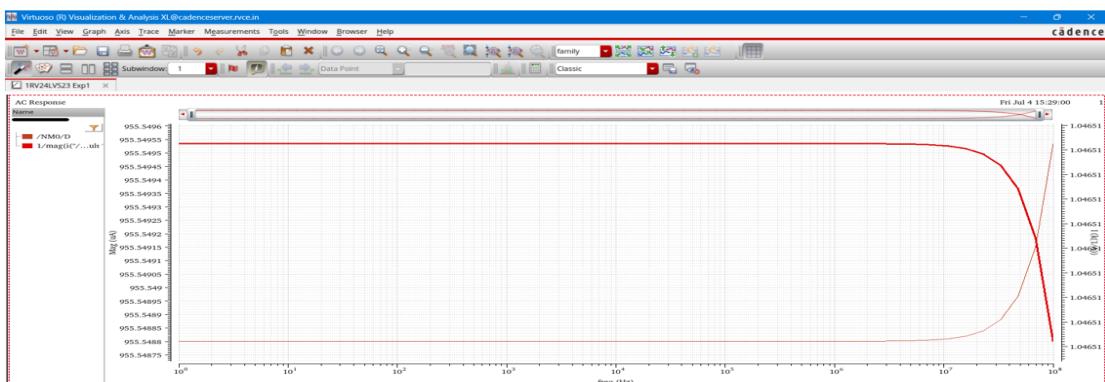
**Fig:12 AC response of Fig 3 MOSFET Configuration**

The AC response of fig 3 MOSFET circuit is as shown in fig 12. The AC response is the plot of Id current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit.



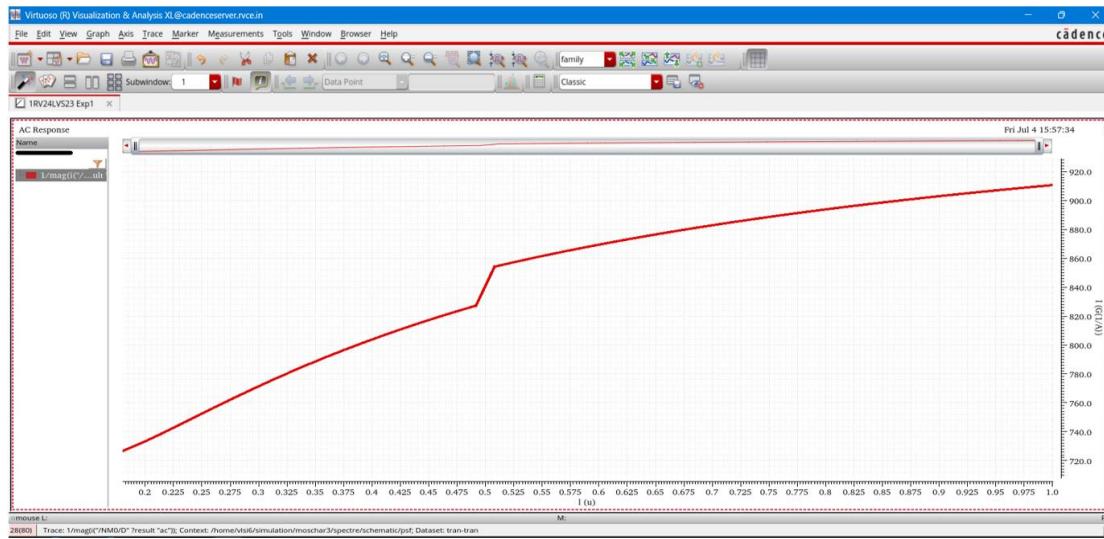
**Fig:13 Rout plot of Fig 3 MOSFET Configuration with varying L**

Perform Parametric analysis for AC response by varying length L from 180nm to 1um in linear steps of 90nm for circuit 3 and view the plot.



**Fig:14 AC response of Fig 4 MOSFET Configuration**

The AC response of fig 4 MOSFET circuit is as shown in fig 14. The AC response is the plot of Id current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit.



**Fig:15 Rout plot of Fig 4 MOSFET Configuration with varying L**

Perform Parametric analysis for AC response by varying length L from 180nm to 1um in linear steps of 90nm for circuit 4 and view the plot.

### INFERENCE:

The MOS transistor was biased with appropriate values of VGS, VDS, and VBS. The width (W) and length (L) of the transistor were chosen as  $2\text{ }\mu\text{m}$  and 180 nm respectively. The transistor was simulated for different input voltages: VGS, VDS, and VSB in the range of 0 V to 1.8 V, and the results were plotted to obtain the DC characteristics. From the resulting graphs, the small signal parameters such as gm, ro, and gmb were extracted using the slope method. These values were then compared with the values obtained using the direct ADE L print option.

The small signal parameters obtained from the plots were:  $\text{gm} = 906.9479\text{ }\mu\text{A/V}$ ,  $\text{ro} = 25.78\text{ k}\Omega$ , and  $\text{gmb} = 264.57\text{ }\mu\text{A/V}$ . The direct values obtained using ADE L were:  $\text{gm} = 918.161\text{ }\mu\text{A/V}$ ,  $\text{ro} = 26.168\text{ k}\Omega$ , and  $\text{gmb} = 276.67\text{ }\mu\text{A/V}$ . AC analysis was performed for three circuit configurations: diode-connected, source-follower, and common-source. The Rout values from AC analysis were obtained and compared between graphical and ADE L methods. For the three configurations, the Rout values were found to be:  $1.046\text{ k}\Omega$ ,  $25.78\text{ k}\Omega$ , and  $871.13\text{ }\Omega$  from plots; and  $1.0456\text{ k}\Omega$ ,  $26.1685\text{ k}\Omega$ , and  $811.046\text{ }\Omega$  from ADE L respectively.

The values obtained from both methods were closely matching, validating the correctness of the simulation and extraction process. The results also demonstrated the behavior of MOS transistors under different biasing conditions and highlighted how different configurations influence the output resistance.

As the channel length reduces, the effect of channel length modulation becomes more dominant, thereby reducing the accuracy of analog models. This emphasized the importance of considering advanced modeling techniques for deep submicron technologies while designing analog circuits.

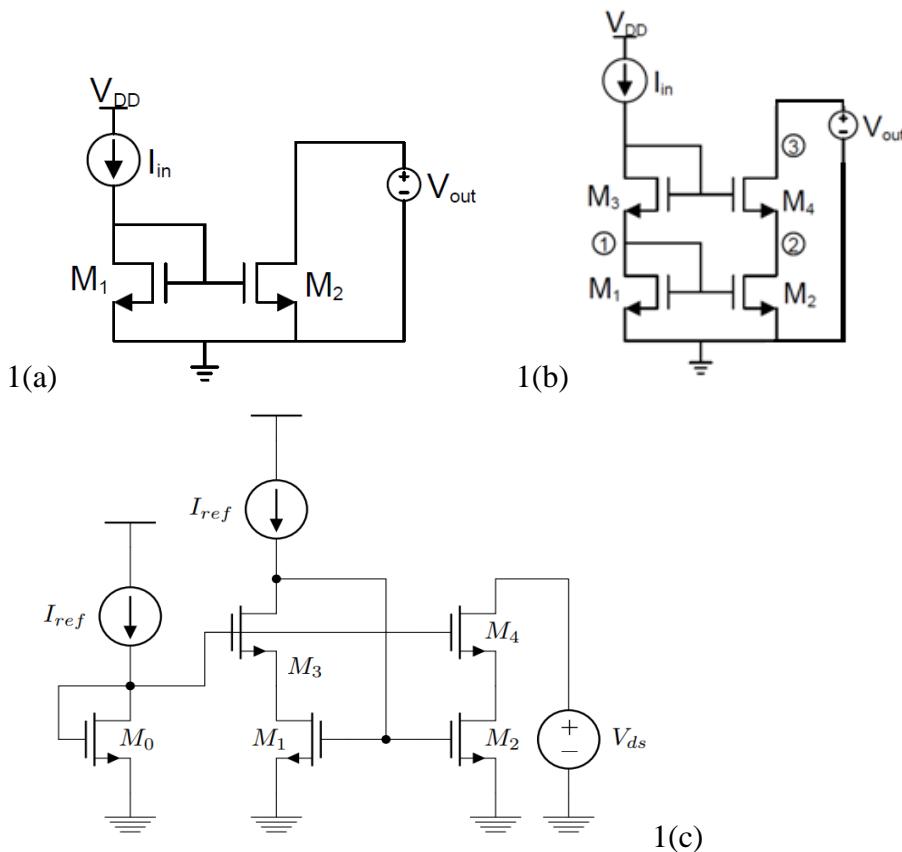
## EXPERIMENT 2

### STUDY OF MOS CURRENT MIRRORS

#### OBJECTIVES:

- i. To plot  $I_D$  vs  $V_{DS}$  of a MOSFET for  $L = L_{min}$ ,  $1\mu m$  ,  $590nm$  and  $180nm$  and observe the effect of channel length modulation at  $V_{DS} = 0.9V$  using  $W = 10\mu m$ .
- ii. To simulate a basic MOS current mirror, cascode MOS current mirror and high swing cascade current mirror using  $I_{REF}$  of  $100 \mu A$  and measure the  $I_{out}$ .
- iii. To estimate low frequency output impedance of all the current mirror circuits given in (ii).
- iv. To estimate  $V_{out,min}$  for all the current mirrors and verify the region of operation for the output transistor(s).

#### CIRCUIT DIAGRAM



**Fig: 1(a) Basic Current mirror, (b)Cascode current mirror, (c) Low voltage cascode current mirror (High swing cascode current mirror)**

#### THEORY

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being copied can be a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current

source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.

The main purpose of the current mirror circuit is to bias the transistors. We need to bias the transistors so that they operate in the desired region. A current mirror circuit is designed in such a way that the current in one active device is controlled by copying the current from another active device. The output current is thus kept constant.

Three main specifications that characterize a current mirror are

- Transfer Ratio or the output current magnitude
- AC output resistance
- Minimum voltage drop

Transfer Ratio is used in the case of a current amplifier or the output current magnitude in the case of a constant current source. AC output resistance determines how much the output current varies with the voltage applied to the mirror. The third specification is in the minimum voltage drop across the output part of the mirror necessary to make it work properly. This minimum voltage is dictated by the need to keep the output transistor of the mirror in active mode. Compliance range is the range of voltages where the mirror works and the voltage marking the boundary between good and bad behavior is called the compliance voltage.

### **Basic MOSFET current mirror:**

The basic current mirror can also be implemented using MOSFET transistors. Transistor M<sub>1</sub> is operating in the saturation or active mode, and same for M<sub>2</sub> transistor in Basic Current mirror in figure 1(a). The output current I<sub>OUT</sub> is directly related to I<sub>REF</sub>(I<sub>in</sub>). The drain current of a MOSFET I<sub>D</sub> is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by I<sub>D</sub> = f(V<sub>GS</sub>, V<sub>DG</sub>), a relationship derived from the functionality of the MOSFET device. In the case of transistor M<sub>1</sub> of the mirror, I<sub>D</sub> = I<sub>in</sub>. Reference current I<sub>in</sub> (I<sub>REF</sub>) is a known current. Using V<sub>DG</sub> = 0 for transistor M<sub>1</sub>, the drain current in M<sub>1</sub> is I<sub>D</sub> = f(V<sub>GS</sub>, V<sub>DG</sub>=0), so we find: f(V<sub>GS</sub>, 0) = I<sub>in</sub> (I<sub>REF</sub>), implicitly determining the value of V<sub>GS</sub>. Thus I<sub>in</sub> (I<sub>REF</sub>) sets the value of V<sub>GS</sub>. The basic current mirror circuit in the fig 1 forces the same V<sub>GS</sub> to be applied to transistor M<sub>2</sub>. If M<sub>2</sub> is also biased with zero V<sub>DG</sub> and provided transistors M<sub>1</sub> and M<sub>2</sub> have good matching of their properties, such as channel length, width, threshold voltage, etc., the relationship I<sub>OUT</sub> = f(V<sub>GS</sub>, V<sub>DG</sub> = 0) applies, thus setting I<sub>OUT</sub> = I<sub>in</sub> (I<sub>REF</sub>). The output current is the same as the reference current when V<sub>DG</sub> = 0 for the output transistor, and both transistors are matched.

- Minimum output voltage is  $V_{MIN(out)} = V_{ON}$
- Output resistance is  $R_{out} = \frac{1}{\lambda D}$
- Input resistance is  $R_{in} \approx \frac{1}{g_m}$
- Current gain accuracy is poor because  $v_{DS1} \neq v_{DS2}$

### Cascode current mirror:

One of the desirable characteristics for a current mirror is a very high output resistance that cascode connection achieves. A MOSFET current mirror based on cascode connection is shown in Fig 1(b). The MOSFETs M2 and M1 form a simple current mirror. M4 acts as the common gate part of the cascode and transfers the drain current of M3 to the output presenting a high output resistance. M3 acts as a diode level shifter and assures that M4 and M2 always remain in saturation. For MOS cascode as dc current gain  $\beta_0 \rightarrow \infty$ , the number of stacked cascode devices can be increased. This will be limited by the MOS substrate leakage current that creates a resistive shunt dominating output resistance for  $V_{OUT} > V_{OUT\min}$ . As  $V_{DS1}=V_{GS1}$ , shows that  $V_{DS2}=V_{DS1}$  when  $V_{GS4}=V_{GS3}$ . With this condition, the systematic current gain of the cascode current mirror is zero due to identical bias on M2 and M4 and  $\beta_F \rightarrow \infty$ . Actually,  $V_{GS4}$  is not exactly equal to  $V_{GS3}$  even with perfectly matched MOSFETs unless  $V_{OUT}=V_{IN}$ . Thus,  $V_{DS2} \approx V_{DS1}$ . The input voltage here is composed of two gate-source drops, each including threshold and overdrive components. Neglecting body effect and assuming that MOSFETs have got equal overdrives we get the following expressions, thus setting  $I_{OUT} = I_{in} (I_{REF})$ :

- $R_{out}: v_{out} = i_{out}[r_{ds4} + r_{ds2} + g_{m4}r_{ds2}r_{ds4}] \approx r_{ds2}g_{m4}r_{ds4}$
- $R_{in}: = \frac{1}{g_{m3}} \| r_{ds3} + \frac{1}{g_{m1}} \| r_{ds1} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \approx \frac{2}{g_m}$
- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$
- $V_{MIN}(\text{in}) = 2(V_T + V_{ON})$
- Current gain match: Excellent since  $v_{DS1} = v_{DS2}$

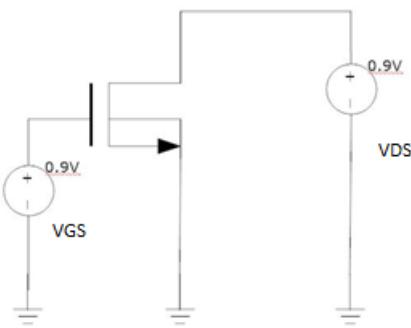
### Low voltage cascode current mirror (High swing cascode current mirror):

In most applications, it is desirable to make (W/L) of Transistor M0 in Fig1(c), smaller so that M1 and M2 can be biased with a slightly larger Vds. This would help counter the body effect of M3 and M4, which have their Vt increased. To save power consumption, Ibias and M0 size can be scaled down a little bit while keeping the same gate voltage. Also, it may be wise to make the length of M1 and M2 larger than the minimum and that of M3 and M4 even larger since M4 often sees a larger voltage Vout. This helps reduce short channel effects.

- $R_{out} \approx g_{m2}r_{ds2}r_{ds1}$
- $R_{in} = ?$   $v_{in} = r_{ds5}(i_{in} - g_{m5}v_{gs5}) + v_{ss} = r_{ds5}(i_{in} + g_{m5}v_{ss}) + v_{ss} = r_{ds5}i_{in} + (1 + g_{m5}r_{ds5})v_{ss}$   
But,  $v_{ss} = r_{ds3}(i_{in} - g_{m3}v_{in})$   

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds5} + r_{ds3} + r_{ds3}g_{m5}r_{ds5}}{g_{m3}r_{ds3}(1 + g_{m5}r_{ds5})} \uparrow \frac{1}{g_{m3}}$$
- $V_{MIN}(\text{out}) = 2V_{ON}$
- $V_{MIN}(\text{in}) = V_T + V_{ON}$
- Current gain is excellent because  $v_{DS1} = v_{DS3}$ .

## EXPERIMENTAL PROCEDURE



**Fig 2: MOSFET**

### MOSFET Characteristics:

1. Draw the circuit as shown in Fig 2 with length of NMOS as L (variable) and width 10um. Select Vdc voltage ( $v1= V_{GS}(0.9V)$   $V_{DS}(0.9V)$ ) at the input of gate and drain terminal of the NMOS respectively.
2. From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.
3. In the Analog Environment window select "Variables → Copy from Cell view". And give the values of L as 1um.
4. Then in the window select “Analyses → Choose”. Select “dc” and then “Component Parameter”. Choose “Select Component” and select  $V_{DS}$  then set start and stop voltages as 0 and 1.8 to get graph of  $I_D$  vs  $V_{DS}$ .
5. Then select “Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic” to set the y-axis. Then run the Parametric Analysis with L varying it from 180nm to 1um in Auto mode with number of steps 3. Then run the simulation to see the results.
6.  $I_D - V_{DS}$  characteristics is obtained for three different values of L. The Id variation which is dy value is observed for the three lengths by choosing A as 0.5V and B as 1.8V and make observations where A and B are two points on graph.
7. Press A and B keys to select two points on the graph and to measure the slope between the two points. In  $I_D - V_{DS}$  plot the points are chosen to be 850mv to 950mv. The slope gives the value of  $gm$ . Calculate inverse to get value of  $r_o$  and make observations.

### Basic Current mirror, Cascode current mirror, Low voltage cascode current mirror (High swing cascode current mirror):

1. Draw the circuit as shown in Fig 1(a) with length of NMOS M1 and M2 as 1um and width 10um. Select Vdc voltage ( $v1=1V$ ,  $Vdd = 1.8V$ ) initially at the input of drain terminal of the NMOS M2 respectively. And  $I_{in}$  as current source  $I_{DC}$  with value 100uA.
2. From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated

graphs. Initially select Save DC operating point only and run the analysis to find the value of VGS.

3. Select Vdc voltage ( $v1=V_{GS}Value$ ) at the input of drain terminal of the NMOS M2 respectively. Then in the ADE L window select “Analyses → Choose”. Select “dc” and then “Component Parameter”. Choose “Select Component” and select  $V_{DS}$  then set start and stop voltages as 0 and 1.8 to get graph of  $I_D$  vs  $V_{DS}$ .

4. Then select “Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic” to set the y-axis. Then run the simulation to see the results.

5.  $I_D - V_{DS}$  characteristics is obtained, measure the value of  $I_{OUT}Current$  at  $V_{GS}$ voltage and  $I_D$  variation which is dy value and  $V$  variation which is dx is observed by choosing A as  $V_{GS}$  voltage and B as 1.8V and make observations where A and B are two points on graph.

6. Perform a Region Plot by using “Outputs → Setup → New Expression → Open. Select opt option and select M2 transistor with region option. Now Perform Parametric Analysis with  $V_{DS}$  from 0 to 1.8V in Linear mode with step size 0.1. Find the minimum value needed to make M2 transistor be in saturation mode. Perform steps as in 3,4,5 with Vdc value as min Vout obtained now and make the observations.

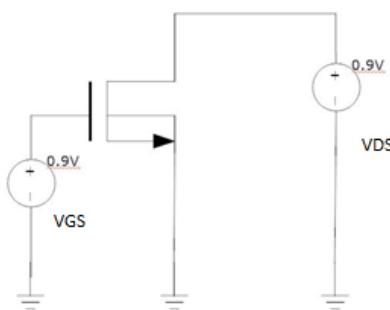
7. Follow the same steps as followed for the Basic Current Mirror. In cascode we Initially find min Vout value where both transistors are in Saturation. Use this as  $V_{DS}$  and perform the DC analysis. Similarly for Low voltage Cascode Current Mirror.

8. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS". This gives the values of all parameters of NMOS which can be used to compare with the graphically obtained values.

9. Draw the circuits shown in fig 1(a),1(b),1(c) and perform the ac analysis with  $V_{sin}$  voltage with name Vout (DC voltage 900mV and Ac magnitude 1V). Then perform the ac analysis with frequency and range 1 to 100M Hz.

10. Plot the inverse of the graph using "Tools → Calculator" which gives the value of small signal output resistance of MOSFETs in different configurations. Verify the results "Results → Print → DC operating point and select NMOS". This gives the values of all parameters of NMOS. The same is performed for all circuits.

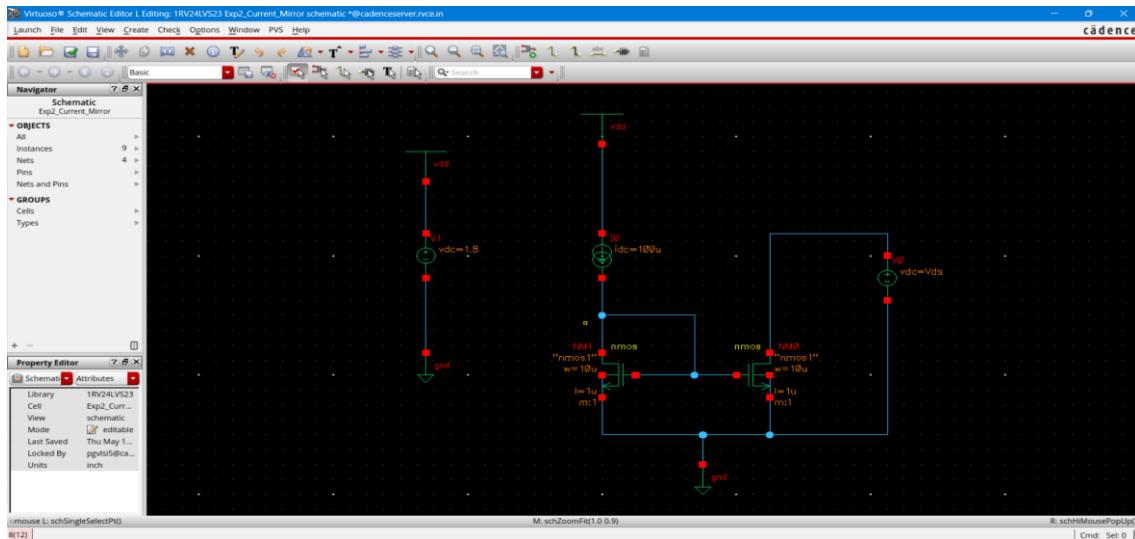
## DESIGN & ANALYSIS



**Fig 3: MOSFET Analysis**

The Parametric Analysis plot of  $I_D - V_{DS}$  of a MOSFET shown in Fig 3 is performed for different values of Length L of the NMOS to observe the effect of Channel length

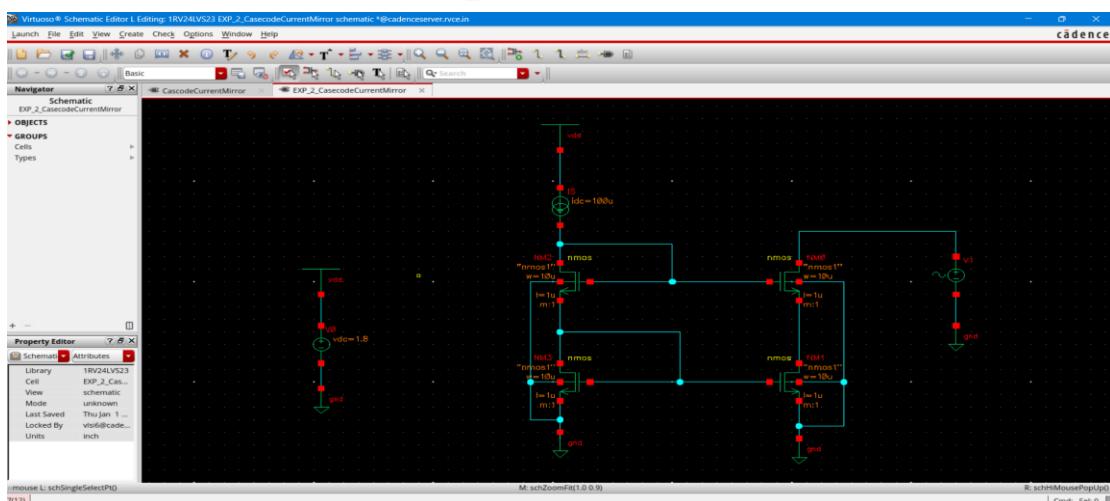
modulation at  $V_{DS}$  as 0.9V and W width of NMOS as 10um. Three plots for the values of L 180nm, 590nm and 1 um are obtained. The Id variation which is dy value is observed for the three lengths by choosing A as 0.5V and B as 1.8V points. The value of  $r_o$  is also calculated for the three different plots choosing A as 850mV and B as 950mV and finding inverse of slope.



**Fig 4: Basic MOSFET Current Mirror Analysis**

The basic current mirror can also be implemented using MOSFET transistors. Transistor M<sub>1</sub> is operating in the saturation or active mode, and same for M<sub>2</sub> transistor in Basic Current mirror in figure 4. The output current I<sub>OUT</sub> is directly related to I<sub>REF</sub>(I<sub>in</sub>). In the case of transistor M<sub>1</sub> of the mirror, I<sub>D</sub> = I<sub>in</sub>. Reference current I<sub>in</sub> (I<sub>REF</sub>) is a known current. Using V<sub>DG</sub> = 0 for transistor M<sub>1</sub>, the drain current in M<sub>1</sub> is I<sub>D</sub> = f(V<sub>GS</sub>, V<sub>DG</sub>=0), so we find: f(V<sub>GS</sub>, 0) = I<sub>in</sub> (I<sub>REF</sub>), implicitly determining the value of V<sub>GS</sub>. Thus I<sub>in</sub> (I<sub>REF</sub>) sets the value of V<sub>GS</sub>. The basic current mirror circuit in the fig 1 forces the same V<sub>GS</sub> to be applied to transistor M<sub>2</sub>. If M<sub>2</sub> is also biased with zero V<sub>DG</sub> and provided transistors M<sub>1</sub> and M<sub>2</sub> have good matching of their properties, such as channel length, width, threshold voltage, etc., the relationship I<sub>OUT</sub> = f(V<sub>GS</sub>, V<sub>DG</sub> = 0) applies, thus setting I<sub>OUT</sub> = I<sub>in</sub> (I<sub>REF</sub>).

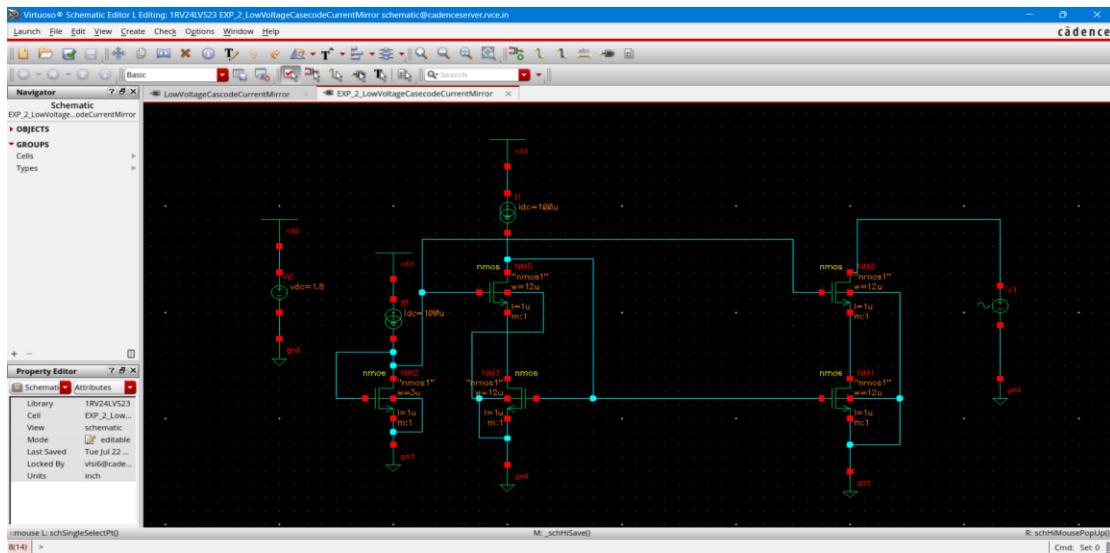
- Minimum output voltage is  $V_{MIN(out)} = V_{ON}$
- Output resistance is  $R_{out} = \frac{1}{\lambda D}$



**Fig 5: Cascode Current Mirror Analysis**

A MOSFET current mirror based on cascode connection is shown in Fig 5. The MOSFETs M2 and M1 form a simple current mirror. M4 acts as the common gate part of the cascode and transfers the drain current of M3 to the output presenting a high output resistance. M3 acts as a diode level shifter and assures that M4 and M2 always remain in saturation. For MOS cascode as dc current gain  $\beta_0 \rightarrow \infty$ , the number of stacked cascode devices can be increased. This will be limited by the MOS substrate leakage current that creates a resistive shunt dominating output resistance for  $V_{OUT} > V_{OUT\min}$ , thus setting  $I_{OUT} = I_{in} (I_{REF})$ .

- $R_{out}: v_{out} = i_{out}[r_{ds4} + r_{ds2} + g_{m4}r_{ds2}r_{ds4}] \approx r_{ds2}g_{m4}r_{ds4}$
- $V_{MIN(\text{out})} = V_T + 2V_{ON}$
- $V_{MIN(\text{in})} = 2(V_T + V_{ON})$



**Fig 6: Low voltage cascode current mirror (High swing cascode current mirror)**

In most applications, it is desirable to make (W/L) of Transistor M0 in Fig 6, smaller so that M1 and M2 can be biased with a slightly larger Vds. This would help counter the body effect of M3 and M4, which have their Vt increased. To save power consumption, Ibias and M0 size can be scaled down a little bit while keeping the same gate voltage. Also, it may be wise to make the length of M1 and M2 larger than the minimum and that of M3 and M4 even larger since M4 often sees a larger voltage Vout. This helps reduce short channel effects.

- $V_{MIN(\text{out})} = 2V_{ON}$
- $R_{out} \approx g_{m2}r_{ds2}r_{ds1}$
- $V_{MIN(\text{in})} = V_T + V_{ON}$

## RESULTS

	Practical values
<b>Simple Current Mirror</b>	
$I_{out}$	<b>99.9966u</b>
$V_{out,min}$	<b>300mV</b>
$R_{out}$	<b>301.753K</b>
<b>Cascode current mirror</b>	

$I_{out}$	<b>99.5016u</b>
$V_{out,min}$	<b>1V</b>
$R_{out}$	<b>847.728K</b>
<b>High Swing cascode current mirror</b>	
$I_{out}$	<b>100.026u</b>
$V_{out,min}$	<b>500mV</b>
$R_{out}$	<b>3.523M</b>

## DISCUSSIONS

The Parametric Analysis plot of  $I_D - V_{DS}$  of a MOSFET shown in Fig 3 is performed for different values of Length L of the NMOS to observe the effect of Channel length modulation at  $V_{DS}$  as 0.9V and W width of NMOS as 10um. Three plots for the values of L 180nm, 590nm and 1 um are obtained. In the fig 7 the red plot for 180nm, yellow for 590nm and green for 1um. The  $I_D$  variation which is  $dY$  value is observed for the three lengths by choosing A as 0.5V and B as 1.8V points. The  $I_D$  variation decreases with increase in L value as shown in table below.

MOSFET (Fig 3)	
L(value)	$dY = I_D$ variation
180 nm	220.98u
590 nm	24.94u
1 um	11.886u

The Parametric Analysis plot of  $I_D - V_{DS}$  of a MOSFET shown in Fig 3 is performed for different values of Length L of the NMOS to observe the effect of Channel length modulation at  $V_{DS}$  as 0.9V and W width of NMOS as 10um. Three plots for the values of L 180nm, 590nm and 1 um are obtained. In the figure 8 red plot for 180nm, yellow for 590nm and green for 1um. The  $R_o$  value which is inverse value of slope is observed for the three lengths by choosing A as 850 mV and B as 950 mV points. The  $R_o$  value increases with increase in L value as shown in table below.

MOSFET (Fig 3)	
L(value)	$R_o$
180 nm	5.833K
590 nm	52.12K
1 um	109.373K

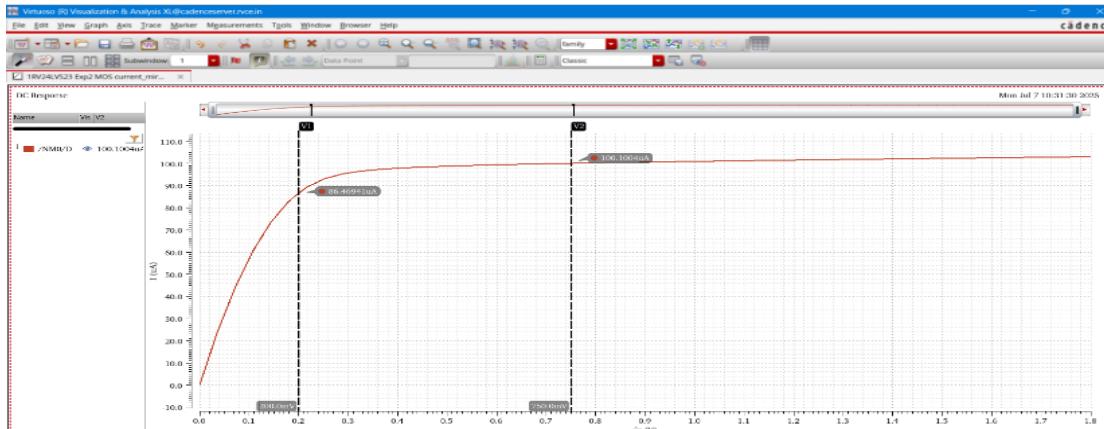
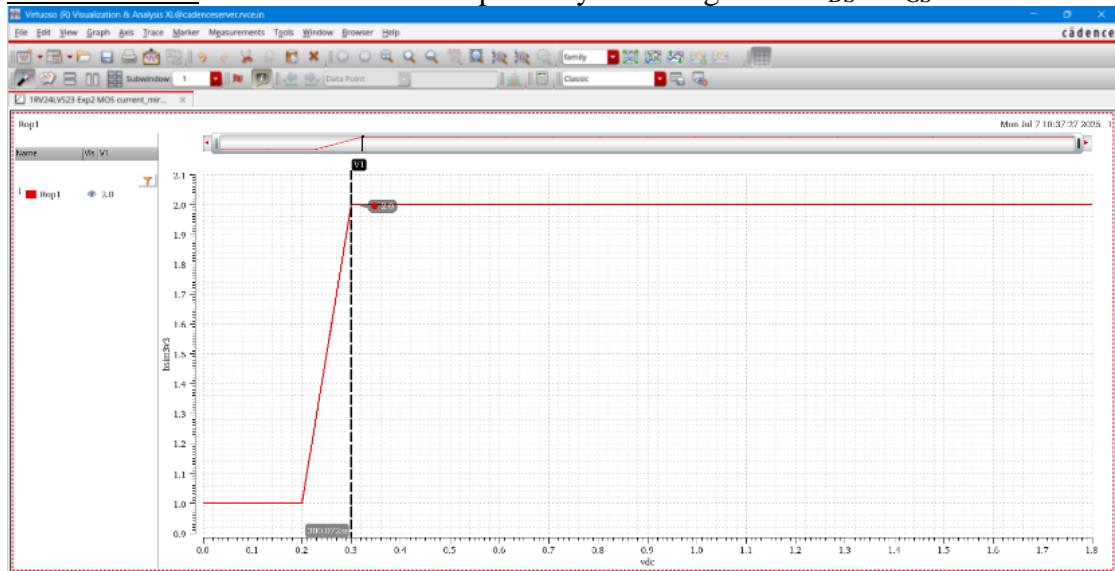


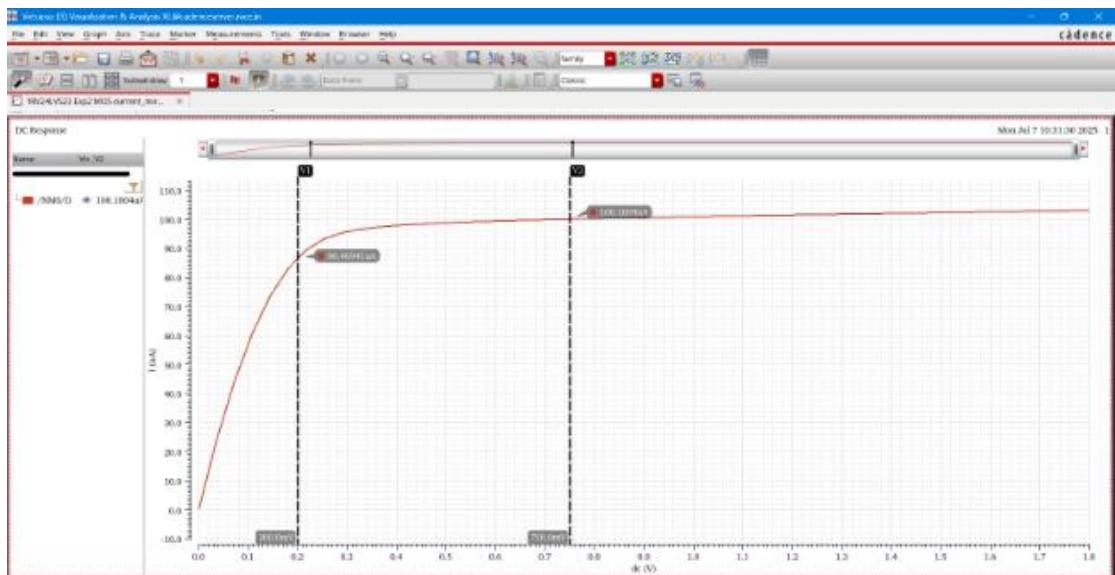
Fig:9  $I_D - V_{DS}$  characteristics for Basic Current Mirror Circuit (730.86 mV)

The figure 9 shows the  $I_D$  -  $V_{DS}$  characteristics for basic current mirror circuit with  $V_{out}$  value of 724.756 mV. This  $V_{out}$  value is obtained by performing DC analysis with only save DC operating point. This is the value of  $V_{GS}$  which is applied to  $V_{DS}$  so that we get an equal current at output  $I_{out} = I_{in}$ . The  $I_{in}$  current is 100 uA and  $I_{out}$  current is 99.9966uA. Hence the current is perfectly matching when  $V_{DS} = V_{GS}$ .



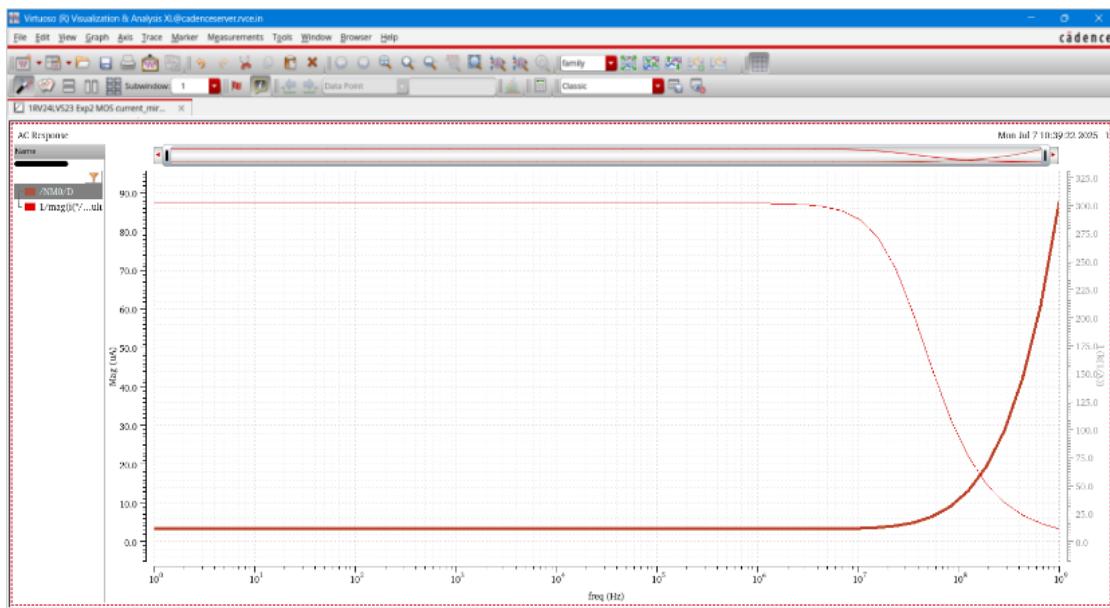
**Fig:10 Region vs  $V_{DS}$  characteristics for Basic Current Mirror Circuit**

We perform a Region Plot by using “Outputs → Setup ” option and selecting opt option and M2 transistor with region option. Now when we perform parametric analysis with  $V_{DS}$  from 0 to 1.8V in Linear mode with step size 0.1 we find the minimum value needed to make M2 transistor be in saturation mode. From the figure 10 the minimum  $V_{out}$  is 300 mV. This voltage is sufficient for M2 to be in saturation.



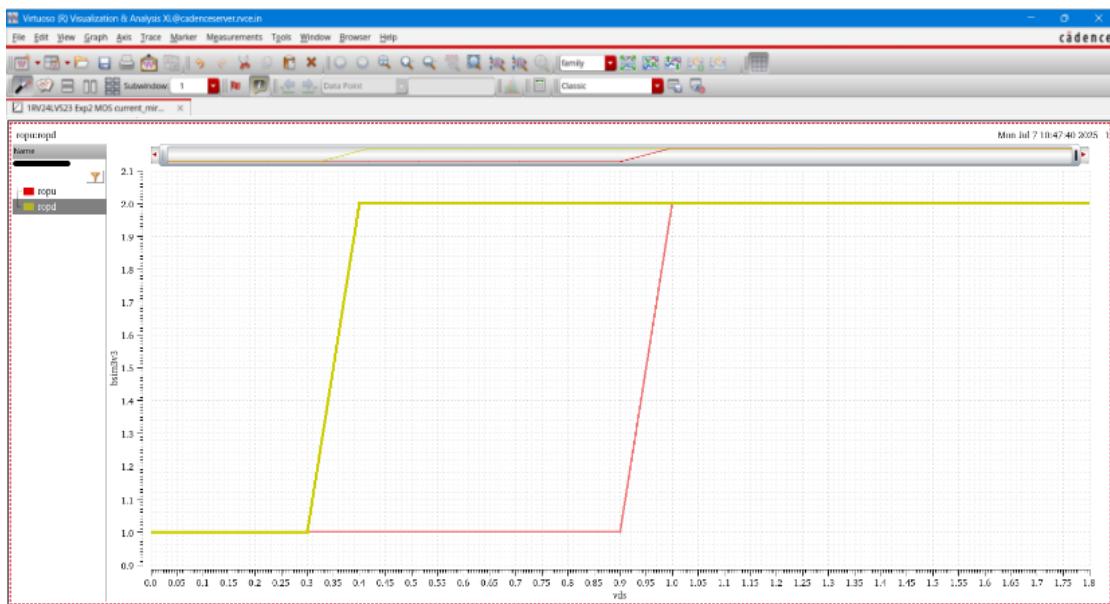
**Fig:11  $I_D$  -  $V_{DS}$  characteristics for Basic Current Mirror Circuit (200 mV)**

The figure 11 shows the  $I_D$  -  $V_{DS}$  characteristics for basic current mirror circuit with  $V_{out}$  value of 300 mV. This  $V_{out}$  value is obtained by performing Region plot with region vs  $V_{DS}$  plot. This is the min value of  $V_{out}$  at which the transistor M2 will be in saturation region. We get an approximate current at output  $I_{out}$ . The  $I_{in}$  current is 100 uA and  $I_{out}$  current is 99.9966uA. Hence the current is not equal to  $I_{in}$ .



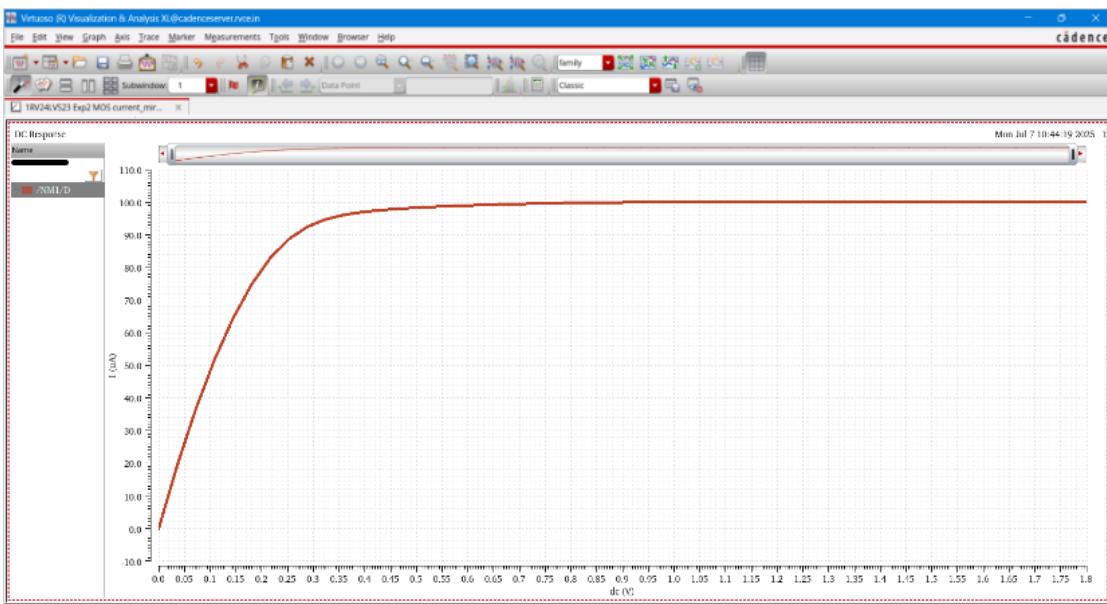
**Fig:12 AC response for Basic Current Mirror Circuit**

The AC response is the plot of Id current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit. The Rout resistance value is 301.753K ohm (1/A) for the Basic Current Mirror Circuit as shown in fig 12.



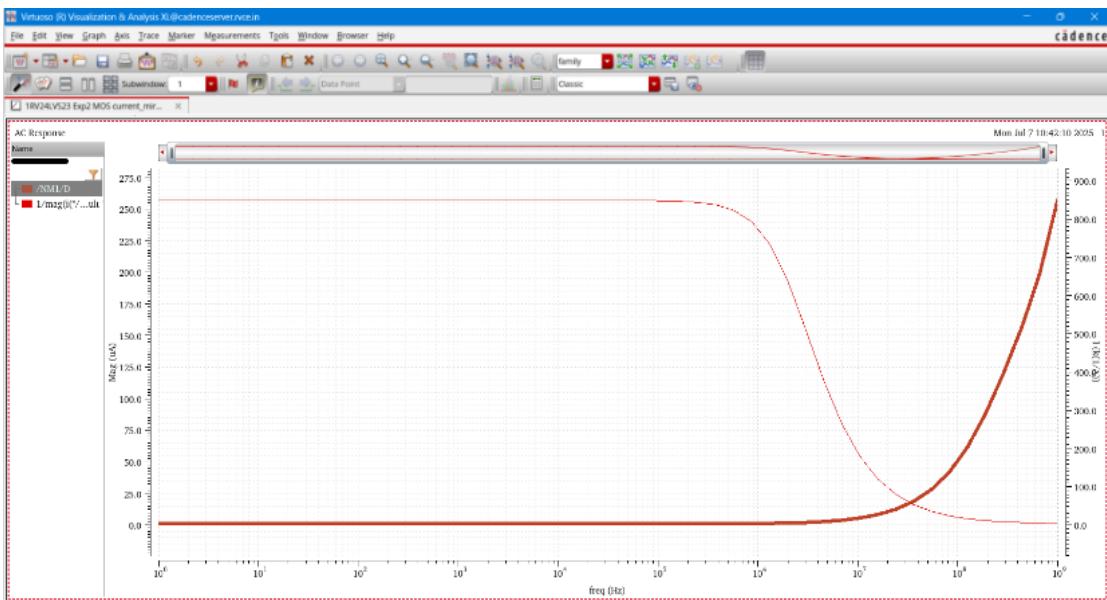
**Fig:13 Region vs V<sub>Ds</sub> characteristics for Cascode Current Mirror Circuit**

We perform a Region Plot by using “Outputs → Setup ” option and selecting opt option and M2 and M4 transistors with region option. Now when we perform parametric analysis with V<sub>Ds</sub> from 0 to 1.8V in Linear mode with step size 0.1 we find the minimum value needed to make M2 and M4 transistors both to be in saturation mode. From the figure 13 the minimum Vout is 1 V. This voltage is sufficient for both M2 and M4 to be in saturation.



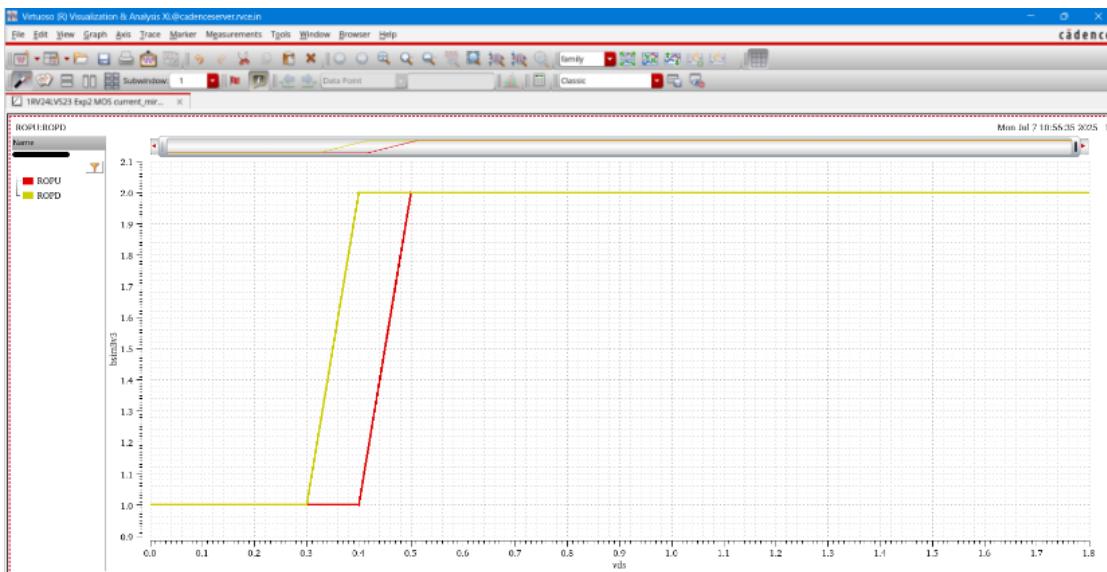
**Fig:14 Id - V<sub>DS</sub> characteristics for Cascode Current Mirror Circuit**

The figure 14 shows the  $I_D$  -  $V_{DS}$  characteristics for cascode current mirror circuit with  $V_{out}$  value of 1 V. This  $V_{out}$  value is obtained by performing Region plot with region vs  $V_{DS}$  plot. This is the min value of  $V_{out}$  at which the transistor M2 and M4 both will be in saturation region. We get an approximate current at output  $I_{out}$ . The  $I_{in}$  current is 100 uA and  $I_{out}$  current is 99.5016uA. Hence the current is almost equal to  $I_{in}$ .



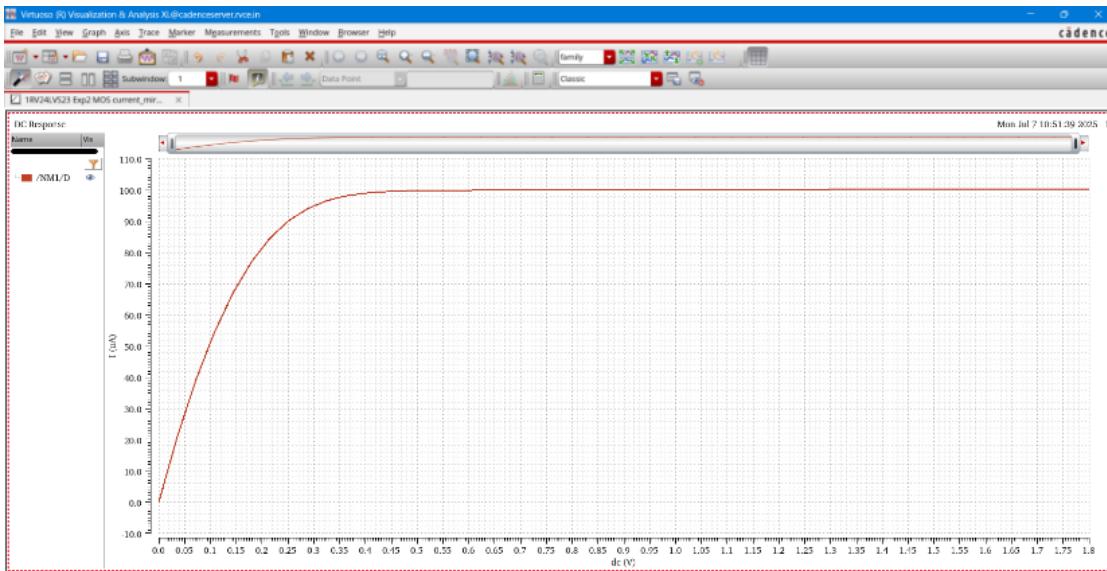
**Fig:15 AC response for Cascode Current Mirror Circuit**

The AC response is the plot of  $I_d$  current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit. The  $R_{out}$  resistance value is 847.728K ohm (1/A) for the Cascode Current Mirror Circuit as shown in figure 15.



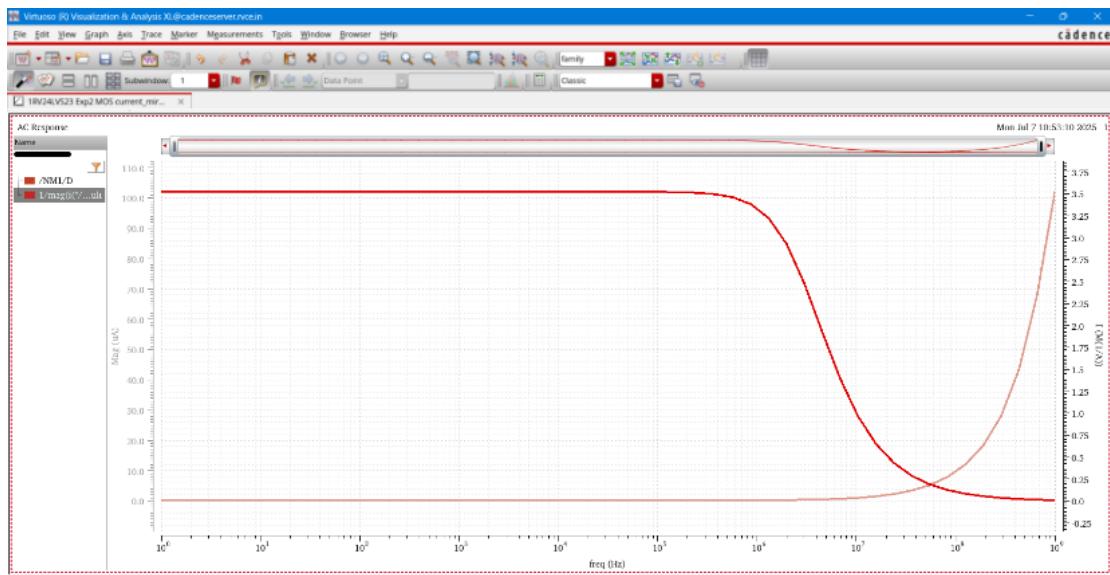
**Fig:16 Region vs V<sub>DS</sub> characteristics for Low voltage cascode Current Mirror Circuit**

We perform a Region Plot by using “Outputs → Setup ” option and selecting opt option and M2 and M4 transistors with region option. Now when we perform parametric analysis with V<sub>DS</sub> from 0 to 1.8V in Linear mode with step size 0.1 we find the minimum value needed to make M2 and M4 transistors both to be in saturation mode. From the fig 16 the minimum V<sub>out</sub> is 500mV. This voltage is sufficient for both M2 and M4 to be in saturation.



**Fig:17 I<sub>D</sub> - V<sub>DS</sub> characteristics for Low voltage cascode Current Mirror Circuit**

The figure 17 shows the I<sub>D</sub> - V<sub>DS</sub> characteristics for cascode current mirror circuit with V<sub>out</sub> value of 600m V. This V<sub>out</sub> value is obtained by performing Region plot with region vs V<sub>DS</sub>plot. This is the min value of V<sub>out</sub> at which the transistor M2 and M4 both will be in saturation region. We get an approximate current at output I<sub>out</sub>. The I<sub>in</sub> current is 100 uA and I<sub>out</sub> current is 100.26uA. Hence the current is almost equal to I<sub>in</sub>.



**Fig:18 AC response for Low voltage cascode Current Mirror Circuit**

The AC response is the plot of  $I_d$  current vs frequency and the frequency range is given from 1-100MHz. The inverted waveform is obtained using tools-calculator option which gives the output resistance of the circuit. The  $R_{out}$  resistance value is 3.523M ohm ( $1/A$ ) for the Cascode Current Mirror Circuit as shown in figure 18.

## INFERENCE

The MOS current mirrors were implemented using different topologies—basic, cascode, and high-swing cascode—with the NMOS devices sized at a width of  $10\ \mu m$  and varied channel lengths from  $180\ nm$  to  $1\ \mu m$ . DC analysis was performed to obtain  $I_D$  vs  $V_{DS}$  characteristics and to evaluate the effect of channel length modulation. It was observed that increasing the channel length reduced the variation in drain current and improved output resistance, confirming that longer channel devices suffer less from channel length modulation.

The small signal output resistance ( $r_o$ ) was extracted from the slope of the  $I_D$ - $V_{DS}$  graph and compared across different lengths, showing that  $r_o$  increased from  $5.833\ k\Omega$  ( $180\ nm$ ) to  $109.373\ k\Omega$  ( $1\ \mu m$ ), validating the theoretical behaviour.

Further, the current mirror circuits were analysed for their output resistance and current matching. The basic current mirror showed an output resistance of  $301.753\ k\Omega$  and nearly perfect current mirroring with  $I_{OUT} \approx I_{REF}$ . The cascode configuration improved the output resistance to  $847.728\ k\Omega$ , while the high-swing cascode provided the best result with  $3.523\ M\Omega$ , demonstrating the advantage of cascode structures in enhancing analog performance.

AC analysis confirmed these findings by plotting the inverted current vs frequency response. The experiment clearly demonstrated the impact of channel length on device performance and showed how cascode and high-swing designs provide better output resistance and improved current matching, making them more suitable for precision analog circuits.

## EXPERIMENT 3

### DESIGN & ANALYSIS OF CS AMPLIFIER CIRCUITS

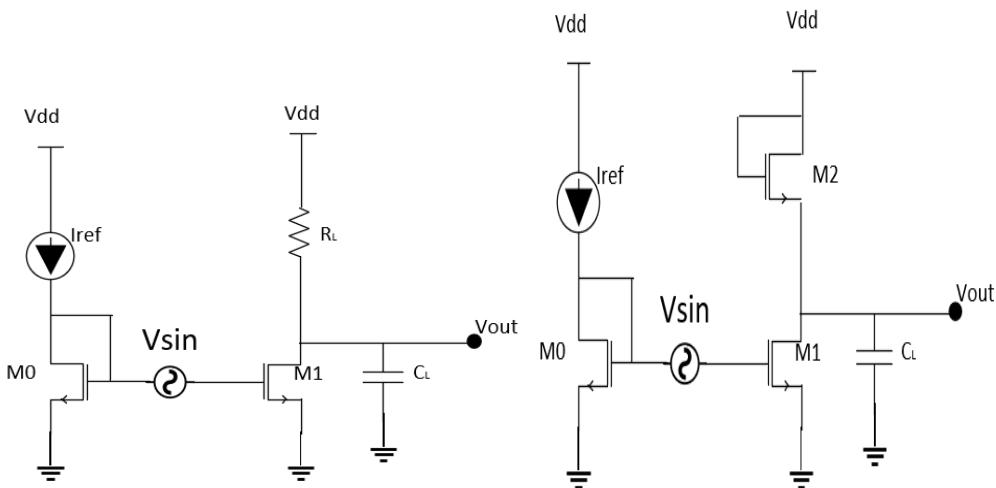
#### OBJECTIVES:

- i. To design and analyze a Common Source Amplifier for the given specifications.
- ii. To perform dc analysis and obtain the dc operating points, small signal parameters and node voltages.
- iii. To perform ac analysis and obtain dc gain, 3dB frequency and unity gain frequency.
- iv. Estimate gain and output impedance and output swing.

#### SPECIFICATIONS

Parameters	Specified Values
Supply Voltage	1.8 V
DC gain	-5
$f_3$ dB	100MHz
Load Capacitance	5pF

#### CIRCUIT DIAGRAM



**Fig: 1(a) Common Source amplifier1(b) CS Amplifier with NMOS diode resistive load**

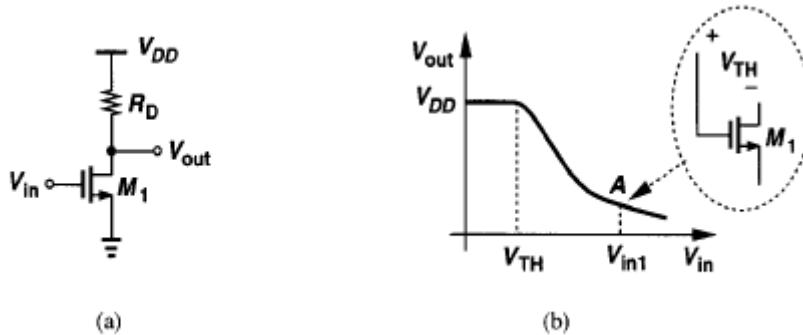
#### THEORY

The common source is the most commonly used MOSFET amplifier. The name “common source” comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and source terminals. Three terminal

devices can be used to implement a controlled source. This property makes them suitable to be used in amplifiers. The working principle of a MOSFET amplifier is controlling the current flowing through drain terminal by setting the gate-to-source voltage. This property can be achieved by operating the MOSFET in the saturation (active) region. In this circuit the MOSFET converts variations in the gate-source voltage into a small signal drain current which passes through a resistive load and generates the amplified voltage across the load resistor.

The voltage gain of CS amplifier depends upon the transconductance  $g_m$ , the linear resistor  $r_o$  and load. In order to increase the gain we have to increase the  $g_m$ .

If the input voltage increases from zero the transistor is off and the output is  $V_{DD}$ . As  $V_{in}$  approaches  $V_{TH}$   $M_1$  begins to turn ON drawing from  $R_D$  lowering the  $V_{out}$ .



**Figure: 2 Common source stage and its characteristics**

## EXPERIMENTAL PROCEDURE

### Common Source amplifier: -

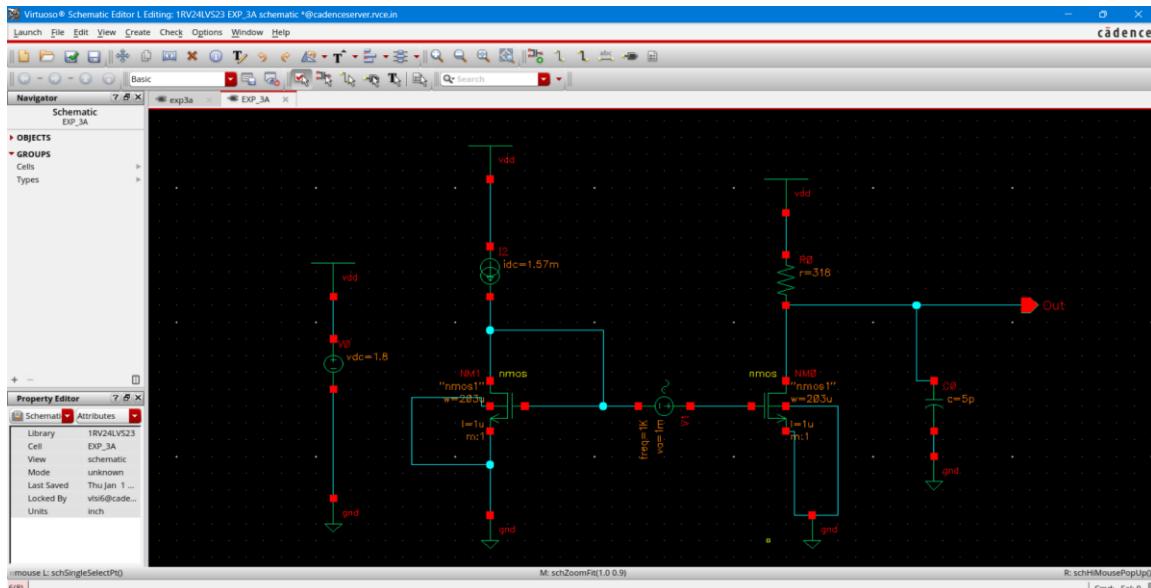
- Current mirror circuit can be used to bias the input mosfet transistor of the amplifier circuit.
- The resistance, current and the width to length ratio of the transistor can be calculated with the below formulae given in the design and analysis section.
- With the obtained values of  $R$ ,  $I_{ref}$ ,  $W/L$  ratio, the circuit in Figure 1(a) is constructed.
- Dummy dc analysis is run by saving the dc operating point without the source in between the current mirror and the CS amplifier. The operating points and the small signal parameters are noted from the operating point table. (Results → Print → Save DC operating points).
- Connect an AC source in between with the ac magnitude = 1, Frequency = 1KHz and amplitude = 5mV. Run AC analysis for frequencies ranging from 1 to 100GHz. The AC response is obtained with frequency on the x-axis and the  $v_{out}$  on the y-axis.
- Convert the graph into dB scale. Right click on the waveform → dependent modifier → dB20. Now the y-axis is converted to decibel scale with each value in dB ( $20 \log(v_{out})$ ). Note down the values of the gain, 3dB frequency and the unity gain frequency.

- Perform transient analysis with stop time as 50m. select the input and output wires. The output voltage swing is determined by calculating the  $V_o(p-p)$  value and also the  $V_{in}(p-p)$  value.

### CS Amplifier with NMOS diode connected load: -

1. Draw the circuit as shown in Fig 1(b) and the length of NMOS set as 1um and width 230um for M0 and M1 NMOS transistor. Then with capacitor  $C_L$  value as 5pF,  $V_{DD}$  as 1.8V and using the value of  $f_{3dB}$  and  $C_L$  the resistance  $R_{out}$  value is found to be 318.80 ohm. Then using design equations the value of W for the diode connected NMOS load is found to be 9.24 um. The current source  $I_{ref}$  value is set as 1.57 mA after analysis.
2. In the DC analysis since the transistors are not in saturation region, the width of M2 is set as w and a region – width plot is obtained using parametric analysis. The value of W of M2 to keep M2 in saturation is obtained from the graph and is found to be 11um. The width of M2 is changed in the circuit.
3. The same steps as mentioned above are followed for obtaining the dc operating points, small signal parameters, 3dB frequency and unit gain frequency.

## DESIGN & ANALYSIS



**Fig 3: Common Source amplifier**

The common source is the most commonly used MOSFET amplifier. The name 'common source' comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and source terminals. The working principle of a MOSFET amplifier is controlling the current flowing through drain terminal by setting the gate-to-source voltage. This property can be achieved by operating the MOSFET in the saturation (active) region. The design equations used in the design and analysis are as follows: -

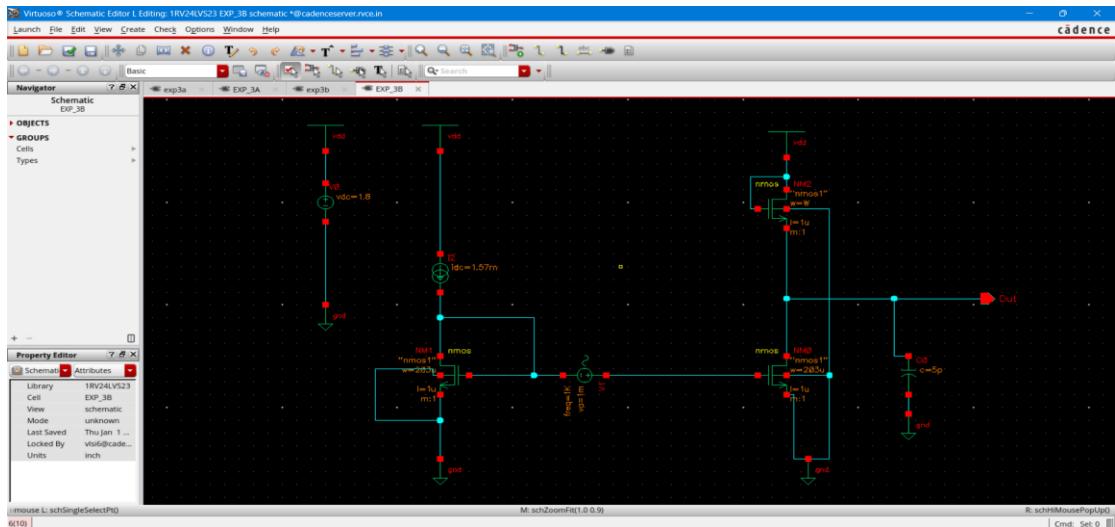
$$f_{3dB} = \frac{1}{2\pi R_L C_L}$$

$$A_V = -g_m R_L$$

$$I_D = \frac{g_m V_{OV}}{2}$$

$$g_m = \sqrt{2I_D \mu_n C_{ox} \frac{W}{L}}$$

Initially using  $f_{3dB}$  and  $C_L$  from the specification the value of  $R_L$  is found to be 318.30 ohm. Then from given gain -5 and  $R_L$  the  $g_m$  is found to be 15.7 m A/V,  $V_{ov}$  value is determined and current  $I_D$  is calculated as 1.57mA. The  $\beta_{eff}$  value is obtained from the print table and the value of  $\mu nC_{ox}$  is calculated and found to be 386.92. With the help of  $\mu nC_{ox}$  and  $gm$  equation the value of  $W/L$  is obtained and found to be 202.88u/1um. Finally the required  $W/L$  ratio is found to be 203 um and L be 1um.



**Figure 4:CS Amplifier with NMOS diode connected load**

In the CS Amplifier with NMOS diode connected load the gain is independent of bias currents and voltages. As the input and output signal levels vary, the gain remains relatively constant, indicating that the input- output characteristics is relatively linear.

$$\begin{aligned} A_v &= -g_{m1} \frac{1}{g_{m2} + g_{mb2}} \\ &= -\frac{g_{m1}}{g_{m2}} \frac{1}{1 + \eta}, \quad A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1 + \eta}. \end{aligned}$$

The above gain equations are used in finding the  $W/L$  ratio of NMOS diode connected load transistor, and the value is found to be 9.24 theoretical.

## RESULTS

(i) Operating points for Common Source amplifier:

Transistor	$V_s(V)$	$V_d(V)$	$V_g(V)$	$V_b(V)$
M1	0	1.28953	655.503m	0

The small signal parameters are as follows:

Transistor	$I_d(A)$	$g_m(A/V)$	$g_{ds}(A/V)$	$r_o(K \text{ ohm})$	Self-gain ( $g_m r_o$ )
M1	1.650596m	14.462m	48.4256u	20.650	298.6403

(ii) Operating points for CS Amplifier with NMOS diode connected load:

Transistor	V <sub>s</sub> (V)	V <sub>d</sub> (V)	V <sub>g</sub> (V)	V <sub>b</sub> (V)
M1	0	237.395m	655.447m	0
M2	1.8	323.7395m	1.8	0

The small signal parameters are as follows:

Transistor	I <sub>d</sub> (A)	g <sub>m</sub> (A/V)	g <sub>ds</sub> (A/V)	r <sub>o</sub> (ohm)	Self-gain (g <sub>m</sub> r <sub>o</sub> )
M1	1.52455m	13.6501m	320.638u	3.11878K	42.1066
M2	1.52458m	2.00856m	104.158u	9.6K	19.2835

## DISCUSSIONS

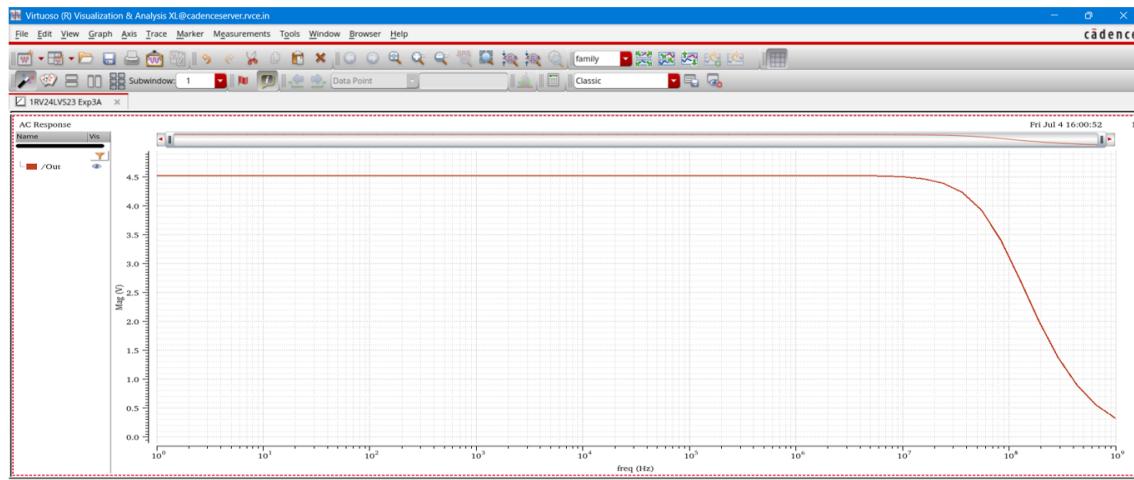


Figure: 5 AC response of CS amplifier with resistive load

The AC analysis is a plot of Vout to frequency. The plot is converted into a dB plot. The frequency range is set from 1-100GHz. AC Analysis is performed to observe the values of gain, 3 dB frequency and unity gain frequency. The gain is 13.1197 \_\_\_\_\_ dB and 3dB frequency \_\_\_\_\_ 95.3919 \_\_\_\_\_ MHz and Unity Gain Frequency is \_\_\_\_\_ 397.494 \_\_\_\_\_ MHz.

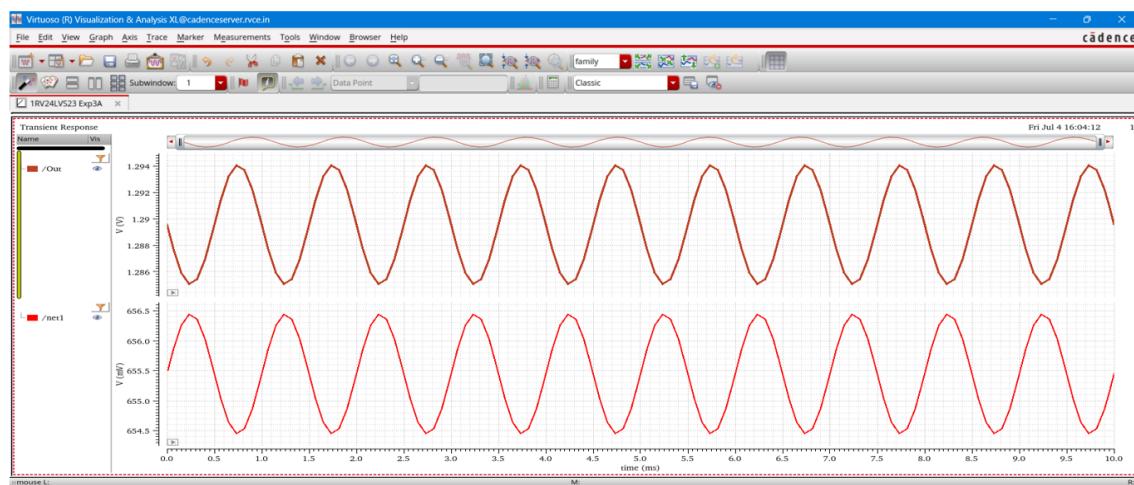
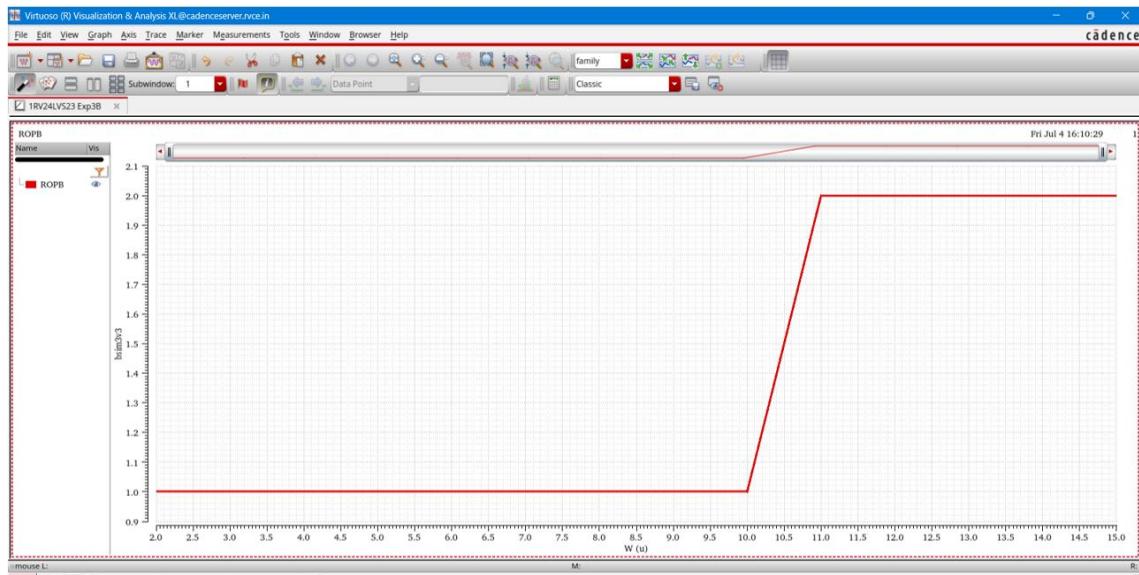


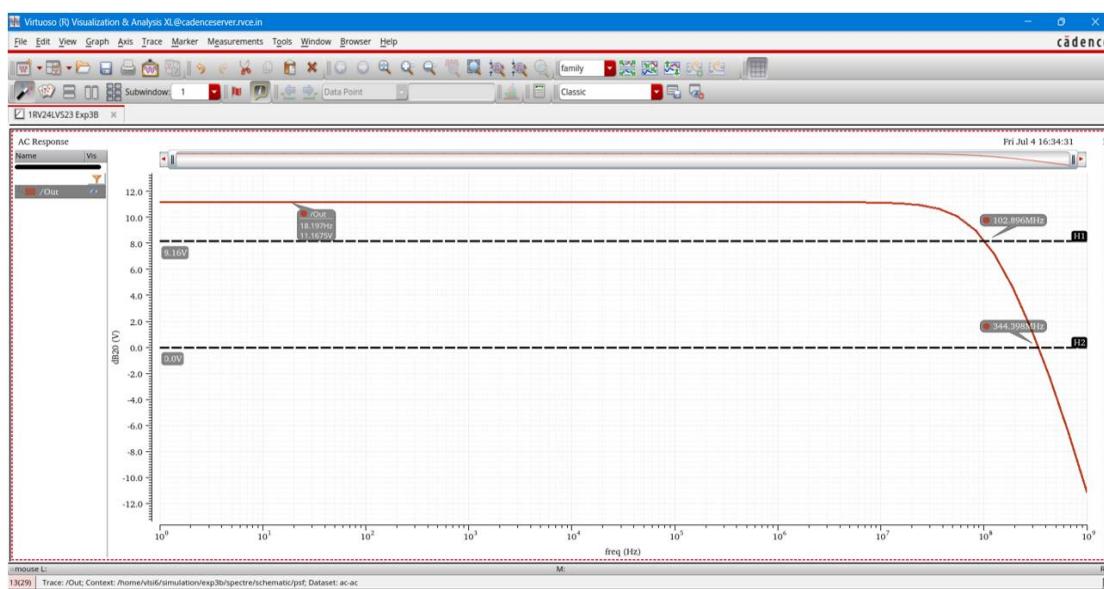
Figure: 6 Transient analysis of CS amplifier with resistive load

The transient analysis provides plot of output and input voltage of the input transistor M1 in the CS amplifier with resistive load.  $V_o(p-p)$  and  $V_{in}(p-p)$  of both the input and output waveforms are calculated using the help of tools calculator.  $V_o(p-p) = \underline{9.006}$  mV and  $V_{in}(p-p) = \underline{1.989}$  m.  $V_o(p-p)/V_{in}(p-p)$  provides the gain =  $\underline{13.14}$  dB.

### CS amplifier with diode connected NMOS load

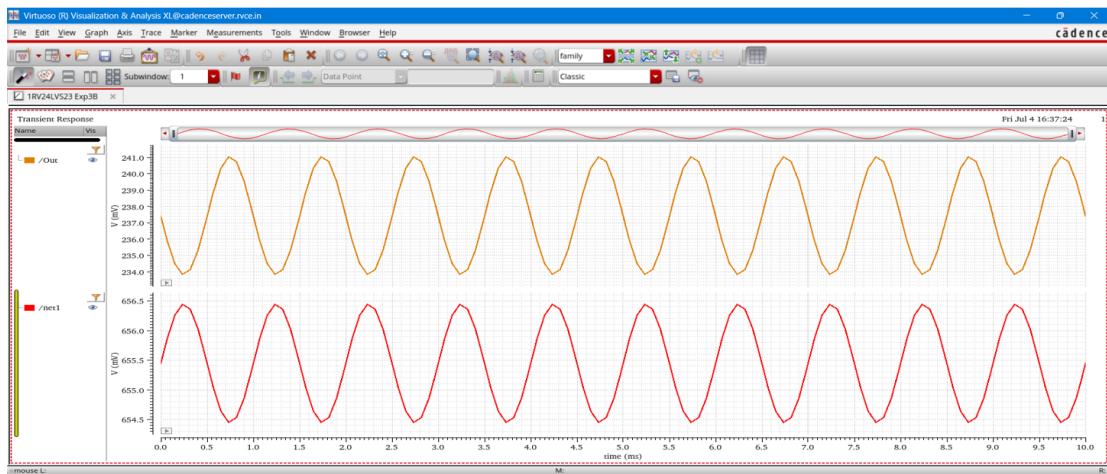


**Figure: 7 Plot of Width vs Region for CS amplifier with NMOS diode connected load**



**Figure: 8 AC response of CS amplifier with NMOS diode connected load**

The AC analysis is a plot of  $V_{out}$  to frequency. The plot is converted into a dB plot. The frequency range is set from 1-10GHz. AC Analysis is performed to observe the values of gain, 3 dB frequency and unity gain frequency. The gain is  $\underline{11.1675}$  dB and 3dB frequency is  $\underline{102.719}$  MHz and Unity Gain Frequency is  $\underline{344.398}$  MHz.



**Figure: 9 Transient analysis of CS amplifier with NMOS diode connected load**

The transient analysis provides plot of output and input voltage of the input transistor M1 in the CS amplifier with resistive load.  $V_o(p-p)$  and  $V_{in}(p-p)$  of both the input and output waveforms are calculated using the help of tools calculator.  $V_o(p-p) = 7.201 \text{ mV}$  and  $V_{in}(p-p) = 1.989 \text{ mV}$ .  $V_o(p-p)/V_{in}(p-p)$  provides the gain = 11.1751 dB.

## INFERENCE

The design and analysis of a Common Source (CS) amplifier were carried out using Cadence tools for the given specifications: a supply voltage of 1.8 V, a DC gain of -5, a 3 dB frequency of 100 MHz, and a load capacitance of 5 pF. Using design equations, the required  $g_m$ , overdrive voltage, drain current, and W/L ratio were calculated. The NMOS width was chosen as 203  $\mu\text{m}$  with a length of 1  $\mu\text{m}$ . DC analysis provided operating point values such as  $ID = 1.65 \text{ mA}$ ,  $g_m = 14.46 \text{ mA/V}$ , and  $r_o = 20.65 \text{ k}\Omega$ , resulting in a self-gain of approximately 298.

AC analysis was performed with a frequency sweep from 1 Hz to 100 GHz and the response was converted to dB scale. The amplifier showed a small-signal gain of 13.11 dB, a 3 dB bandwidth of 95.39 MHz, and a unity gain frequency of 397.49 MHz. Transient analysis was also conducted using a small AC input of 5 mV. From the resulting waveforms, the peak-to-peak output voltage was measured to be 9.006 mV, and the input swing was 1.989 mV, giving a gain of 13.14 dB, confirming the amplifier's expected linear behavior.

The CS amplifier with an NMOS diode-connected load was then analysed. A parametric sweep was performed to determine the proper width of M2 to ensure it remained in saturation, which was found to be 11  $\mu\text{m}$ . After adjusting the sizing, DC analysis showed that both transistors operated at 1.52 mA with  $g_m$  values of 13.65 mA/V and 2.008 mA/V, and output resistances of 3.1  $\text{k}\Omega$  and 9.6  $\text{k}\Omega$ , respectively.

The AC response of the diode-connected configuration showed a gain of 11.16 dB, a 3 dB frequency of 102.71 MHz, and a unity gain frequency of 344.39 MHz. Transient analysis gave an output swing of 7.201 mV and a gain of 11.17 dB. Overall, the experiment successfully demonstrated the design and frequency response of both resistive and diode-loaded CS amplifiers, highlighting the trade-offs between gain, output swing, and complexity in analog circuit design.

## EXPERIMENT 4

### DESIGN & ANALYSIS OF BASIC AMPLIFIER STAGES USING PDM

#### **OBJECTIVES:**

- i. To design and analyze a Common Source Amplifier with current source load for the given specifications.
- ii. To design and analyze a Cascode Amplifier with the given specifications.
- iii. To perform dc analysis and obtain the dc operating points, small signal parameters and node voltages.
- iv. To perform ac analysis and obtain dc gain, 3dB frequency and unity gain frequency.
- v. Estimate gain and output impedance of both circuits.

#### **SPECIFICATIONS**

Parameters	Specified Values
Supply Voltage	1.8 V
Power	$\leq 250 \mu\text{W}$
UGF	150MHz
Load Capacitance	100fF

#### **CIRCUIT DIAGRAM**

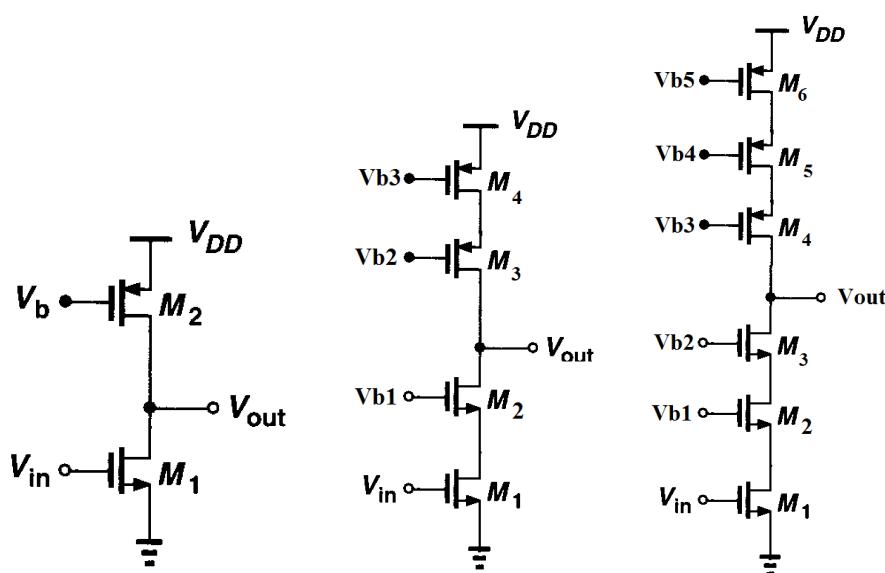


Fig : 1(a) Common Source amplifier with current source load, 1(b) Cascode Amplifier  
1(c) Triple Cascode Amplifier

## THEORY

The main goal of a MOSFET amplifier, or any amplifier for that matter, is to produce an output signal that is a faithful reproduction of its input signal but amplified in magnitude. This input signal could be a current or a voltage, but for a MOSFET device to operate as an amplifier it must be biased to operate within its saturation region. MOSFET (or, Metal-Oxide-Silicon FET) is an excellent choice for small signal linear amplifiers because of its extremely high input impedance which makes them easy to bias. Since the source terminal is common to the input and output terminals, the circuit is called common source amplifier.

PDM is a technique proposed to simplify analog design and is primarily based on voltage and current distribution at different nodes of a circuit. Apart from being technology independent, PDM is also free from complex mathematical expressions governing the devices and the circuit. Instead of relying on traditional analytical methods, PDM directly uses the simulator as a device sizing tool to meet the desired performance from the circuit. This is achieved by first designing the circuit with moderate performance by logically allocating node voltages and currents, and then modifying the potentials and currents (dc operating points) to meet the target specifications.

In applications requiring a large voltage gain in a single stage, the CS amplifier with resistive load or diode connected load is not sufficient. Because increasing the load resistance limits the output voltage swing. A more practical approach is to replace the load with a current source. Both the transistors will operate in saturation region. Since the total impedance seen at the output node is equal to  $r_{O1} \parallel r_{O2}$ , the gain is

$$A_v = -g_m(r_{O1} \parallel r_{O2}).$$

The brief algorithm of PDM is as follows:

The algorithm consists of 3 steps:

### 1. Initial Bias Conditions:

- Nodes which are kept at known potentials like common mode level are identified. Typically, the input and output terminals are kept at common mode levels (VCM) or at VDD/2.
- As a starting point, the voltage distribution is done symmetrically or uniformly about the nodes whose potentials are known and fixed. This provides adequate drain-source drop to easily bias the transistors in the saturation region.
- After allocation of drain-source potentials, the  $|V_{BS}|$  Vs.  $|V_{TH}|$  plot is referred and the threshold voltage of all transistors are estimated. The threshold voltages of the transistors are denoted as  $V_T$  where  $u$  is the number of transistors between the chosen device and the supply rail (GND for NMOS and VDD for PMOS), and  $v$  denotes whether the device is of type NMOS or PMOS and takes notation 'n' or 'p' respectively.
- A suitable gate voltage is chosen such that the overdrive is 5 - 10 % of VDD. This allows adequate inversion with minimum voltage headroom and maximum output swing. To keep transistors in saturation, care should be taken that the overdrive is smaller than the drain-source drop.
- From power dissipation constraint and slew rate requirement, the drain current of all the transistors are calculated.

## 2. Transistor Sizing:

- The simulator is used as the transistor sizing tool. Transistors with  $u = 0$  is selected as the starting point. The predefined terminal voltages are applied and using the simulator the width of the device is found which sets the desired drain current.
- Generalizing the sizing algorithm, to find the width of a transistor with  $u = m$ , we draw a schematic comprising of transistors with  $u = m, m - 1, \dots, 0$ , of either  $v = n$  or  $v = p$ , and connect them in the same way as in original schematic. We now apply only the end terminal voltages manually, i.e., for transistor with  $u = m$ , we apply the topmost drain voltage if  $v = n$  or bottommost source voltage if  $v = p$  and all the gate potentials. The intermediate drain-source nodes need not be biased since their potentials are generated by transistors with  $u = m - 1, m - 2, \dots, 0$  which are already sized before sizing transistor with  $u = m$ .
- Once all the transistor dimensions are known and fed into the simulator, the entire circuit is simulated for DC operating points.

## 3. Performance Tuning:

Once the schematic is properly biased with all transistors in saturation region, the node voltages are manipulated to get the desired performance from the circuit. The node voltages can be simply changed by following the above-mentioned steps for new set of node potentials.

## EXPERIMENTAL PROCEDURE

### Common Source amplifier with current source load: -

1. Draw the circuit as shown in Fig 1(a) with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width 2um initially. Select Vdc voltage with DC voltage as 1.8 V for the Vdd. The value at the input of gate terminal of the NMOS and PMOS are calculated using the 'Algorithm for finding the DC operating points' and PDM method.

2. Draw the basic circuit as shown in Fig 2 with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width W initially. Select Vdc voltage with DC voltage as 570mV and 900mV for gate and drain of NMOS and 1.13V, 1.8V and 900mV as gate, source and drain terminal for PMOS. The value at the input of gate terminal of the NMOS and PMOS are calculated using the 'Algorithm for finding the DC operating points' and PDM method.

From the cell view select "Launch → ADE L" to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.

3. In the Analog Environment window select "Variables → Copy from Cell view". And give the values of W as 2um.

4. Then in the window select "Analyses → Choose". Select "dc" and then "Component Parameter". Choose "Select Component" and select NMOS / PMOS and select 'simW' option then set start and stop voltages as 400n to 50u to get graph of  $I_D$  vs W.

5. Then select "Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic" to set the y-axis for NMOS and source current for PMOS. Then run the simulation to see the results.

6.  $I_D - W$  graph is obtained for different values of W. The W value corresponding to a  $I_D$  value of 100uA current is noted down.

7. The calculated W values are replaced for the PMOS and NMOS transistors in Fig 1(a) and dc analysis is performed with only 'Save dc operating point option' and they verified to operate in saturation region only. Then the dc operating point and node voltages for drain, gate, body and source terminals are noted down.

8. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS / PMOS". This gives the values of all small signal parameters of NMOS / PMOS which  $g_m$ ,  $g_{ds}$ , self gain are noted down.

9. Then perform the ac analysis with  $V_{sin}$  voltage source at input ( Dc voltage 570mV and Ac magnitude 1V ). Then perform the ac analysis with frequency range from 1 to 10G Hz. And view the plot in db20 scale by " Selecting the graph → Right Click → Dependent Modifier → db20".

10. Then select "Outputs → To Be Plotted → Select Output voltage wire for  $V_{out}$  in Schematic" to set the y-axis. Observe the plot for gain and note down the 3db frequency and unity gain frequency.

### Cascode Amplifier and Triple Cascode Amplifier :

1. For cascode amplifier and triple cascode amplifier we draw the circuit as shown in Fig 1(b) and 1(c) respectively with length of NMOS and PMOS as 500nm (2 to 3 times of  $L_{min}$  180nm ) and width 2um initially.

2. Select Vdc voltage with DC voltage as 1.8 V for the  $V_{dd}$ . The value at the input of gate terminal of the NMOS and PMOS are calculated using the 'Algorithm for finding the DC operating points' and PDM method. The basic circuits are implemented to find the values of W for all the NMOS and PMOS present in cascode and triple cascode amplifier.

3. Follow the same steps as followed for the Common Source amplifier with current source load to find the value of W and substitute it in the main circuit and obtain the dc operating points, small signal parameters and node voltages by DC analysis. And perform ac analysis observe the plot for gain and note down the 3db frequency and unity gain frequency.

### DESIGN & ANALYSIS

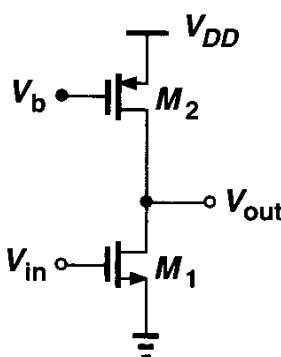


Fig 3 : Common Source amplifier with current source load

The common source is the most commonly used MOSFET amplifier. The name 'common source' comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and source terminals. A practical approach

for CS amplifier is to replace the load with a current source. Both the transistors will operate in saturation region. Since the total impedance seen at the output node is equal to  $r_{O1} \parallel r_{O2}$ , the gain is

$$A_v = -g_m(r_{O1} \parallel r_{O2}).$$

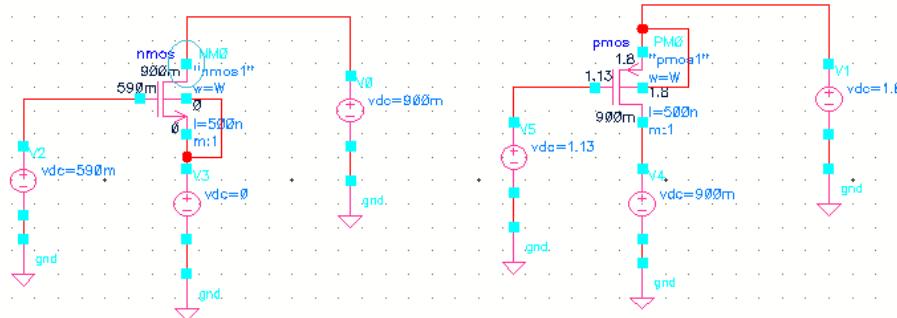


Figure 4 : The basic circuits used to find W value for NMOS and PMOS

From the given specifications we have Vdd value as 1.8 V and Power  $\leq 250 \mu\text{W}$  we can estimate the max current as  $I_{\max}$  given by Power / Vdd and the value is 138.8 uA , so we choose a current of 100uA for design.

The value of  $V_{ov}$  is chosen to be 5% of Vdd that is 90mV. Gate bias for input transistor is  $V_{ov} + V_t$  . NMOS transistor M1 is the input transistor with value 570mV. (480mv for  $V_{tn}$  and 90mv for  $V_{ov}$ ).

The  $V_b$  values to be given for other transistors are derived from the algorithm to find the dc operating point values. The node voltages to be given for the NMOS and PMOS transistors are calculated using PDM technique. Then using steps in procedure all the required values are noted down.

For the design and calculation of gate bias and source voltage of NMOS transistor :  $n_n$  is number of NMOS transistors in stack ,  $V_{top,n}$  is drain potential of top most NMOS transistor and  $V_{bottom,n}$  is source potential of bottom most NMOS transistor .

$$\begin{aligned} V_{S,n}[u] &\downarrow [u \times (V_{top,n} - V_{bottom,n})] / n_n \\ V_{G,n}[u] &\downarrow V_{S,n}[u] + V_{TH,n}[u] + 0.05 V_{DD} \end{aligned}$$

For the design and calculation of gate bias and source voltage of PMOS transistor :  $n_p$  is number of PMOS transistors in stack ,  $V_{top,p}$  is source potential of top most PMOS transistor and  $V_{bottom,p}$  is drain potential of bottom most PMOS transistor .

$$\begin{aligned} V_{S,p}[u] &\downarrow V_{DD} - [u \times (V_{top,p} - V_{bottom,p})] / n_p \\ V_{G,p}[u] &\downarrow V_{S,p}[u] - V_{TH,p}[u] - 0.05 V_{DD} \end{aligned}$$

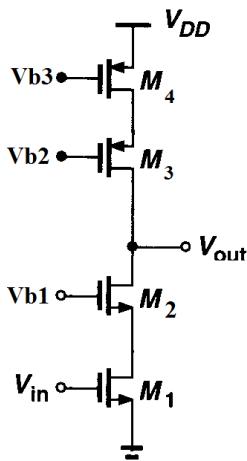


Fig 5 : Cascode Amplifier

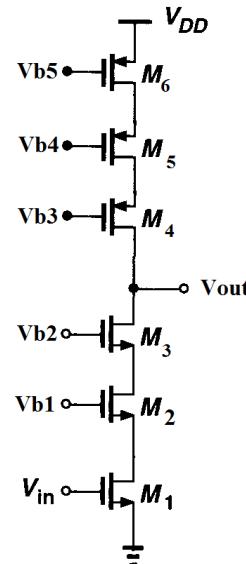


Fig 6 : Triple Cascode Amplifier

The cascade of a CS stage and CG stage is called a cascode amplifier. The cascode amplifier circuit have a lot of advantages over the single stage amplifier like, better input and output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate. A popular application of this topology is in building constant current sources. The high output impedance yields a current source closer to the ideal, but at the cost of voltage headroom. The current source  $I_1$  can be implemented with a PMOS cascode, exhibiting impedance equal to  $[1 + (g_{m3} + g_{mb3}) r_{o3}] r_{o4} + r_{o3}$ . The maximum output voltage swing is given by:

$$V_{DD} - (V_{GS1} - V_{TH1}) - (V_{GS2} - V_{TH2}) - |V_{GS3} - V_{TH3}| - |V_{GS4} - V_{TH4}|.$$

The total output impedance and hence the gain equations are given by :

$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2}\} \parallel \{[1 + (g_{m3} + g_{mb3})r_{o3}]r_{o4} + r_{o3}\},$$

$$|A_v| \approx g_{m1}[(g_{m2}r_{o2}r_{o1}) \parallel (g_{m3}r_{o3}r_{o4})].$$

The same principle is used in the design of triple cascode amplifier with the increase in output impedance and hence increase in total gain of the amplifier. The total output gain equation is given by :

$$|A_v| \approx g_{m1}[(g_{m3}r_{o3}g_{m2}r_{o2}r_{o1}) \parallel (g_{m4}r_{o4}g_{m5}r_{o5}r_{o6})]$$

## RESULTS

(i) Operating points for the Common Source amplifier with current source load

Transistor	V <sub>S</sub> (V)	V <sub>D</sub> (V)	V <sub>G</sub> (V)	V <sub>B</sub> (V)
M1	0	949.612m	590m	0
M2	1.8	949.612m	1.21	1.8

The small signal parameters are as follows:

Transistor	$I_D$ (A)	$g_m$ (A/V)	$g_{ds}$ (A/V)	$r_o$ (K ohm)	Self gain ( $g_m r_o$ )
M1 (NM0)	100.351u	1.2508m	6.6833u	149.626	187.1522
M2 (PM0)	100.351u	1.1913m	9.3533u	106.914	127.3666

(ii) Operating points for Cascode Amplifier

Transistor	$V_s$ (V)	$V_D$ (V)	$V_G$ (V)	$V_B$ (V)
M1 (NM0)	0	450.547m	590m	0
M2 (NM1)	450.547m	902.979m	1.04	450.547m
M3 (PM1)	1.4078	902.979m	760m	1.4078
M4 (PM0)	1.8	1.4078	1.4078	1.8

The small signal parameters are as follows:

Transistor	$I_D$ (A)	$g_m$ (A/V)	$g_{ds}$ (A/V)	$r_o$ (K ohm)	Self gain ( $g_m r_o$ )
M1	100.001u	1.2550m	12.1547u	82.2726	103.2521
M2	99.9978u	1.2583m	12.0959u	82.6724	104.0266
M3	99.9983u	923.723u	11.6127u	86.1126	79.5441
M4	100.001u	1.1943m	14.3626u	69.6251	83.1532

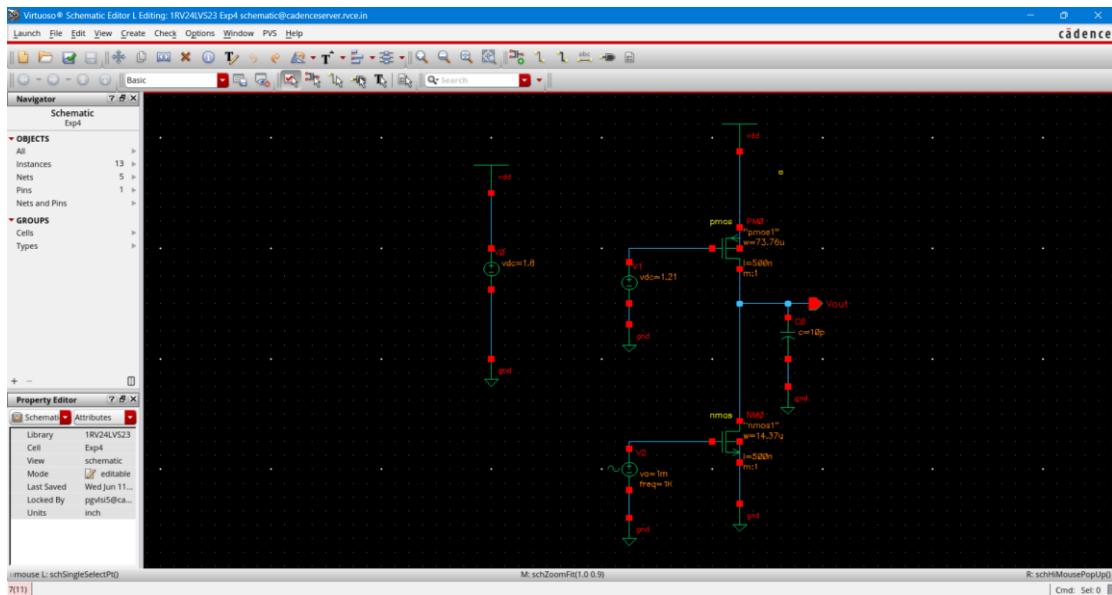
(iii) Operating points for Triple Cascode Amplifier

Transistor	$V_s$ (V)	$V_D$ (V)	$V_G$ (V)	$V_B$ (V)
M1 (NM0)	0	300.394m	500m	0
M2 (NM1)	300.394m	598.315m	890m	300.394m
M3 (NM2)	598.316m	896.383m	1.19	598.315m
M4 (PM0)	1.2521	896.383m	610m	1.2521
M5 (PM1)	1.5361	1.25213	910m	1.5361
M6 (PM2)	1.8	1.53612	1.21	1.8

The small signal parameters are as follows:

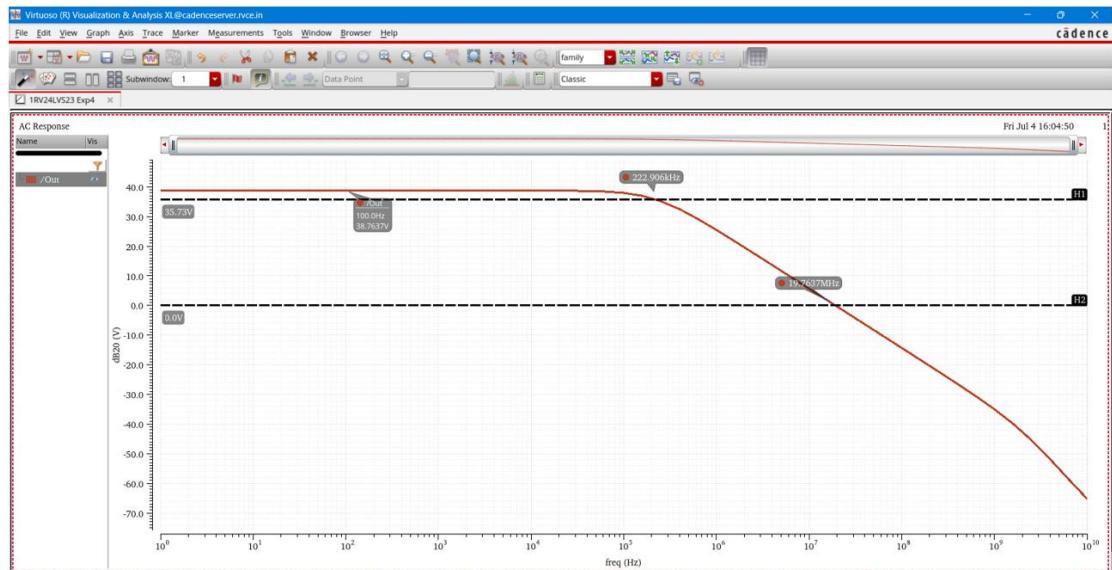
Transistor	$I_D$ (A)	$g_m$ (A/V)	$g_{ds}$ (A/V)	$r_o$ (K ohm)	Self gain ( $g_m r_o$ )
M1	99.99u	1.2520m	21.9299u	45.5999	57.091
M2	99.99u	1.2543m	22.2281u	44.9882	56.4286
M3	99.99u	1.2416m	22.0704u	45.3095	56.2562
M4	99.99u	945.231u	17.2085u	58.1107	54.928
M5	99.99u	1.0071m	23.7689u	42.0718	42.3705
M6	99.99u	1.1904m	23.5688u	42.429	50.5074

## DISCUSSIONS



**Fig 1. Circuit for CS Amplifier with Current source load**

DC analysis is performed for  $I_D - W$  parameter with the help of ‘simW’ option. The value of W for NMOS and PMOS are found. This value is substituted in the CS amplifier circuit. The W values are found to be  $73.76\mu\text{m}$  for PMOS and  $14.37\mu\text{m}$  for NMOS. The transistors are verified to be operating in saturation region.



**Fig 2  $A_v$  (dB 20 ) - frequency characteristics for Common Source amplifier with current source load**

The AC analysis is a plot of  $A_v$  (dB 20 ) - frequency and the frequency range is given from 1-10GHz. AC Analysis is performed to verify the gain. The values of 3 dB frequency and unity gain frequency are obtained. The gain is  $37.8412$  dB and 3dB frequency is  $252.525$  KHz and Unity Gain Frequency is  $20.1578$  MHz.

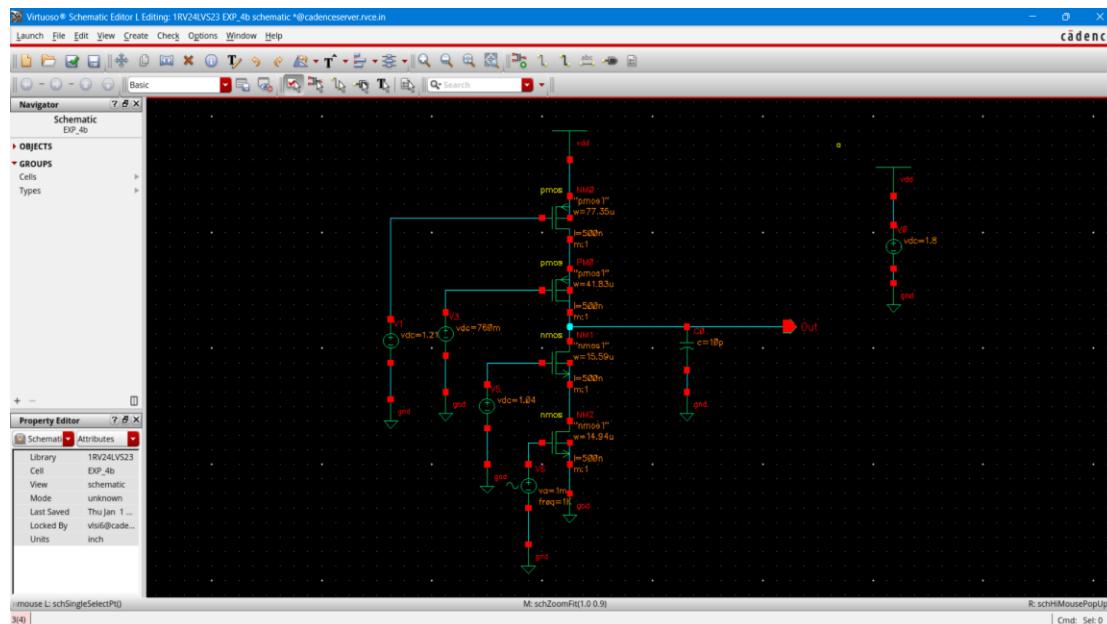


Fig 3. Circuit for Cascode Amplifier

DC analysis is performed for  $I_D$  - W parameter with the help of ‘simW’ option. The value of W for NMOS and PMOS are found and placed in the Cascode amplifier circuit. The W values found are 77.34  $\mu\text{m}$  and 41.49  $\mu\text{m}$  for PMOS and 14.94  $\mu\text{m}$  and 15.04  $\mu\text{m}$  for NMOS. The transistors are checked to be operating in saturation region.

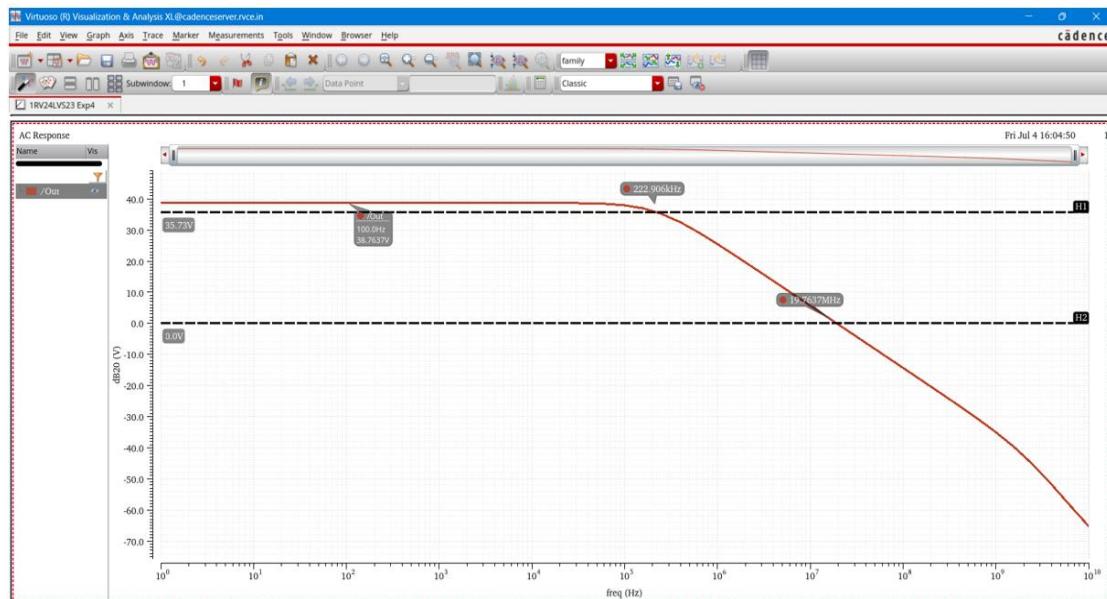


Fig:4  $A_v$  (dB 20 ) - frequency characteristics for Cascode amplifier

The AC analysis is a plot of  $A_v$  (dB 20) - frequency and the frequency range is given from 1-10GHz. AC Analysis provides the gain, the values of 3 dB frequency and unity gain frequency. The gain is 72.6305 dB and 3dB frequency is 4.6087 KHz and Unity Gain Frequency is 20.2642 MHz.

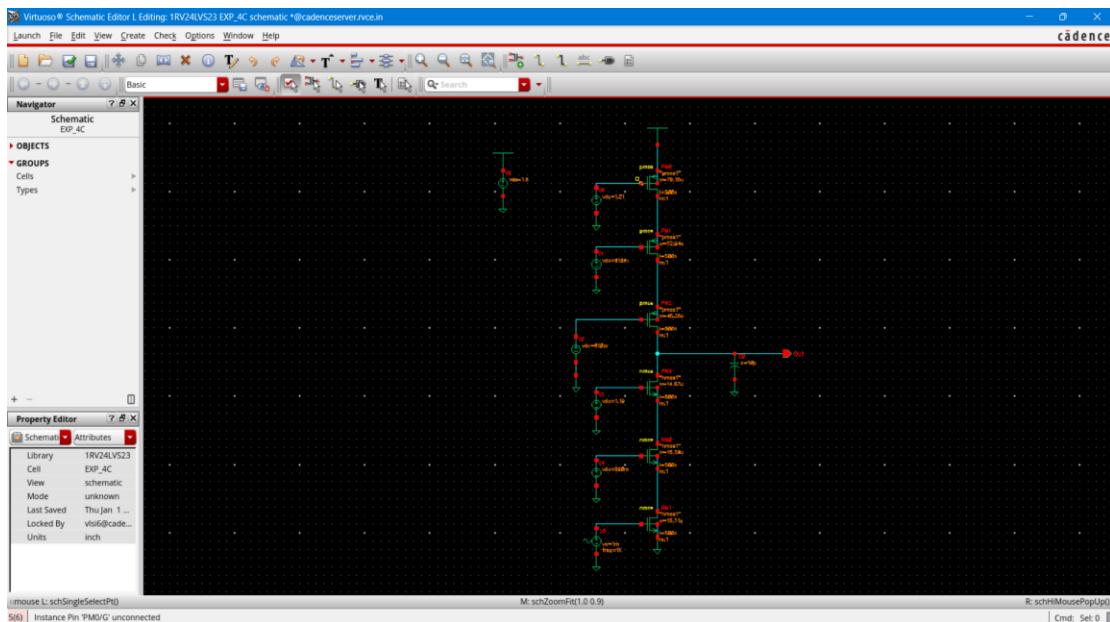
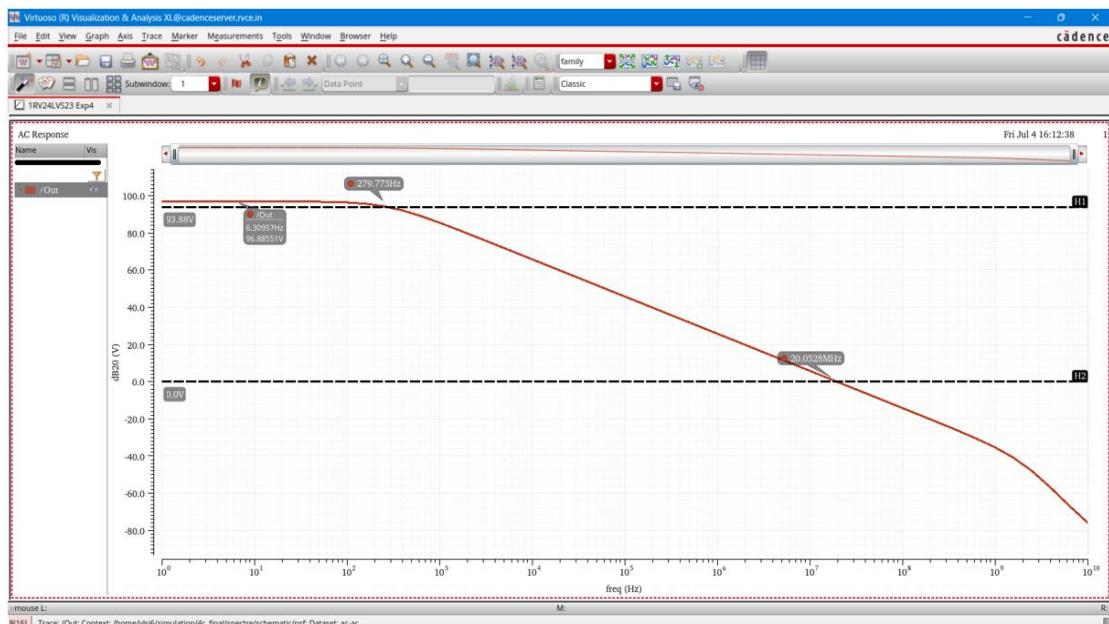


Fig 5. Circuit for Triple Cascode Amplifier

Initially the DC analysis is performed for  $I_D$  - W parameter and the value of W for NMOS and PMOS are found and placed in the Triple Cascode amplifier circuit. The W values found are  $79.15\text{ }\mu\text{m}$ ,  $52.9\text{ }\mu\text{m}$  and  $44.76\text{ }\mu\text{m}$  for PMOS and  $14.98\text{ }\mu\text{m}$ ,  $15.4\text{ }\mu\text{m}$  and  $15.3\text{ }\mu\text{m}$  for NMOS. The transistors are verified to be operating in saturation region.

Fig:6  $A_v$  (dB 20 ) - frequency characteristics for Triple Cascode amplifier

Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) - frequency and the frequency range is given from 1-10GHz. The gain is  $97.6938\text{ dB}$  and 3dB frequency is  $254.299\text{ Hz}$  and UGF is  $20.0557\text{ MHz}$ .

The inference from this graph is that as frequency increases, the gain of the triple cascode amplifier decreases.

## INFERENCE

The experiment involved designing and analysing a Common Source (CS) amplifier with a current source load and extended it to Cascade and Triple Cascade amplifier configurations. The PDM was used to determine DC node voltages and transistor dimensions to meet the given specifications—supply voltage of 1.8 V, power  $< 250 \mu\text{W}$ , and a unity gain frequency of 150 MHz. Using PDM, the gate voltages and widths for both NMOS and PMOS were calculated to ensure all transistors operated in the saturation region.

For the CS amplifier with current source load, DC analysis confirmed correct biasing, and AC analysis showed a gain of 37.84 dB, 3 dB frequency of 252.5 kHz, and unity gain frequency of 20.15 MHz. The transistor dimensions were finalized using ID vs W plots for a target current of 100  $\mu\text{A}$ . Small signal parameters were extracted and matched the required design goals.

The Cascade amplifier showed improved performance with a gain of 72.63 dB and unity gain frequency of 20.26 MHz. The Triple Cascode amplifier further increased the gain to 97.69 dB, though with a lower 3 dB bandwidth. In all three cases, DC and AC analysis confirmed that transistor stacking improves gain and output impedance while keeping the design within power and voltage constraints.

The experiment demonstrated that cascading stages in amplifier design significantly improves gain and performance metrics. The use of PDM simplified the sizing and biasing process, making the design flow more intuitive and technology-independent.

## EXPERIMENT 5

### DESIGN & ANALYSIS OF DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

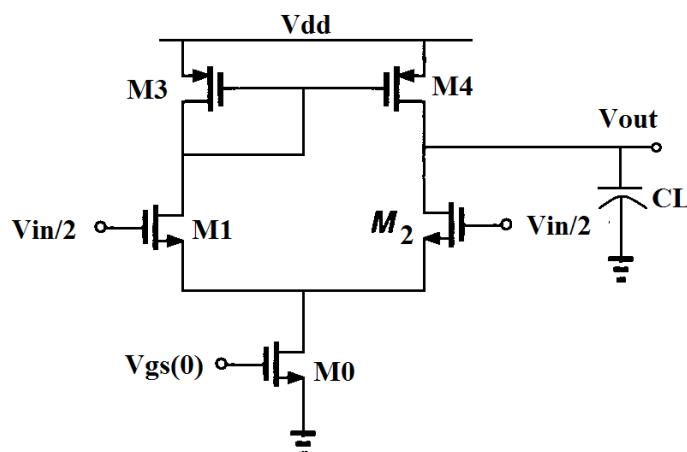
#### **OBJECTIVES:**

- i. To design and analyze a Differential Amplifier with active load for the given specifications using two different methods Potential Distribution Method (PDM) and Analytical method.
- ii. To perform dc analysis and obtain the dc operating points, small signal parameters and node voltages.
- iii. To perform ac analysis and obtain dc gain, 3dB frequency and unity gain frequency and verify slew rate.
- iv. Estimate gain and output impedance of both circuits.

#### **SPECIFICATIONS**

Parameters	Specified Values
Supply Voltage	1.8 V
Gain	40 dB
ICMR <sup>-</sup>	0.8 V
ICMR <sup>+</sup>	1.6 V
Load Capacitance	10pF
Slew Rate	5 V/ $\mu$ sec
Gain-Band width product	5MHz

#### **CIRCUIT DIAGRAM**

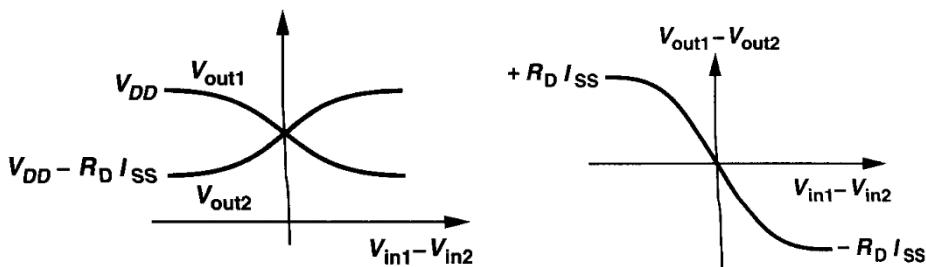


**Fig: 1 Differential Amplifier with active load**

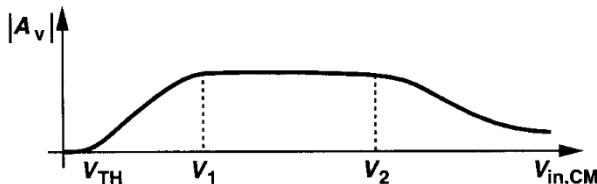
## THEORY

A Differential Amplifier is an analog circuit with two inputs and one output in which the output is ideally proportional to the difference between the two voltages. It is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs.

The differential signal is defined as one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential i.e., they must exhibit equal impedances at that potential. The center potential in differential signaling is called "common mode" CM level. An important advantage of differential operation is higher immunity to environmental noise and increase in maximum achievable voltage swings. The differential pair employs a current source  $I_{ss}$  to make  $I_{D1} + I_{D2}$  independent of  $V_{in,cm}$ . Thus, if  $V_{in1} = V_{in2}$ , the bias current of each transistor will be  $I_{ss}/2$  and the output common mode level is  $V_{DD} - R_D I_{ss}/2$ .



**Fig: 2 Input and output characteristics of a differential pair**



**Fig: 3 Small signal differential gain of a differential pair**

Single ended output has one output and in the pull up network the PMOS transistors gates are connected to their drain terminals. Differential Amplifiers allow the process of single-ended input to complementary differential outputs or differential inputs to differential outputs. These amplifiers feature two separate feedback loops to control the differential and common-mode output voltages. Analog Devices fully differential amplifiers are configured with a VOCM pin, which can be easily adjusted for setting output common-mode voltage. When a current mirror is used for biasing the transistors then it is called passive. Similarly, when a current mirror is used as a load then it acts as an active load to a differential Amplifier.

The load of the differential pair can be implemented by active loads using diode connected load or current source loads. Diode connected loads consume large headroom voltage and hence we consider differential Amplifier with current source load as the active load. As shown in figure 1, M1 and M2 are n-channel devices and form the diff pair biased with  $I_{ss}$ . The load circuit consists of M3 and M4, both p-channel devices, connected in a current-mirror configuration. A one-sided output is taken from the common drains of M2 and M4. When a common-mode voltage  $V_1 = V_2 = V_{CM}$  is applied the current  $I_{ss}$  splits evenly between transistors M1 and M2, and  $I_{D1}$

$= I_{D2} = I_{SS} / 2$ . There are no gate currents, therefore  $I_{D3} = I_{D1}$  and  $I_{D4} = I_{D2}$ . And the gain is given by: -

$$A_v = -g_{mN}(r_{ON} \parallel r_{OP}).$$

## EXPERIMENTAL PROCEDURE

### Differential Amplifier with active load using PDM method: -

1. Draw the circuit as shown in Fig 1 with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width 2um initially. Select Vdc voltage with DC voltage as 1.8 V for the Vdd. The value at the input of gate terminal of the NMOS and PMOS are calculated using the 'Algorithm for finding the DC operating points' and PDM method.
2. Draw the basic circuit with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width W initially. Select Vdc voltage with DC voltage as 590mV, 0V and 180mV for gate, source and drain of NMOS M0. Then 900mV, 180mV and 900mV as gate, source and drain of NMOS M1(M2) and 900mV, 1.8V and 900mV as gate, source and drain terminal for PMOS M3(M4). The value at the input of gate terminal of the NMOS and PMOS are calculated using the 'Algorithm for finding the DC operating points' and PDM method.

From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.

3. In the Analog Environment window select "Variables → Copy from Cell view". And give the values of W as 2um.
4. Then in the window select “Analyses → Choose”. Select “dc” and then “Component Parameter”. Choose “Select Component” and select NMOS / PMOS and select 'simW' option then set start and stop voltages as 400n to 50u to get graph of  $I_D$  vs W.
5. Then select “Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic” to set the y-axis for NMOS and source current for PMOS. Then run the simulation to see the results.
6.  $I_D$  – W graph is obtained for different values of W. The W value corresponding to a  $I_D$  value of 50uA and 25uA currents for respective graphs and transistors is noted down.
7. The calculated W values are replaced for the PMOS and NMOS transistors in Fig 1 and dc analysis is performed with only 'Save dc operating point option' and they are verified to operate in saturation region only. Then the dc operating point and node voltages for drain, gate, body and source terminals are noted down.
8. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS / PMOS". This gives the values of all small signal parameters of NMOS / PMOS which  $g_m$ ,  $g_{ds}$ , self-gain is noted down.
9. Then perform the ac analysis with  $V_{sin}$  voltage source at input (Dc voltage 590mV and Ac magnitude 1V). Then perform the ac analysis with frequency range from 1 to 10G Hz. And view the plot in db20 scale by "Selecting the graph → Right Click → Dependent Modifier → db20".

10. Then select “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic” to set the y-axis. Observe the plot for gain and note down the 3db frequency and unity gain frequency.

### Differential Amplifier with active load using analytical calculations method: -

1. Draw the circuit as shown in Fig 1(a) with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width 2um initially. Select Vdc voltage with DC voltage as 1.8 V for the Vdd. The value at the input of gate terminal of the NMOS and PMOS are calculated using the general equations for differential amplifier and transistors as mentioned in the design.

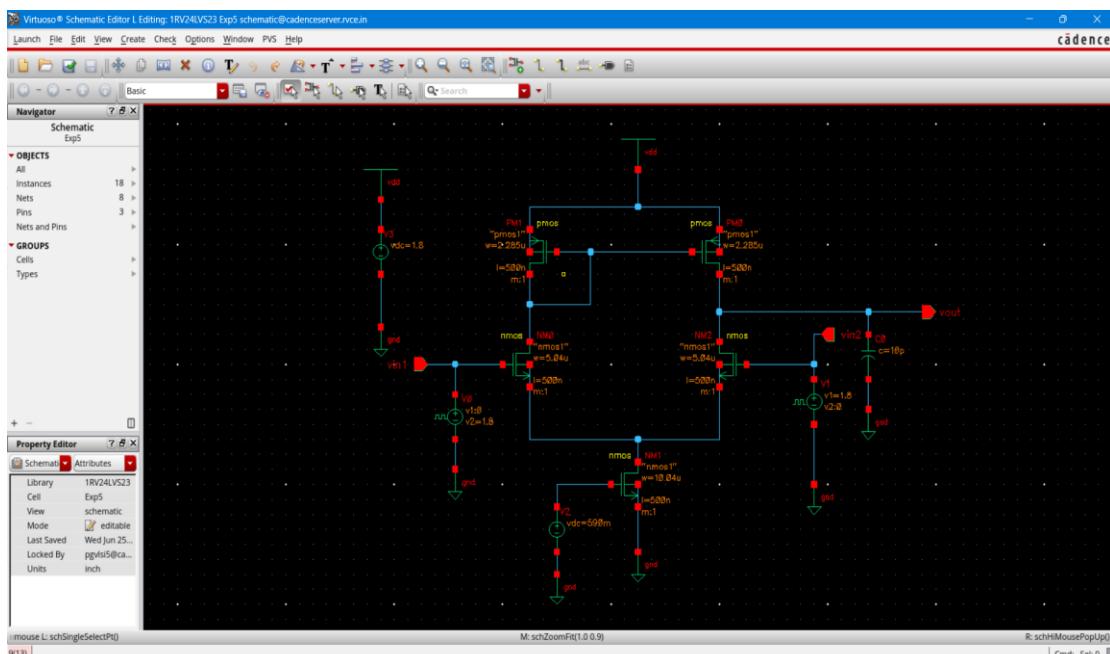
2. Select Vdc voltage with DC voltage as 1.8 V for the Vdd. To find the value of W and substitute it in the main circuit use the general equations. Follow the same steps as followed for the Differential amplifier using PDM method and obtain the dc operating points, small signal parameters and node voltages by DC analysis.

3. Perform ac analysis and observe the plot for gain and note down the 3db frequency and unity gain frequency. The only difference will be in the values of gate input, intermediate node voltages and W values designed and calculated.

4. Then to verify the slew rate the negative terminal of differential amplifier is shorted to output line. i.e., gate of M2 transistor is shorted to Vout line and a vpulse signal i.e., a step input is applied at gate of transistor M1 with V<sub>1</sub> as 0V and V<sub>2</sub> as 0.9V.

5. Then a transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic and input wire for M1”. In the plot for Vout versus time axis calculate the slope which gives the slew rate required to be verified.

## DESIGN & ANALYSIS



**Fig 4: Differential Amplifier with active load**

### Using PDM method: -

From the given specifications we have  $C_L$  value as 10pF and slew rate 5V/ usec we can estimate the max current as  $I_{max}$  given by slew rate  $\times C_L$  and the value is 50 uA, so we choose a current of 50uA for design which splits as 25 uA for each branch.

The value of  $V_x$  is chosen to be 10% of  $V_{DD}$  that is 180mV. NMOS transistor M0 is the current source transistor with value 590mV (using algorithm). And the gate of input transistors M1 and M2 is chosen to be 900mV.

The  $V_b$  values to be given for other transistors are derived from the algorithm to find the dc operating point values. The node voltages to be given for the NMOS and PMOS transistors are calculated using PDM technique. Then using steps in procedure all the required values are noted down.

For the design and calculation of gate bias and source voltage of NMOS transistor:  $n_n$  is number of NMOS transistors in stack,  $V_{top,n}$  is drain potential of top most NMOS transistor and  $V_{bottom,n}$  is source potential of bottom most NMOS transistor .

$$\begin{aligned} V_{S,n}[u] &\longrightarrow [u \times (V_{top,n} - V_{bottom,n})] / n_n \\ V_{G,n}[u] &\longrightarrow V_{S,n}[u] + V_{TH,n}[u] + 0.05 V_{DD} \end{aligned}$$

For the design and calculation of gate bias and source voltage of PMOS transistor:  $n_p$  is number of PMOS transistors in stack,  $V_{top,p}$  is source potential of top most PMOS transistor and  $V_{bottom,p}$  is drain potential of bottom most PMOS transistor .

$$\begin{aligned} V_{S,p}[u] &\longrightarrow V_{DD} - [u \times (V_{top,p} - V_{bottom,p})] / n_p \\ V_{G,p}[u] &\longrightarrow V_{S,p}[u] - V_{TH,p}[u] - 0.05 V_{DD} \end{aligned}$$

The total output impedance and hence the gain equations are given by:

$R_{out} = (r_{o2} \parallel r_{o4})$  or we can find using  $(r_{o1} \parallel r_{o3})$

$$A_v = -g_{mN}(r_{ON} \parallel r_{OP}).$$

### Using Analytical calculations method: -

The value at the input of gate terminal of the NMOS and PMOS are calculated using the general equations for differential amplifier and transistors as mentioned in the design. To find the value of W and substitute it in the main circuit use the general equations. From the given specifications we have  $C_L$  value as 10pF and slew rate 5V/usec we can estimate the max current as  $I_{max}$  given by slew rate \*  $C_L$  and the value is 50 uA, so we choose a current of 50uA for design which splits as 25 uA for each branch.

The value of  $V_x$  is chosen to be 10% of  $V_{DD}$  that is 180mV. Gate bias for current source transistor M0 is  $V_{ov} + V_t$ .

Equations used for analytical method calculations:

- The current through all the devices are found out using the formula

$$\text{Slew rate} = \frac{dvo}{dt} \quad |_{\text{max}} = \frac{Io}{CL}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right) V_{ov}^2$$

$$V_{ov} = V_{gs} - V_t$$

- In the above equations  $V_{ov}$  is the overdrive voltage.
- $(W/L)$  is determined using the equation

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)} I_D$$

- $\text{ICMR}^-$  decides the  $(W/L)$  value of the lower transistors.

$$\text{ICMR}^- = V_{GS1} + V_{ov5}$$

- The Gain Bandwidth product can be used to find the  $(W/L)$  of the input transistors.

$$\text{Gain} = g_m 1,2 (r_{o1,2} \parallel r_{o3,4})$$

$$\text{Gain} * \text{Bandwidth} = \text{DC gain} * \text{Dominant pole}$$

$$\text{Dominant pole} = 1/SC_L (r_{o1,2} \parallel r_{o3,4})$$

$$\text{Gain} * \text{Bandwidth} = g_m 1,2 / 2\pi C_L$$

- The  $\text{ICMR}^+$  decides the  $(W/L)$  value of the upper transistors.

$$\text{ICMR}^+ = V_{DD} - |V_{GS3,4}| + V_{tn}$$

NMOS transistor M0 is the current source transistor with value 680mV. (500mv for  $V_{tn}$  and 180mv for  $V_x$ ). The gate of input transistors M1 and M2 is chosen to be 900mV.

For M1 to be in saturation we can use the standard equation  $V_{GS} > V_{th}$  and  $V_{DS} \geq (V_{GS} - V_{th})$  and find value of  $V_y$ . Then use the current equation to find  $(W/L)_3$ : -

$$I_D = \frac{\mu_n C_{ox} W}{2} \left( V_{GS} - V_T \right)^2 (1 + \lambda V_{ds})$$

## RESULTS

- (i) Operating points for Differential Amplifier with current source load using PDM method: -

Transistor	$V_s(V)$	$V_D(V)$	$V_G(V)$	$V_B(V)$
M0	0	454.526m	590m	0
M1 (M2)	454.526m	914.04m	1.04	454.526m
M3 (M4)	1.8	914.04m	914.04m	1.8

(ii)The small signal parameters are as follows:

Transistor	$I_D$ ( $\mu A$ )	$g_m$ ( $\mu A/V$ )	$g_{ds}$ ( $\mu A/V$ )	$r_o$ (K ohm)	Self-gain ( $g_m r_o$ )
<b>M0</b>	47.083	631.663	5.94105	168.32	106.322
<b>M1 (M2)</b>	23.5405	320.427	2.9737	336.28	107.753
<b>M3 (M4)</b>	23.566	96.296	1.6176	618.189	59.529

(iii) Operating points for Differential Amplifier with current source load using analytical calculations method: -

Transistor	$V_s$ (V)	$V_D$ (V)	$V_G$ (V)	$V_B$ (V)
<b>M0</b>				
<b>M1 (M2)</b>				
<b>M3 (M4)</b>				

The small signal parameters are as follows:

Transistor	$I_D$ ( $\mu A$ )	$g_m$ ( $\mu A/V$ )	$g_{ds}$ ( $\mu A/V$ )	$r_o$ (K ohm)	Self-gain ( $g_m r_o$ )
<b>M0</b>					
<b>M1 (M2)</b>					
<b>M3 (M4)</b>					

## DISCUSSIONS

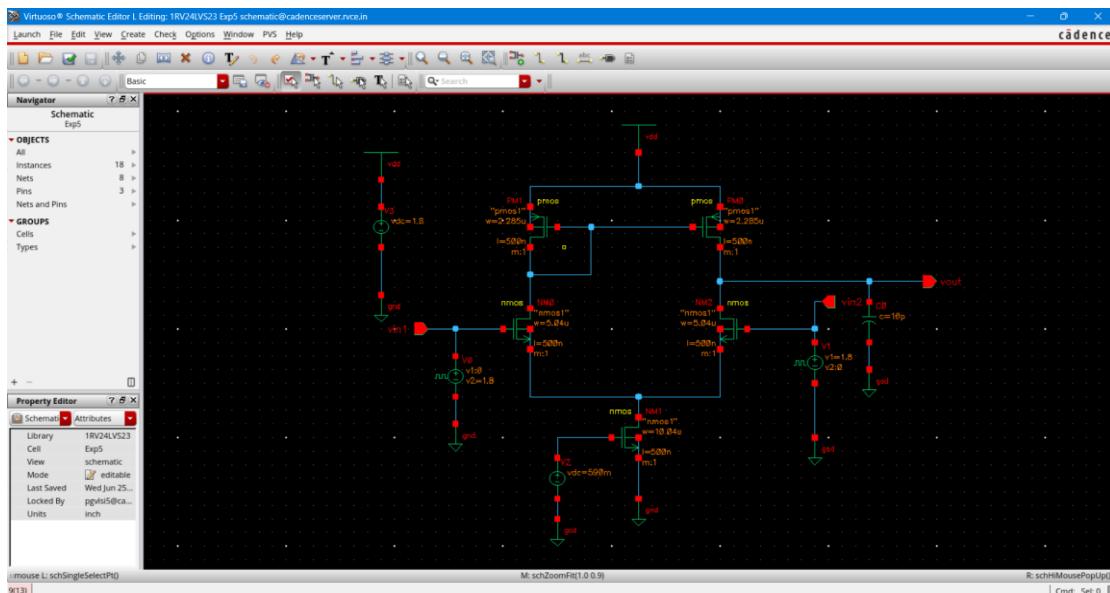
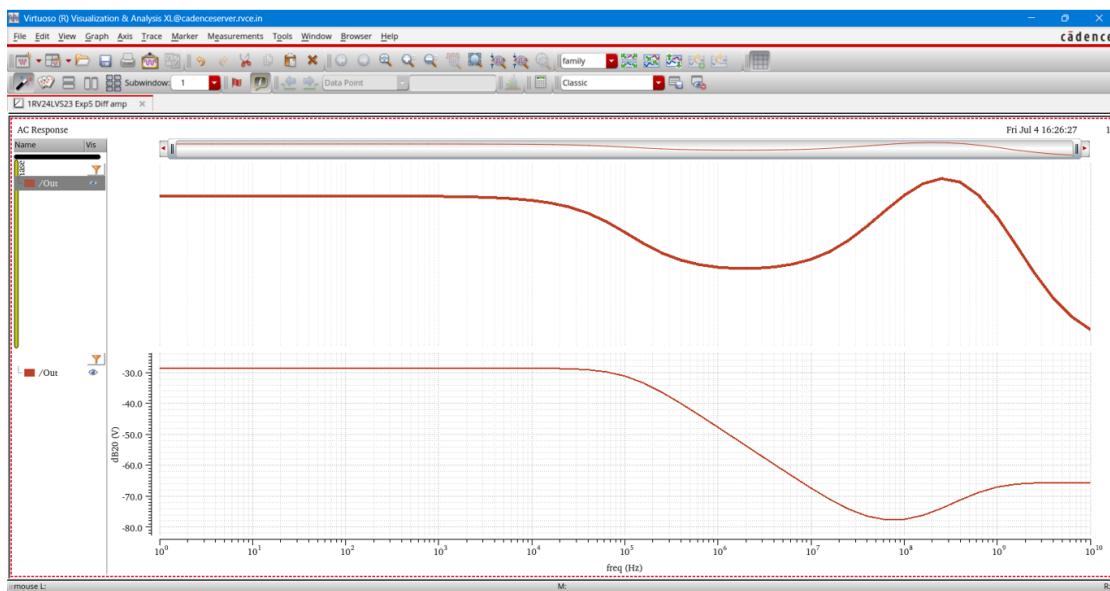


Fig 5. Circuit of Differential Amplifier using PDM method

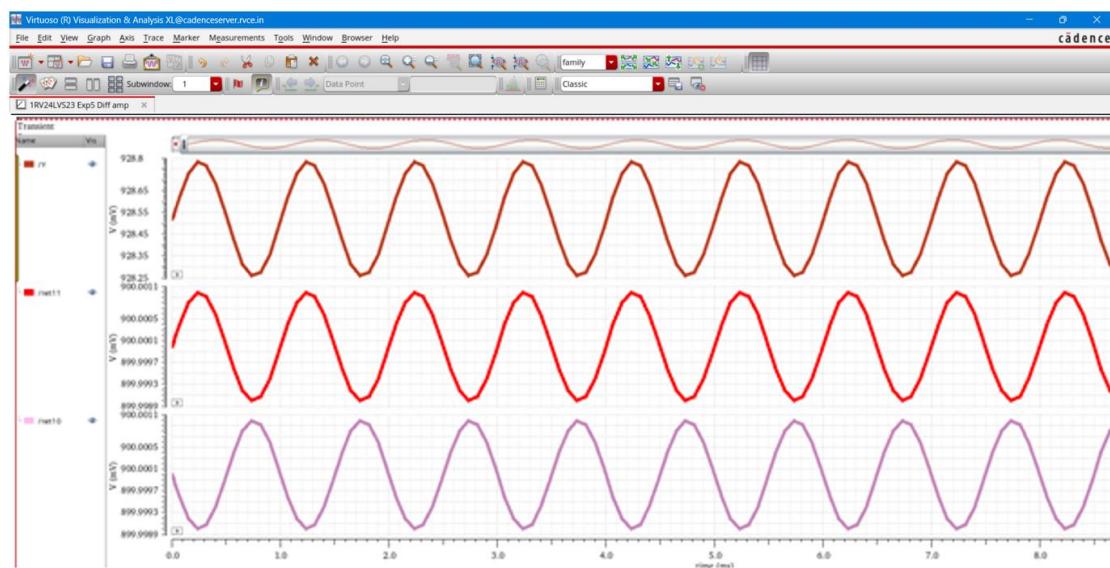
Initially the DC analysis is performed for  $I_D$  - W parameter and the value of W for NMOS and PMOS are found and placed in the Differential amplifier circuit. The W

values found are \_\_\_\_\_  $\mu\text{m}$  for PMOS M3 (M4) and \_\_\_\_\_  $\mu\text{m}$  for NMOS NM1 (NM2) and \_\_\_\_\_  $\mu\text{m}$  for NMOS M0. The transistors are verified to be operating in saturation region. The circuit is as shown in Figure 5.



**Fig:6**  $A_v$  (dB 20) – frequency characteristics for Differential Amplifier with active load using PDM method

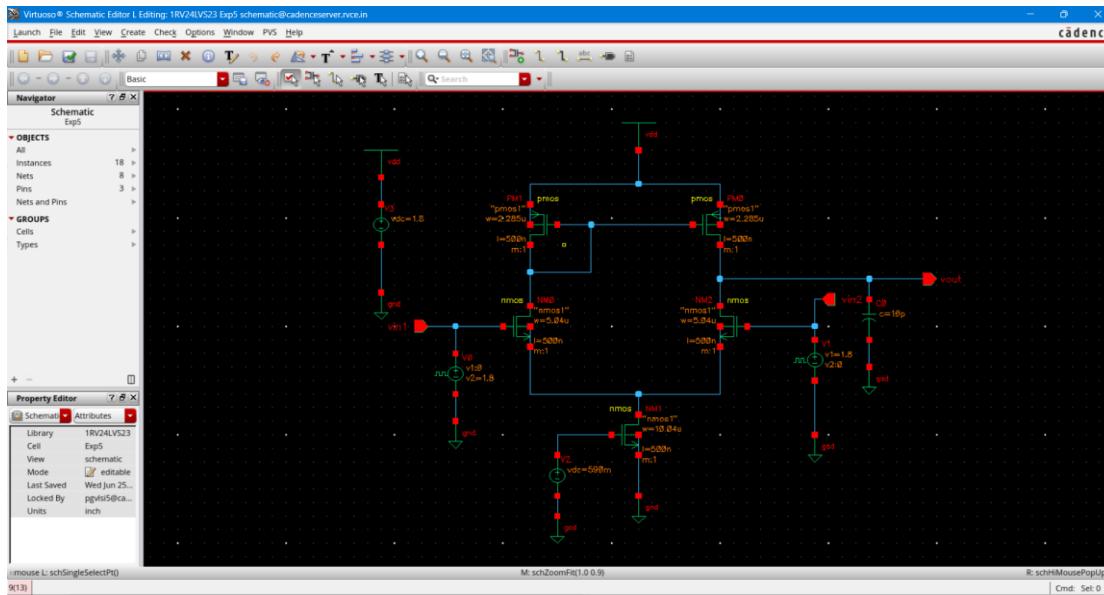
Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) – frequency and the frequency range are given from 1-10GHz. The gain is \_\_\_\_\_ dB and 3dB frequency is \_\_\_\_\_ KHz and UGF is \_\_\_\_\_ MHz.



**Fig:7** Transient Analysis for Differential Amplifier with active load using PDM method

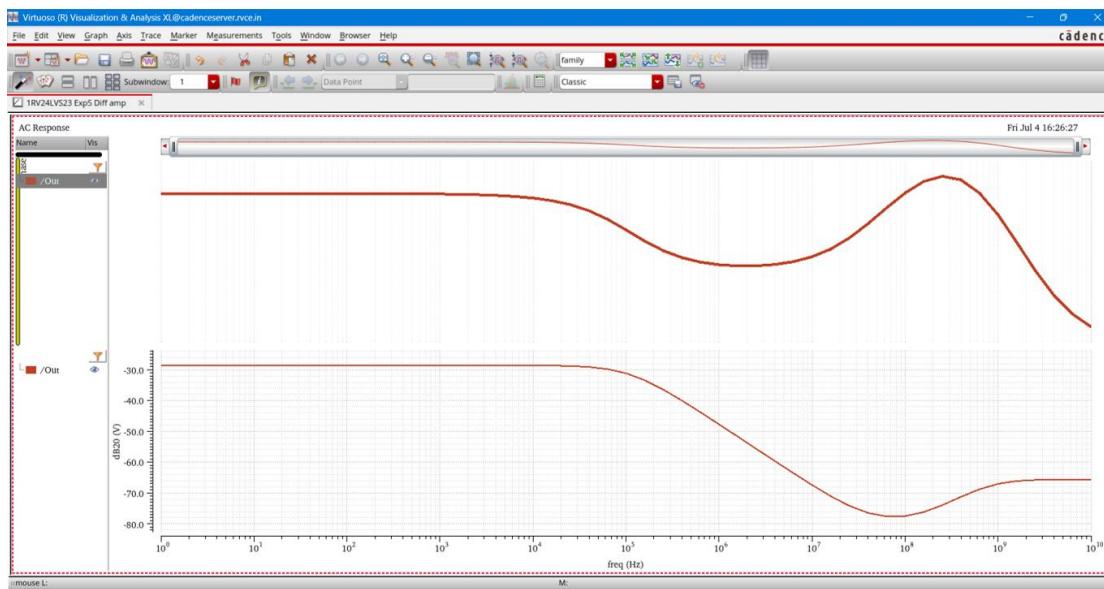
The plot of output and input voltage of the input transistor in the Differential amplifier with active load is obtained by the transient analysis. The peak-to-peak voltage of both

the input and output waveforms are calculated to obtain output swing which is 1.06 V. It is as shown in Figure 6 using PDM method.



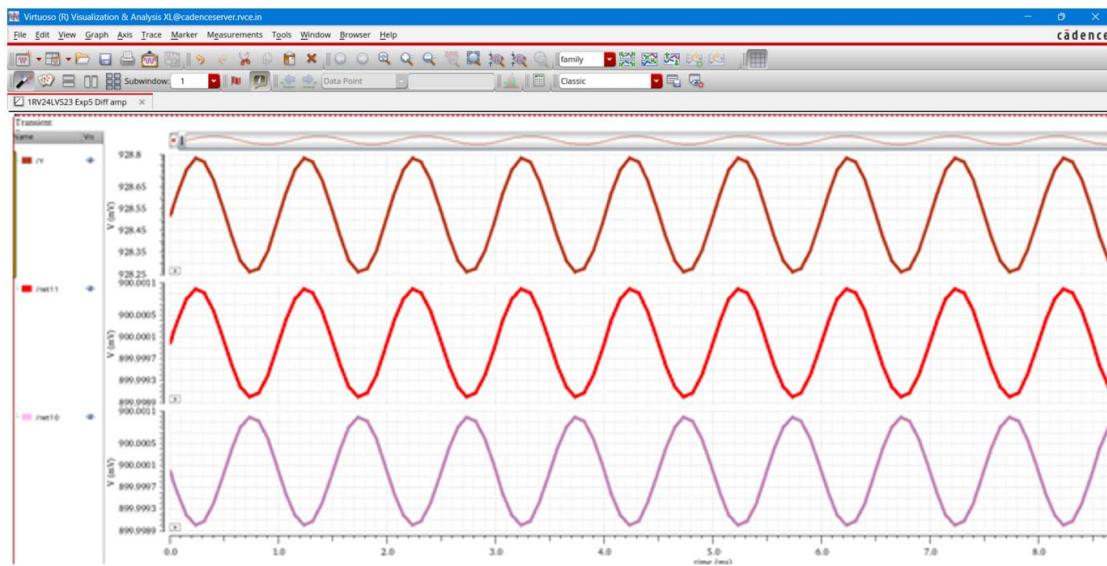
**Fig 8. Circuit of Differential Amplifier using analytical method**

Initially the DC analysis is performed for  $I_D - W$  parameter and the value of W for NMOS and PMOS are found and placed in the Differential amplifier circuit. The W values found are \_\_\_\_\_ $\mu\text{m}$  for PMOS M3 (M4) and \_\_\_\_\_ $\mu\text{m}$  for NMOS NM1 (NM2) and \_\_\_\_\_ $\mu\text{m}$  for NMOS M0. The transistors are verified to be operating in saturation region. The circuit is as shown in Figure 8.



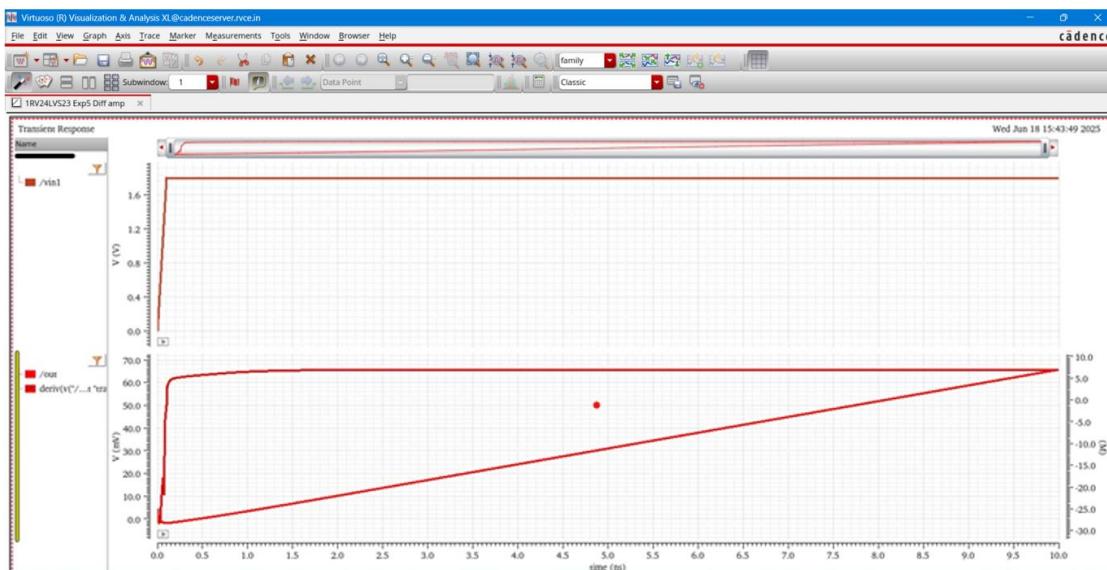
**Fig:9  $A_v$  (dB 20) – frequency characteristics for Differential Amplifier with active load using analytical calculations.**

Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) – frequency and the frequency range are given from 1-10GHz. The gain is \_\_\_\_\_dB and 3dB frequency is \_\_\_\_\_KHz and UGF is \_\_\_\_\_MHz.



**Fig:10 Transient Analysis for Differential Amplifier with active load using analytical calculations.**

The plot of output and input voltage of the input transistor in the Differential amplifier with active load is obtained by the transient analysis. The peak to peak voltage of both the input and output waveforms are calculated to obtain output swing which is 1.2V. It is as shown in figure 8 using analytical method.



**Fig:11 Slew rate calculation for Differential Amplifier**

Then a transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic and input wire for M1”. In the plot for Vout versus time axis calculate the slope which gives the slew rate required to be verified. The slew rate is found to be 3.78V/  $\mu$ sec.

## INFERENCE

The design and analysis of a Differential Amplifier with an active load were performed and verified to ensure they meet the given specifications. The gate terminal voltages of the NMOS and PMOS transistors were calculated using both analytical and PDM (Point-Driven Method) approaches. The widths (W) of various transistors were determined to ensure operation in the saturation region.

DC analysis was carried out to obtain the DC operating points, small-signal parameters, and node voltages. The results were tabulated.

AC analysis was then performed to verify the gain and determine the 3 dB frequency and unity-gain frequency. The AC response was plotted as  $A_v$  (in dB) versus frequency over a range of 1–10 GHz. The same analysis procedure was followed using analytical calculations, and the results were compared.

Transient analysis of the Differential Amplifier with an active load was conducted using both analytical and PDM methods. It was observed that the peak-to-peak output voltage ( $V_{op-p}$ ) and gain were higher when using the analytical method.

In submicron design, channel length modulation significantly affects circuit behavior, causing deviations from ideal performance. As a result, traditional long-channel design equations no longer yield accurate design parameters.

Channel length modulation reduces the output resistance, which complicates the design process. This leads to more complex, time-consuming, and iterative methodologies, extending the overall design cycle and reducing accuracy.

## EXPERIMENT 6

### DESIGN & ANALYSIS OF TELESCOPIC OPAMP WITH DIFFERENTIAL INPUT

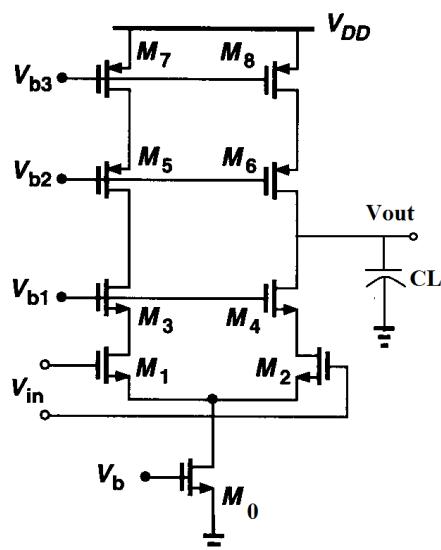
#### **OBJECTIVES:**

- i. To design and analyze a Telescopic OpAmp with differential input for the given specifications.
- ii. To analyze using PDM method and calculate the node and gate voltages.
- iii. To perform dc analysis and obtain the dc operating points, small signal parameters and node voltages.
- iv. To perform ac analysis and obtain dc gain, 3dB frequency and unity gain frequency.
- v. Estimate gain and output impedance of the circuit.

#### **SPECIFICATIONS**

Parameters	Specified Values
Supply Voltage	1.8 V
Gain	40 dB
ICMR <sup>-</sup>	0.8 V
ICMR <sup>+</sup>	1.6 V
Load Capacitance	10pF
Slew Rate	5 V/ $\mu$ sec
Gain-Band width product	5MHz

#### **CIRCUIT DIAGRAM**



**Fig: 1 Telescopic OpAmp with differential input**

## THEORY

An operational amplifier (or an op-amp) is an integrated circuit (IC) that operates as a voltage amplifier. An op-amp has a differential input. That is, it has two inputs of opposite polarity. An op-amp has a single output and a very high gain, which means that the output signal is much higher than input signal.

An operational amplifier (often op-amp or OpAmp) is a DC coupled high gain electronic voltage amplifier with a differential input and a single-ended output. In this configuration an op-amp produces an output potential (relative to circuit ground) that is typically hundreds of thousands of times larger than the potential difference between its input terminals. Operational amplifiers had their origins in analog computers, where they were used to perform mathematical operations in many linear, non-linear, and frequency-dependent circuits.

In order to achieve a high gain, the differential cascode topologies are used. These circuits increase gain at the cost of output swing and additional poles. These configurations are called telescopic cascode OpAmp.

A fully differential telescopic operational amplifier design is presented which achieve both high dc gain and high unity-gain frequency. Trade-offs among such factors as bandwidth, gain, phase, margin, bias current, signal swing, slew rate, and power are made evidently. The two-stage operational amplifier achieves broader unity bandwidth and increases the DC gain.

The gain and output swing equations are given by:

$$A_v \approx g_{m1}[(g_{m3}r_{O3}r_{O1})||(g_{m5}r_{O5}r_{O7})]$$

$$\text{Output swing} = 2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + |V_{OD5}| + |V_{OD7}|)]$$

## EXPERIMENTAL PROCEDURE

### Telescopic OpAmp with differential input using PDM method: -

1. Draw the circuit as shown in Fig 1 with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width 2um initially. Select Vdc voltage with DC voltage as 1.8 V for the Vdd. The value at the input of gate terminal of the NMOS and PMOS are calculated using the formula and PDM method.
2. Draw the basic circuit with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width W initially. Select Vdc voltage with DC voltage as 660mV, 0V and 180mV for gate, source and drain of NMOS M0. Then 760mV, 180mV and 360mV as gate, source and drain of NMOS M1(M2) and 940mV, 360mV and 1.106V as gate, source and drain terminal for PMOS M3(M4).

Then 700mV, 1.31V and 1.106mV as gate, source and drain of PMOS M5(M6) and 1.15V, 1.8V and 1.31V as gate, source and drain terminal for PMOS M7(M8).

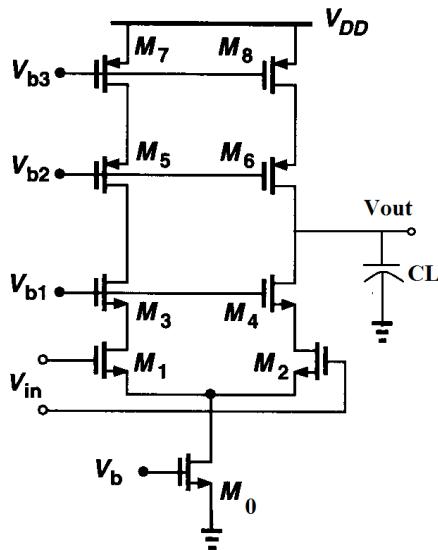
The value at the input of gate terminal of the NMOS and PMOS are calculated using the formula and PDM method.

From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.

3. In the Analog Environment window select "Variables → Copy from Cell view". And give the values of W as 2um. Then in the window select “Analyses → Choose”. Select “dc” and then “Component Parameter”. Choose “Select Component” and select NMOS / PMOS and select 'simW' option then set start and stop voltages as 400n to 50u to get graph of  $I_D$  vs W.
4. Then select “Outputs → To Be Plotted → Select Drain node for  $I_D$  current in Schematic” to set the y-axis for NMOS and source current for PMOS. Then run the simulation to see the results.
5.  $I_D - W$  graph is obtained for different values of W. The W value corresponding to a  $I_D$  value of 50uA and 25uA currents for respective graphs and transistors is noted down.
6. The calculated W values are replaced for the PMOS and NMOS transistors in Fig 1 and dc analysis is performed with only 'Save dc operating point option' and they are verified to operate in saturation region only. Then the dc operating point and node voltages for drain, gate, body and source terminals are noted down.
7. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS / PMOS". This gives the values of all small signal parameters of NMOS / PMOS which  $g_m$ ,  $g_{ds}$ , self-gain is noted down.
8. Then perform the ac analysis with  $V_{sin}$  voltage source at input (Dc voltage provided by M0, Ac magnitude 1V, frequency 10kHz and amplitude 5mV). Then perform the ac analysis with frequency range from 1 to 10G Hz. And view the plot in db20 scale by "Selecting the graph → Right Click → Dependent Modifier → db20".
9. Then select “Outputs → To Be Plotted → Select Output voltage wire for  $V_{out}$  in Schematic” to set the y-axis. Observe the plot for gain and note down the 3db frequency and unity gain frequency.
10. Then for transient analysis response select “Outputs → To Be Plotted → Select  $V_{out}$  and  $V_{in}$  voltage wires in Schematic”. Then run the simulation to see the results. And note down output swing.
11. Then to verify the slew rate the negative terminal of telescopic OpAmp is shorted to output line. i.e., gate of M2 transistor is shorted to  $V_{out}$  line and a vpwl signal i.e., a step input is applied at gate of transistor M1 with  $V_1$  as 0V and  $V_2$  as 1.8V. Then a

transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic and input wire for M1”. In the plot for Vout versus time axis calculate the slope which gives the slew rate required to be verified.

## DESIGN & ANALYSIS



**Fig 2: Telescopic OpAmp with differential input**

### Using PDM method: -

From the given specifications we have  $C_L$  value as 10pF and slew rate 5V/ usec we can estimate the max current as  $I_{max}$  given by slew rate  $\times C_L$  and the value is 50 uA, so we choose a current of 50uA for design which splits as 25 uA for each branch.

The value of  $V_x$  is chosen to be 10% of  $V_{DD}$  that is 180mV. NMOS transistor M0 is the current source transistor with value 660mV (using  $V_{ov} + V_t$ ). And the gate of input transistors M1 and M2 is chosen to be 900mV.

The  $V_b$  values to be given for other transistors are derived from the algorithm to find the dc operating point values. The node voltages to be given for the NMOS and PMOS transistors are calculated using PDM technique. Then using steps in procedure all the required values are noted down.

For the design and calculation of gate bias and source voltage of NMOS transistor:  $n_n$  is number of NMOS transistors in stack,  $V_{top,n}$  is drain potential of top most NMOS transistor and  $V_{bottom,n}$  is source potential of bottom most NMOS transistor .

$$V_{S,n}[u] \longrightarrow [u \times (V_{top,n} - V_{bottom,n})] / n_n$$

$$V_{G,n}[u] \longrightarrow V_{S,n}[u] + V_{TH,n}[u] + 0.05 V_{DD}$$

For the design and calculation of gate bias and source voltage of PMOS transistor:  $n_p$  is number of PMOS transistors in stack,  $V_{top,p}$  is source potential of top most PMOS transistor and  $V_{bottom,n}$  is drain potential of bottom most PMOS transistor .

$$\begin{aligned} V_{S,p}[u] &\longrightarrow V_{DD} - [u \times (V_{top,p} - V_{bottom,p})] / n_p \\ V_{G,p}[u] &\longrightarrow V_{S,p}[u] - V_{TH,p}[u] - 0.05 V_{DD} \end{aligned}$$

The gain and output swing equations are given by:

$$A_v \approx g_m 1 [(g_m 3 r_o 3 r_o 1) \parallel (g_m 5 r_o 5 r_o 7)]$$

$$\text{Output swing} = 2[V_{DD} - (V_{OD1} + V_{OD3} + V_{CSS} + |V_{OD5}| + |V_{OD7}|)]$$

## RESULTS

- (i) Operating points for Telescopic OpAmp with differential input using PDM method: -

Transistor	<b>V<sub>S</sub>(V)</b>	<b>V<sub>D</sub> (V)</b>	<b>V<sub>G</sub> (V)</b>	<b>V<sub>B</sub> (V)</b>
<b>M0</b>	0	300.06m	690m	0
<b>M1 (M2)</b>	300.06m	601.17m	900m	300.06m
<b>M3 (M4)</b>	601.17m	934.659m	1.29	601.17m
<b>M5 (M6)</b>	1.350565	934.659m	660m	1.350565
<b>M7 (M8)</b>	1.8	1.350565	1.11	1.8

The small signal parameters are as follows:

Transistor	I <sub>D</sub> ( $\mu$ A)	g <sub>m</sub> ( $\mu$ A/V)	g <sub>ds</sub> ( $\mu$ A/V)	r <sub>o</sub> (K ohm)	Self-gain (g <sub>m</sub> r <sub>o</sub> )
<b>M0</b>	50.0033	412.766	18.2014	65.7834	27.1531
<b>M1 (M2)</b>	25.0017	202.407	7.88961	126.749	25.6548
<b>M3 (M4)</b>	25.0017	204.395	6.19082	161.53	33.0159
<b>M5 (M6)</b>	25.0017	184.033	3.78248	264.377	48.6540
<b>M7 (M8)</b>	25.0017	184.734	3.37267	296.501	54.7738

## DISCUSSIONS

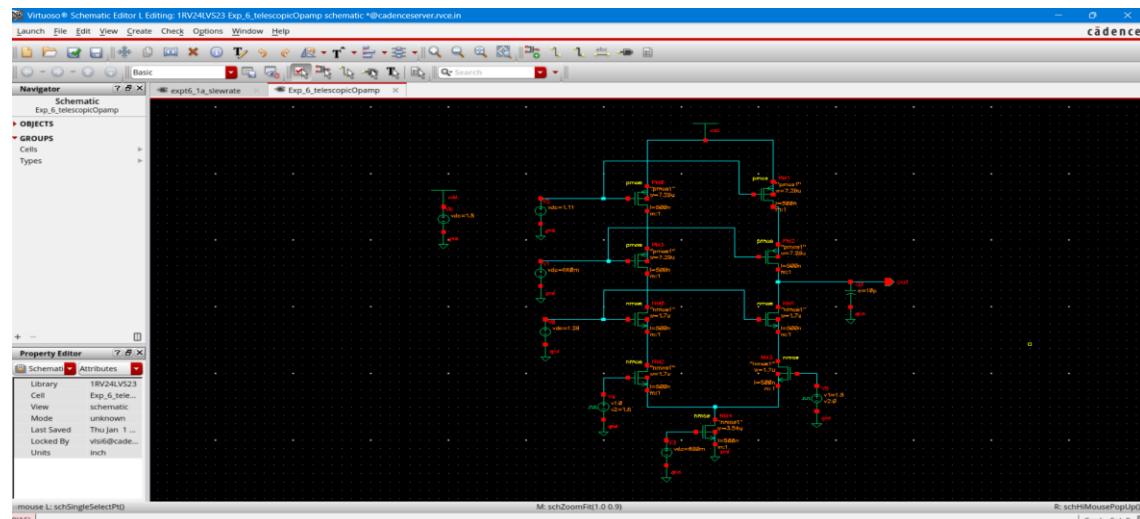
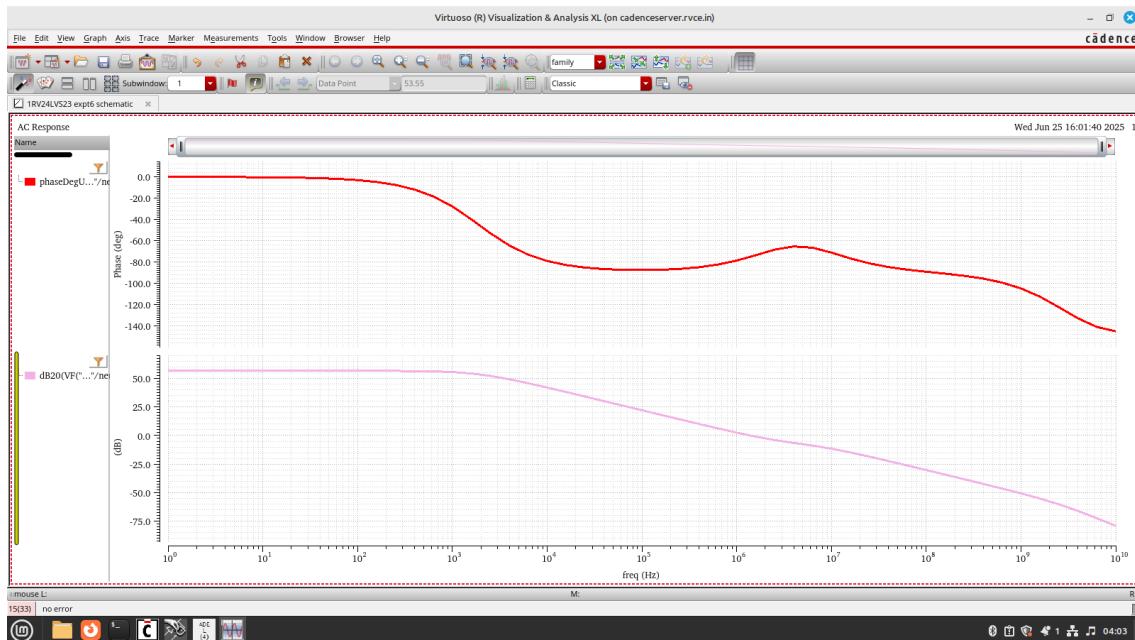


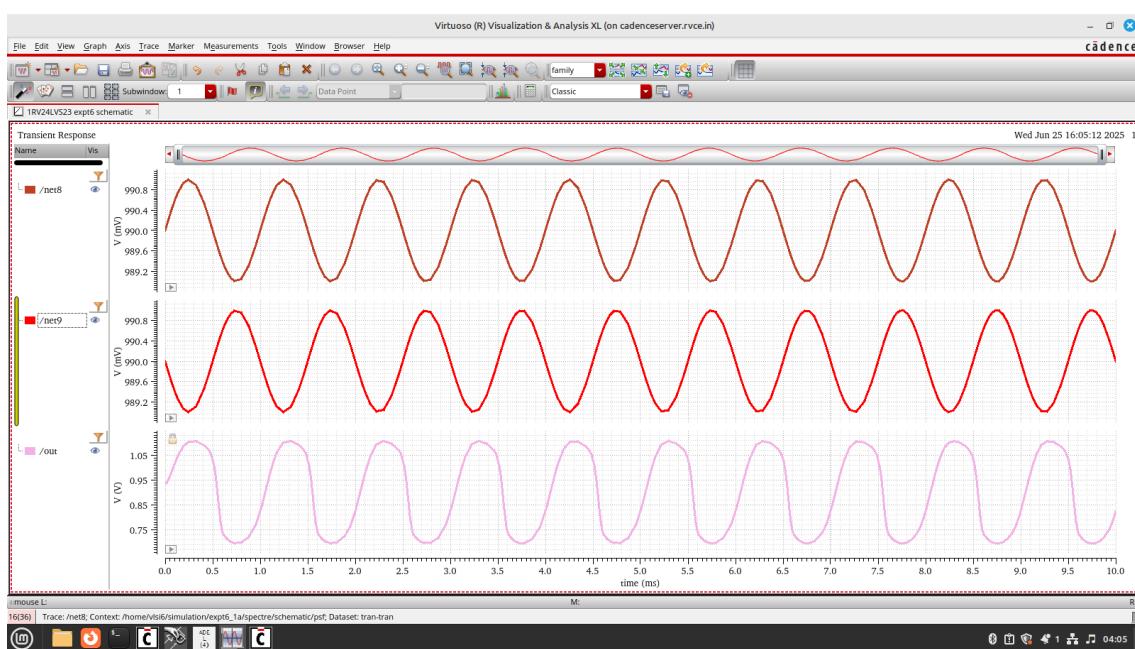
Fig 3: Telescopic OpAmp circuit

Initially the DC analysis is performed for  $I_D$  - W parameter and the value of W for NMOS and PMOS are found and placed in the Telescopic OpAmp circuit. The W values found are 7.28  $\mu\text{m}$  for PMOS PM7 (PM8), PM5 (PM6) and \_1.699\_  $\mu\text{m}$  for NMOS NM3 (NM4), \_1.699\_  $\mu\text{m}$  for NMOS NM1 (NM2) and \_3.53\_  $\mu\text{m}$  for NMOS M0. The transistors are verified to be operating in saturation region.



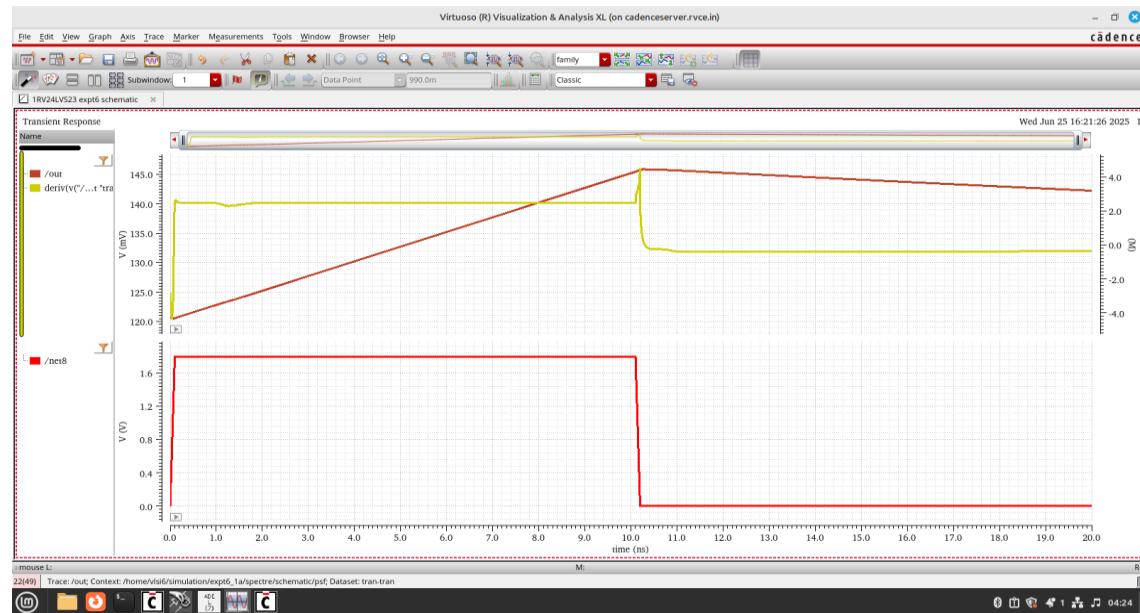
**Fig 4:  $A_v$  (dB 20) – frequency characteristics for Telescopic OpAmp with differential input using PDM method**

Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) – frequency and the frequency range are given from 1-10GHz. The gain is \_51.32\_ dB and 3dB frequency is \_7.607\_ KHz and UGF is \_2.989\_ KHz.



**Fig 5: Transient Analysis for Telescopic OpAmp with differential input using PDM method**

The plot of output and input voltage of the input transistor in the Telescopic OpAmp with differential input is obtained by the transient analysis. The peak-to-peak voltage of both the input and output waveforms are calculated to obtain output swing which is 1.095 V.



**Fig 6: Slew rate calculation for Telescopic OpAmp with differential input**

Then a transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for  $V_{out}$  in Schematic and input wire for  $M1$ ”. Using the plot for  $V_{out}$  versus time axis calculate derive plot which gives the slew rate required to be verified. The slew rate is found to be 2.49623 V/ $\mu$ s.

## INFERENCE

The design and analysis of a Telescopic OpAmp with differential input were performed using the PDM (Point-Driven Method) and verified to ensure they meet the given specifications. The specifications included a gain of 40 dB, a load capacitance of 10 pF, a slew rate of 5 V/ $\mu$ s, and a gain-bandwidth product of 5 MHz.

The gate terminal voltages of the NMOS and PMOS transistors were calculated based on the threshold voltage ( $V_t$ ), tail voltage, and overdrive voltage using the PDM approach. The transistor widths were chosen using ID vs W plots to ensure operation in the saturation region with a total tail current of 50  $\mu$ A (25  $\mu$ A per branch).

DC analysis was used to extract operating points and small-signal parameters such as  $gm$ ,  $r_o$ , and node voltages. AC analysis was performed to determine the gain and frequency performance. The simulated gain was 51.32 dB with a 3 dB frequency of 7.6 kHz and a unity gain frequency of 2.989 MHz. Transient analysis was done to find the output swing and slew rate, which was measured as 2.49 V/ $\mu$ s.

While the Telescopic OpAmp offers high gain and is suitable for low-power analog systems, it has limited voltage swing due to stacked transistors and headroom loss in the current source. The PDM method is simple for initial design but lacks precision. For designs requiring higher output swing and better flexibility, a Folded Cascode OpAmp is often preferred.

## EXPERIMENT 7

### DESIGN & ANALYSIS OF TWO STAGE OPAMP

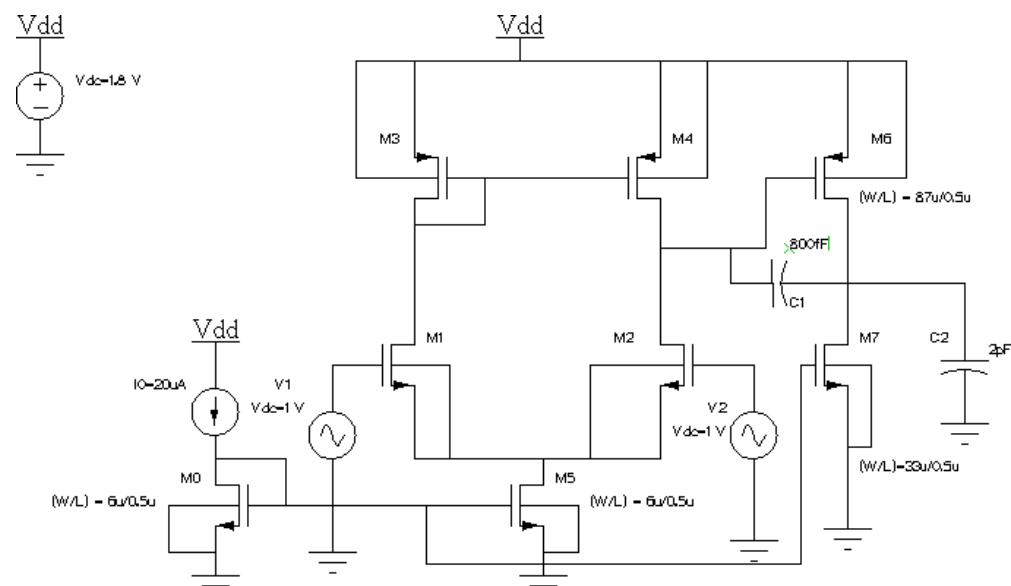
#### OBJECTIVES:

- i. To design and analyze a two stage OpAmp using NMOS differential pair for the given specifications.
- ii. To perform dc analysis and obtain the dc operating points, small signal parameters and node voltages.
- iii. To perform ac analysis and obtain dc gain, 3dB frequency and unity gain frequency.
- iv. To estimate phase margin.

#### SPECIFICATIONS

Parameters	Specified Values
Supply voltage	1.8 V
Power dissipation	< 300 mW
Small signal gain	>60dB
Slew rate	20 V/ $\mu$ s
GBW	30 MHz
Load capacitance	2 pF
ICMR	0.8 to 1.6 V

#### CIRCUIT DIAGRAM



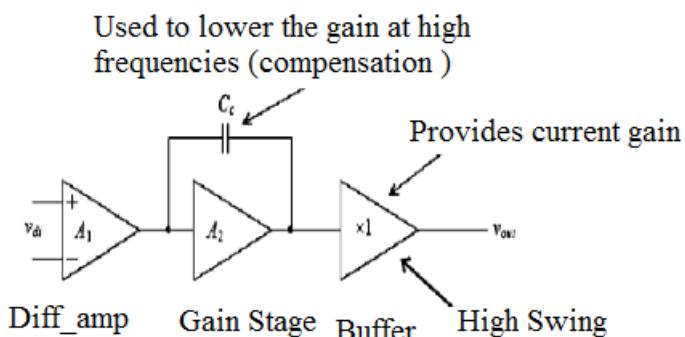
**Fig 1: Circuit diagram of Two-stage Opamp with frequency compensation**

## THEORY

An operational amplifier (or an op-amp) is an integrated circuit (IC) that operates as a voltage amplifier. An op-amp has a differential input. That is, it has two inputs of opposite polarity. An op-amp has a single output and a very high gain, which means that the output signal is much higher than input signal.

An operational amplifier (often op-amp or opamp) is a DC coupled high gain electronic voltage amplifier with a differential input and a single-ended output. In this configuration an op-amp produces an output potential (relative to circuit ground) that is typically hundreds of thousands of times larger than the potential difference between its input terminals. Operational amplifiers had their origins in analog computers, where they were used to perform mathematical operations in many linear, non-linear, and frequency-dependent circuits.

Single stage Op-Amps give a considerable amount of gain by cascading at the load and input side but this limits the output swings. However, these circuits can be used for considerable number of applications. For high end applications we prefer two stage opamp, where in first stage mainly contributes for gain and second stage though it increases gain but it mainly concentrates on increasing the swing.



**Fig 2: Two-stage Opamp components**

There is no constraint on considering the type of amplifier that can be used for each stage. Various amplifiers can be used for the 1<sup>st</sup> stage as well as the 2<sup>nd</sup> stage. Usually, 2<sup>nd</sup> stage is configured as the common source stage so as to allow maximum output swings. As shown in above figure 1 a differential simple amplifier is considered for the first stage whose swing is increased by connecting a Common-source PMOS amplifier.

The gain of the first stage can also be increased by replacing the load in cascode manner. The gain of first and second stage can be given as  $gm_2 * (r_{02} \parallel r_{04})$  and  $gm_7 * (r_{06} \parallel r_{07})$  respectively. The only problem with two-stage OpAmp is the inclusion of another pole and due to which the stability is not guaranteed, this is the reason why the OpAmp with several stages are not widely used as each stage results in inclusion of a pole. The solution for this problem can be given by using frequency compensation techniques.

## EXPERIMENTAL PROCEDURE

1. Draw the circuit as shown in Fig 1 with length of NMOS and PMOS as 500nm (2 to 3 times of Lmin 180nm) and width according to the design conditions. along with vdd, Vdc, gnd, current sources from analog library.
2. From the cell view select “Launch → ADE L” to open the simulator. Then perform the dc analysis by plugging in the appropriate parameters to obtain the simulated graphs.
3. Dc analysis is performed with only 'Save dc operating point option' and they are verified to operate in saturation region only. Then the dc operating point and node voltages for drain, gate, body and source terminals are noted down.
4. After DC Analysis in the Analog Environment window select "Results → Print → DC operating point and select NMOS / PMOS". This gives the values of all small signal parameters of NMOS / PMOS which  $g_m$ ,  $g_{ds}$ , self-gain is noted down.
5. Then perform the ac analysis with Vsine voltage source at input (DC voltage 900mV and Ac magnitude 1V). Then perform the ac analysis with frequency range from 1 to 10G Hz. And view the plot in db20 scale by " Selecting the graph → Right Click → Dependent Modifier → db20".
6. Then select “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic” to set the y-axis. Observe the plot for gain and note down the 3db frequency and unity gain frequency.
7. Then a transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic and input wire for M1”. In the plot calculate the peak-to-peak voltage swing of the output.
8. Using AC analysis response plot the graph phase vs frequency to get phase margin and gain bandwidth.

## RESULTS

- (i) Operating points for Differential Amplifier with current source load using PDM method: -

<b>Transistor</b>	<b>V<sub>S</sub> (V)</b>	<b>V<sub>D</sub> (V)</b>	<b>V<sub>G</sub> (V)</b>	<b>V<sub>B</sub> (V)</b>
<b>M1(M2)</b>	443.354m	878.929m	1.04	443.354m
<b>M3 (M4)</b>	1.8	878.929m	878.929m	1.8
<b>M5</b>	0	443.554m	596.991m	0
<b>M6</b>	1.8	830.864m	878.929m	1.8
<b>M7</b>	0	830.864m	596.991m	0

The small signal parameters are as follows:

Transistor	$I_D$ (uA)	$g_m$ (A/V)	$g_{ds}$ (A/V)	$r_o$ (K ohm)	Self-gain ( $g_m r_o$ )
<b>M1 (M2)</b>	10.8824	137.577u	1.48847u	673.531K	92.662
<b>M3 (M4)</b>	10.8824	40.8216u	716.64n	1.3954M	56.962
<b>M5</b>	21.7647	279.914u	2.83962u	352.195K	91.016
<b>M6</b>	21.7647	82.0277u	1.36066u	734.936K	60.285
<b>M7</b>	21.7647	82.0277u	1.36066u	734.936K	60.285

## DISCUSSIONS

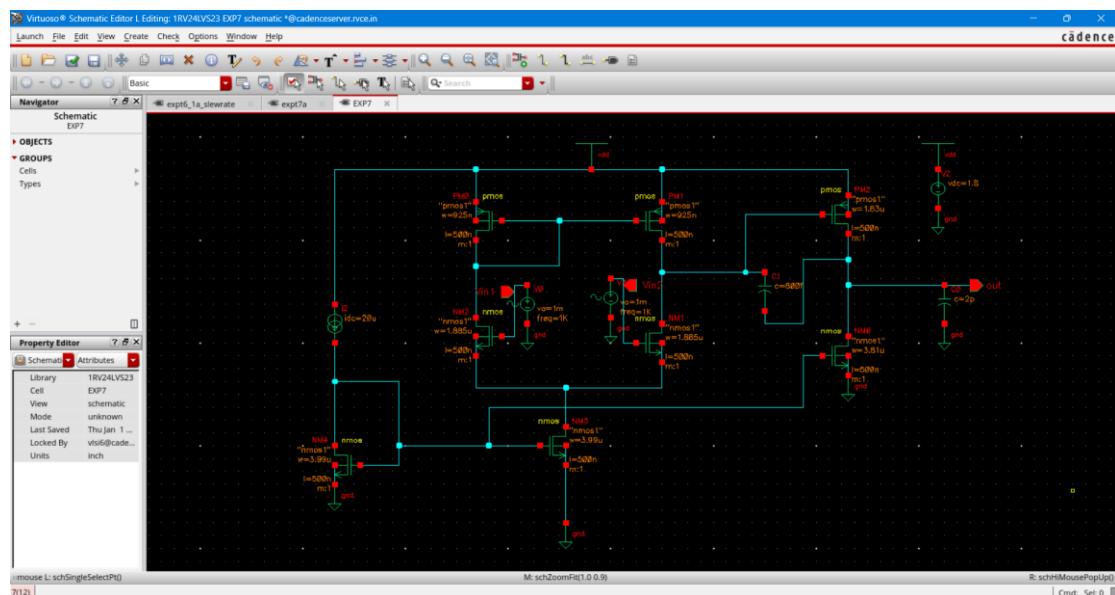


Fig 3: Schematic of a Two Stage Opamp

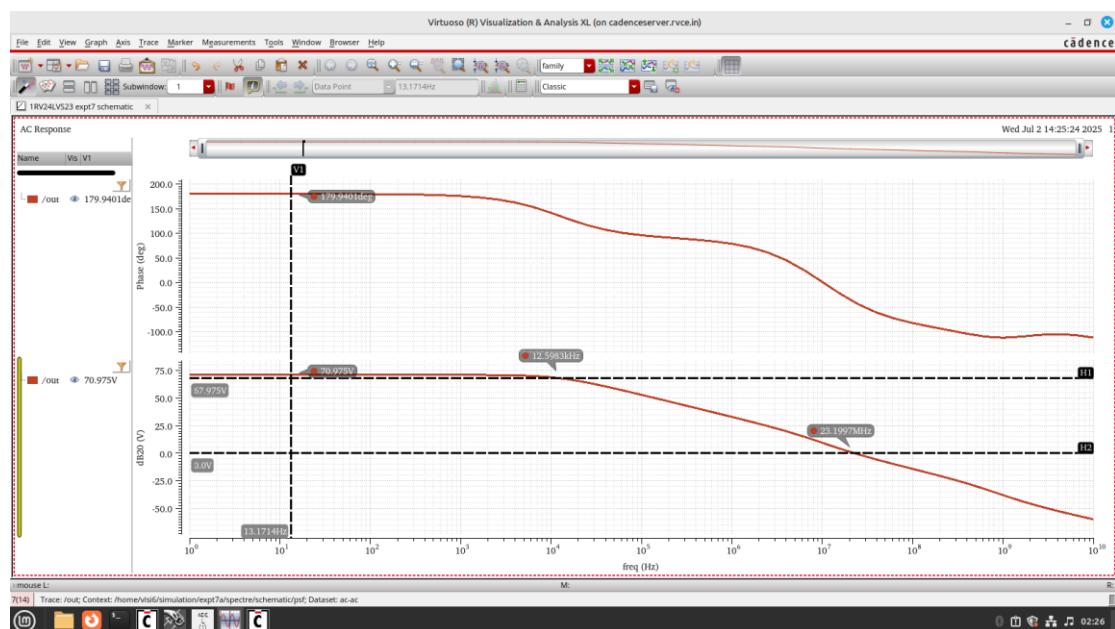
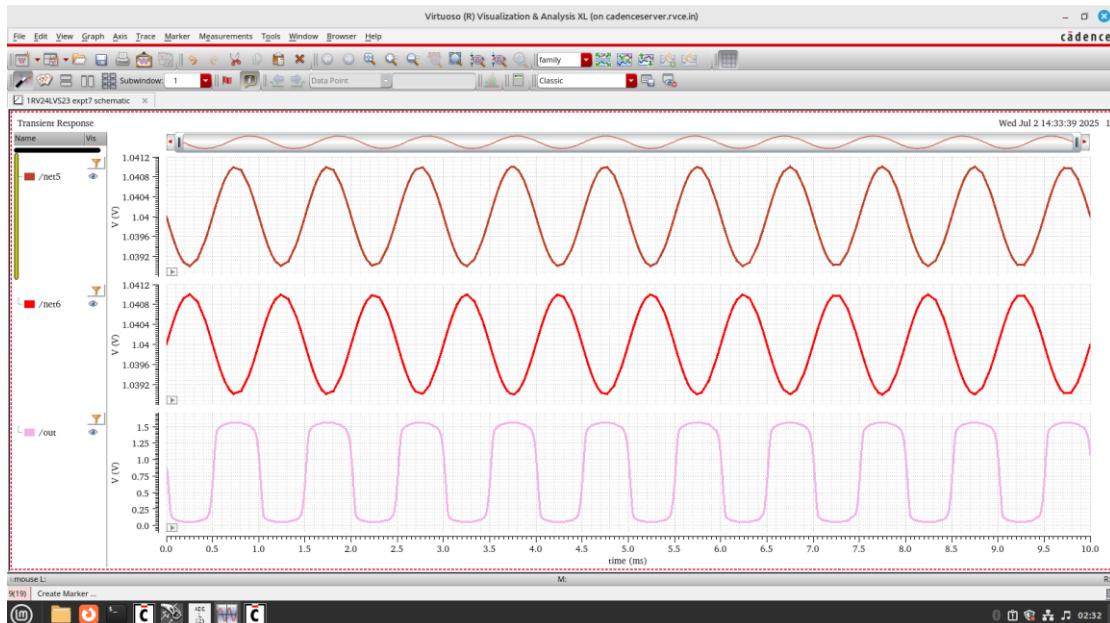


Fig 4:  $A_v$  (dB 20) – frequency characteristics for two stage opamp

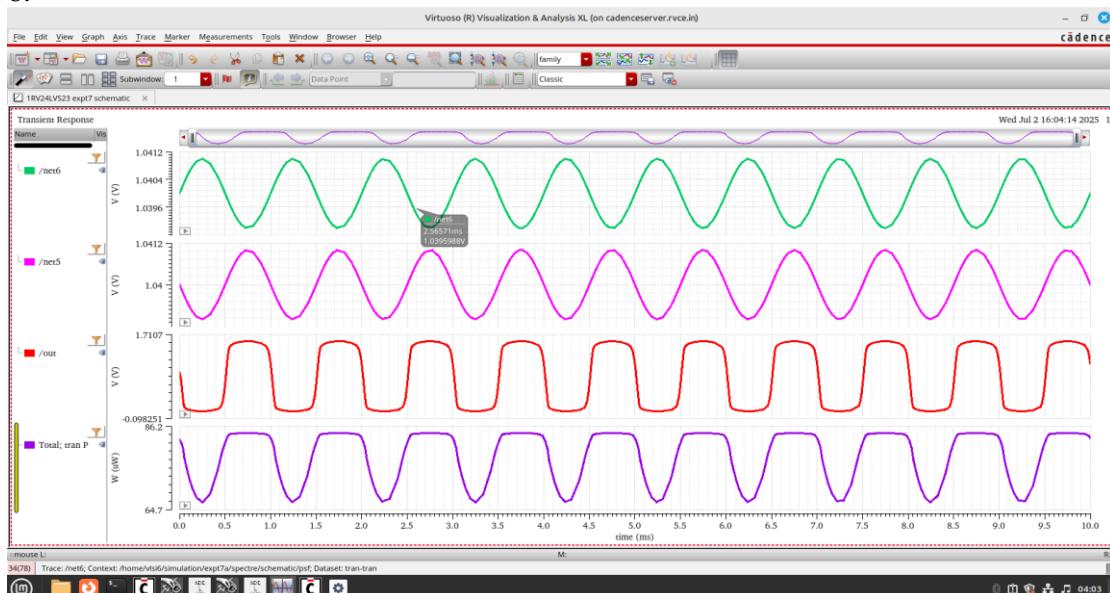
Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) – frequency and the frequency range are given from 1-10GHz. The gain is 73.215 dB and 3dB frequency is 9.993 KHz and UGF is 22.398 MHz.

Then a transient analysis is performed with “Outputs → To Be Plotted → Select Output voltage wire for Vout in Schematic and input wire for M1”. The plot of output and input voltage of the two stage OpAmp is obtained by the transient analysis. The peak-to-peak voltage of output waveform is calculated to obtain output swing which is 1.65 V. It is as shown in figure 4.

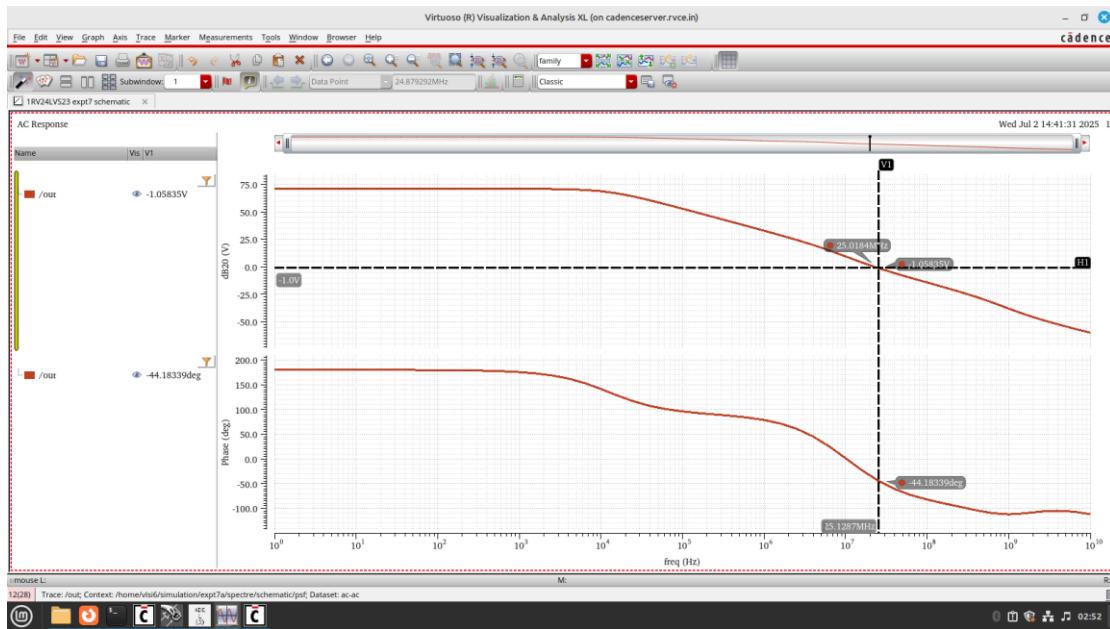


**Fig 5: Transient Analysis for Two stage OpAmp**

Then a transient analysis is performed with save all power option. After transient analysis using results browser the plot of power consumed for the whole circuit is plotted and average value is calculated. It is found to be 73.3 uW which is less than the designed value 300 mW.Hence power constraint is satisfied and plot is shown in Figure 6.



**Fig 6: Power analysis of two stage OpAmp**



**Fig 7: Phase Margin Plot**

Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) – frequency and the frequency range are given from 1Hz-50GHz. The phase margin plot of two stage OpAmp is as done using phase margin plot which is as shown in figure 7. It has a phase margin of  $140.4353^\circ$ .

## INFERENCE

The design and analysis of a Two-Stage Operational Amplifier (OpAmp) were performed using a differential input NMOS stage followed by a PMOS gain stage. The design met the given specifications such as gain  $> 60$  dB, slew rate of  $20 \text{ V}/\mu\text{s}$ , GBW of  $30 \text{ MHz}$ , and power dissipation  $< 300 \mu\text{W}$ . The circuit was built with a compensation capacitor for stability, and transistor sizing was done using a minimum channel length of  $500 \text{ nm}$ .

DC analysis was performed to verify that all transistors operated in the saturation region. The DC operating points and small signal parameters like  $g_m$ ,  $g_{ds}$ , and  $r_o$  were obtained and tabulated. From the AC analysis, the amplifier achieved a gain of  $73.2$  dB, a  $3$  dB frequency of  $9.993 \text{ kHz}$ , and a unity gain frequency of  $22.39 \text{ MHz}$ . These results confirmed that the gain and bandwidth specifications were satisfied.

Transient analysis showed a peak-to-peak output swing of  $1.65 \text{ V}$ , and power analysis confirmed a low average power consumption of  $73.3 \mu\text{W}$ , which is well within the given specification. The phase margin was calculated to be  $140.4^\circ$ , indicating a highly stable amplifier, although such high margin may slow down the time response.

The two-stage OpAmp offers high gain, good output swing, and low power operation. However, it comes with reduced bandwidth and a slower response. For applications requiring faster settling time or higher bandwidth, a trade-off with power and area may be needed, or alternative topologies like folded cascode can be considered.

## EXPERIMENT 8

### DESIGN & ANALYSIS OF BANDGAP REFERENCE

#### OBJECTIVES:

- i. To design and analyze a Bandgap reference for the given specifications.
- ii. To perform dc analysis and obtain the dc operating points and node voltages.
- iii. To perform dc analysis over temperature and observe the variation of the reference.
- iv. Estimate the average variation over a temperature range.

#### SPECIFICATIONS

Parameters	Specified Values
Supply Voltage	3.3 V
DC bias current	5 $\mu$ A
Number of diodes	2

#### CIRCUIT DIAGRAM

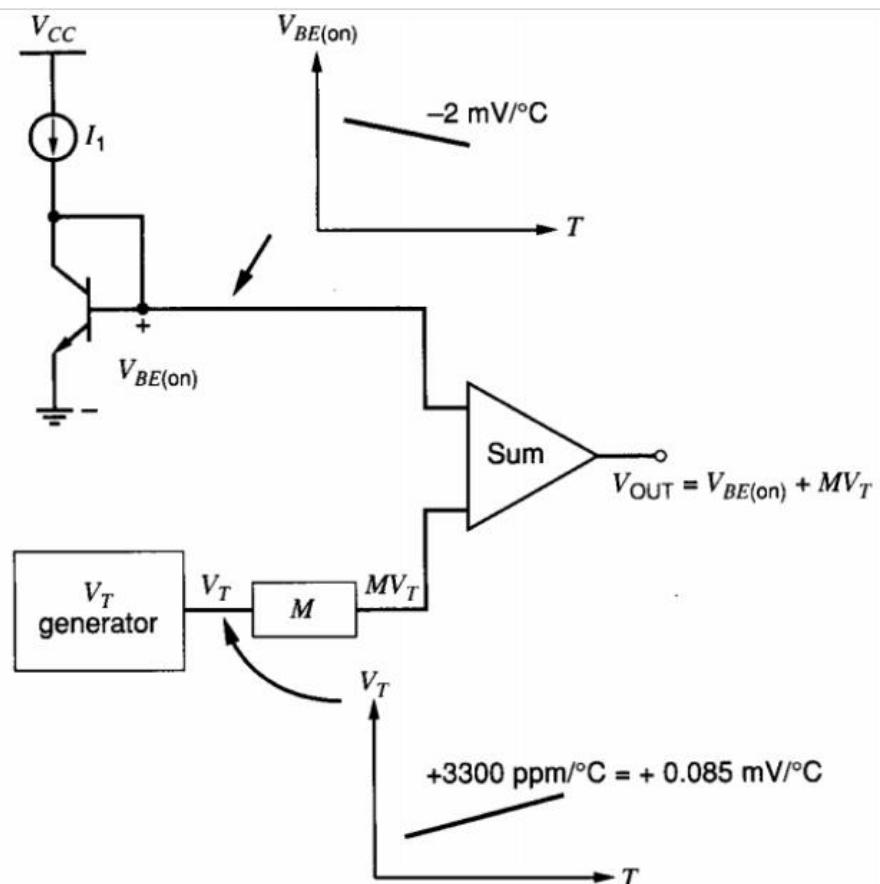


Fig 1: Bandgap Reference generation

## THEORY

In Figure 1, the base-emitter voltage has a temperature coefficient of  $-2 \text{ mV}/^\circ\text{C}$  and easily concluded that  $Mk/q$  should be  $2 \text{ mV}/^\circ\text{C}$ . To be more accurate, we should express the base-emitter voltage in terms of device parameters and use the obtained equations to calculate the factor M. The final result of the analysis which gives the output voltage as:

$$V_{\text{OUT}}|_{T=T_0} = V_{G0} + \gamma V_{T0}$$

$V_{G0}$  is the band-gap voltage of silicon, which is  $1.205 \text{ V}$ .  $\gamma$  is a parameter related to the doping level in the base.  $T_0$  denotes the temperature at which the temperature coefficient of the bandgap reference is set to zero. Hence, the thermal voltage,  $V_{T0}$ , and the bandgap output,  $V_{\text{OUT}}|_{T=T_0}$ , are considered at  $T=T_0$ . Assume that the bandgap output is set to zero at  $T_0=300\text{K}$ . Hence, we have  $V_{T0}=26\text{mV}$ . Assuming a typical value of  $\gamma = 3.2$ , we obtain

$$V_{\text{OUT}}|_{T=300\text{K}} = 1.205\text{V} + (3.2 \times 26\text{mV}) = 1.2882\text{V}$$

As we can see the output voltage of a normal bandgap reference is close to the bandgap voltage of silicon, explaining the name given to this type of voltage reference.

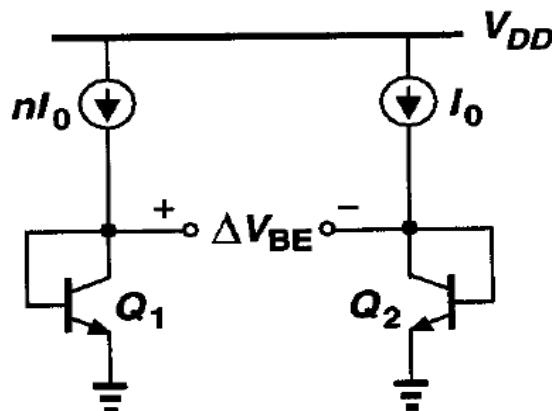


Fig 2: PTAT generation

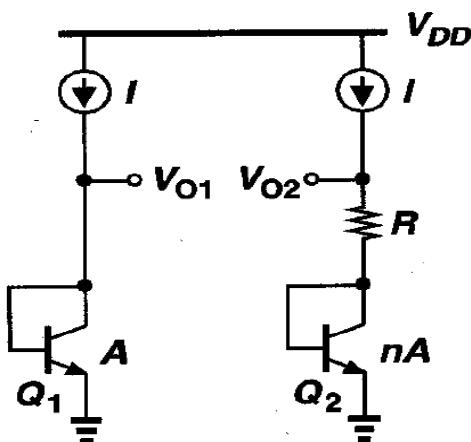


Fig 3: Conceptual generation of BGR

The figures 2, 3 show the generation of CTAT, PTAT and conceptual generation of temperature-independent voltage. a bandgap reference needs to generate a voltage equal

to the thermal voltage. Instead of generating a voltage equal to  $V_T$ , we can generate a voltage that's proportional to the thermal voltage. However, the proportionality factor should be temperature independent so that we can successfully apply the concepts discussed in the previous section. Let's see if there is an easy way to achieve this. We know that the base-emitter voltage of a BJT is given by the following equation:

$$V_{BE} = V_T \ln(I_c/I_s)$$

where  $I_c$  and  $I_s$  are the collector and the saturation currents, respectively. If  $I_c$  and  $I_s$  were temperature independent, the base-emitter voltage would be equal to  $V_T$  multiplied by the temperature independent factor  $\ln(I_c/I_s)$

However, we know that the proportionality factor is not temperature independent. Let's consider the  $V_{BE}$  difference of two transistors  $Q_1$  and  $Q_2$ :

$$V_{BE1} - V_{BE2} = V_T \ln(I_{c1}/I_{s1}) - V_T \ln(I_{c2}/I_{s2}) = V_T \ln(I_{c1}I_{c2}I_{s2}I_{s1})$$

In this case, we can make the  $V_{BE}$  difference a constant factor of the thermal voltage by making both the collector currents ratio ( $I_{c1}I_{c2}$ ) and the saturation currents ratio ( $I_{s2}I_{s1}$ ) constant. Scaling the emitter areas of the transistors allows us to set the saturation currents ratio. For the collector currents ratio, we can simply use current sources to set the bias current of the transistors. Thus, it is possible to make the  $V_{BE}$  difference a constant factor of the thermal voltage. Bandgap references usually use the  $V_{BE}$  difference of two BJTs to create the “ $V_T$  generator” block in Figure 1.

The design of R facilitates the design of desired BGR. The drawback of this circuit is that it requires a starting mechanism and is not easy to fabricate.

## EXPERIMENTAL PROCEDURE

1. Draw the circuit of the conceptual BGR in cadence virtuoso schematic.
2. Evaluate the values of R and R1 to establish the required reference voltage.
3. Assign the values of the resistors in the schematic.
4. Provide required DC bias through voltage and current sources.
5. Save the schematic entry and check for any errors and warnings.
6. Remove the same if encountered any errors.
7. Perform DC analysis by choosing the DC option in analysis window and saving the DC operating point.
8. Run the DC analysis to obtain the output DC voltage.
9. Perform DC analysis over temperature to measure the variation of the voltage over temperature range.
10. Measure the slope and compute the average variation for the given temperature range.

## DESIGN & ANALYSIS

The conceptual BGR should have ideally no variation over temperature. The BGR is designed as follows.

$$V_{ref} = \alpha_1 V_{ptat} + \alpha_2 V_{ctat} \quad (1)$$

The equation (1) is the design equation for BGR. We can fix the values of  $\alpha_1$  and  $\alpha_2$  to obtain the values of resistors required.

$V_{ref}$  should remain constant w.r.t temperature which implies,

$$\partial V_{ref}/\partial T = 0 \quad (2)$$

From (2), we can rewrite the design equation as,

$$\alpha_1(\partial V_{ptat}/\partial T) + \alpha_2(\partial V_{ctat}/\partial T) = 0 \quad (3)$$

We know the values of slope of CTAT and PTAT. Assuming  $\alpha_2 = 1$ , we get

$$\begin{aligned} \alpha_1(85\mu V/K) + \alpha_2(-1.6mV) &= 0 \\ \alpha_1 &= 18.82 \end{aligned} \quad (4)$$

Using the values of  $\alpha_1$  and  $\alpha_2$ , we can calculate the values of the resistors as follows.

$$I_o R_1 = V_t \ln(N) = (26mV * \ln(2))/5\mu A = 3.6K\Omega$$

$$R_2 = \alpha_1 R_1 / \ln(N) = (18.82 * 3.6K) / \ln(2) = 96.5K\Omega$$

## RESULTS

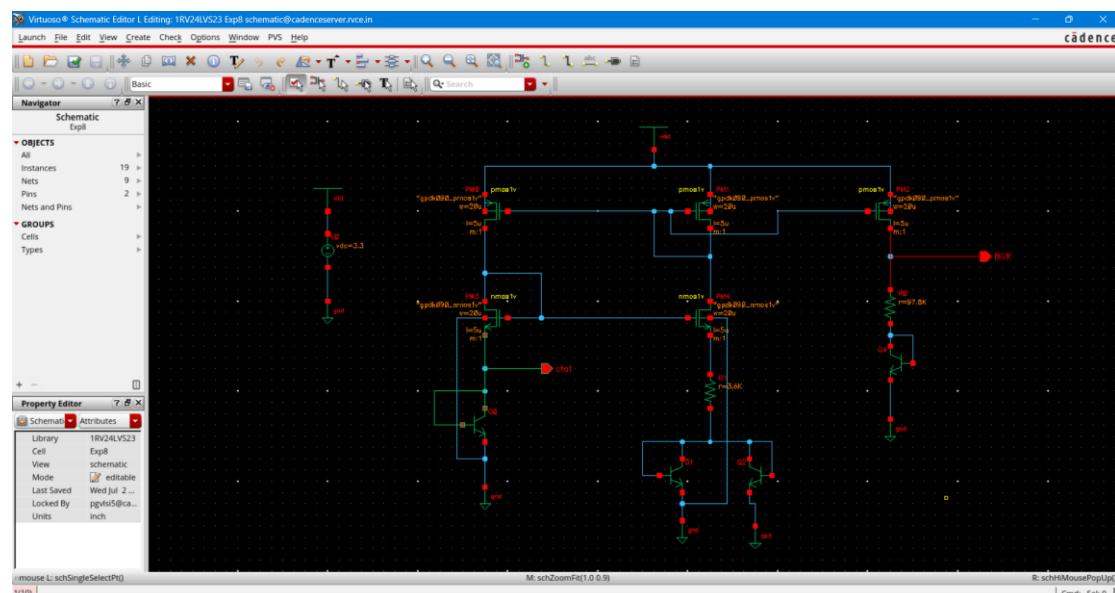
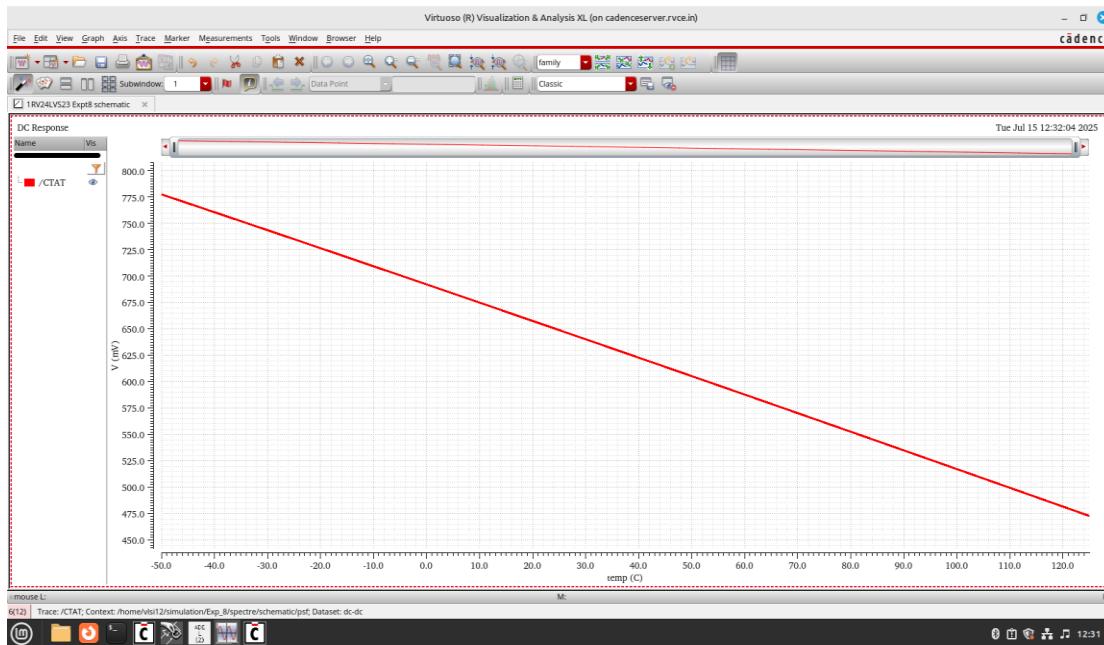


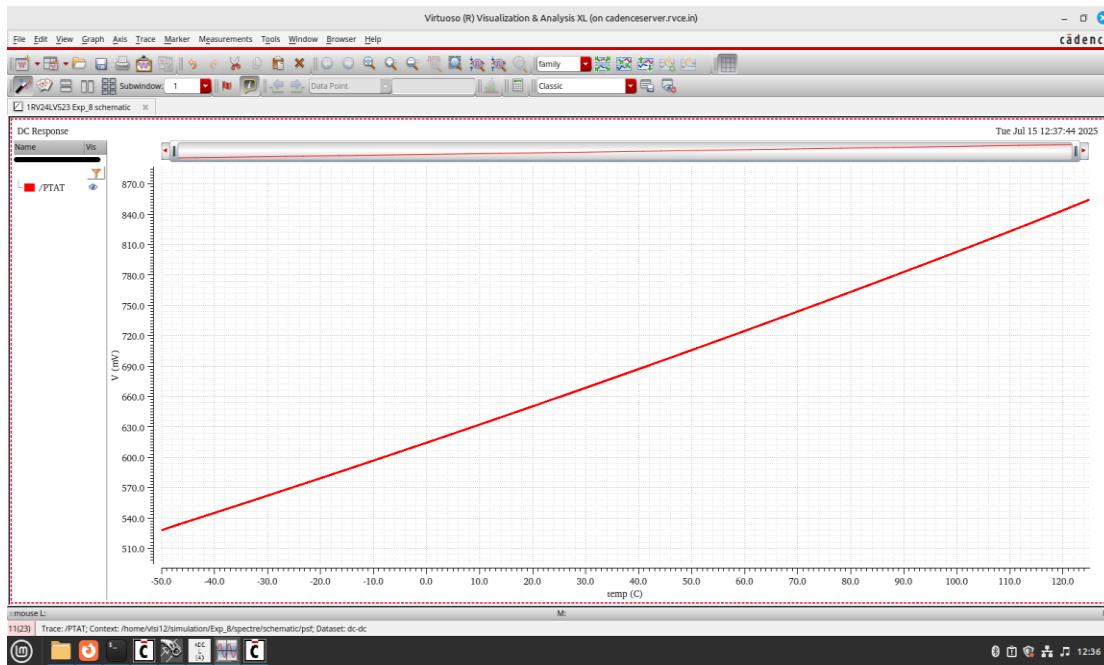
Fig 4. Circuit for BGR

DC analysis of the circuit in Figure 1, provides the below outputs.



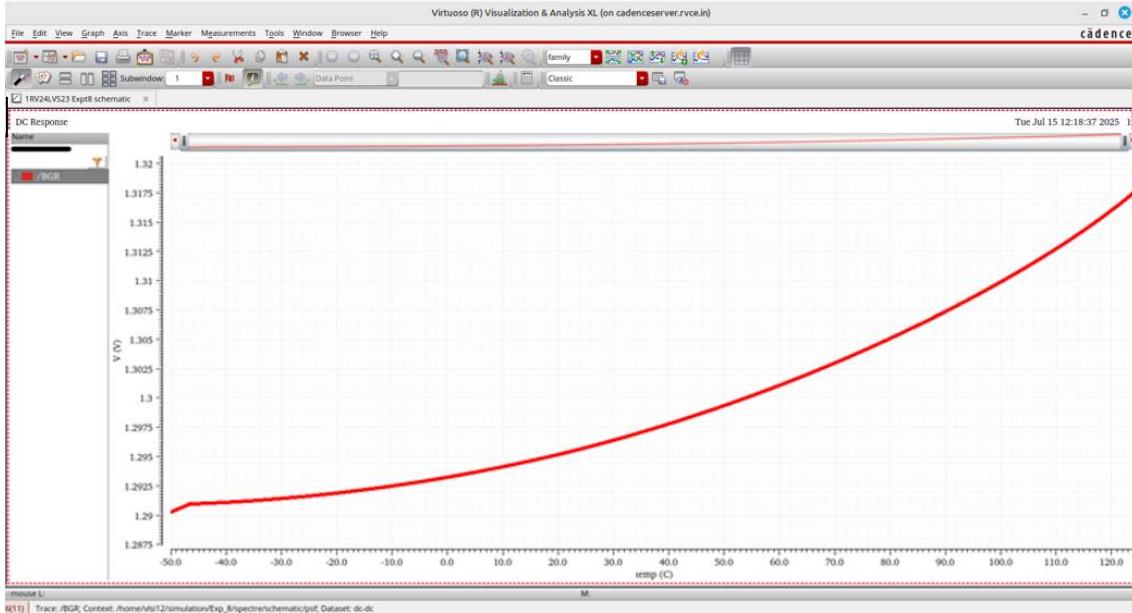
**Fig 5: CTAT curve for BGR circuit**

The Figure 5, shows the CTAT component in the BGR variation over the temperature. The temperature range is 0-125 degree Celsius, the typical process corners in design. The slope of the curve is almost equal to the theoretically calculated slope for CTAT.



**Fig 6: PTAT curve for BGR circuit**

The Figure 6, shows the PTAT component in the BGR variation over the temperature. The temperature range is 0-125 degree Celsius, the typical process corners in design. The slope of the curve is almost equal to the theoretically calculated slope for PTAT.



**Fig 7: BGR curvature**

The Figure 7, represents the BGR output voltage variation with respect to temperature. The circuit provides constant voltage up to second order precision. The constant voltage was obtained by fine tuning the output resistance from the calculated resistance value.

## INFERENCE

The design and analysis of a Bandgap Reference (BGR) circuit were carried out to generate a temperature-independent voltage. The design used a conceptual topology involving CTAT and PTAT components, which were balanced using calculated resistor values. The objective was to achieve a constant output voltage over a wide temperature range using a low bias current of  $5 \mu\text{A}$  and two diodes, with a supply voltage of 3.3 V.

Using theoretical equations, the values of  $\alpha_1$  and  $\alpha_2$  were derived to match the CTAT and PTAT slopes. Based on this, the required resistors were calculated as  $R_1 = 3.6 \text{ k}\Omega$  and  $R_2 \approx 96.5 \text{ k}\Omega$ . A current mirror circuit was implemented using MOSFETs to bias the BGR. The schematic was simulated using Cadence Virtuoso, and DC analysis was performed to obtain operating points and verify the output voltage.

Further, temperature sweep analysis was carried out from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  to observe the behavior of CTAT and PTAT components individually. The BGR output showed minor curvature, and the voltage remained nearly constant across the temperature range. To fine-tune performance, output resistance was adjusted, and a value of  $101 \text{ k}\Omega$  yielded optimal stability in the reference voltage.

The BGR circuit achieved a temperature-stable output using theoretical design and simulation. While the conceptual design is not practical for fabrication due to startup limitations, it demonstrates key principles in precision analog design and highlights the importance of resistor tuning in achieving temperature independence.

## EXPERIMENT 9

### LAYOUT OF CS AMPLIFIER

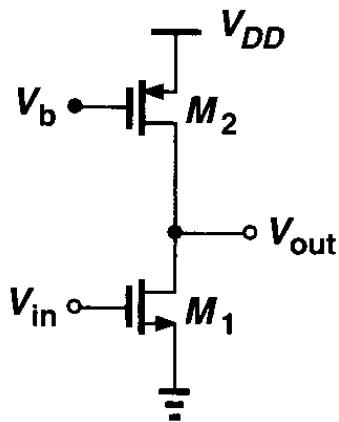
#### OBJECTIVES:

- i. To create layout for a Common Source Amplifier with current source PMOS load
- ii. To perform dc analysis, ac analysis and obtain dc gain, bandwidth and unity gain frequency.
- iii. To perform transient analysis and check gain for a small signal of  $2 \mu\text{Vpp}$ , 1KHz
- iv. Estimate gain and output impedance of both circuits.
- v. Compare pre layout and post layout simulation results

#### SPECIFICATIONS

Parameters	Specified Values
Supply Voltage	1.8 V
Power	$\leq 250 \mu\text{W}$
UGF	150MHz
Load Capacitance	100fF

#### CIRCUIT DIAGRAM



**Fig 1: Common Source amplifier with current source PMOS load**

#### THEORY

Three terminal devices can be used to implement a controlled source. This property makes them suitable to be used in amplifiers. A transistor is an example of a device of this kind. In particular, MOSFET (metal-oxide-semiconductor field-effect transistor) is a widely used three terminal device. The working principle of a MOSFET amplifier is

controlling the current flowing through drain terminal by setting the gate-to-source voltage. This property can be achieved by operating the MOSFET in the saturation (active) region. The common source is the most commonly used MOSFET amplifier. The name “common source” comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and source terminals. In order to cancel the nonlinear relationship of  $V_{GS}$  versus  $I_D$  biasing techniques are used.

In applications requiring a large voltage gain in a single stage, the CS amplifier with resistive load or diode connected load is not sufficient. Because increasing the load resistance limits the output voltage swing. A more practical approach is to replace the load with a current source. Both the transistors will operate in saturation region. Since the total impedance seen at the output node is equal to  $r_{O1} \parallel r_{O2}$ , the gain is

$$A_v = -g_m(r_{O1} \parallel r_{O2}).$$

### **Integrated circuit layout**

Integrated circuit layout, also known IC layout, IC mask layout, or mask design, is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit.

When using a standard process - where the interaction of the many chemical, thermal, and photographic variables are known and carefully controlled - the behaviour of the final integrated circuit depends largely on the positions and interconnections of the geometric shapes. Using a computer-aided layout tool, the layout engineer or layout technician places and connects all of the components that make up the chip such that they meet certain criterion typically: performance, size, density, and manufacturability. This practice is often subdivided between two primary layout disciplines: Analog and Digital.

The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are

- Design Rule Checking (DRC),
- Layout Versus Schematic (LVS),

### **Design Rule Check**

Design Rules are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

### **DRC and LVS**

Design Rule Check (DRC) and Layout Versus Schematic (LVS) are verification processes. Reliable device fabrication at modern deep-sub micron ( $0.13\text{ }\mu\text{m}$  and below) requires strict observance of transistor spacing, metal layer thickness, and power density rules. DRC exhaustively compares the physical netlist against a set of "foundry design rules" (from the foundry operator), then flags any observed violations.

The LVS process confirms that the layout has the same structure as the associated schematic; this is typically the final step in the layout process. The LVS tool takes as an input a schematic diagram and the extracted view from a layout. It then generates a netlist from each one and compares them. Nodes, ports, and device sizing are all compared. If they are the same, LVS passes and the designer can continue. LVS tends to consider transistor fingers to be the same as an extra-wide transistor.

## LAYOUT PROCEDURE

1. Draw the CS amplifier schematic with NMOS and PMOS length as 500nm and width according to value obtained for design specifications. Connect the input and output pins to the schematic and create a symbol for it.
2. Draw a test circuit using the symbol and given sources for vdd and input ports using analog library vdc and vpulse and vsin sources with appropriate values.
3. Perform DC analysis with only save dc operating point and note down the dc operating point, small signal parameters and then perform ac analysis using frequency in the range 1 to 100G and Vout wire. Observe dc gain, unity gain frequency and 3db frequency. These are the pre-layout analysis performed.
4. Launch → layout XL from cs amplifier schematic → create → new layout, view → layout, open using layout editor.
5. Go to Option- display
  - Modify minor spacing = 0.3
  - Major spacing = 0.6
  - X snap spacing = 0.01
  - Y snap spacing = 0.01
6. Go to DRC edit and enable notify in the checkbox.
7. Go to Connectivity → Generate → All from Source In I/O pins tab → Change metal 1 draw to metal 1 pin for the input and output pins. Enable create label and click label Options → height = 0.2.
8. Push all the cells inside boundary box, press shift+F to view the internal structure of the transistors.
9. Tools → create ruler(k) and define height = 60um, cell height is the lowest possible integer multiple of M1 routing grid that accommodates more complex cell such as flip flop or full adder.
10. Select metal 1 layer from Window, create shape → rectangle and draw VDD and GND with width = 1.2um.
11. Create VIA- M1\_PSUB is placed at the origin.
12. Create VIA- M1\_NWELL is placed at the X=0, Y=60 position.

13. Place the PMOS with min 0.2um and max 10um from the PR Boundary (y-axis) and the NMOS with min 0.2um and max 10um from the PR Boundary (y-axis).

14. Choose metal 1 → create wiring → wire

- Connect the source of NMOS to GND.
- Choose the source of PMOS to VDD.
- Short the drains and place Vout pin on it.
- Gate: Select POLY- create Rectangle and place the respective pins on NMOS (Vin) and PMOS (Vb)
- Create Poly\_M1 VIA for gate (poly) and pin (metal) connection.

15. Draw the nwell with height=2/3 of height of cell. And insert additional VIA connections for NMOS and PMOS where distance is more than 10 um.

16. Adjust the PR boundary for cell height and min cell width possible, the width should be multiple of 0.6.

17. Run DRC

To run DRC for the layout, select Assura → Run DRC make sure Technology selected has gpdk180. Select Ok to Run DRC. If any errors then errors, will be displayed. Debug and Run DRC.

18. Run LVS

To run LVS, select on Assura → Run LVS. Check Run. Window should pop up saying that LVS Run was successful. In case of errors, check out the errors with schematic and Run LVS again.

19. RC Extraction

- Go to QRC → setup
- Select spectre and gpdk180 Technology and extraction as RC.
- Go to I/O tab and select reference node to GND.
- Go to QRC → Run. Ensure output view is selected as av\_extracted.
- It creates an av\_extracted view of the cs amplifier. It consists of resistance and capacitance which constitute the analog model of the design.
- 

## POST LAYOUT SIMULATION

1. Go to Virtuoso TAB → New → Cell view → Cell: (cell name should be same as inverter test schematic) → Type: CONFIG → Click on OK.
2. New Config → window → View: schematic Use template: Spectre → Click on Ok.
3. New window POPS up → Select → Inv test schematic → Right click → select cell view: av\_extracted → Save → Open

4. Perform the dc analysis, ac analysis in similar manner performed for the pre layout analysis. Compare these values with those obtained from the pre layout analysis.

## ANALYSIS

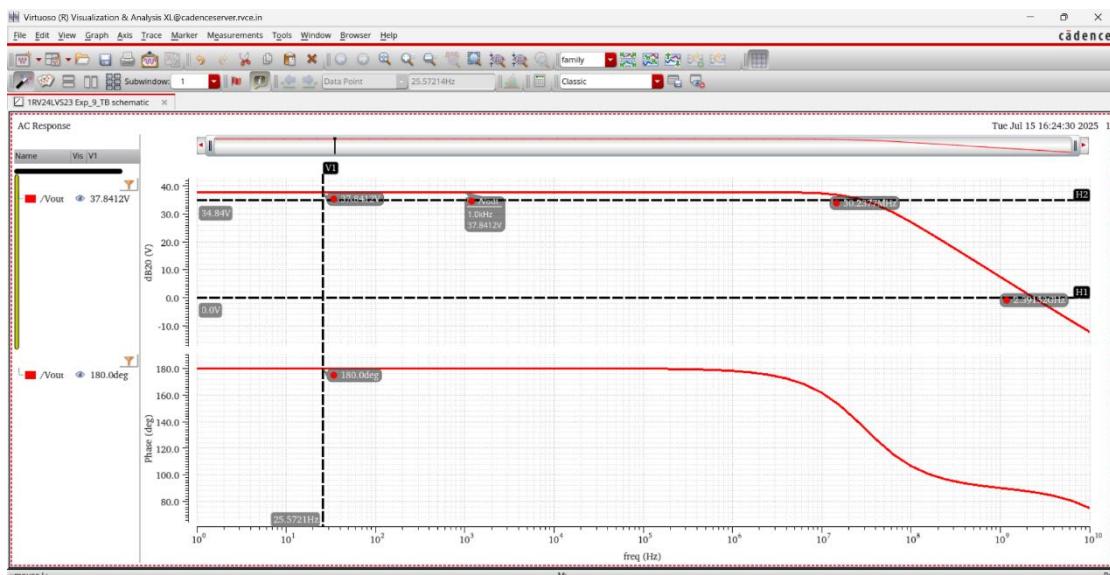
### Operating point

### CS Amplifier

Transistor	V <sub>S</sub>	V <sub>D</sub>	V <sub>G</sub>	V <sub>B</sub>
M1	0	899.07m	570m	0
M2	1.8	899m	1.13	1.8

Transistor	I <sub>D</sub> (uA)	g <sub>m</sub> (mA /V)	g <sub>ds</sub> (uA /V)	r <sub>o</sub> (K ohm)	Self-gain (g <sub>m</sub> r <sub>o</sub> )
M1	99.99	1.17	7.34	136.12	185.646
M2	-99.99	837.88u	7.76	128.84	107.957

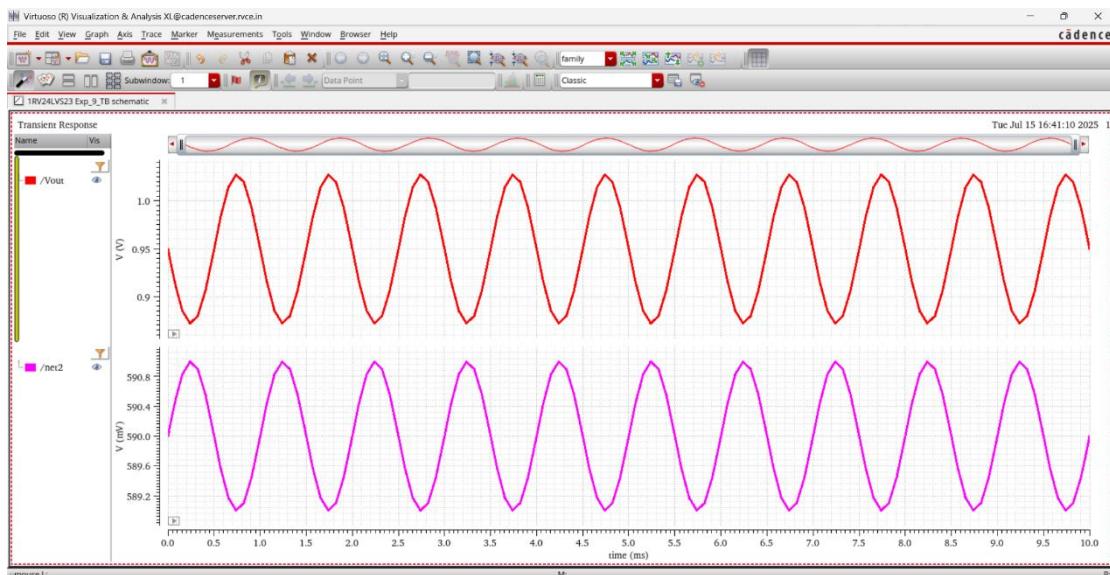
## PRE-LAYOUT SIMULATION RESULTS



**Fig 2: A<sub>v</sub> (dB 20) – frequency characteristics for Common Source amplifier with current source load**

Initially the DC analysis is performed for I<sub>D</sub> - W parameter and the value of W for NMOS and PMOS are found and placed in the CS amplifier circuit. The W values found are 12.95 um for PMOS and 1.05 um for NMOS. The transistors are verified to be operating in saturation region.

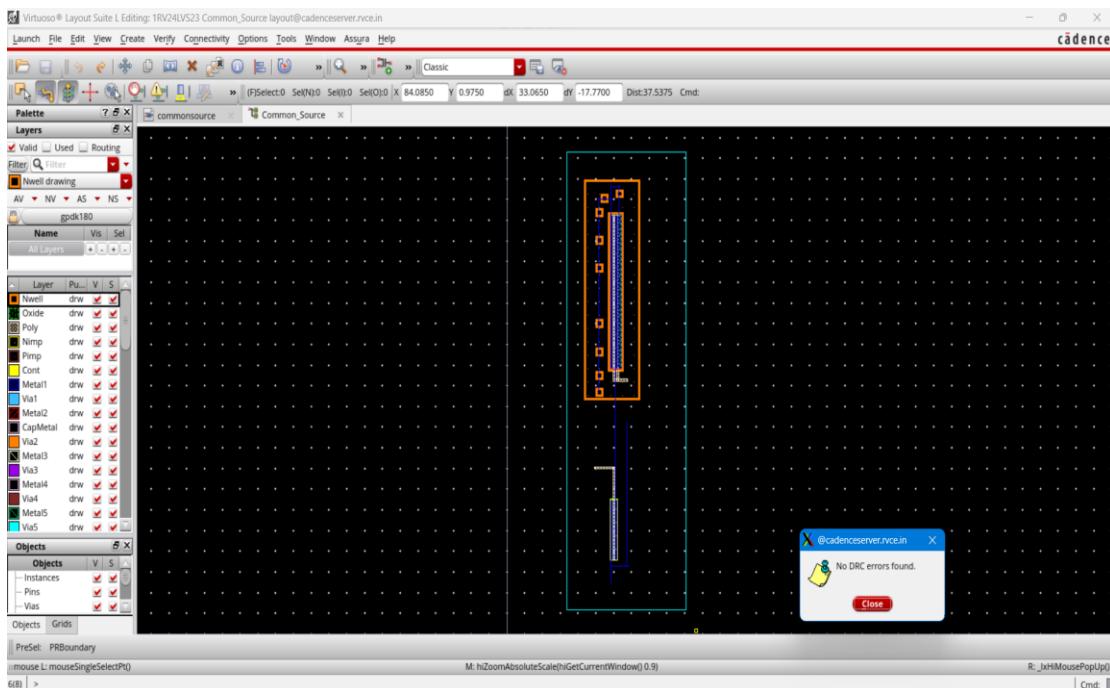
Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of A<sub>v</sub> (dB 20) – frequency and the frequency range are given from 1-10GHz. The gain is 19.692 dB and 3dB frequency is 7.76MHz and UGF is 78.9226MHz. It is as shown in figure 2.



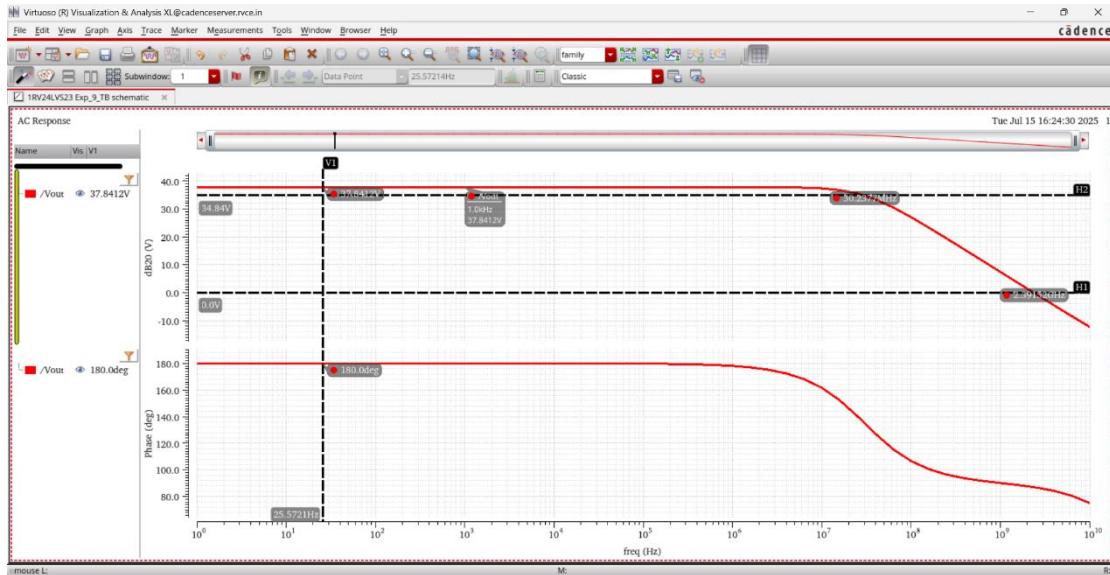
**Fig 3: Transient Analysis for Cascode Amplifier**

The plot of output and input voltage of the input transistor in the CS amplifier with active load is obtained by the transient analysis. The peak-to-peak voltage of the output waveform is calculated to obtain output swing which is 1.32V. It is as shown in figure 3.

## POST LAYOUT SIMULATION RESULTS



**Fig 4: Layout for CS Amplifier with active PMOS load**



**Fig 5:  $A_v$  (dB 20) – frequency characteristics for Common Source amplifier with current source load**

The Layout of CS amplifier with active PMOS load is shown in figure 4. Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) - frequency and the frequency range is given from 1-10GHz. The gain is 19.703 dB and 3dB frequency is 7.73MHz and UGF is 78.425MHz. It is as shown in figure5.

### COMPARISON OF PRELAYOUT AND POST LAYOUT SIMULATION RESULTS

Simulation Type	Gain (dB)	3 dB Freq (MHz)	Unity gain Freq (MHz)
Pre-Layout	19.692	7.76	78.9226
Post-Layout	19.703	7.73	78.425

The comparison of pre layout and post layout simulations of CS amplifier is as shown in the figure. The gain in dB increases for the post layout simulation and the 3dB frequency and unity gain frequency slightly reduces. The values found are approximately equal. And the results are verified.

### INFERENCE

The design and analysis of a Common Source Amplifier with a current source PMOS load were successfully carried out using the Cadence Virtuoso platform. The schematic was implemented as per the specifications with a supply voltage of 1.8 V, a power constraint of  $\leq 250 \mu\text{W}$ , and a load capacitance of 100 fF. Through proper transistor sizing and biasing, the amplifier was made to operate in the saturation region, ensuring high gain and linearity. Pre-layout simulations included DC, AC, and transient analyses which confirmed the amplifier's gain to be 19.692 dB, with a 3 dB frequency of 7.76 MHz and a unity gain frequency of 78.92 MHz.

Post-layout simulation was performed after the layout passed Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification. The layout was done considering the placement of NMOS and PMOS transistors, metal routing, well definitions, and via placements as per the design guidelines. An av\_extracted view was generated to include parasitic capacitance and resistance effects introduced during the physical design. The post-layout analysis yielded a gain of 19.703 dB, with slight reductions in bandwidth (3 dB frequency of 7.73 MHz) and UGF (78.42 MHz), confirming that the parasitic effects had minimal but noticeable influence on high-frequency performance.

The results from both pre-layout and post-layout simulations were in close agreement, validating the design methodology. The slight variations observed were primarily due to layout-induced parasitics, which affect bandwidth more than gain. This highlights the critical importance of layout optimization and physical verification in analog design. The experiment successfully demonstrated the complete flow of analog IC design—from schematic capture to layout generation and post-layout validation reinforcing the role of accurate modeling and skilled layout practices in achieving performance targets in integrated circuit design.

## EXPERIMENT 10

### LAYOUT OF DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

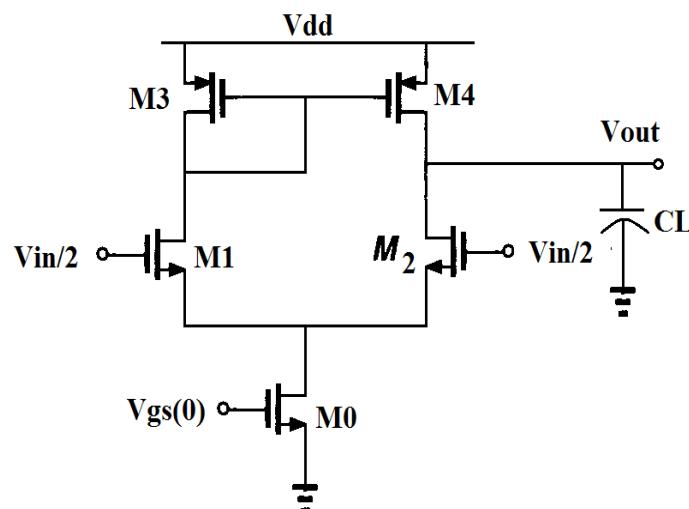
#### OBJECTIVES:

- i. To create layout for a Differential Amplifier with active load
- ii. To perform dc analysis, ac analysis and obtain dc gain, bandwidth and unity gain frequency.
- iii. To perform transient analysis and check gain for a small signal of 10 mVpp, 10 kHz
- iv. Estimate gain and output impedance of both circuits.
- v. Compare pre layout and post layout simulation results

#### SPECIFICATIONS

Parameters	Specified Values
Supply Voltage	1.8 V
Gain	40 dB
ICMR <sup>-</sup>	0.8 V
ICMR <sup>+</sup>	1.6 V
Load Capacitance	10pF
Slew Rate	5 V/ $\mu$ sec
Gain-Band width product	5MHz

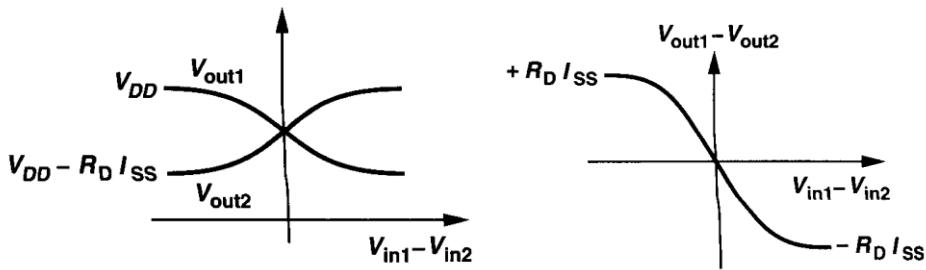
#### CIRCUIT DIAGRAM



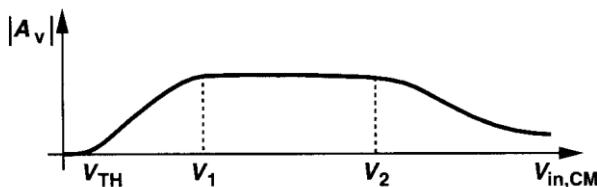
**Fig 1: Differential Amplifier with active load**

## THEORY

The differential signal is defined as one that is measured between two nodes that have equal and opposite signal excursions around a fixed potential i.e., they must exhibit equal impedances at that potential. The center potential in differential signaling is called "common mode" CM level. An important advantage of differential operation is higher immunity to environmental noise and increase in maximum achievable voltage swings. The differential pair employs a current source  $I_{ss}$  to make  $I_{D1} + I_{D2}$  independent of  $V_{in,cm}$ . Thus, if  $V_{in1} = V_{in2}$ , the bias current of each transistor will be  $I_{ss}/2$  and the output common mode level is  $V_{DD} - R_D I_{ss}/2$ .



**Fig: 2 Input and output characteristics of a differential pair**



**Fig 3: Small signal differential gain of a differential pair**

The load of the differential pair can be implemented by active loads using diode connected load or current source loads. Diode connected loads consume large headroom voltage and hence we consider differential Amplifier with current source load as the active load. As shown in figure 1, M1 and M2 are n-channel devices and form the diff pair biased with  $I_{ss}$ . The load circuit consists of M3 and M4, both p-channel devices, connected in a current-mirror configuration. A one-sided output is taken from the common drains of M2 and M4. When a common-mode voltage  $V_1 = V_2 = V_{CM}$  is applied the current  $I_{ss}$  splits evenly between transistors M1 and M2, and  $I_{D1} = I_{D2} = I_{ss} / 2$ . There are no gate currents, therefore  $I_{D3} = I_{D1}$  and  $I_{D4} = I_{D2}$ . And the gain is given by:-

$$A_v = -g_{mN}(r_{ON} \parallel r_{OP}).$$

## Integrated circuit layout

Integrated circuit layout, also known IC layout, IC mask layout, or mask design, is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit.

When using a standard process - where the interaction of the many chemical, thermal, and photographic variables are known and carefully controlled - the behaviour of the final integrated circuit depends largely on the positions and interconnections of the geometric shapes.

Using a computer-aided layout tool, the layout engineer or layout technician places and connects all of the components that make up the chip such that they meet certain criterion typically: performance, size, density, and manufacturability. This practice is often subdivided between two primary layout disciplines: Analog and Digital.

The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are

- Design Rule Checking (DRC),
- Layout Versus Schematic (LVS),

### **Design Rule Check**

Design Rules are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

### **DRC and LVS**

Design Rule Check (DRC) and Layout Versus Schematic (LVS) are verification processes. Reliable device fabrication at modern deep-sub micrometer ( $0.13\text{ }\mu\text{m}$  and below) requires strict observance of transistor spacing, metal layer thickness, and power density rules. DRC exhaustively compares the physical netlist against a set of "foundry design rules" (from the foundry operator), then flags any observed violations.

The LVS process confirms that the layout has the same structure as the associated schematic; this is typically the final step in the layout process. The LVS tool takes as an input a schematic diagram and the extracted view from a layout. It then generates a netlist from each one and compares them. Nodes, ports, and device sizing are all compared. If they are the same, LVS passes and the designer can continue. LVS tends to consider transistor fingers to be the same as an extra-wide transistor.

### **LAYOUT PROCEDURE**

1. Draw the Differential amplifier schematic with NMOS and PMOS length as 500nm and width according to value obtained for design specifications. Connect the input and output pins to the schematic and create a symbol for it.
2. Draw a test circuit using the symbol and given sources for vdd and input ports using analog library vdc and vpulse and vsin sources with appropriate values.
3. Perform Dc analysis with only save dc operating point and note down the dc operating point, small signal parameters and then perform ac analysis using frequency in the range 1 to 100G and Vout wire. Observe dc gain, unity gain frequency and 3db frequency. These are the pre-layout analysis performed.
4. Launch → layout XL from cs amplifier schematic → create → new layout, view → layout, open using layout editor.
5. Go to Option- display

- Modify minor spacing = 0.3
  - Major spacing = 0.6
  - X snap spacing = 0.01
  - Y snap spacing = 0.01
6. Go to DRC edit and enable notify in the checkbox.
7. Go to Connectivity → Generate → All from Source In I/O pins tab → Change metal 1 draw to metal 1 pin for the input and output pins. Enable create label and click label Options → height = 0.2.
8. Push all the cells inside boundary box, press shift+F to view the internal structure of the transistors.
9. Tools → create ruler(k) and define height = 45um, cell height is the lowest possible integer multiple of M1 routing grid that accommodates more complex cell such as flip flop or full adder.
10. Select metal 1 layer from Window, create shape → rectangle and draw VDD and GND with width = 1.2um.
11. Create VIA → M1\_PSUB is placed at the origin.
12. Create VIA → M1\_NWELL is placed at the X=0, Y=45 position.
13. Place the PMOS with min 0.2um and max 10um from the PR Boundary (y-axis) and the NMOS with min 0.2um and max 10um from the PR Boundary (y-axis).
14. Make all the connections between the respective terminals of NMOS and PMOS using metal and poly wire according to schematic and place metal pins on them. Create Poly\_M1 VIA for gate (poly) and pin (metal) connection.
15. Draw the nwell with height=2/3 of height of cell. And insert additional VIA connections for NMOS and PMOS where distance is more than 10 ums.
16. Adjust the PR boundary for cell height and min cell width possible, the width should be multiple of 0.6.
17. Run DRC  
To run DRC for the layout, select Assura → Run DRC make sure Technology selected has gpdk180. Select Ok to Run DRC. If any errors then errors, will be displayed. Debug and Run DRC.
18. Run LVS  
To run LVS, select on Assura → Run LVS. Check Run. Window should pop up saying that LVS Run was successful. In case of errors, check out the errors with schematic and Run LVS again.
19. RC Extraction
  - Go to QRC → setup
  - Select spectre and gpdk180 Technology and extraction as RC.

- Go to I/O tab and select reference node to GND.
- Go to QRC → Run. Ensure output view is selected as av\_extracted.
- It creates a av\_extracted view of the cs amplifier. It consists of resistance and capacitance which constitute the analog model of the design.

## POST LAYOUT SIMULATION

1. Go to Virtuoso TAB → New → Cell view → Cell: (cell name should be same as inverter test schematic) → Type: CONFIG → Click on OK.
2. New Config → window → View: schematic Use template: Spectre → Click on Ok.
3. New window POPS up → Select → Inv test schematic → Right click → select cell view: av\_extracted → Save → Open
4. Perform the dc analysis, ac analysis in similar manner performed for the pre layout analysis. Compare these values with those obtained from the pre layout analysis.

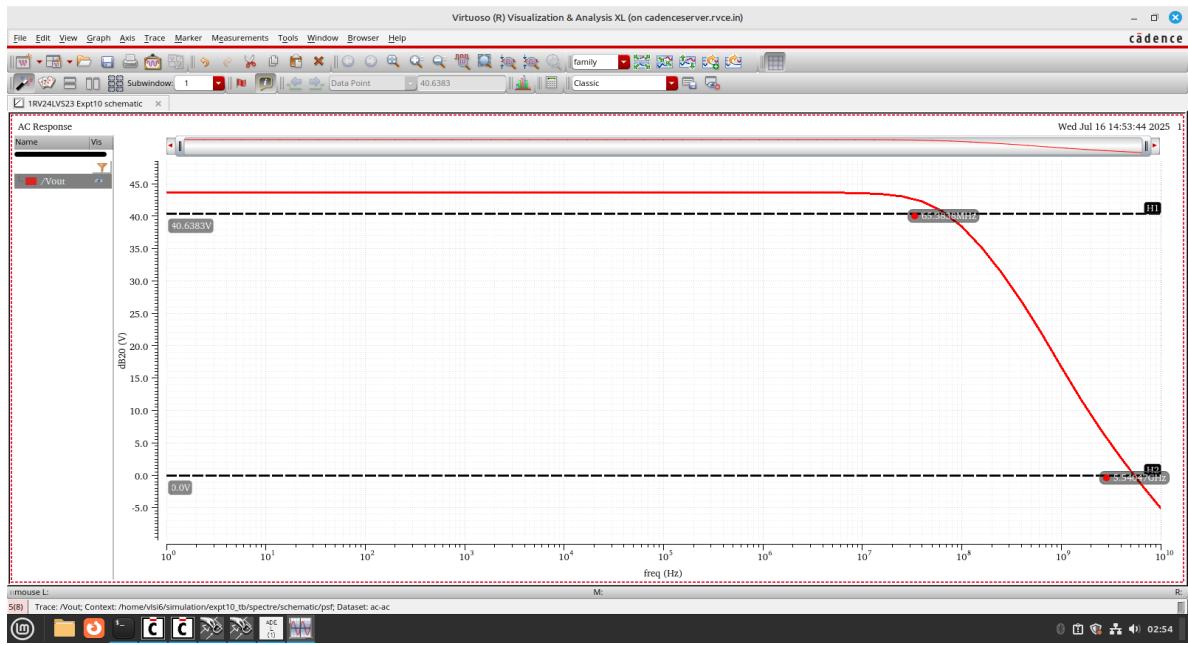
## ANALYSIS

### Operating point

Transistor	V <sub>S</sub> (V)	V <sub>D</sub> (V)	V <sub>G</sub> (V)	V <sub>B</sub> (V)
M0	0	0.192	0.590	0
M1 (M2)	0.192	0.922	0.9	0.192
M3 (M4)	1.8	0.922	0.922	1.8

Transistor	I <sub>D</sub> (uA)	g <sub>m</sub> (mA /V)	g <sub>ds</sub> (mA /V)	r <sub>o</sub> (K ohm)	Self gain (g <sub>m</sub> r <sub>o</sub> )
M0	45.59	604.51	22.81	43.84	26.49
M1 (M2)	22.79	171.67	1.74	574.71	98.59
M3 (M4)	-22.79	95.06	1.57	636.94	60.25

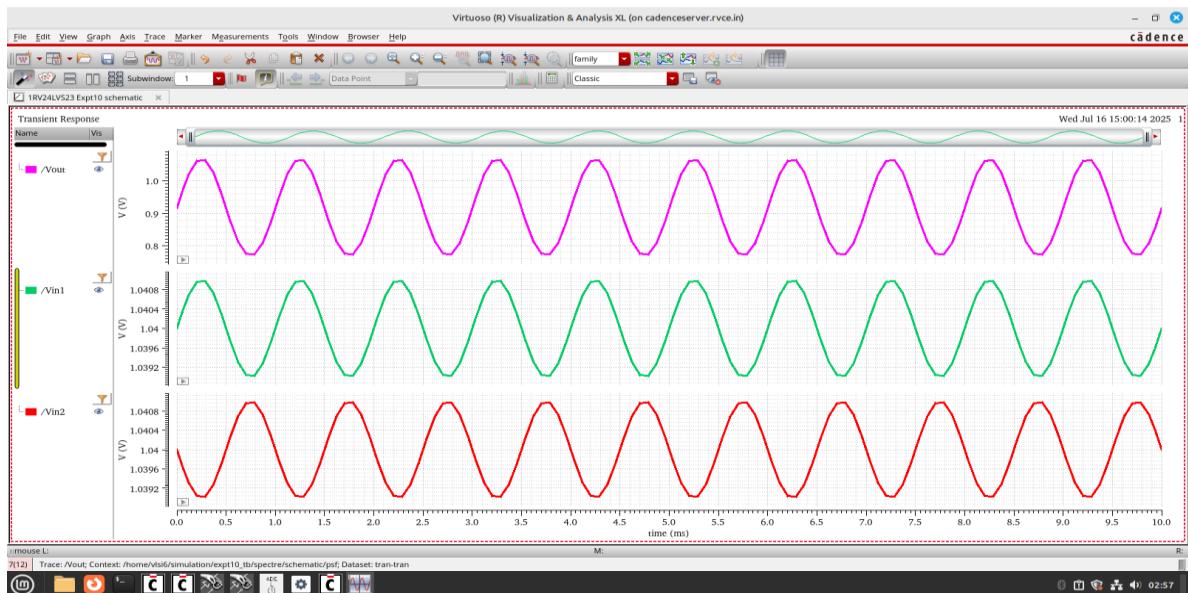
## PRE-LAYOUT SIMULATION RESULTS



**Fig 4:  $A_v$  (dB 20) – frequency characteristics for Differential amplifier with active load**

Initially the DC analysis is performed for  $I_D$  - W parameter and the value of W for NMOS and PMOS are found and placed in the Differential amplifier circuit. The W values found are 2.283um for PMOS M3 (M4) and 1.238 um for NMOS NM1 (NM2) and 9.936 um for NMOS M0. The transistors are verified to be operating in saturation region.

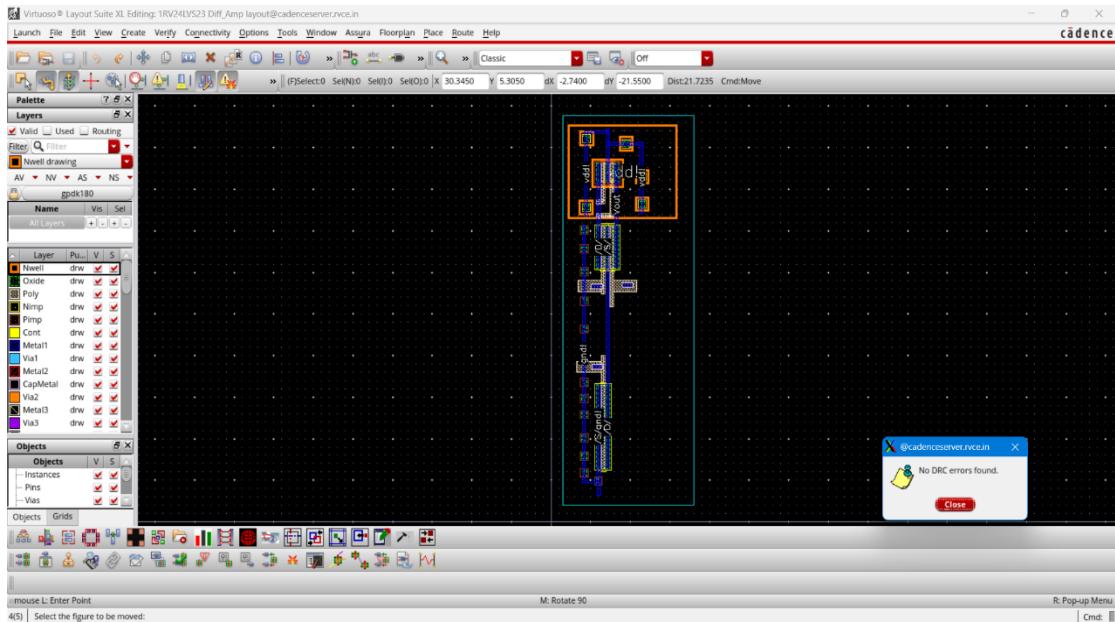
Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) - frequency and the frequency range is given from 1-10GHz. The gain is 40.218 dB and 3dB frequency is 52.18 KHz and UGF is 5.491 MHz.



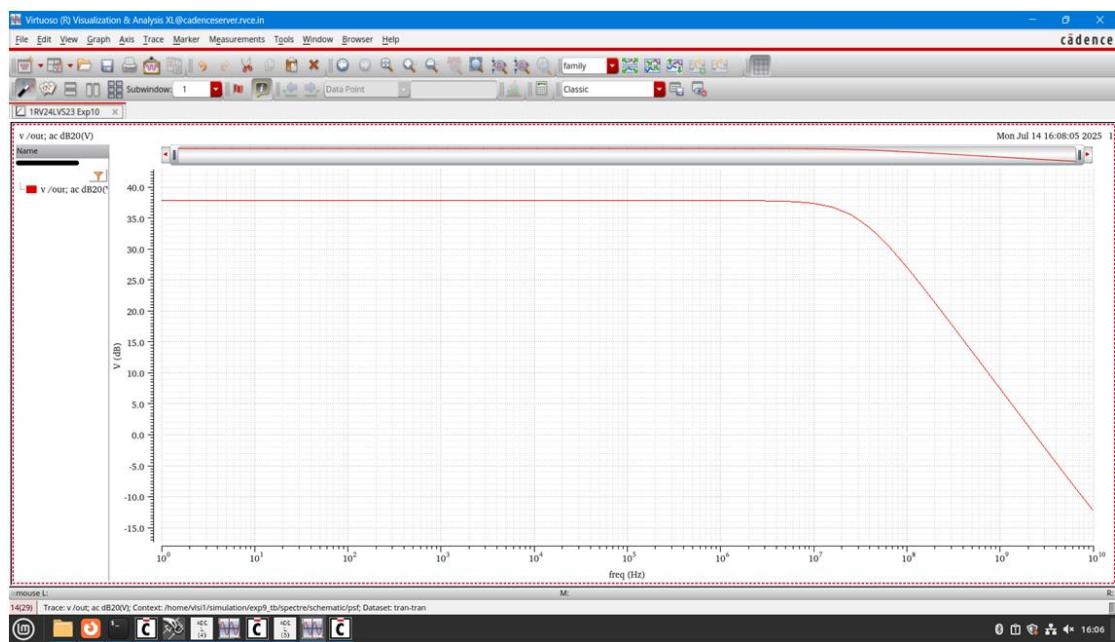
**Fig 5: Transient Analysis for Differential Amplifier with active load**

The plot of output and input voltage of the input transistor in the Differential amplifier with active load is obtained by the transient analysis. The peak-to-peak voltage of the output waveform is calculated to obtain output swing which is 812.7 mV. It is as shown in figure 5.

## POST LAYOUT SIMULATION RESULTS

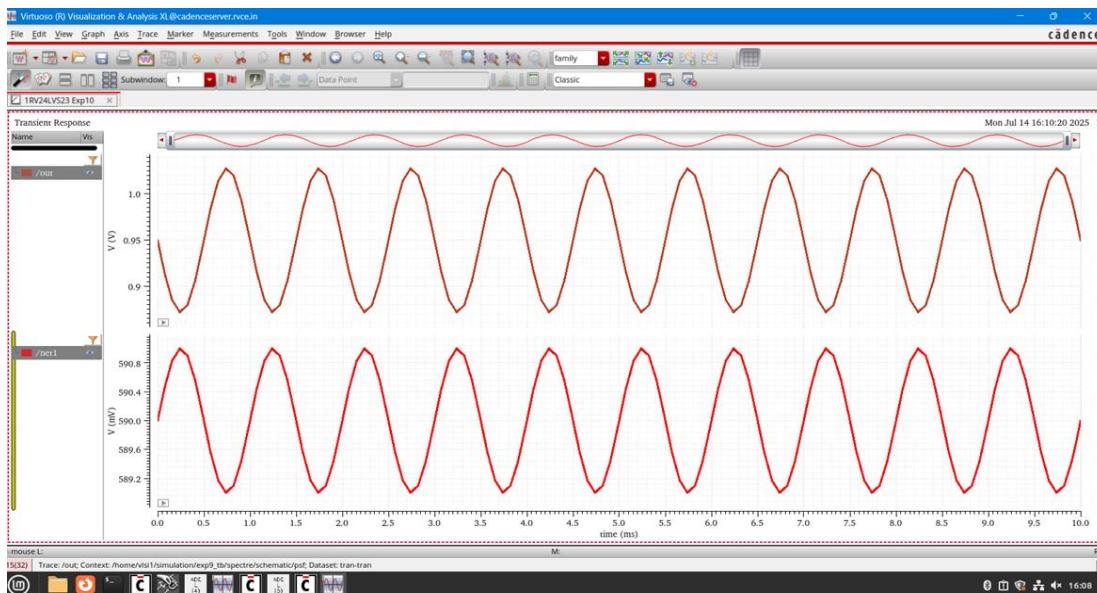


**Fig 6: Layout for Differential Amplifier with active load**



**Fig 7:  $A_v$  (dB 20) – frequency characteristics for Common Source amplifier with current source load**

Then AC Analysis is performed to verify the gain and find out the values of 3 dB frequency and unity gain frequency. The AC analysis is a plot of  $A_v$  (dB 20) - frequency and the frequency range is given from 1-10GHz. The gain is 40.546 dB and 3dB frequency is 49.713 KHz and UGF is 5.432 MHz. It is as shown in figure .



**Fig 8: Transient Analysis for Differential Amplifier with active load**

The plot of output and input voltage of the input transistor in the CS amplifier with active load is obtained by the transient analysis. The peak-to-peak voltage of the output waveform is calculated to obtain output swing which is 846.8 mV. It is as shown in figure 8.

### COMPARISON OF PRELAYOUT AND POST LAYOUT SIMULATION RESULTS

Simulation Type	Gain (dB)	3 dB Freq (K Hz)	Unity gain Freq (M Hz)
Pre-Layout	40.218	52.180	5.491
Post Layout	40.546	49.713	5.432

The comparison of pre layout and post layout simulations of Differential amplifier is as shown in the figure. The gain in dB increases for the post layout simulation and the 3dB frequency and unity gain frequency slightly reduces. The values found are approximately equal. And the results are verified.

### INFERENCE

The design and analysis of a differential amplifier with an active load have been performed and verified to ensure they align with the given specifications. However, the performance of a design—regardless of how well the design procedure is followed—depends heavily on the layout engineer's skill and the quality of the layout produced. In this design, the differential pair is implemented for layout without considering manufacturing process defects. To address issues related to matching and reduce process variations, various layout techniques must be adopted to ensure the

Design achieves optimal performance. Unlike standard cell layouts in digital design, analogue layout is more focused on performance optimisation, often involving trade-offs between area and power to ensure uniform process variation and adopt symmetric physical design techniques. These methods can further influence the performance of the system or its components.