

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth S

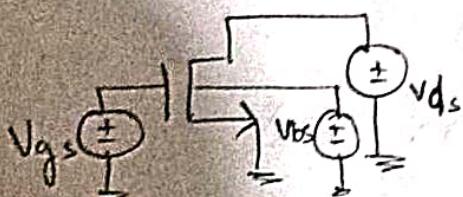
Dept./Lab AICO Lab Class \_\_\_\_\_ Expt./No. 01

Title Study of MOS IV characteristics.

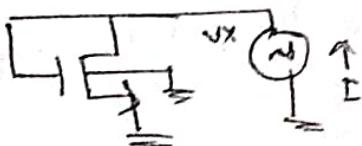
### Objectives:-

- To setup a MOS transistor to obtain  $I_D - V_{GS}$ ,  $I_D - V_{DS}$ ,  $I_D - V_{SB}$  characteristics.
- To estimate the small signal parameters  $g_m, r_o$  and  $g_{mb}$  from IV characteristics.
- compare the  $I_D - V_{DS}$  characteristics of MOSFET's in different configurations.
- compare the small signal parameters obtained from graphical method and direct printing option from ADEL.

### Circuit diagram:-

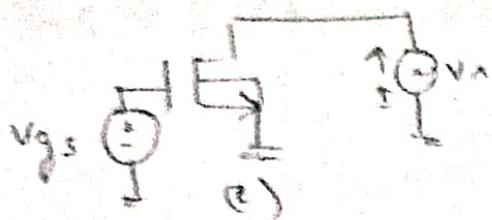


MOSFET simulation  
setup (1)  
(a)

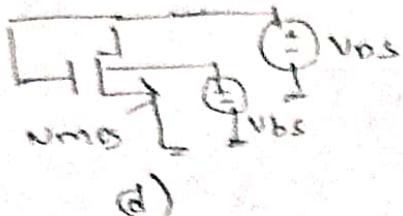


MOSFET configuration (2)  
(b)  
CNMOS diode connected

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MOSFET configuration



MOSFET configuration (mosfet load connected load with VDS)

(d)

### Operations of MOSFET:

$\rightarrow$  Cut-off Region  $\rightarrow V_{GS} < V_{TH}$

$$I_D = 0$$

$\rightarrow$  Triode region / Linear Region :-

$$V_{GS} > V_{TH}$$

$$V_{DS} < V_{GS} - V_{TH}$$

MOSFET acts as resistor

$$I_D = \text{linear w/l } \left[ (V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$\rightarrow$  Saturation Region:- ( $\lambda \neq 0$ )

$$V_{GS} > V_{TH}$$

$$V_{DS} > V_{GS} - V_{TH}$$

MOSFET is on

$$I_D = \frac{\text{linear w/l}}{2} [V_{GS} - V_{TH}]^2 (1 + \lambda V_{DS})$$

### Procedure:-

① Draw the circuit as shown in fig, with length of nmos as 180μm and width as 24μm. Select VDS voltage  $V_{DS} = V_{GS} = 0.9V$  &  $V_{BS} = 0V$

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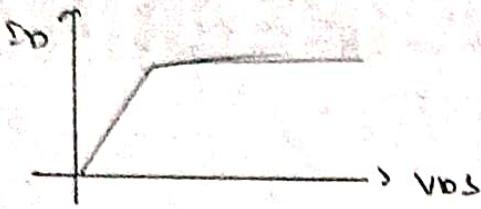
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Title \_\_\_\_\_

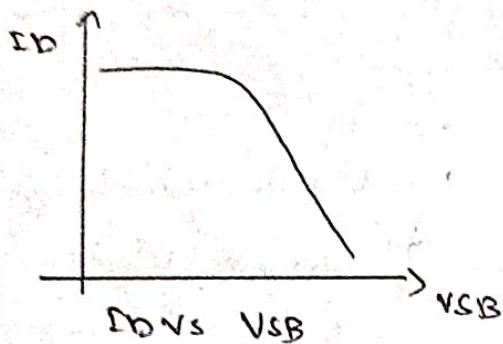
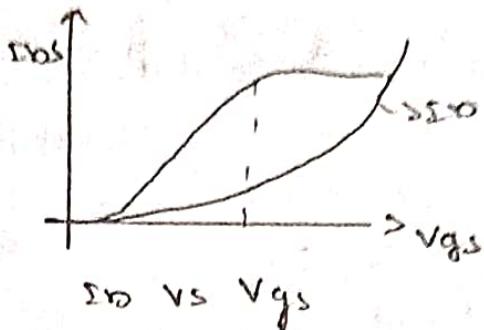
- 1] Perform DC analysis by launching ABEL window & obtain  $V_{GS}$  characteristics by selecting  $V_{GS}$  as component parameter  $I_D$ , characteristics by selecting  $V_{DS}$  as component parameter  $I_D - V_{DS}$ ,  $I_D - V_{GS}$  by selecting  $V_{DS}$  as parameter
- 2] using calculation
- (1)  $I_D - V_{GS}$  characteristics gives  $g_m$
  - (2)  $I_D - V_{SB}$  characteristics gives  $g_{mb}$
  - (3)  $I_D - V_{DS}$  characteristics gives  $r_o$
- 3] Draw circuit in fig. and perform analysis with  $V_{GS}$  with  $V_x$  name
- DC voltage = 0.9V  
AC magnitude = 1V  
freq. range = 1-100 mHz
- 4] using calculator find small signal output resistance of MOSFET in different configuration obtain DC operating point of all parameters.
- 5] For circuit in fig. perform parametric analysis
- L - from 180nm - 14nm  
linear steps - 90nm

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## Graphs



$I_D$ - $V_{DS}$  characteristics



## Equations:

$$g_m = \frac{\partial I_D}{\partial V_{DS}}, \quad R_{out} \quad r_o = \gamma \lambda I_D$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$$

$$R_{out} = \frac{1}{g_m + g_{mb}} \parallel r_o$$

## Result:-

### DC analysis:-

Nmos fig(a)

$g_m$

$r_o$

$g_{mb}$

### AC analysis

Nmos fig(b)

$g_m$

$r_o$

$R_{out}$

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Nmos fig(1)

80 =

Nmos fig(2)

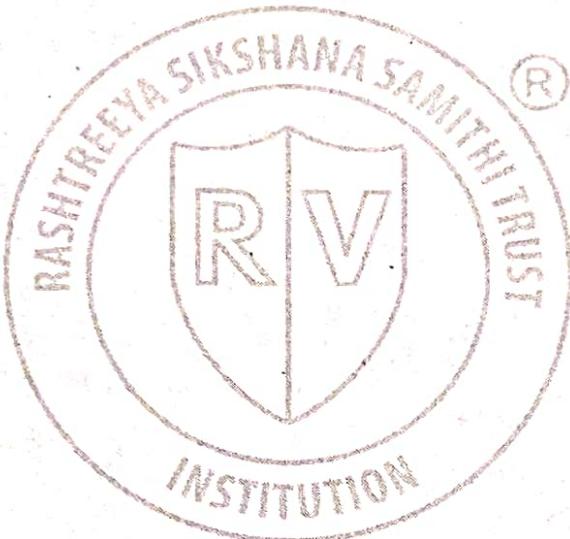
gm

ro

gmb

Rout

Inference:-



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## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth S

Dept./Lab AICD Lab Class \_\_\_\_\_ Expt./No. 02

Title Study of Mos Current Mirror

### Objective:

- (i) To plot  $\frac{I_o}{V_{DS}}$  vs  $V_{DS}$  for  $L = 50\text{nm}$  &  $180\text{nm}$  and observe the channel length modulation at  $W = 10\text{um}$  and  $V_{DS} = 0.9V$
- (ii) To estimate MOS current mirror, cascade MOS mirror using current source of  $100\text{mA}$
- all (iii) To estimate low frequency output impedance of current mirror circuits.
- (iv) To verify the region of operation of o/p transistor for all current mirror.

### Circuit diagram:-

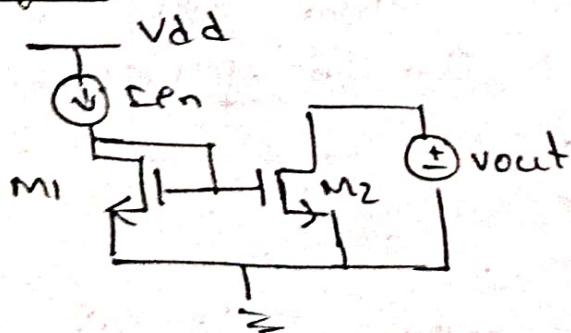


fig (a) Basic current mirror.

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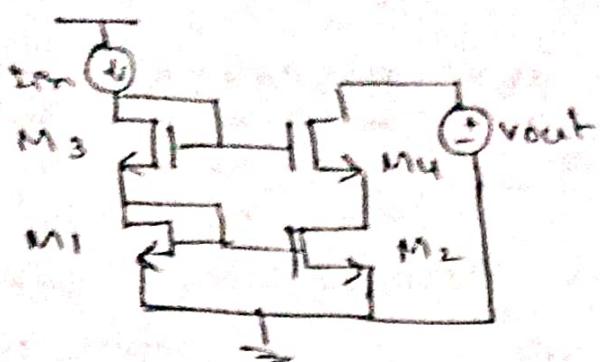


Fig (b)

Cascade current mirror

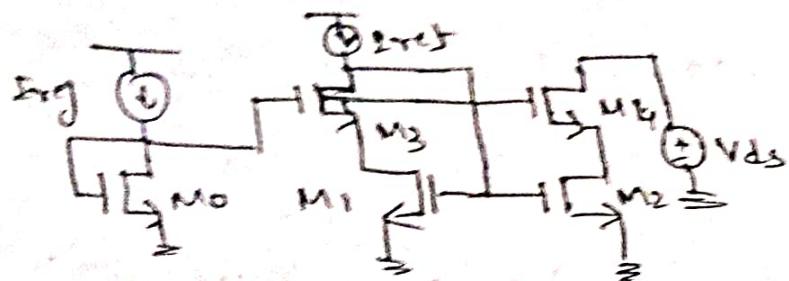
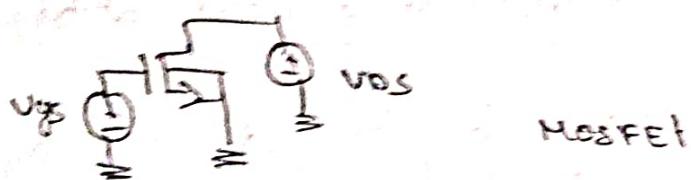


Fig (c)

Low voltage cascode current mirror



MOSFET

### Procedure:-

(i) Draw the circuit in the above fig and obtain  $V_{DS}$ ,  $V_S$ ,  $I_D$  characteristics by performing AC analysis.

$$V_{GS} = 0.9V > V_{DS}$$

$$L = 1\text{ }\mu\text{m}$$

(ii) Perform parametric analysis with varying  $L$  b/w 180nm - 1um auto mode with no. of steps 3

(iii) Find  $g_m$  &  $r_o$

### Current mirror:-

a) Draw the circuit shown in fig a)

$$L=1\text{ }\mu\text{m}, W=1\text{ }\mu\text{m}, I_{DN}=100\text{ }\mu\text{A}$$

b) Perform DC analysis and find  $V_{GS}$

c) Select  $V_{DC}$  ( $V_I=V_{GS}$ ) @ M<sub>2</sub> input of drain terminal

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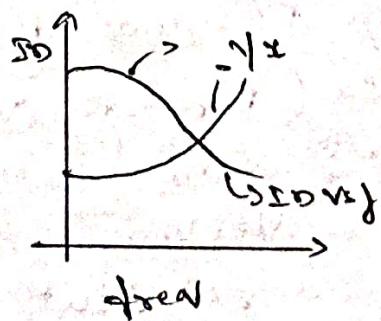
Title \_\_\_\_\_

Terminal and characteristics Perform DC analysis to obtain  $I_D$  vs  $V_{DS}$

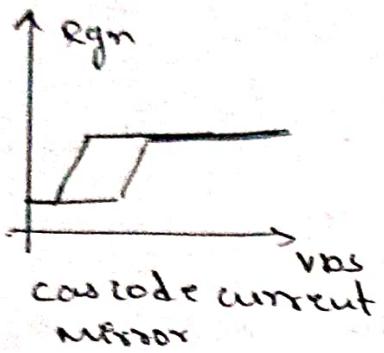
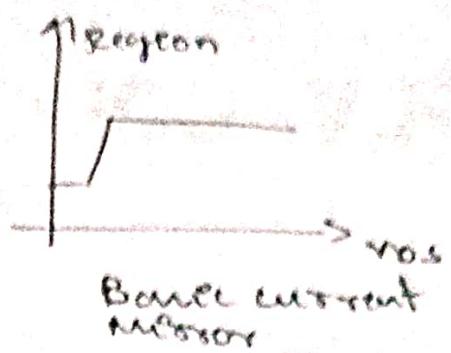
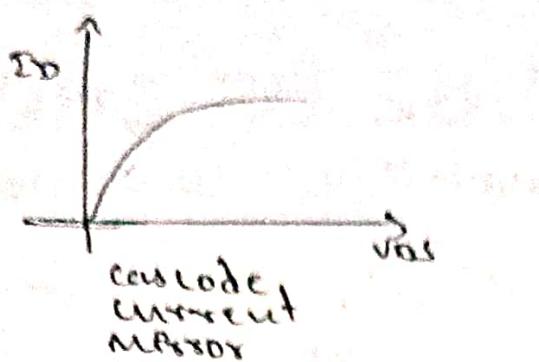
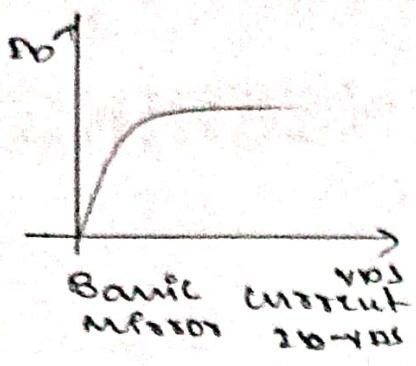
- Measure  $I_D$  from  $I_D$  vs  $V_{DS}$
- Perform parametric analysis with  $V_{DS}$  from  $0 \rightarrow 1.8V$  linear mode, step size  $\geq 0.1$  to find the min values needed to make  $M_2$  transistor in saturated mode.
- Follow the same steps from fig b and fig c circuits. In cascode we initially found min  $V_{out}$  value where both transistors are in saturation.
- Perform ac analysis for all circuits in fig(c)
- $V_{DS} = 0.9V$   
AC magnitude = 1V  
frequency =  $1 \rightarrow 100MHz$
- Find small signal o/p resistance in different configuration.

### Graphs

- AC analysis for MOSFET
- ↳ Basic current mirror
- ↳ Cascode current mirror
- ↳ Low voltage Cascode mirror.



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### EQUATIONS:-

#### (i) Basic current mirror:

$$V_{DS(\text{out})} \Rightarrow V_{ON}$$

$$R_{PN} = 1/g_m$$

$$R_{out} = 1/\lambda R_{D1}$$

$V_{DS1} \neq V_{DS2} \rightarrow$  poor current gain

#### (ii) Cascode current mirror:

$$R_{out} \approx r_{ds2} \quad g_{m4} \quad r_{ds4}$$

$$V_{min}(\text{out}) = 2(V_T - V_{ON})$$

$$R_{PN} = 1/g_{m1} + 1/g_{m3} = 2/g_{m1}$$

$V_{DS1} = V_{DS2} \Rightarrow$  excellent current gain.

#### (iii) Low voltage cascode current mirror:

$$R_{out} = g_{m2} r_{ds2} r_{ds1}$$

$$R_{PN} = r_{ds1} + (1 + g_{m3} r_{ds3}) V_{SS}$$

$$V_{SS} = r_{ds3} (R_{PN} - g_{m3} V_{PN})$$

$$V_{min}(\text{out}) = 2V_{ON}$$

$$V_{min}(I_0) = V_T + V_{ON}$$

$$V_{DS1} = V_{DS3} \Rightarrow$$
 excellent current gain

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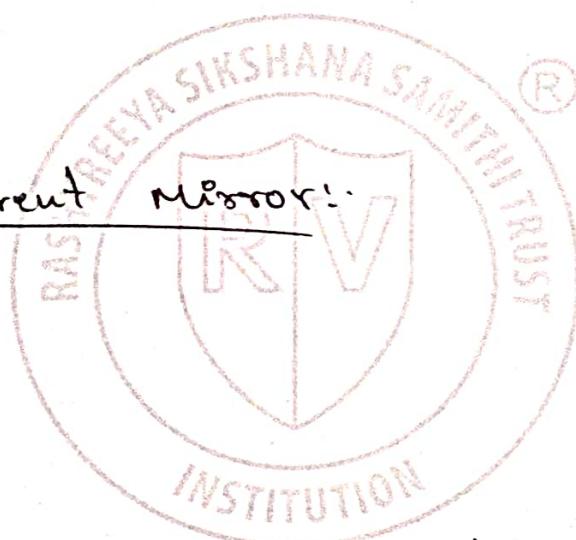
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Title \_\_\_\_\_

### Result:-

#### (i) Basic current mirror:-

- .)  $R_{out}$
- .)  $I_{out}$
- .)  $A_f$



#### (ii) Cascade current mirror:-

- .)  $R_{out}$
- .)  $I_{out}$
- .)  $V_D(\text{open})$

#### (iii) Low voltage cascade current mirror

- .)  $I_{out}$
- .)  $R_{out}$
- .)  $V_D(\text{open})$

### Inference:-

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## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth S

Dept./Lab Aico lab Class \_\_\_\_\_ Expt./No. 03

Title Design and Analysis of CS amplifier circuits.

### Objectives:-

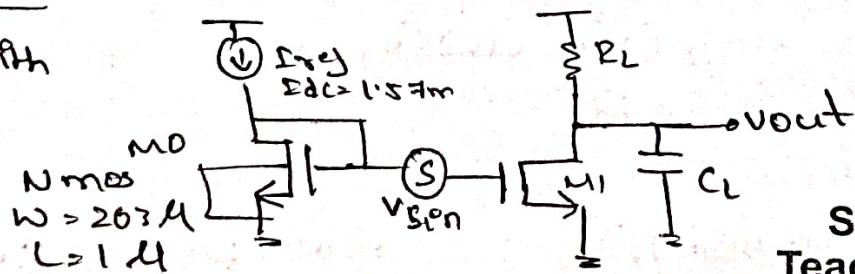
- (i) To design & analysis a CS amplifier for given specification
- (ii) To perform dc analysis & obtain the dc operating points, small signal parameters & node voltage.
- (iii) To perform ac analysis & obtain dc gain, 3dB frequency & unity gain frequency.
- (iv) Estimate gain, output impedance & op swing.

### Specifications:-

Parameters	Specified value
Supply voltage	10.8V
DC gain	5
f <sub>3dB</sub>	100MHz
Load capacitance	5PF

### Circuit diagram :-

- (i) CS ampli., with Resistive load



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## Design & Analysis:

### NMOS amplifier

$$f = \frac{1}{2\pi R_L C_L}$$

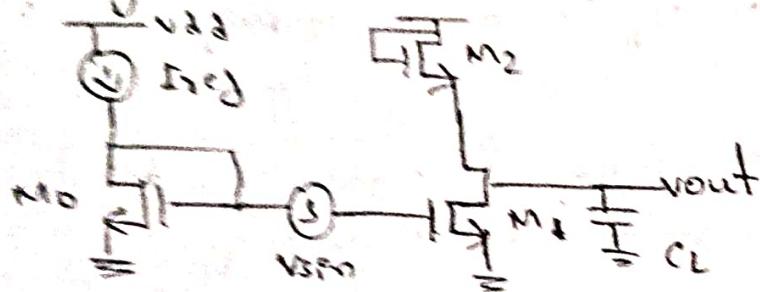
$$AV = -g_m R_L$$

$$I_D = g_m V_{GS}$$

$$g_m = \sqrt{2SD \ln(2eN)}$$

$$g_m = \sqrt{2SD \ln(2eN)} / L$$

### Circuit diagram



CC amplifiers with NMOS  
diode connected load.

### Calculation:

$$f = \frac{1}{2\pi R_L C_L} \Rightarrow R_L = \frac{1}{2\pi f C_L}$$

$$R_L = \frac{1}{2\pi \times 60 \times 10^3 \times 5 \times 10^{-12}}$$

$$R_L = 318.3 \Omega$$

$$g_m = \frac{|AV|}{R_L} = \frac{5}{318.3} \Rightarrow 15.7 \text{ mA/V}$$

$$V_{GS} = -730 \text{ to } -753 \text{ mV}$$

$$V_{TH} = 542 \text{ to } 767 \text{ mV}$$

$$I_D = \frac{1}{2} \underbrace{4 \ln(2eN)}_{g_m} \omega / 2 \underbrace{(V_{GS} - V_{TH})(V_{GS} - V_{TH})}_{V_{DS}}$$

$$I_D = 1.57 \text{ mA}$$

$$g_m = \sqrt{2SD \ln(2eN)} / L, \text{ linear for } L = 180 \mu \text{m} \approx 388.125 \text{ mA}$$

$$\omega / L = \frac{202.25 \times 4}{121} \text{ [finger 5]}$$

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### Procedure:-

- (i) current mirror circuit can be used to bias HEMT/  
MOSFET transmitter of ampl. circuit.
- (ii) obtain the values of  $R_L$ ,  $f_{req}$ , W/L ratio from  
the circuit
- (iii) run dummy dc analysis.
- (iv) connect an AC source in b/w with ac magnitude =  
frequency =  $1\text{kHz}$ . Amplitude 5mV. Run AC analysis  
for freq ranging from  $1 \rightarrow 10\text{GHz}$ .
- (v) convert the graph into dB scale note down the  
values of A gain, 3dB frequency & the VGF
- (vi) Perform transient analysis with stop time  
cons, the O/p voltage is determined by calculating  
 $V_{O(p-p)}$  value and also  $V_{in}(p-p)$  value.

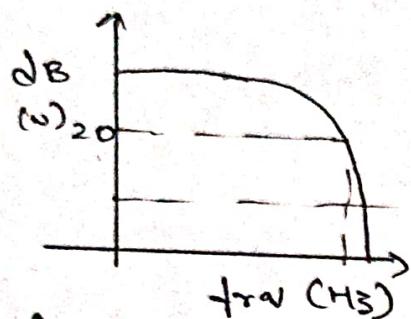
### Cs ampl. with diode connected load:-

- (i) Draw the circuit as shown in 1b & the length  
of NMOS is set as width 203um for 10 nmos  
transistor.
- (ii) In DC analysis since the transistors are not in  
saturation region, the width of  $M_2$  is  
set as W & a region width post is  
obtained using parameteric analysis.

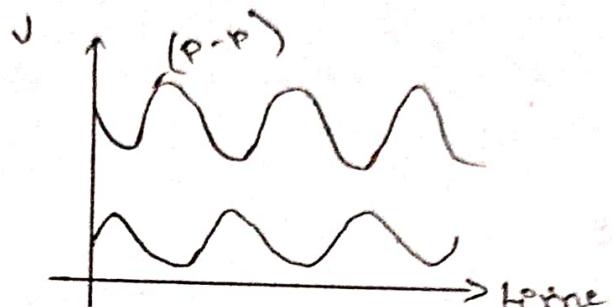
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(iii) Transient analysis ~~After~~ The same steps as mentioned are followed for obtaining the DC operating points, small signal parameters, 3dB frequency and unit gain freq. (UGF)

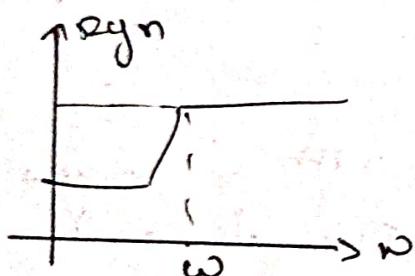
### Graphs



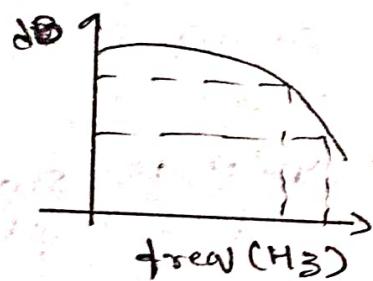
Ac response of CS  
amp with resistive  
load



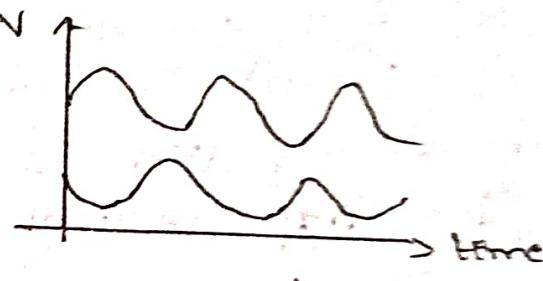
Transient analysis  
with Resistive load



plot width vs rgm  
(nmos connected load)



Ac response



Transient  
analysis

### Results :-

#### (i) CS amp with Resistive load:

- $A_V (\text{in dB}) =$
- $A_V (\text{in dB}) =$
- $A_V (\text{mg}) =$
- $f_{\text{req}} =$
- $f_{\text{req}} (\text{UGF}) =$

Ac analysis

$$\frac{A_V \cdot V_{\text{out}}}{V_{\text{in}}} =$$

$$V_{\text{out}} (\text{P-P}) =$$

$$V_{\text{in}} (\text{P-P}) =$$

Transient  
analysis

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(ii) CS amplifier with NMOS diode connected load:-

•  $W = 11 \text{ Mm}$  for  $M_2$  such that  $M_1$  will be in saturation

$$Av(\text{endB}) =$$

$$Av(\text{mag}) =$$

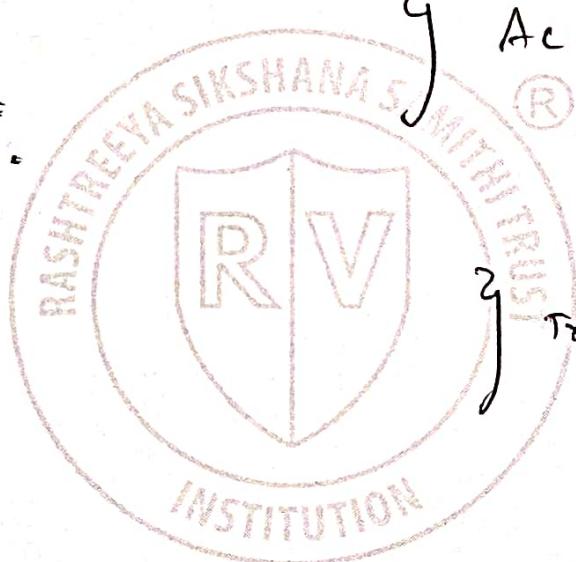
$$\frac{1}{3} \text{ dB}$$

$$\frac{1}{2} (\text{dB})(\text{UHF})$$

$$V_{in} (\text{P-P}) =$$

$$V_{out} (\text{P-P}) =$$

$$Av = \frac{V_{out}}{V_{in}} =$$



Ac analysis

Transient analysis.

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## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth.s

Dept./Lab AICO Lab Class \_\_\_\_\_ Expt./No. 04

Title Design and Analysis of Basic amplr stages using PDM

### Objective:-

- (i) To design and analyse common source amplr with current load , cascode amplr triple cascode as amplr
- (ii) To perform dc analysis and obtain dc operating points , small signal parameters & node voltages.
- (iii) To perform Ac analysis & obtain dc gain 3dB,
- (iv) Estimate gain & o/p impedance of both ccts.

### Specifications:-

Parameter	Specified value
Supply Voltage	1.8V
Power	$\leq 250\text{mW}$
VGF	150 MHz
Load capacitance	100 pF

### Circuit diagram:-

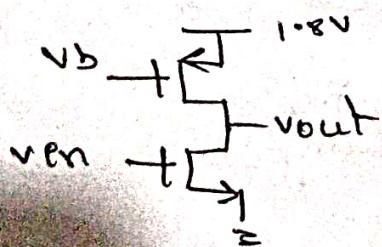


fig a)

CS w/ the  
current source  
load.

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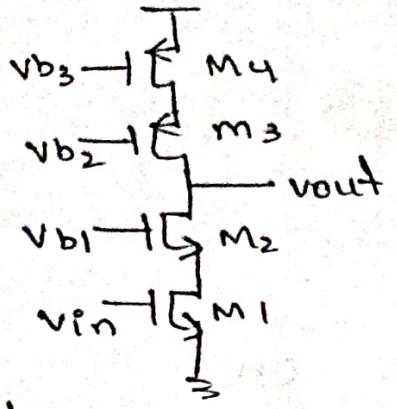


fig (b) cascode Amplx

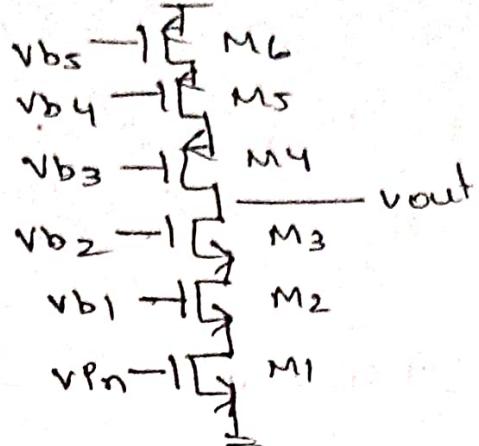


fig (c) triple cascode Amplx

### Design and Analysis:-

$L = 3$  times of  $180\text{n} \approx 500\text{n}$

$$(Vg)_n = V_s + V_{th} + 0.05V_{DD} \Rightarrow 590\text{mV}$$

$$(Vg)_p = V_s - |V_{th}| - g_{om} \Rightarrow 1.2\text{V}$$

$$\text{Power} = 250\text{mW}$$

$$V_{DD} = 1.8\text{V}$$

$$P > V_s$$

$$I \Rightarrow 138.8\text{mA}$$

CS amplx with current source load:-

$$Av = -g_{m1} (r_{o1} \parallel r_{o2})$$

cascode Amplx:-

$$Av = g_{m1} [ (g_{m2} r_{o2} r_{o1}) \parallel (g_{m3} r_{o3} r_{o4}) ]$$

Triple cascode Amplx:-

$$Av = g_{m1} \{ (g_{m3} r_{o3} g_{m2} r_{o2} r_{o1}) \parallel (g_{m4} r_{o4} g_{m5} r_{o5} r_{o6}) \}$$

Procedure:- (CS amplx with current source load)

- (1) Draw the Ckt as shown in fig a, with length as  $500\text{n}$  &  $W = 2\text{Um}$  initially.

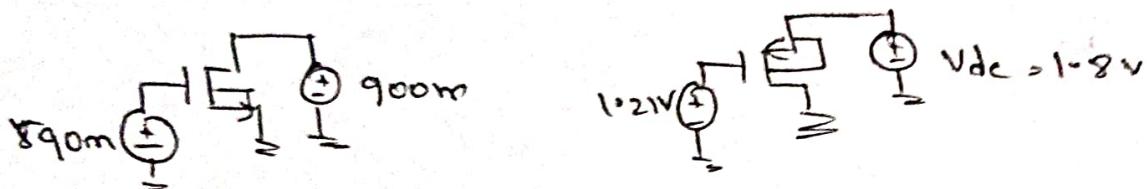
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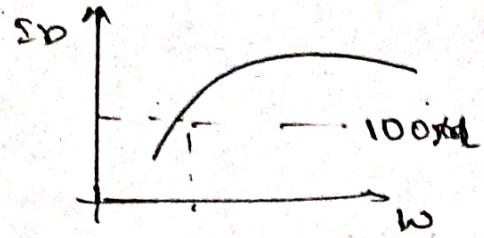
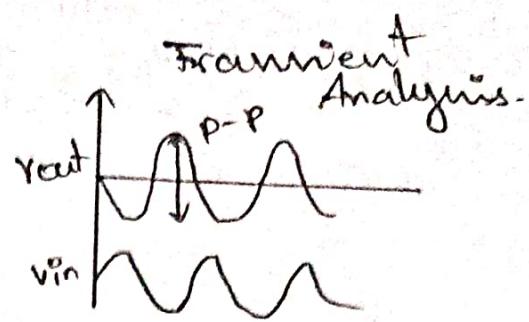
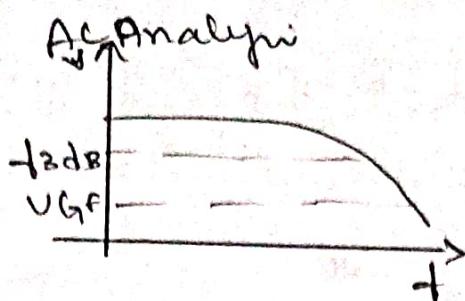
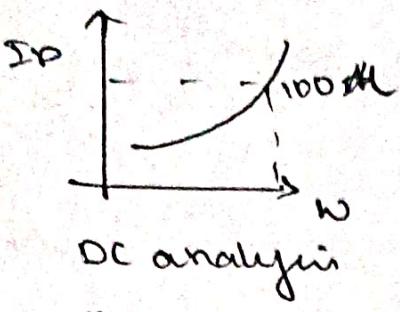
- (i) calculate the width of both NMOS and PMOS by performing DC analysis ( $I_D$  vs  $w$ )
- (ii) set the width of both NMOS & PMOS provided respective voltages & perform AC analysis to calculate the gain -  $f_{3dB}$  & UGF
- (iv) perform transient analysis to calculate  $\frac{dP}{dt}$  for  $i/p$  &  $o/p$  then calculate gain

### Cascade & Triple cascode Ampl.

- (i) Perform the same steps as mentioned for each stage of the cascode cc Ampl & first obtain the values of width for each PMOS & NMOS. for the flow of required current
- (ii) After finding out, rigup the circuit as shown in b&c and then perform AC & transient analysis.

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Teacher Incharge

## Graphs



## Results :-

$$I = 100 \text{ mA}$$

(i) CS amplifier with current source load

$$\text{PMOS } (M_2) \Rightarrow w_2 =$$

$$\text{PMOS } (M_1) \Rightarrow w_1 =$$

$$\begin{aligned} g_{4L} &= g_{BC} \\ V_{G1} &= \end{aligned}$$

$$A_V (\text{dB}_{20}) =$$

$$f_3 \text{ dB} =$$

$$V_{GF} =$$

$$g_{AC}$$

$$V_{out} (\text{P-P}) =$$

$$V_{in} (\text{P-P}) =$$

$$A_V =$$

$$y \text{ Transient}$$

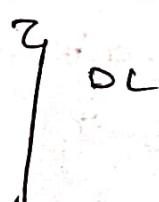
(ii) cascode Amplx

$$w_1 =$$

$$w_2 =$$

$$w_3 =$$

$$w_4 =$$



$$\begin{cases} V_{G1} \\ V_{G2} \\ V_{G3} \\ V_{G4} \end{cases} =$$

$$V_o (\text{dB}_{20}) =$$

$$y \text{ Ac}$$

$$f_3 (\text{dB}) =$$

$$V_{GF} (\text{dB}) =$$

$$A_V (\text{mag}) =$$

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

$$V_{out} (P-P) =$$

$$V_{in} (P-P) =$$

$$A_v =$$

$\frac{V_{out}}{V_{in}}$  Transient

(iii) Triode Amplifier :-

$$N_1 =$$

$$W_2 =$$

$$W_3 =$$

$$W_4 =$$

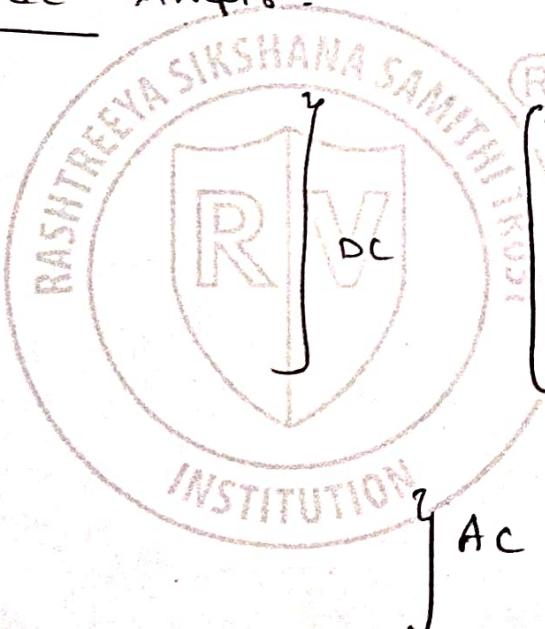
$$W_5 =$$

$$W_6 =$$

$$A_v (dB_{20}) =$$

$$f_z (dB) =$$

$$V_{GF} (dB) =$$



$$\begin{cases} V_{g1} = \\ V_{g2} = \\ V_{g3} = \\ V_{g4} = \\ V_{g5} = \\ V_{g6} = \end{cases}$$

$$V_{out}(P-P) =$$

$$V_{in} (P-P) =$$

$$A_v =$$

$\frac{V_{out}}{V_{in}}$  Transient

Inference:-

Signature of  
Teacher Incharge

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth - S

Dept./Lab AICD Lab Class \_\_\_\_\_ Expt./No. 05

Title Design and Analysis of differential Amps with Active load.

### Objective:-

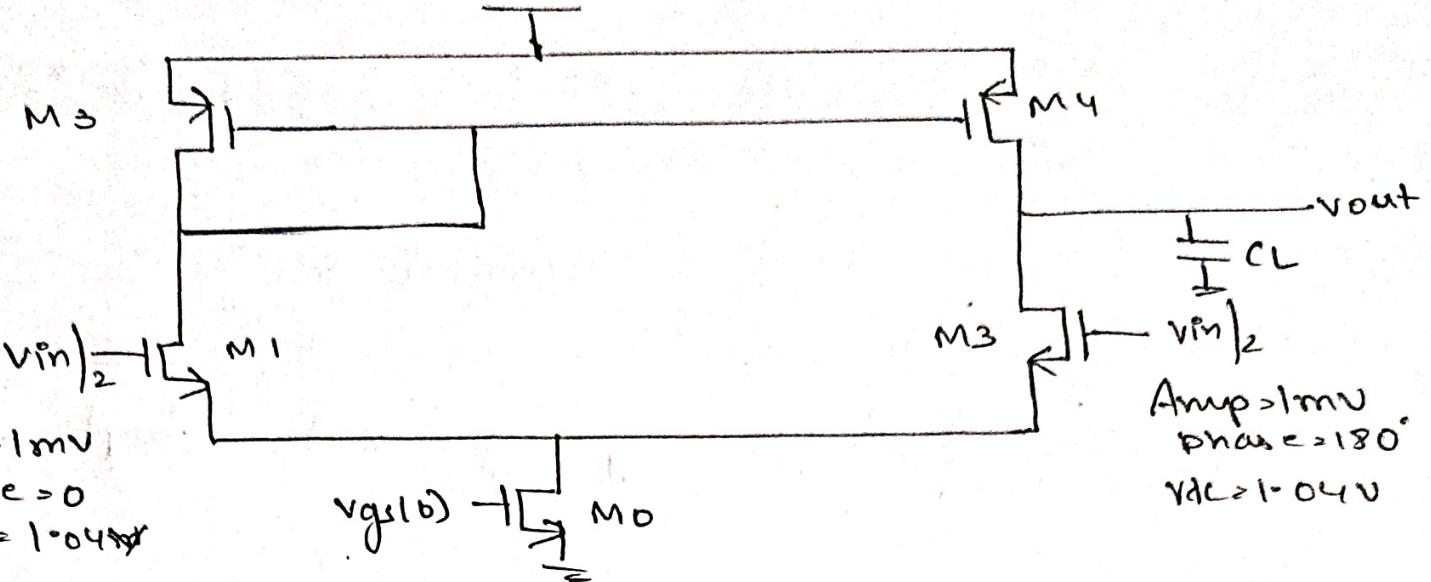
- (i) To design and analyse differential amplifiers with active load for the given spec using PDM.
- (ii) To perform DC analysis & obtain DC operating points, small signal parameters & node voltages.
- (iii) To perform AC analysis & obtain dc gain, 3dB freq., UGF & to verify slew rate

### Specification:-

Parameters	Specified Value
Supply voltage	1.8V
Gain	40dB
ICMR -	0.8V
ICMR+	1.6V
Load capacitance	10PF
Slew rate	5V/ms
Gain Bandwidth Product	5MHz

### Circuit diagram:-

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Sizing transistors :-

$M_0$  :-

$$v_g \rightarrow \begin{cases} 0.45 \\ w_0 = w \\ (At I_D = 50 \text{ mA}) \end{cases} \quad v_g = V_S + V_{TH} + \tau \cdot V_{DD} = 590 \text{ mV}$$

$$w_0 = 9.900 \mu\text{m}$$

$M_1, M_2$  :-

$$v_g \rightarrow \begin{cases} 0.9 \text{ V} \\ w_1, 2 = w \\ 0.48 \mu\text{m} \end{cases} \quad v_g = V_S + V_{TH} + \tau \cdot V_{DD} = 1.04 \text{ V}$$

$$(At I_D = 50 \text{ mA})$$

$$w_1 = w_2 = 5.042 \mu\text{m}$$

$M_3, M_4$  :-

$$w_3, 4 = N \quad \begin{cases} 0.9 \text{ V} \\ 0.9 \text{ V} \end{cases} \quad w_3 = w_4 = 2.283 \mu\text{m}$$

$$(At I_D = 50 \text{ mA})$$

Design :-

$$\Delta V = 40 \text{ dB}, \text{ slew rate} = 5 \text{ V/ms} \quad | \quad L = 500 \text{ nm}$$

$$\left( \frac{dV_o}{dt} \right) \quad | \quad I_{SS} = \text{slewrate} \times C_L$$

$$\rightarrow 50 \text{ mA}$$

$$V_{out} = V_{DD}/2 = 0.9 \text{ V}$$

$$v_g = 0.9/2 = 0.45 \text{ V}$$

$$| \quad \frac{\Sigma I_S}{2} = 25 \text{ mA}$$

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

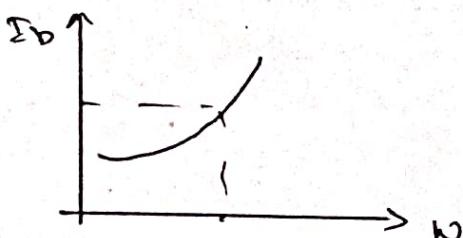
Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

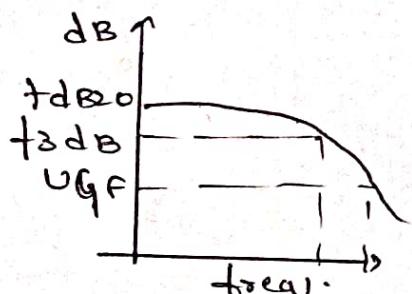
### Procedure :-

- (i) Find the P/P gate voltage of each transistor & find the width of each transistor by performing dc analysis b/w  $20 \text{ V}$  &  $0 \text{ V}$  (from noon - soon)
- (ii) Perform dummy dc analysis to find the dc operating voltages.
- (iii) Perform Ac analysis (from  $1 \rightarrow 10\text{GHz}$ ) to calculate gain,  $f_3\text{dB}$ ,  $U_{GF}$
- (iv) Perform transient analysis to find the peak to peak voltage of both P/P & B/LP
- (v) calculate slew rate.

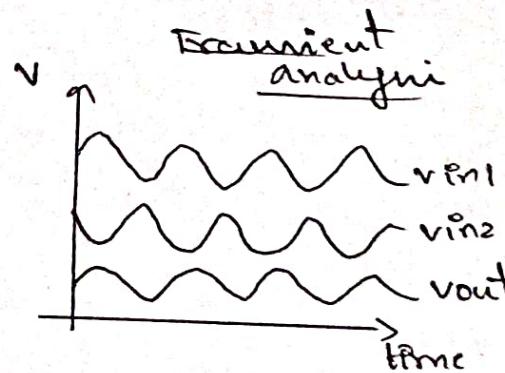
### Graphs



DC analysis

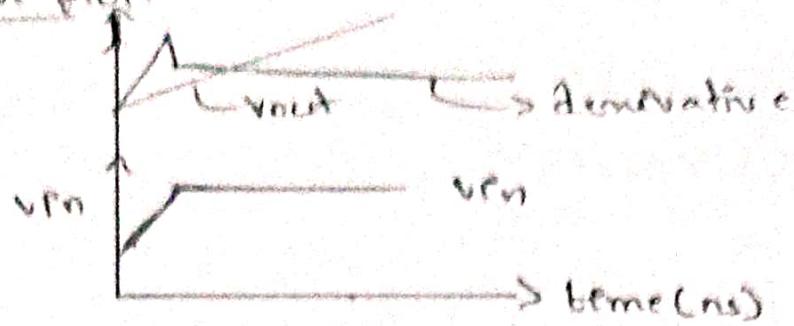


AC analysis



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### Detailed plot:-



### Results:-

$$M_0(\omega) =$$

$$M_1 = M_2(\omega) =$$

$$M_3 = M_4(\omega) =$$

$$\text{Gain}(dB_{20}) =$$

$$A_n(\text{mag}) =$$

$$f_3(\text{dB}) =$$

$$f_0(\text{dB})(\text{DGF}) =$$

$$\text{Peak to peak } V_{\text{out}} =$$

$$V_{\text{in}1} =$$

$$V_{\text{in}2} =$$

$$AV =$$

$$\text{Slew rate} =$$

### Inference :-

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth S

Dept./Lab Aico Lab Class \_\_\_\_\_ Expt./No. 06

Title Design & Analysis of telescopic opamp with differential input.

### Objectives:-

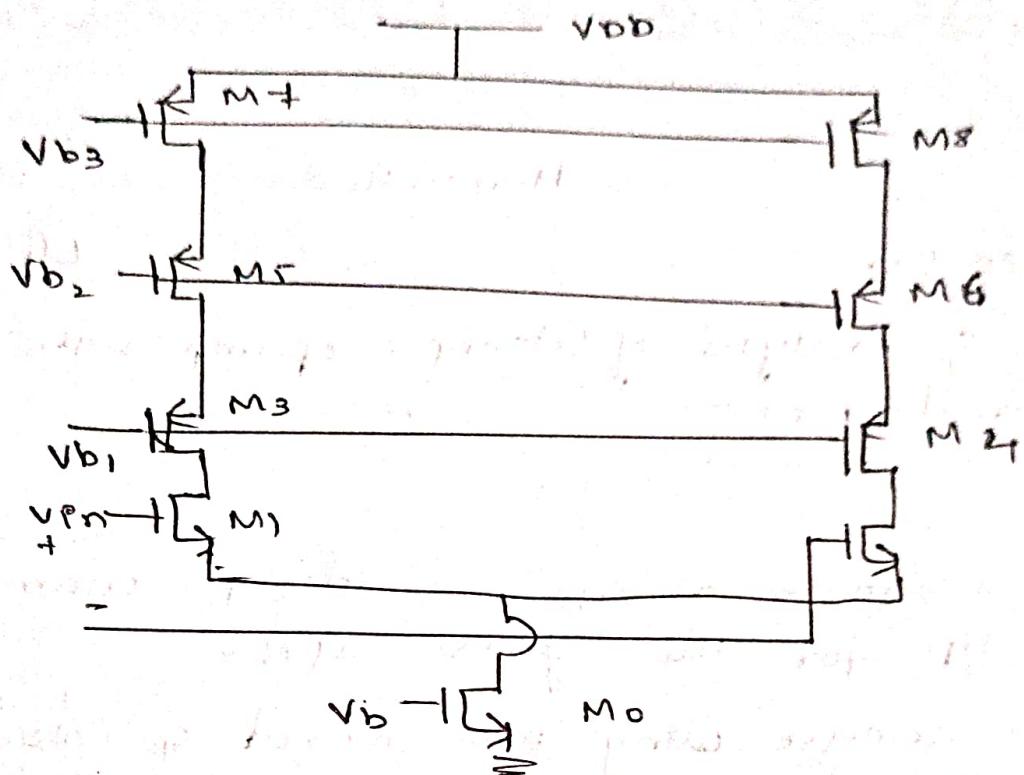
- (i) TO design & analyse a telescopic opamp with differential I/P for the given spec.
- (ii) TO analyse using PPM, method & calculate node & gate voltages.
- (iii) TO perform DC analysis & obtain the DC operating points, small signal parameters & node voltages.
- (iv) TO perform AC analysis & obtain dc gain, 3dB frequency UGF.
- (v) TO perform transient analysis to calculate gain.

### Specifications:-

Parameters	Specified value
Supply Voltage	1.8V
Gain	40dB
ICMR -	0.8V
ICMR +	1.6V
Load capacitance	10PF
Slew rate	5V/ms
Gain Bandwidth Product	5MHz

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Teacher Incharge

## Circuit Diagram:-



## Design:-

$$V_{DD} = 1.8V$$

$$\text{Gain} = 40 \text{dB}$$

$$C_L = 10 \text{ pF}$$

$$\text{Slew rate} = 5 \text{ V/ms}$$

$$I_{SS} = C_L \times S \times R$$

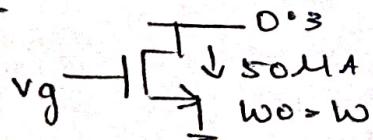
$$\rightarrow 50 \mu\text{A}$$

$$V_{TH} = 600 \text{ mV}$$

$$L \rightarrow 500 \text{ nm}$$

## Sizing Transistors:-

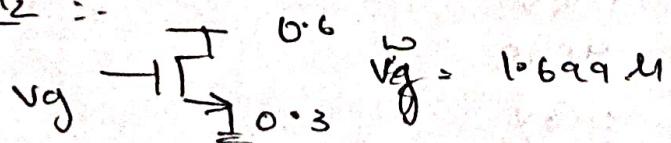
$M_0$  :-



$$V_g = V_s + V_{TH} + 5 \cdot V_{DD}$$

$$W = 3.539 \mu$$

$M_1, M_2$  :-



# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

M<sub>3</sub>, M<sub>4</sub>:

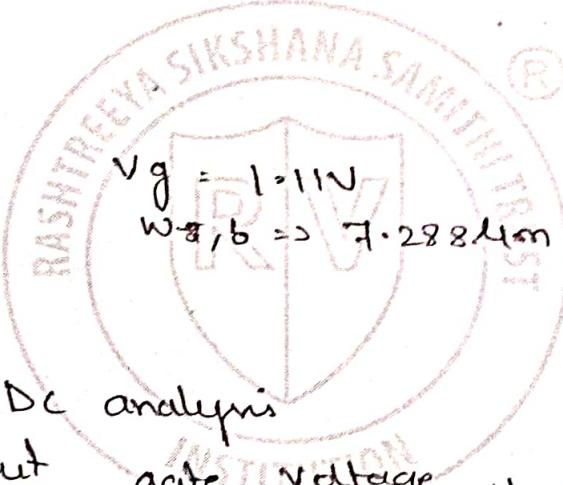
$$V_g \rightarrow \begin{cases} 1 & 0.9 \\ 0 & 0.6 \end{cases} V_{25mA} \quad V_g = 0.6 + 6.9 \text{ mV} = 1.29 \text{ V}$$

$$W_3 = 4 \Rightarrow 1.699 \mu\text{m}$$

M<sub>5</sub>, M<sub>6</sub>; M<sub>7</sub>, M<sub>8</sub>:

$$V_g \rightarrow \begin{cases} 1 & 1.8 \\ 0 & 1.35 \end{cases} V_{25mA} \quad V_g = 1.11 \text{ V}$$

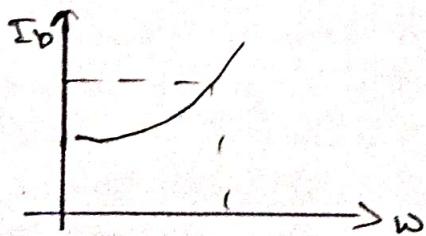
$$W_8, b \Rightarrow 7.288 \mu\text{m}$$



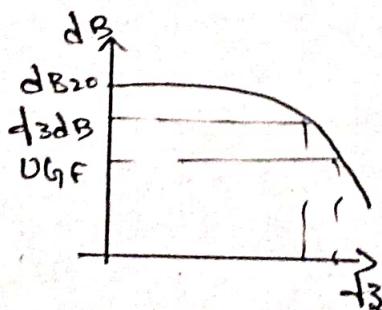
Procedure:-

- (i) Run dummy DC analysis
- (ii) Find the input gate voltage of each transistor
- Extend the width of each transistor.
- (iii) Perform AC analysis
- (iv) Perform transient analysis to find the P-P voltages

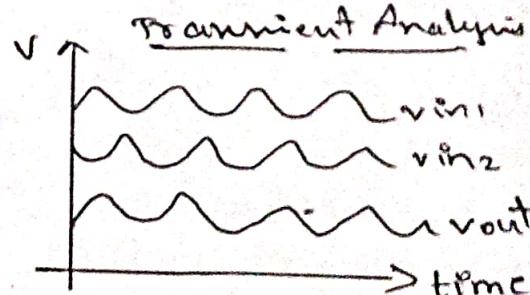
Graphs:-



DC analysis



AC analysis



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## Results:

$$\rightarrow N_0 = \\ N_{1,2} = \\ N_{3,4} = \\ N_{5,6} = \\ N_{7,8} =$$

$$Gain \text{ (dB)} =$$

$$d \text{ (dB)}$$

$$V_{bf} \text{ (dB)} =$$

$$V_{in1} \text{ (P-P)} =$$

$$V_{in2} \text{ (P-P)} =$$

$$V_{out} \text{ (P-P)} =$$

$$AV =$$

Inference :

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_ Hernanthi S.

Dept./Lab Aico Lab Class \_\_\_\_\_ Expt./No. 07

Title Design & Analysis of Two stage OPAMP.

### Objective:-

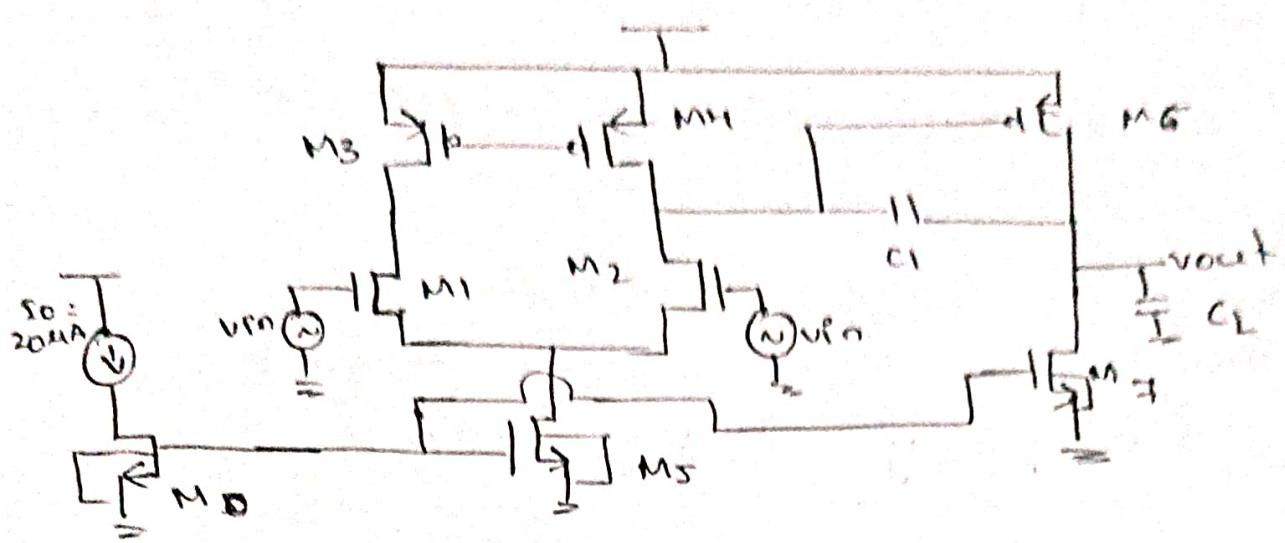
- (i) To design and analyse a 2 stage opamp using NMOS differential pair for the given spec.
- (ii) To perform DC analysis & obtain the DC operating points, small signal parameters & node voltages.
- (iii) To perform AC analysis & obtain AC gain, 3dB freq, UGF.
- (iv) To perform transient analysis to calculate P-P voltage.

### Specifications:-

Parameters	Specified values
Supply voltage	1.8V
Power consumption	≤ 300mW
Small signal gain	> 60dB
G <sub>BW</sub>	30MHz
Slewrate	20V/ms
Load capacitance	2PF
I <sub>CNR</sub>	0.8 - 1.6V

### Circuit Diagram:-

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Two stage opamp with frequency compensation.

$$V_{in1} = V_{in2} = 1.04V$$

$V_{in1}$	$V_{in2}$
Ac	0
Phase	180

Intial	0
Phase	180

### Procedure :-

- (i) Draw the circuit as shown with NCFs as given.
- (ii) From the cell view , select launch, ADEL , then Perform DC analysis
- (iii) DC analysis performed with any , Save dc operating point
- (iv) After DC - Analysis in Analog Environment window, select Results  $\rightarrow$  Print  $\rightarrow$  DC operating point & select device
- (v) AC analysis with V<sub>sin</sub> voltage source at i/p is performed with freq. range from  $1 \rightarrow 104\text{Hz}$
- (vi) select outputs  $\rightarrow$  to be plotted  $\rightarrow$  select o/p voltage & wire for v<sub>out</sub> in schematic.

# R.V. COLLEGE OF ENGINEERING

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

- (vii) Perform transient analysis by selecting op-amp M1 from schematic & plot both the op-amp waveform & calculate the P-P voltage swing.
- (viii) Using AC analysis response plot the graph.

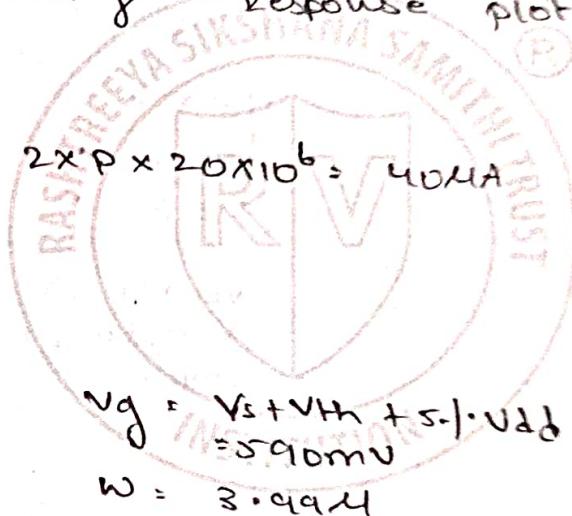
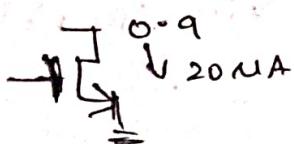
### Design

$$I_{ss} = C_L \times S_L \Rightarrow 2 \times 10^{-6} \times 20 \times 10^6 = 40 \text{ mA}$$

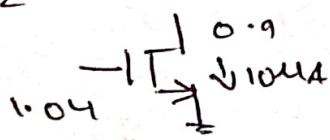
$$V_{th} = 500 \text{ mV}$$

$$S_f \cdot g_{VDD} = 90 \text{ mV}$$

M5



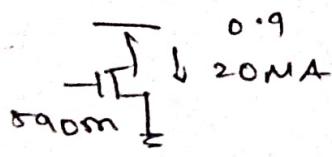
M1, M2



$$V_{gs} = V_s + V_{th} + S_f \cdot V_{dd}$$

$$W_1 = 1.882 \mu\text{m}$$

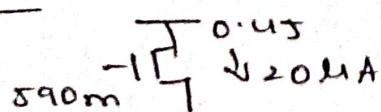
M4 :-



$$V_g = 590 \text{ mV}$$

$$W_4 = 3.810 \mu\text{m}$$

M0 :-



$$V_g = 590 \text{ mV}$$

$$W_0 = 3.99 \mu\text{m}$$

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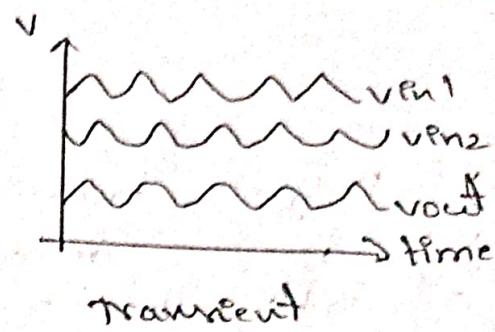
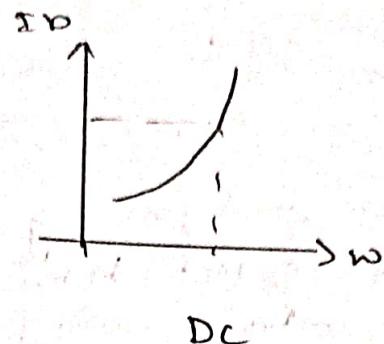
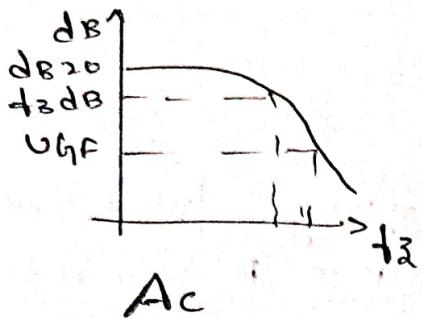
M<sub>3,4</sub>

$$10mA \text{ at } 0.9 \text{ V}$$

$$\omega_{3,4} = 922.93 \text{ rad/s}$$

$$V_g > 0.9 \text{ V}$$

Waveform:-



Results

$$\begin{aligned} \omega_0 &= \\ \omega_1 &= \\ \omega_2 &= \\ \omega_3 &= \\ \omega_4 &= \\ \omega_5 &= \\ \omega_6 &= \\ \omega_7 &= \end{aligned}$$

$$\text{Gain} =$$

$$+3 \text{ dB} =$$

$$\text{UGF} =$$

$$V_{out}(P-P) =$$

$$V_{in2}(P-P) = V_{in2}(P-P) =$$

$$AV =$$

Inference:-

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_

Name Hemanth S

Dept./Lab AICD Lab

Class \_\_\_\_\_

Expt./No. 08

Title Design and Analysis of Bandgap Reference.

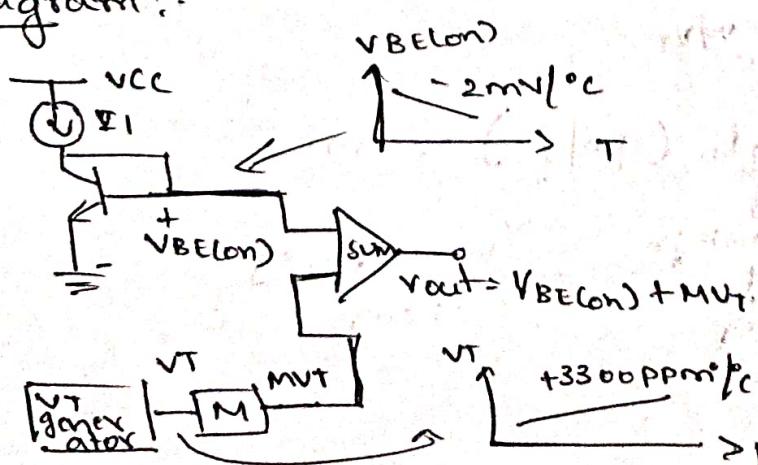
### Objectives:-

- (i) To design & analyse a bandgap reference for the given specifications.
- (ii) To perform DC analysis and obtain the DC operating points & Node voltages.
- (iii) To perform DC analysis over temperature & observe the variation of the reference.
- (iv) Estimate the avg. variation over a temp. range.

### Specification:-

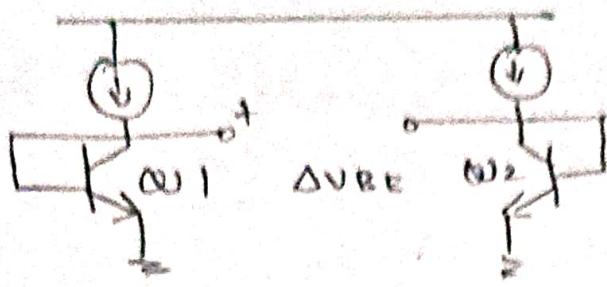
Parameter	Specified value
Supply Voltage	3.3 V
DC Bias current	5 mA
Number of diodes	2

### Circuit diagram:-

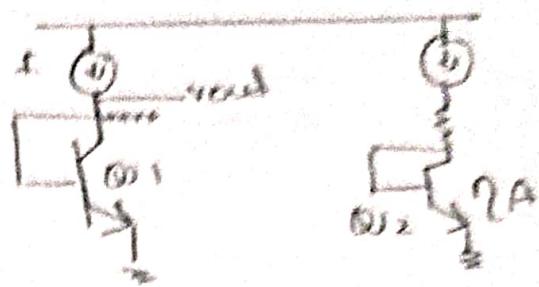


Fig(a) Bandgap  
Reference  
generation

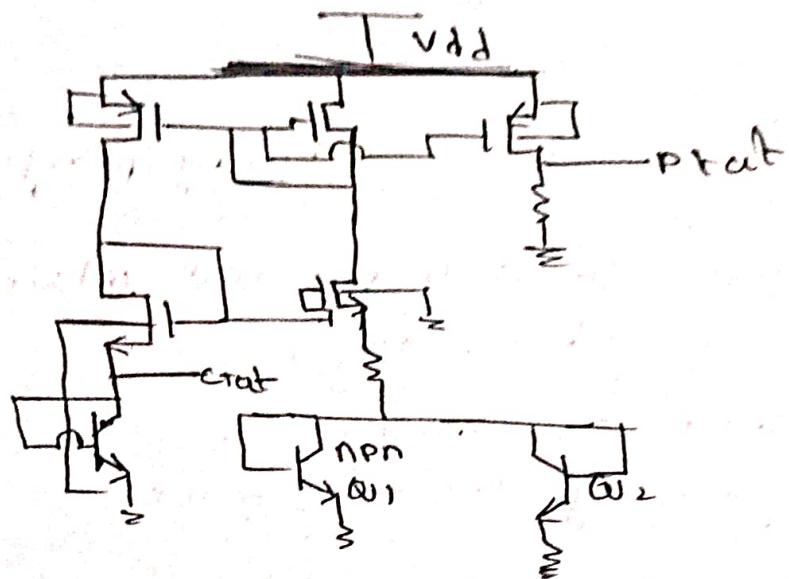
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PTAT generation



concept of BGR



complete BGR circuit.

## Design

Specification  $\rightarrow V_{DD} = 8.3V$        $N = 2$  for PTAT generation  
 $I_{DC} = 5mA$

CTAT

$$I_D = I_{D0} e^{\frac{V_D}{NVT}}$$

$$V_0 = V_{Tn} \ln \left( \frac{I_D}{I_S} \right) \Rightarrow \text{CTAT}$$

Weak fn of Temp.      Strong fn of Temp.

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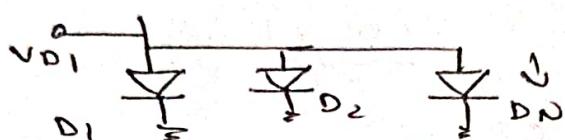
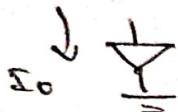
## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

PTAT



$$I_0 = n \Sigma$$

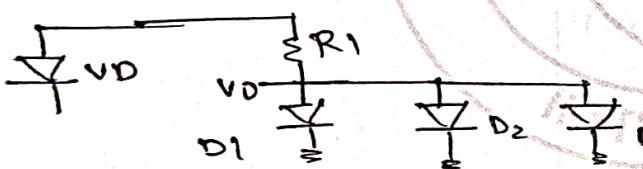
$$V_{D1} = V_T \ln\left(\frac{I_0}{I_s}\right)$$

$$\Rightarrow V_T \ln\left(\frac{I_0}{n I_s}\right)$$

$$V_D - V_{D1} = V_T \ln\left(\frac{I_0}{I_s}\right) - V_T \ln\left(\frac{I_0}{n I_s}\right)$$

$$\Rightarrow V_T \ln(n)$$

A  $\uparrow$   $T \uparrow$   $V_T \uparrow$



$$V_D - V_{D1} = \Sigma I R_1 = V_T \ln(n)$$

$$I_0 = \frac{V_T}{R_1} \ln(n)$$

$$V_R2 = \Sigma I R_2 = V_T \ln(n) \underbrace{\frac{R_2}{R_1}}$$

$$V_{RD2} = \alpha V_T \rightarrow \alpha_1 \xrightarrow{\text{PTAT}}$$



separate PTAT

$$S_{D1} \alpha_1 = \frac{R_2}{R_1} \ln(n)$$

$$V_{ref} = \alpha_1 \text{PTAT} + \alpha_2 \text{CTAT}$$

$$\Rightarrow \alpha_1 V_T + \alpha_2 V_D$$

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$$\frac{dV_{BEF}}{dt} = 0 \Rightarrow \alpha_1 \frac{dV_F}{dt} + K_1 \frac{dV_B}{dt} = 0$$

$$\alpha_1 \left( \frac{dV_B}{dt} \right) + K_1 (-1.6mV) = 0$$

Assume  $K_1 = 1 \Rightarrow \alpha_1 = \frac{1.6mV}{-1.6mV} = -12.82$

NOW  $I_D = SVA \quad N=2$  for PTAT

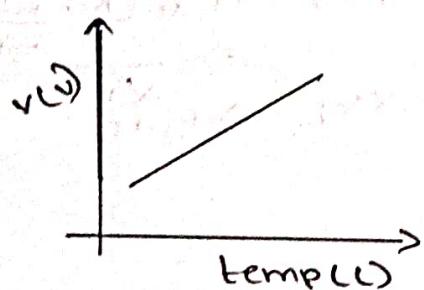
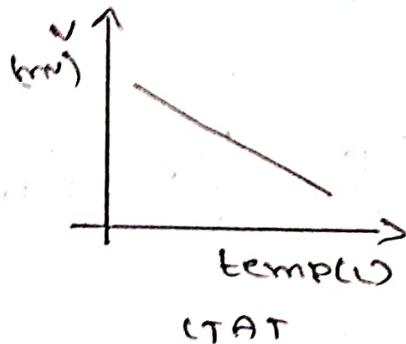
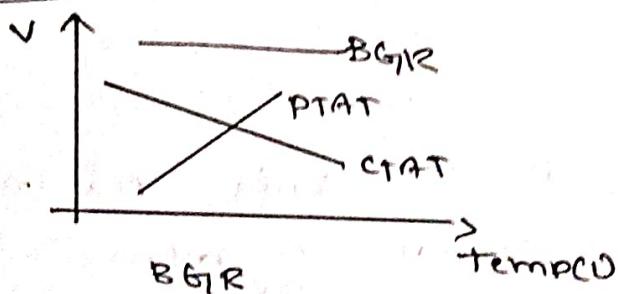
$$V_D - V_{D1} = I_D R_1 = V_T \ln(N)$$

$$R_1 = \frac{V_T \ln(N)}{I_D} = \frac{2.6m \times \ln(2)}{5A} \\ = 3.604 \text{ k}\Omega$$

$$\text{Also } \alpha_1 = R_2 / R_1 \ln(N)$$

$$R_2 = \frac{R_1 \alpha_1}{\ln(N)} = 97.8 \text{ k}\Omega$$

Graphs:



PTAT

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expt./No. \_\_\_\_\_

Title \_\_\_\_\_

Results:-



Inference!:-

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Teacher Incharge

# R.V. COLLEGE OF ENGINEERING®

## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth S

Dept./Lab AICD Lab Class \_\_\_\_\_ Expt./No. 09

Title Layout of CS Amplifier

### Objectives:-

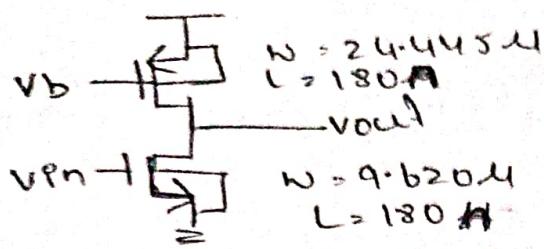
- (i) TO create layout for a common source amplifier, with current source pmos load.
- (ii) TO perform dc Analysis, AC analysis & obtain dc gain bandwidth & unity gain freq.
- (iii) TO perform transient analysis & check gain for a small signal of 2mV p-p 1KHz.
- (iv) Estimate gain & o/p impedance of both current source.
- (v) compare prelayout & post layout simulation results.

### Specification:-

Parameters	specified values
Supply voltage	1.8V
Power	$\leq 250 \text{ mW}$
UGF	150MHz
Load capacitance	100fF

### Circuit diagram:-

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### Procedure:-

- (I) Draw the CS ampli schematic with PMOS & NMOS length 180μm & width according to value obtained for design spec.
- (II) Create symbol
- (III) Perform DC analysis
- (IV) Create layout through ADE window.
- (V) Perform RL extraction.
- (VI) Observe the DC gain, UGF & 3dB freq, using AC analysis in range 1 → 106 Hz

### Analysis:-

- (I) operating point of transistor M<sub>1</sub> & M<sub>2</sub> :-

Transistor	$V_s(V)$	$V_o(V)$	$V_g(V)$	$V_d(V)$	$\Sigma O$	$L$	$W$
M <sub>1</sub>							
M <sub>2</sub>							

- (II) Prelayout & post layout simulation:-

Simulation type	Gain	3dB-freq & UGF
Prelayout		
Post layout		

### Inference:-

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## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name Hemanth.S \_\_\_\_\_

Dept./Lab Aics Lab Class \_\_\_\_\_ Expt./No. 10

Title Layout of Differential Amplifier with Active Load

### Objective:-

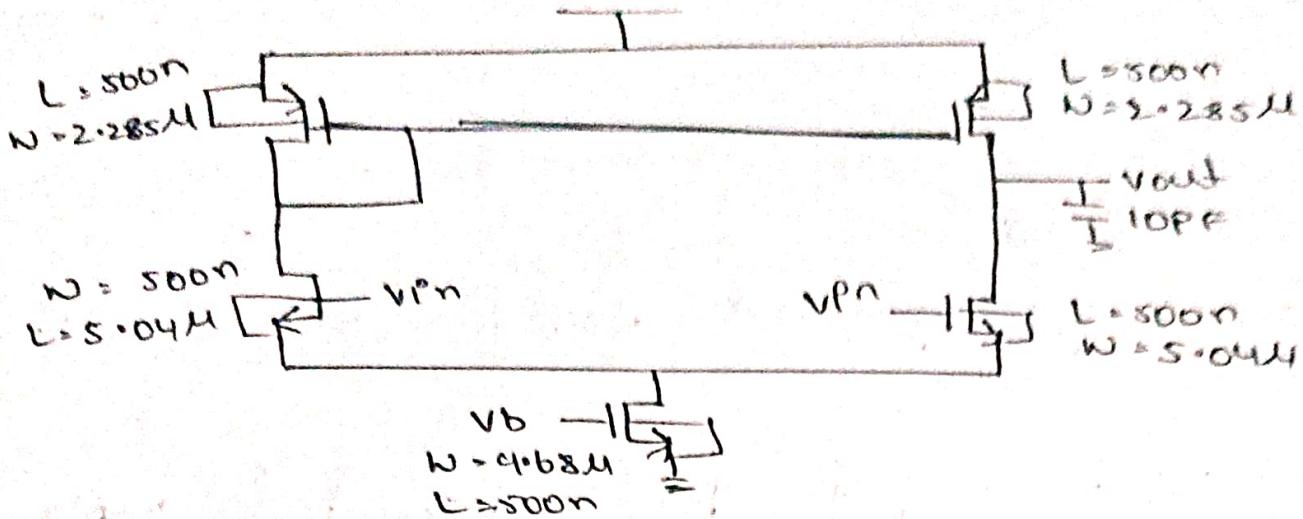
- (i) To create Layout for a differential amplr with active load.
- (ii) To perform DC analysis, AC analysis, & obtain DC gain, Bandwidth & VGF
- (iii) To perform transient analysis & check gain for a small signal of 10mV p-p at 10KHz.
- (iv) Estimate gain & o/p impedance of the Ckt
- (v) compare prelayout & post layout simulation results.

### Specification:-

Parameters	Specified Values
Supply Voltage	1.8V
Gain	40dB
ICMR	0.8V
ICMRE	1.6V
Load cap.	10PF
Slew rate	5V/nas
Gain Bandwidth Product	5MHz

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## Circuit Diagram:



### procedure:-

- (i) Draw the differential amplifier schematic with pmos and nmos length as soon & width acc. to value obtained from design specifications.
  - (ii) Create symbol, draw test ckt.
  - (iii) Perform DC analysis to know DC operating point
  - (iv) Create the layout through ADE window.
  - (v) Perform RC Extraction.
  - (vi) Observe the DC gain, NGF & 3dB frequency using AC analysis in the range 1-10Ghz.

### Analysis :-

(1) operating point of transistor using

Transistor	$V_S(V)$	$V_D(V)$	$V_G(V)$	$V_B(V)$	$I_D(MA)$	$\omega$
M0	-0.5	-0.5	-0.5	-0.5	0	0
M1 ( $m_2$ )	-0.5	-0.5	-0.5	-0.5	0	0
M2 ( $m_3$ )	-0.5	-0.5	-0.5	-0.5	0	0

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## OBSERVATION / DATA SHEET

Date \_\_\_\_\_ Name \_\_\_\_\_

Dept./Lab \_\_\_\_\_ Class \_\_\_\_\_ Expl./No. \_\_\_\_\_

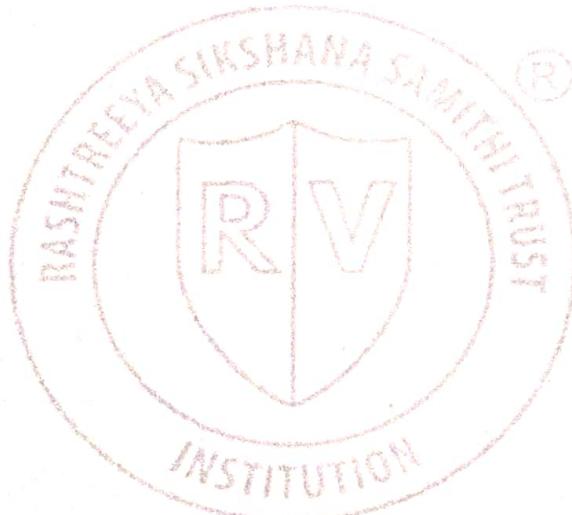
Title \_\_\_\_\_

(i) Pre layout Post layout simulation.

Simulation type Gain (dB) 3dB - f<sub>cen</sub> (kHz) UGF (MHz)

Pre layout  
Post layout

Inference:-



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