ELSEVIER

PII: S0142-0615(96)00045-2

Electrical Power & Energy Systems, Vol. 19, No. 4, pp. 221–227, 1997

0142-0615/97/$17.00+0.00

The implementation and effectiveness of linear interpolation within digital simulation

P Kuffel and K Kent
Manitoba Hydro, 820 Taylor Avenue, Winnipeg, Manitoba, Canada

G Irwin
Manitoba HVDC Research Centre, 400–1619 Pembina Highway, Winnipeg, Manitoba, Canada

*The greater use of detailed models and the increasing size and complexity of system studies in power system digital simulation has resulted in the need to re-examine the ability of digital computations performed at finite time intervals to accurately represent the actual system. These concerns are manifested in two distinct areas. The first is the ability to switch elements at a specific point in time. Traditional digital simulation techniques allow switching elements to change state only at discrete computation times, whereas in reality switching can occur at any instant in time. The second area of concern is in the ability to accurately represent detailed control systems. These concerns are of particular importance in simulations containing a large number of controlled switching devices, such as HVdc systems or ac systems containing FACTs devices. This paper presents a discussion of the implementation and effectiveness of linear interpolation techniques in a digital simulation program. The paper addresses interpolation in both the network solution and the control system. The CIGRE HVdc Benchmark Model (Szechtman, M. et al., Electra, 1991, **135** and Wess, T. and Ring, H., CIGRE Report, WG 14-02, 1988) with detailed control models is used to demonstrate how linear interpolation is implemented and its effectiveness. All simulation results presented were generated using EMTDC (Nayak, O. et al., IEEE Computer Applications in Power, 1995, 8(1)), but the techniques discussed can be applied to any electromagnetic transients program.* © Elsevier Science Ltd. All rights reserved.

Keywords: digital simulation, Interpolation, HVdc, controls

I. Introduction

In the past, digital simulations of HVdc systems consisted of small network models, so concerns related to time step errors could be addressed by reducing the time step size. This solution resulted in significantly increased run times, however since the system model was small, the study turnaround time penalties associated with simulation time step reduction were acceptable. Reduction of the time step size was also an effective way to reduce the inherent discretization errors within the controls model. However, as the combination of increased system model size and the use of detailed controls models has become more common [1–3], the reduction of simulation time step size has become an impractical solution.

The use of trapezoidal integration as the solution method in electromagnetic transients programs [4] is based on the assumption that the change of any parameter from one time step to the next is linear. Since the change in a given parameter across a time step is assumed to be linear, it is possible to implement interpolation between time steps. This can effectively result in a "quasi-continuous time" solution with very little impact on overall run times.

Some presently available electromagnetic transient simulation programs employ interpolation techniques [5,6].

Interpolation can be implemented in two distinct areas. The first of these is in the network solution, and the second is in the controls model.

II. Interpolation within the network solution

A basic electromagnetic transients solution algorithm solves the network differential equations by applying trapezoidal integration in discrete time steps. The selection of the time step is usually based on the time constants in the system model. A typical time step for most transient studies is 50 μs. However, when fast acting switching devices such as thyristors, diodes, or surge arresters must be modelled, the 50 μs time step may not provide sufficient accuracy in the simulation of these devices.

To illustrate this, Figure 1 shows an example of a current through a diode (or thyristor).

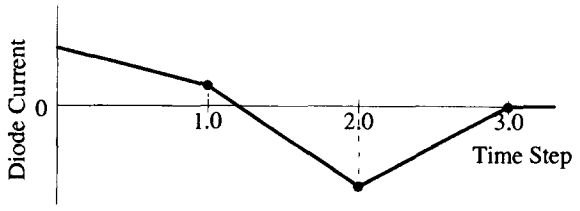

Figure 1. Simulated diode switching off at a current zero—fixed time step

Referring to Figure 1, the diode should switch off when the current goes through zero, but due to the time step chosen, it will not be turned off until time 2.0. This error in the switching time can result in the following negative effects:

- incorrect power flow due to inaccurate firing times and controller errors,
- switching instabilities due to interactions between many switching devices,
- the generation of non-characteristic harmonics,
- errors in the overall solution.

A smaller time step can be used to minimize these errors, but will result in longer execution times. A multiple or variable time step algorithm can also be applied, but requires significant structural changes to existing programs and will result in longer execution times.

Linear interpolation can be applied to eliminate the above problems without significantly increasing execution times or affecting the overall structure of electromagnetic transient type programs. Figure 2 shows the same diode current but with a basic interpolating switching algorithm. After the main program calculates the voltages and currents at time 2.0 (but before proceeding to the next time step), all switching devices are polled to see if their switching criteria has been met. For example, the diode's criteria would be to switch its branch resistance to a high value when the current goes negative. Each device polled then returns a quantity X (where $0.0 < X < 1.0$) which is the fraction of a time step when it should have switched. The minimum X value, indicating the device to switch first, is then used to interpolate all system voltages and currents to this point. The network conductance matrix (G) can then be retriangularized normally to implement the switching, using a Gaussian type solution method.

In the example, $X = 0.2$, and the voltages and currents are given by:

$$v(1.2) = v(1.0) + 0.2(v(2.0) - v(1.0)) \text{ and}$$

$$i(1.2) = i(1.0) + 0.2(i(2.0) - i(1.0))$$

Or, in general form:

$$v(T - \Delta t + X\Delta t) = v(T - \Delta t) + X(v(T) - v(T - \Delta t)) \text{ and}$$

$$i(T - \Delta t + X\Delta t) = i(T - \Delta t) + X(i(T) - i(T - \Delta t))$$

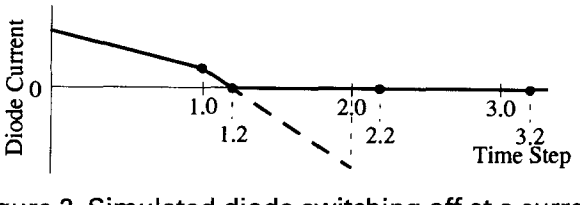

Figure 2. Simulated diode switching off at a current zero—with interpolation

where T is time at the end of the regular time step and Δt is the time step.

The interpolation is a very fast operation compared to the time required to re-solve the network due to the switching. In some algorithms, the interpolation can also be limited to a local subsystem, since each subsystem is mathematically isolated from other subsystems by the inherent delays in the travelling waves on transmission lines and cables of sufficient length for a given solution time step.

Once the system voltages and currents are obtained at time 1.2, a normal time step can be taken to time 2.2. The polling procedure should be repeated to check for additional switching requirements before the end of the time step. Figure 2 shows the normal time steps continuing to 2.2, 3.2, etc., but this may not be a practical method to implement in existing programs as all controls and system models would have to recognize the effective time step shift in their local integration scheme. A suitable alternative would be to do one final interpolation between 1.2 and 2.2 to return back to time 2.0, which is back on the original time step. Note that the time step has not been changed (which would require the time consuming task of rebuilding the entire G matrix) and the control system and other dynamic models are still only evaluated at the regular fixed time step intervals.

Figure 3 shows the switching sequence and method used for all studies in this paper. An additional 1/2 step interpolation is automatically invoked after every time step in which a switching occurs. This eliminates time step to time step numerical oscillations (chatter) in inductive node voltages or in the current in capacitive loops which can result from the use of trapezoidal integration. Other solutions to eliminate chatter have been to add artificial damping resistors or to take two rectangular integration time steps, known as the Critical Damping Adjustment (CDA) method [7].

The 1/2 step interpolation method used here has the advantage that it always uses the proven and stable trapezoidal integration method and requires no extra programming once a basic interpolation algorithm has been implemented. Since chatter can also be initiated from transients other than switching, such as steps in voltage or current sources, a chatter detection algorithm should also be used to observe all node voltages and system currents for chatter.

This interpolation method is nearly transparent to all other controls and system models and can thus be implemented in existing programs without major compatibility problems. An enhancement of the method described above which allows instantaneous transitions due to switching operations as opposed to transitions which occur over one time step, is presently being tested.

III. Example—basic forced commutation circuit

The simple circuit in Figure 4 is the basis of many power electronic and FACTS devices which employ a Gate

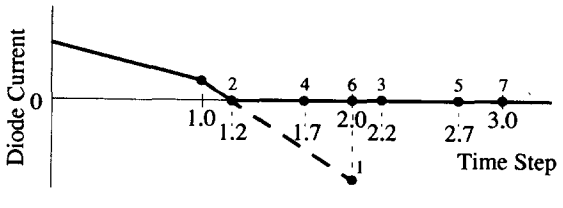

Figure 3. Diode switching off at a current zero with interpolation and chatter removal

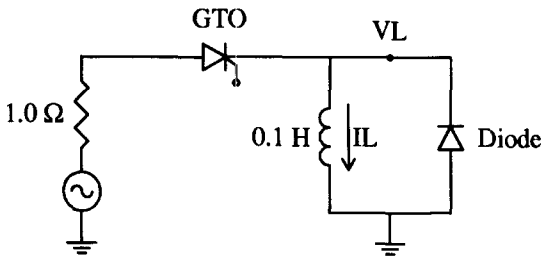

Figure 4. Basis of forced commutation in inductive circuits

Turn-Off device (GTO) and a free-wheeling diode. Note that the inductor could be the reactance of a transformer.

Figure 5 shows the simulated inductor voltage (*VL*) when the GTO is turned on and off at 100 Hz, and Figure 6 shows the inductor currents (*IL*). The simulation time step is 50 μS and snubber circuits are not used across either the GTO or the diode.

When the GTO interrupts the inductor current (*IL*), a large voltage spike is created due to the $L\,di/dt$ effect. However, the diode across the inductor should conduct almost immediately so that the current can circulate in the diode-inductor loop.

This circuit is challenging for simulation using digital EMT techniques, because *VL* is an inductive node subject to numerical chatter, and the diode must turn on almost immediately after the GTO turns off.

Each figure has three plots:

(1) with chatter removal and with interpolation
(2) with chatter removal, but without interpolation and
(3) without chatter removal and without interpolation.

When both chatter removal and interpolation techniques are used, the waveforms are as expected. Note that the dc offset in the inductor current (*IL*) in Figure 6 is maintained.

When only a chatter removal technique is employed, but interpolation is not used, the results seem realistic, except that *VL* shows a large negative voltage spike (approximately −4,000 kV) when the GTO first turns off because the inductor is open-circuit for one time step. Note that the inductor current also falls to 0 instead of maintaining the dc offset. If interpolation was used, the diode would conduct when the voltage crosses 0, and the voltage would remain at 0. Reducing the simulation time step would have little effect in this case, but adding artificially large snubber circuits to provide an alternate path for the inductor current would improve the results slightly.

Without chatter removal or interpolation, the results show severe numerical oscillations initiated by the use of trapezoidal integration at an inductive node. The voltage in the third graph of Figure 5 oscillates from approximately 15,000 to −15,000 kV. The oscillation is driven by the chatter

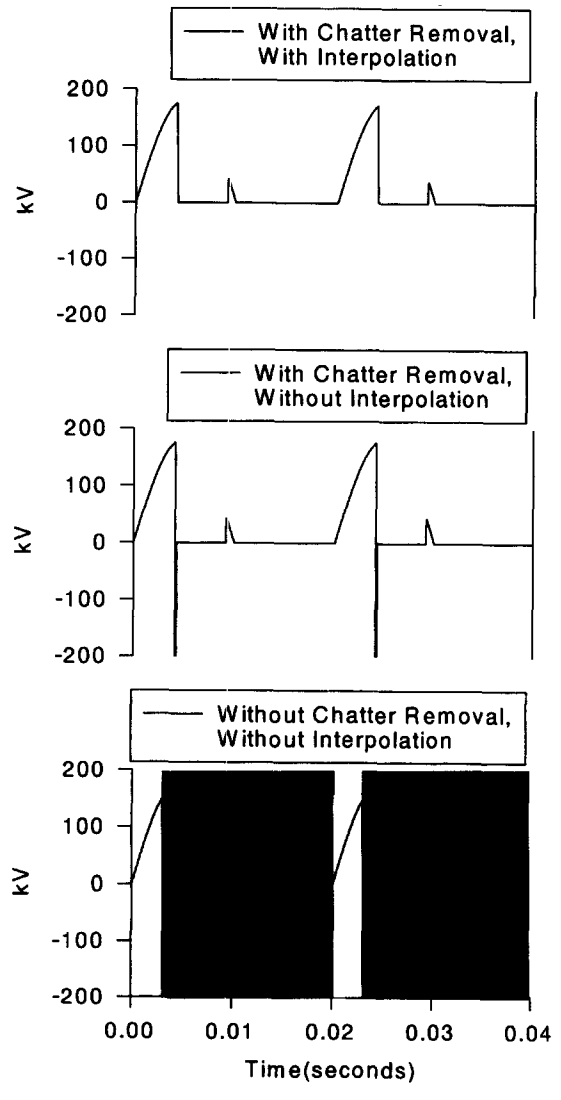

Figure 5. Inductor voltage (*VL*)

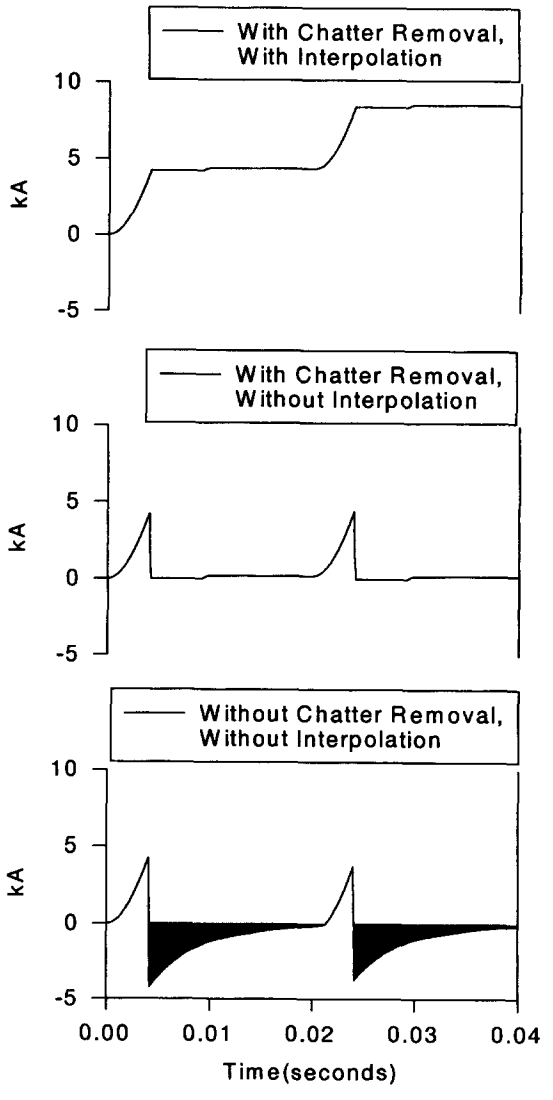

Figure 6. Inductor current (*IL*)

phenomena, but is affected by the repeating diode switching. This appears as a solid black region on the same scale as the other plots, and is clearly not realistic.

IV. Interpolation within the control models

Historically, control system models were only processed at the discrete times defined by the simulation time step. To conform with standard models, the implementation of linear interpolation within the controls models must involve the correction of control system elements to account for events which occurred at any instant in time between the fixed solution time step.

In order to demonstrate how this is accomplished, consider the measurement of the extinction angle for an HVdc inverter valve. The extinction angle is defined as the time from the instant when the current in the valve goes to zero to the time that the voltage across the valve goes positive. One method of measuring the extinction angle in a practical control system is to start an integrator at the instant in time that the valve current extinguishes and sample the integrator output at the instant in time that the voltage across the valve becomes positive. The sampled value is then a representation of the extinction angle for that valve.

Consider the CIGRE HVdc Benchmark Model [8,9] extinction angle measurement circuit as shown in Figure 7. The input to the integrator and the integrator time constant are chosen such that the sampled output of the circuit is a direct measure of the extinction angle, if the system frequency is assumed to be constant at 50 Hz. The CIGRE Benchmark Model is configured such that the normal controlled value of the extinction angle at the inverter is 15°. For the output of the circuit to be equal to 15° the time between current zero in the valve and positive voltage across the valve must be exactly 833.3333 μs. With a 50 μs time step, for example, the nearest solution point where the extinction angle measurement could occur would be at 850 μs.

Figure 8 shows the operation of this control circuit calculated at discrete time steps. As is seen from Figure 8a, the start of the integrator is delayed by time dt_1, which can be up to one time step. Likewise from Figure 8b it is seen that the sampling of the output is delayed by time dt_2, which can also be up to one time step. Although these two errors counteract each other, the net result is that a maximum error of one time step can result. Although an error of one time step may not appear to be substantial, if the solution time step is 50 μs (which is typical), one time step corresponds to 0.9° for 50 Hz systems. This translates to a 6% error if the desired extinction angle is 15°.

In order to implement linear interpolation within this circuit, it is necessary to calculate correction factors at both the time step of starting the integrator and at sampling of its output. With reference to Figure 8a, the correction factor required at the time step of starting the integrator

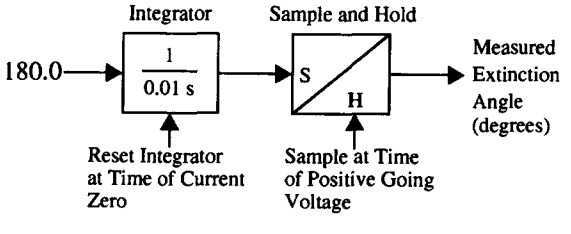

Figure 7. Extinction angle measurement circuit used in the CIGRE HVdc benchmark model

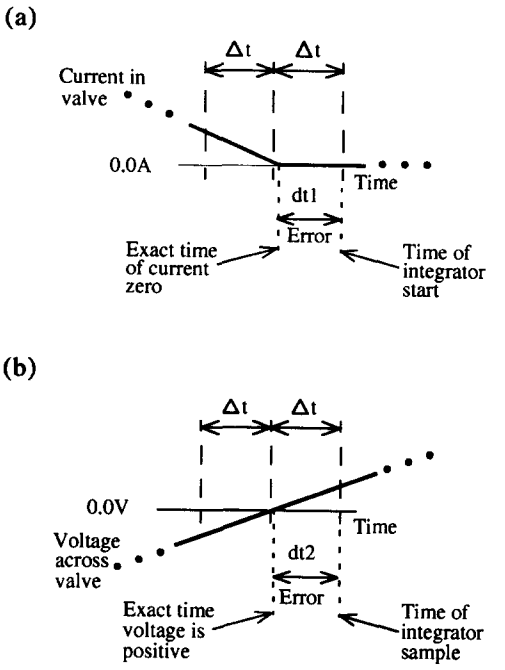

Figure 8. Simulation of extinction angle measurement circuit without interpolation. (a) Start of integrator and (b) sampling of integrator

corresponds to the output of the integrator over time dt_1 and is given by:

$$\text{Offset at start of integration} = (180.0/0.01)dt_1 \quad (1)$$

This correction factor is then applied as an offset to the integrator when it is started. With reference to Figure 8b, the correction factor required at the time step of sampling the integrator corresponds to the negative of the output of the integrator over time dt_2 and is given by:

$$\text{Offset at time of sampling} = -(180.0/0.01)dt_2 \quad (2)$$

This correction factor is applied as on offset to the value to be sampled at the time step of sampling.

Figure 9 shows a comparison of the outputs of the extinction angle measurement circuit shown in Figure 7 with and without linear interpolation.

The input signals for the example were configured to produce an extinction angle of exactly 15° and the simulation

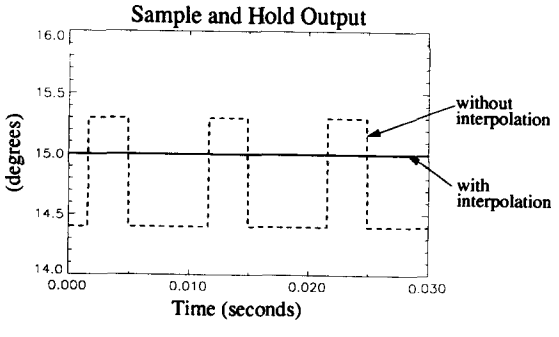

Figure 9. Comparison of the output of the extinction angle measurement circuit with and without interpolation

time step used was 50 μs. From Figure 9 it can be seen that the case with interpolation produces the exact expected result, whereas the case without interpolation produces a result which varies between 14.4° and 15.3°. The total variation in the output is therefore 0.9° which corresponds to an error of one time step as given by:

$$\frac{0.9 \times 0.01}{180.0} = 50.0\,\mu s \qquad (3)$$

It has been shown [1–3] that simplified generic transfer function models may not accurately simulate the dynamic response of a system. This is partly because standard control building blocks which are supplied with electromagnetic transient simulation programs may not include interpolation features. As such, detailed studies require the development of custom control functions, in which interpolation techniques can be incorporated.

V. Case studies

In order to evaluate the effectiveness of linear interpolation, the CIGRE HVdc Benchmark Model [8,9] was used. The Benchmark model is a 50 Hz, monopolar cable system rated at 1000 MW and 500 kV. It has a low reactance in the dc circuit and a large dc cable capacitance. The inverter compensation is made up of shunt capacitors and ac filters, including a low order damped filter. The inverter is normally in extinction angle control and the rectifier is in current control.

The effectiveness of interpolation is demonstrated with two sets of Benchmark Model cases:

(1) steady state operation at various time steps to evaluate the steady state response, and
(2) a three-phase inverter ac bus fault for various time steps to evaluate the dynamic response.

Three levels of interpolation were considered:

(1) interpolation within the controls and the network solution,
(2) interpolation within the network solution only, and
(3) no interpolation within the controls or network solution.

Since the inverter extinction angle is particularly sensitive to time step errors as discussed above, this parameter is presented as a measure of the effectiveness of interpolation to improve the accuracy of the overall solution.

The control system used in the Benchmark model [9] contains many features typically found in actual HVdc systems. These include high response (minimal lag) controls, and controls whose inputs consist of square, pulse type signals. These types of controls are very sensitive to time step related errors due to their fast response and dependence on the exact time that a step change occurs at their inputs. The extinction angle controller, the current error controller, and the phase locking circuits within the Benchmark Model are examples of such circuits.

VI. Discussion of results

VI.1 *Steady state performance*

Figure 10 shows the variation of the measured extinction angle obtained under steady state conditions, for the three levels of interpolation at each simulation time step considered. The results in Figure 10 show a significant reduction in

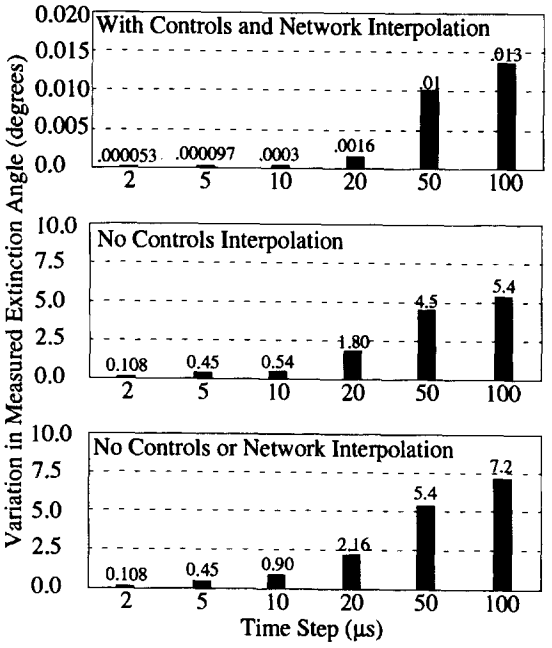

Figure 10. Steady state variation in the measured extinction angle at various simulation time steps

the variation of measured extinction angle in the case with full interpolation within both the control system and network solution. This is true even when comparing the larger simulation time step results for the case of full interpolation with the reduced simulation time step results for the cases with only partial or no interpolation. The results for the cases with partial or no interpolation also show a variation in the measured extinction angle which is significantly larger than that which is expected due to a single time step error in the measurement, as was discussed previously. This increased variation is caused by the response of the overall system to all of the inherent single time step errors in the solution of the control system and network models. The magnitude of the interaction depends on the system and controls being simulated. This illustrates the need to carefully coordinate the control modeling with the network solution.

Figure 11 shows the CPU times obtained for one second of simulation on a DEC Alpha 3000 Model 900 workstation for the three levels of interpolation, at each simulation time step considered. The results in Figure 11 show that the inclusion of the full interpolation results in a very minor increase in run times for a given solution time step. The results also show the

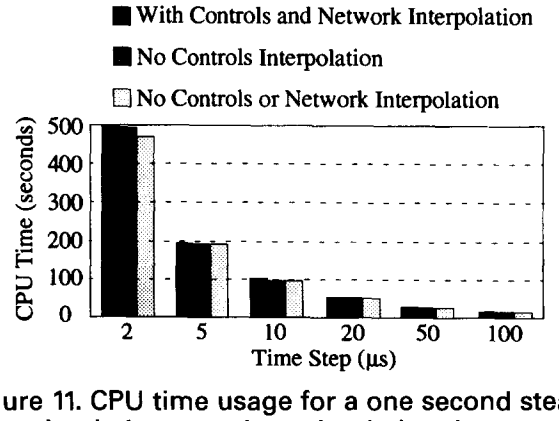

Figure 11. CPU time usage for a one second steady state simulation at various simulation time steps

significant run time penalties associated with solution time step reduction, regardless of the level of interpolation included. The run times are seen to be inversely proportional to the time step.

VI.2 *Dynamic performance*

In Figures 12 and 13, the measured extinction angle and inverter dc current are shown, for a five cycle inverter ac commutating bus three phase to ground fault. The figures present results for time steps of 2, 20, 50 and 100 μs only, in order to make the curves distinguishable. Results for 5 and 10 μs time steps are not shown since they are very similar to the corresponding results obtained for a 2 μs time step.

The results in Figures 12 and 13 show good agreement for all three levels of interpolation at a time step of 2 μs. This is to be expected, since the effects of single time step errors on the overall solution become less pronounced as the time step is reduced. However, when the solution time step is increased, discrepancies between the results for corresponding time steps with different levels of interpolation are apparent.

The case of full interpolation within the control system and network solution shows consistent results regardless of the simulation time step. For cases with only partial or no interpolation, the results at larger time steps are drastically different. Specifically, the 50 and 100 μs time step cases show secondary commutation failures during the recovery, as evident from the measured extinction angle of zero and a corresponding sharp increase in the measured current, whereas cases with smaller time steps or full interpolation are not even close to commutation failure.

VII. Conclusions

The implementation of interpolation and the results presented indicate the following:

(1) the implementation of interpolation within the network

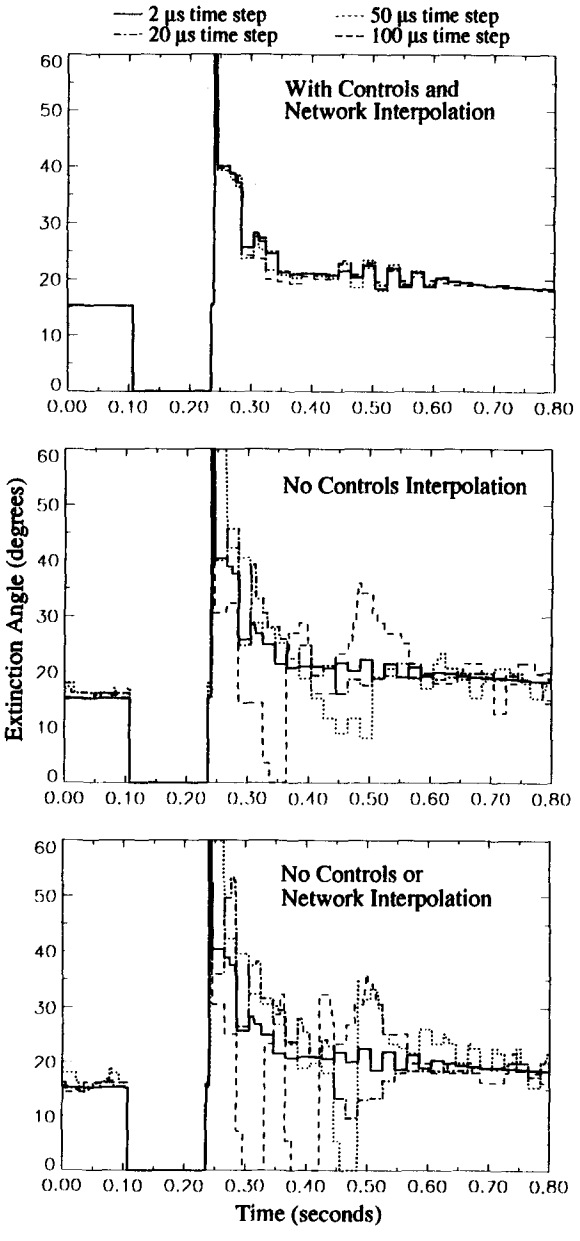

Figure 12. Measured extinction angle for a 5 cycle inverter 3-phase fault at various simulation time steps

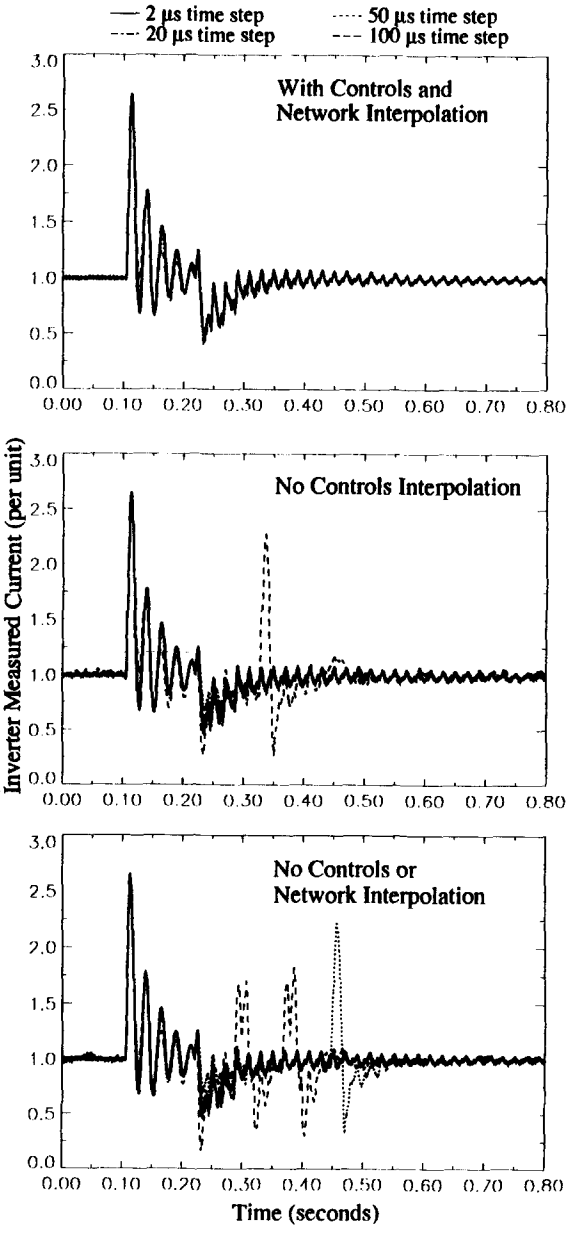

Figure 13. Measured inverter current for a 5 cycle inverter 3-phase fault at various simulation time steps

and control models resulted in a significant improvement in accuracy for a given simulation time step;

(2) improvements in accuracy were also realized by reducing the simulation time step, however the time step had to be reduced substantially to obtain any significant gains in accuracy;

(3) the use of interpolation within the network and control models had a negligible effect on execution time, whereas a reduction in the simulation time step resulted in an increase in the execution time which was inversely proportional to the reduction in the time step size;

(4) the implementation of interpolation within the network and control models must be carefully coordinated to result in improved accuracy;

(5) the implementation of interpolation within an existing digital simulation program was accomplished without major compatibility problems;

(6) the implementation of interpolation within the network solution provided an effective means of incorporating numerical chatter removal, which can further improve the accuracy of results;

(7) in the cases not using interpolation inconsistent results which were dependent on the time step chosen were obtained. The use of interpolation produced consistent results over the entire range of time steps studied.

In summary, the use of interpolation within the network solution and control model in electromagnetic transient simulation programs provides a significant improvement in the accuracy of results, thus increasing confidence, without sacrificing efficiency.

VIII. References

1. Kuffel, P., Kent, K. L., Mazur, G. B. and Weekes, M. A., Development and validation of detailed control models of the Nelson river bipole I HVDC system. *IEEE Transactions on Power Delivery*, 1993, **8**(1), 351–358.
2. Hammad, A., Minghetti, R., Hasler, J., Eicher, P., Bunch, R. and Goldsworthy, D., Control modelling and verification for the Pacific intertie HVDC 4-terminal scheme. *IEEE Transactions on Power Delivery*, 1993 **8**(1), 367–375.
3. Morin, G., Bui, L. X., Casoria, S. and Reeve, J., Modeling of the Hydro Quebec–New England HVDC system and digital controls with EMTP. *IEEE Transactions on Power Delivery*, 1993, **8**(2), 559–566.
4. Dommel, H. W., Digital computer solution of electromagnetic transients in single- and multiphase networks. *IEEE Transactions on Power Apparatus and Systems*, 1969, **PAS-88**(4), 388–399.
5. Krueger, K. H. and Lasseter, R. H., HVDC simulation using NETOMAC, IEEE Montech '86, Conference on HVDC Power Transmission, Montreal, Canada 1986.
6. Nayak, O., Irwin, G. and Neufeld, A., GUI enhances electromagnetic transients simulation tools. *IEEE Computer Applications in Power*, 1995, **8**(1), 17–22.
7. Lin, J. and Martí, J. R., Implementation of the CDA Procedure in the EMTP. *IEEE Transactions on Power Systems*, 1990, **5**(2), 394–402.
8. Szechtman, M., Wess, T. and Thio, C. V., First benchmark model for HVDC control studies. *Electra*, 1991, **135**, 55–73.
9. Wess, T. and Ring, H., FGH Controls for the HVdc benchmark model study. Report presented to CIGRE WG 14–02, 1988.