Comparison Research between XY and Odd-Even Routing Algorithm of a 2-Dimension 3X3 Mesh Topology Network-on-Chip

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***Abstract*—The Network-on-Chip (NoC) has been recognized as a paradigm to solve System-on-Chip (SoC) design challenges. The routing algorithm is one of key researches of a NoC design. XY routing algorithm, which is a kind of distributed deterministic routing algorithms, is simple to be implemented. Odd-Even (OE) routing algorithm, whose implementation is complex, is a sort of distributed adaptive routing algorithms with deadlock-free ability. We demonstrate the two routing algorithms in details at first. XY routing algorithm and OE routing algorithm are then simulated and compared based on a 3X3 mesh topology NoC with NIRGAM simulator. The simulation results show that OE routing algorithm, whose P parameter equals to 1.09, increases P parameter greatly as compared to XY routing algorithm, whose P parameter equals to 0.86, in a 2-dimension 3X3 mesh topology NoC, with Constant Bit Rate (CBR) traffic condition of each tail.**

Keywords-system-on-chip; network-on-chip; xy routing algorithm; odd-even routing algorithm

I. INTRODUCTION

System-on-chip (SoC) designs provide integrated solutions to challenging design problems in the telecommunications, multimedia, and consumer electronics domains. However, the designs of SoCs encounter some challenges with the advanced process technologies and SoC complexity scales. The challenges include the negative effect of technology scaling on global interconnects, growing system complexity, the need to construct flexible multi-use designs and platforms and so on. The Network-on-Chip (NoC) has been recognized to solve these challenges [1-5]. The routing algorithm is one of key researches of a NoC design [6]. In this paper, we give an overview of NoC design approach in section two at fist. In section three, we present details of XY and Odd-Even (OE) routing algorithm. Section four gives the architecture of a 3X3 mesh topology NoC. Simulation results and analysis based on this topology are in section five. At last, conclusions are provided.

II. OVERVIEW OF NOC DESIGN APPROACH

According to NoC design approach, designers use network design technology to analyze and design SoCs. In other words, designers view a SoC as a micro-network of components. SoC interconnection design can be done using the micro-network stack paradigm, which is an adaptation of the protocol stack [7] (Fig. 1). Thus the electrical, logic, and functional properties of the interconnection scheme can be abstracted.

Global wires are the physical implementation of the communication channels. The trend toward faster and lower-power communication may decrease reliability as an unfortunate side effect. In NoC design approach, physical layer design finds a compromise between competing quality metrics and provide a clean and complete abstraction of channel characteristics to above micro-network layers [2]. The data-link layer abstracts the physical layer as an unreliable digital link. The main purpose of data-link protocols is to increase the reliability of the link up to a minimum required level, under the assumption that the physical layer by itself is not sufficiently reliable [3]. At the data-link layer, a key task is to achieve the specified communication reliability level [5]. At the network layer, packet data transmission can be customized by the choice of switching and routing algorithms. The former, (e.g., circuit, packet, and cut-through switching), establishes the type of connection while the latter determine the path followed by a message through the network to its final destination. Switching and routing algorithms for NoC affect heavily performance. Atop the network layer, the communication abstraction is an end-to-end connection. The transport layer decomposes messages into packets at the source. It also decides the order of packets and reassembles the messages at the destination. Another transport-layer task is flow control. Flow control can mitigate the effect of congestion by regulating the amount of data that enters the network, at the price of some throughput penalty [6].

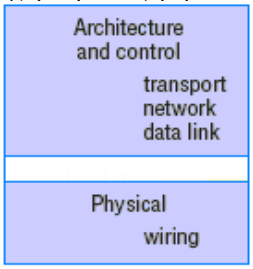

Figure 1. The Protocol Stack from which the stack paradigm of network on chip can be adapted.

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III. XY AND OE ROUTING ALGORITHM

The routing algorithm, which defines the path taken by a packet between the source and the destination, is a main task in network layer design of NoC. According to where routing decisions are taken, it is possible to classify the routing in source and distributed routing [8]. In source routing, the whole path is decided at the source router, while in distributed routing each router receives a packet and decides the direction to send it. According to how a path is defined to transmit packets, routing can be classified as deterministic or adaptive. In deterministic routing, the path is uniquely defined by the source and target addresses. In adaptive routing, the path is a function of the network traffic [8][9]. In the following text, two different routing algorithms are demonstrated in details.

A. XY Routing Algorithm

The XY routing algorithm is one kind of distributed deterministic routing algorithms. For a 2-Dimesion mesh topology NoC, each router can be identified by its coordinate (x, y) (Fig. 2). The XY routing algorithm compares the current router address (Cx,Cy) to the destination router address (Dx,Dy) of the packet, stored in the header flit. Flits must be routed to the core port of the router when the (Cx,Cy) address of the current router is equal to the (Dx,Dy) address. If this is not the case, the Dx address is firstly compared to the Cx (horizontal) address. Flits will be routed to the East port when Cx<Dx, to West when Cx>Dx and if Cx=Dx the header flit is already horizontally aligned. If this last condition is true, the Dy (vertical) address is compared to the Cy address. Flits will be routed to South when Cy<Dy, to North when Cy>Dy. If the chosen port is busy, the header flit as well as all subsequent flits of this packet will be blocked. The routing request for this packet will remain active until a connection is established in some future execution of the procedure in this router. The following text is the algorithm XY:

```
Algorithm XY
/*Source router: (Sx,Sy);destination router: (Dx,Dy); current
router: (Cx,Cy).*/
begin
if (Dx>Cx) //eastbound messages
return E;
 else
 if (Dx<Cx) //westbound messages
 return W;
else
 if (Dx=Cx) { //currently in the same column as
                //destination
   if (Dy<Cy)    //southbound messages
   return S;
   else
   if (Dy>Cy)    //northbound messages
   return N;
   else
   if (Dy=Cy)   //current router is the destination router
   return C;
   }
end
```

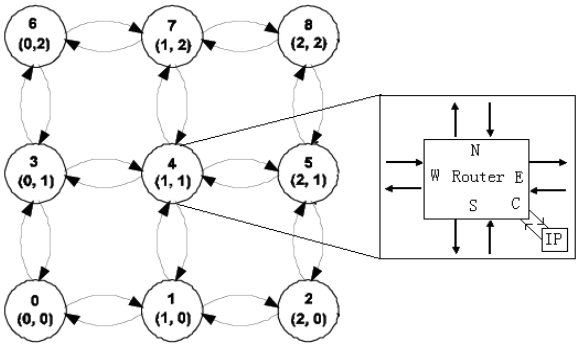

Figure 2. A 2-Dimension 3X3 Mesh Topology Network on Chip

The implement of XY routing algorithm is simple. However, it is deterministic routing algorithm, which means this routing algorithm only provides a routing path for a pair of source and destination. Moreover, XY routing algorithm can not avoid from deadlock appearance.

B. OE Routing Algorithm

OE routing algorithm is a distributed adaptive routing algorithm which is based on odd-even turn model. It exerts some restrictions, for avoiding and preventing from deadlock appearance. Odd-even turn model facilitates deadlock-free routing in two-dimensional (2D) meshes with no virtual channels. Explaining some definitions are necessary in order to represent this algorithm.

In a two-dimension mesh with dimensions X*Y each node is identified by its coordinate (x, y). In this model, a column is called even if its x dimension element is even numerical column. Also, a column is called odd if its x dimension element is an odd number. A turn involves a 90-degree change of traveling direction. A turn is a 90-degree turn in the following description. There are eight types of turns, according to the traveling directions of the associated channels. A turn is called an ES turn if it involves a change of direction from East to South. Similarly, we can define the other seven types of turns, namely EN, WS, WN, SE, SW, NE, and NW turns, where E, W, S, and N indicate East, West, South, and North, respectively. As a whole, there are two main theorems in odd-even algorithm:

Theorem1: NO packet is permitted to do EN turn in each node which is located on an even column. Also, No packet is permitted to do NW turn in each node that is located on an odd column.

Theorem 2: NO packet is permitted to do ES turn in each node that is in an even column. Also, no packet is permitted to do SW turn in each node which is in an odd column.

The following test is a minimal OE routing algorithm in which avail_dimension_set contains dimensions that are available for forwarding the packet:

```
Algorithm OE
/*Source router: (Sx,Sy);destination router: (Dx,Dy); current
router: (Cx,Cy).*/
begin
avail_dimension_set<-empty;
Ex<-Dx-Cx;
Ey<-Dy-Cy;
```

```
if (Ex=0 && Ey=0)   //current router is destination
return C;
if (Ex=0){      //current router in same column as //destination
       if (Ey<0)
       add S to avail_dimension_set;
       else
       add N to avail_dimension_set;
    }
else{
      if (Ex>0){             //eastbound messages
        if (Ey=0){         //current in same row as destination
        add E to avail_demision_set;
        }
        else{
    if(Cx % 2 != 0 or Cx=Sx)  //N/S turn allowed only in odd
                                  //column.
    if(Ey < 0)
    add S to avail_dimension_set;
    else
    add N to avail_dimension_set;
    if(Dx% 2 != 0 or Ex != 1) {
                               //allow to go E only if destination
                               // is odd column
    add E to avail_dimension_set;
                              //because N/S turn not allowed in
                              //even column
          }
       }
    }
    else {                          // westbound messages
    add W to avail_dimension_set;
    if(Cx%2=0)         //allow to go N/S only in even
                       //column, because N->W and S->W
                      //not allowed in odd column
    if(Ey<0)
    add S to avail_dimension_set;
    else
    add N to avail_dimension_set;
    }
}
Select a dimension from avail_dimension_set to forward the
packet.
end
```

OE routing algorithm is more complex than XY routing algorithm. However, it is one kind of adaptive routing algorithm. For a pair of source and destination, it can provide a group of routing paths and it can prevent from dead lock appearance.

IV. Architecture of a 2-Dimension 3X3 Mesh Topology NoC

The routing Algorithm is simulated based on a 2-Dimension 3X3 mesh topology NoC (Fig. 2). In the Fig. 2, each circle represents a tile in the network. Each tile consists of an IP core connected to a router by a bidirectional core channel (C). A tile is connected to neighbor tiles by four bidirectional channels (N, E, S and W). Each tile is identified by a unique integer ID. Also, each tile can be identified by a pair x-coordinate and y-coordinate. Our 2-Dimesion 3X3 mesh topology NoC is designed using wormhole switching mechanism, in which packets are divided into flits. A packet consists of 3 types of flits, which are head flit, data flit and tail flit. We have implemented the architecture consisting of only input buffers. The number of buffers is 8 in input channel FIFO. Both XY routing algorithm and OE routing algorithm are based on these characteristics.

V. Simulation Results and Analysis

The simulation is performed on NIRGAM simulator, a simulator for NoC Interconnect Routing and Application Modeling version 1.1. NIRGAM is an extensible and modular systemC based simulator [10]. Both XY and OE routing algorithm are performed in the same application mapping, traffic conditions and simulation control. All of the tiles are attached to Constant Bit Rate (CBR) traffic generator. The packet size is 8 bytes with a random destination mode. The percentage load is 50% which mean that 50% of maximum bandwidth is used. The interval between successive flits is 2 clock cycles. The simulation runs 1000 clock cycles and the clock frequency is 1 GHz. Synthetic traffic generators generate traffic in the first 300 clock cycles with warm-up period of 5 clock cycles.

Performance of routing algorithm is measured on a per-channel basis, while performance metrics include average latency (in clock cycles) per packet and average throughput (in Gbps) for each channel. Fig. 3 illustrates the simulation results of XY routing algorithm and Fig. 4 is the simulation results of OE routing algorithm.

Fig. 5 is the top view of the histograms. R0 - R8 shows the placement of tiles/routers. Red bar between R0 and R1 represents metric for eastward channel from R0 to R1. Blue bar between R0 and R1 represents metric for westward channel from R1 to R0. Green bar between R0 and R3 represents metric for northward channel from R0 to R3. Orange bar between R0 and R3 represents metric for southward channel from R3 to R0.

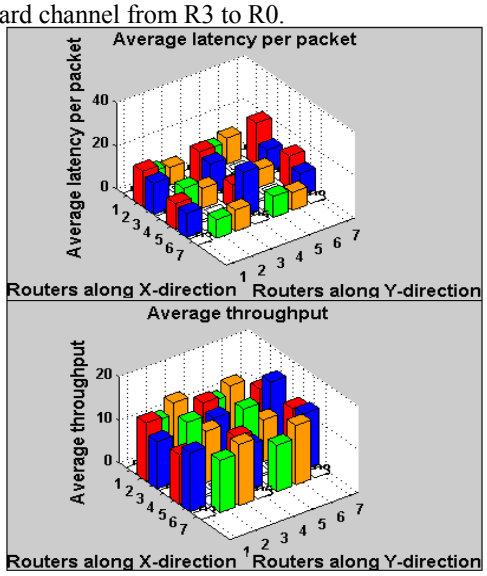

Figure 3. Average latency per packet and Average throughput statistical histogram of XY routing algorithm based on 2-Dimension 3X3 mesh topology NoC.

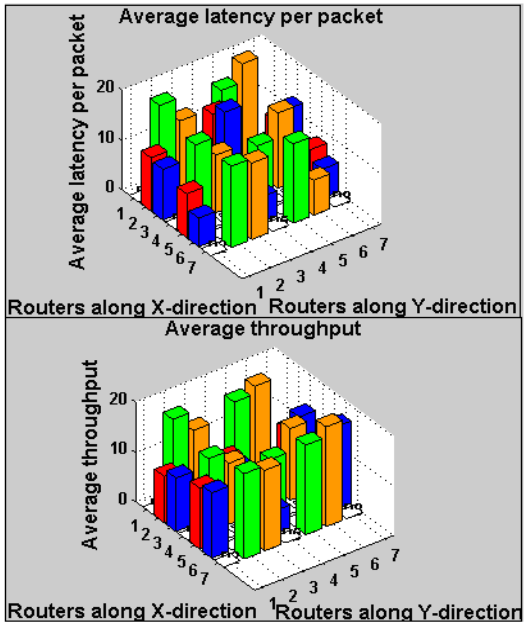

Figure 4. Average latency per packet and Average throughput statistical histogram of OE routing algorithm based on 2-Dimension3X3 mesh topology NoC.

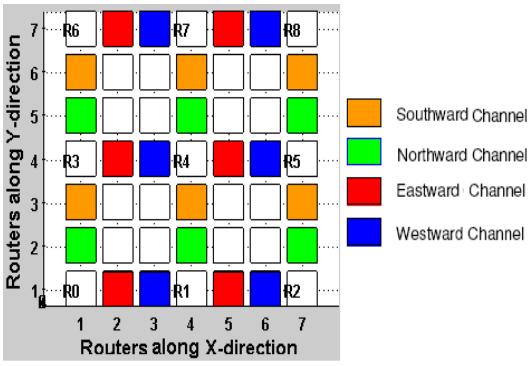

Figure 5. Top view of the histogram

TABLE I. KEY PERFORMANCE SIMULATION PARAMETERS OF XY ROUTING ALGORITHM AND OE ROUTING ALGORITHM

		Max of Channel	Min of Channel	Average of Network
XY	Latency per packet (Clock Cycles)	20.5	7.3	13.6
	Throughput (Gbps)	15.5	9.6	11.7
OE	Latency per packet (Clock Cycles)	19.5	5.0	11.9
	Throughput (Gbps)	20.0	4.5	13.0

In Fig. 3, X-direction channel latency is averagely lager than Y-direction channel latency and X-direction channel throughput averagely equals Y-direction throughput for XY routing algorithm. For OE routing algorithm, X-direction channel latency is averagely smaller than Y-direction channel latency and X-direction channel throughput is also smaller than Y-direction throughput in Fig. 4. These are characteristics of the two kinds of routing algorithms for a 2-Dimension 3X3 mesh topology NoC.

A group of key performance parameters are included in TABLE I. The Average of Network is the mean value of all channels. The latency of OE routing algorithm is shorter than that of XY routing algorithm. Meanwhile, the throughput of OE routing algorithm is larger than that of XY routing algorithm. We can define an average performance parameter P to evaluate the average performance of different routing algorithm:

P= Average Throughput of Network/ Average Latency per packet of Network

If value of parameter P is larger, the performance will be better. P(XY)= 0.86 and P(OE)=1.09. Thus, OE routing algorithm fits with our NoC better than XY routing algorithm.

VI. CONCLUSIONS

The routing algorithm is one of network layer researches of a NoC design, whose design approach can be adapted from a protocol stack including physical layer, data link layer, network layer and transport layer. Based on a 2-Dimension 3X3 mesh topology NoC, two different routing algorithms, XY routing algorithm and OE routing algorithm, are simulated on NIRGAM simulator platform and compared with latency per packet and throughput metrics. For XY routing algorithm, X-direction channel latency is averagely lager than Y-direction channel latency and X-direction channel throughput is averagely all square with Y-direction throughput. For OE routing algorithm, X-direction channel latency is averagely smaller than Y-direction channel latency and X-direction channel throughput is also smaller than Y-direction throughput. Comparing with performance parameter P, P(XY)=0.86 and P(OE)=1.09, OE routing algorithm fit with 2-Dimension 3X3 mesh topology NoC better than XY routing algorithm with Constant Bit Rate (CBR) traffic condition. However, our conclusions are just fit for a 2-Dimension 3X3 mesh topology NoC. For other topologies, additional researches are needed to do in the future.

REFERENCES

[1] P. Guerrier and A. Greiner, “A generic architecture for on-chip packet-switched interconnections,”Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE 2000), Mar. 2000, pp. 250–256, doi: 10.1109/DATE.2000.840047.

[2] A. Hemani, A. Jantsch, S. Kumar, A. Postula, J. Oberg, M. Millberg. et al, “Network on a chip: an architecture for billion transistor era,” Proc. IEEE NorChip, 2000.

[3] W. Dally and B. Towles, “Route packets, not wires: on-chip interconnection networks,” Proc. Design Automation Conference, Jun. 2001, pp. 684–689.

[4] M. Sqroi, M. Sheets, A. Mihal, K. Keutzer, S. Malik, J. Rabaey, et al.“Addressing the system-on-a-chip interconnect woes through communication-based design”, Proc. Design Automation Conference, Jun 2001, pp.667-672.

[5] S. Kumar, A. Jantsch, J. Soininen, M. Forsell, M. Millberg, J. Oberg . et al, “A network on chip architecture and design methodology,” Proc. IEEE Computer Society Annual Symposium on VLSI, Apr. 2002, pp. 105–112, doi: 10.1109/ISVLSI.2002.1016885.

[6] R. Marculescu, H. Jingcao, U. Y. Ogras, “Key research problems in NoC design: a holistic perspective,” Proc. Third IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS’05) , Sept. 2005, pp.69-74, doi: 10.1145/1084834.1084856.

[7] J. Walrand, P. Varaiya, High-performance communication networks. Morgan Kaufman, 2000.

[8] J. Duato, S. Yalamanchili, L. Ni, Interconnection networks: an engineering approach, Morgan Kaufmann, Revised Edition, 2002.

[9] L. M. Ni, P. K. Mckinley, “A Survey of Wormhole Routing Techniques in Direct Networks”, Computer, vol. 26(2), Feb 1993, pp. 62 –76, doi: 10.1109/2.191995

[10] L. Jain. NIRGAM Version 1.1 Manual, Sep 2007, pp. 1-2.