Network-on-Chip Architecture: An Overview

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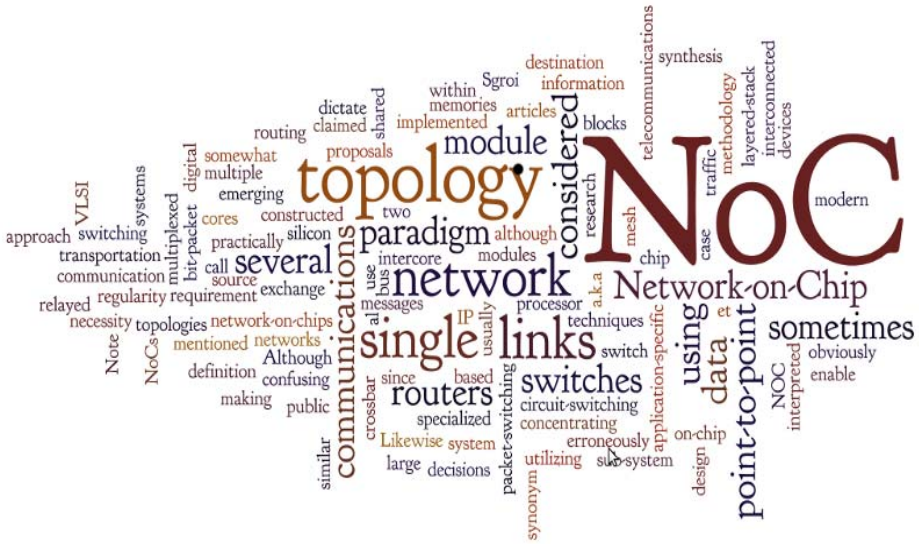
Overview



- Introduction
  - Multi-core chip
  - Challenges
  - Network-on-Chip
- Architecture
  - Regular Topology
  - Irregular Topology
  - Emerging Interconnect
- Conclusion

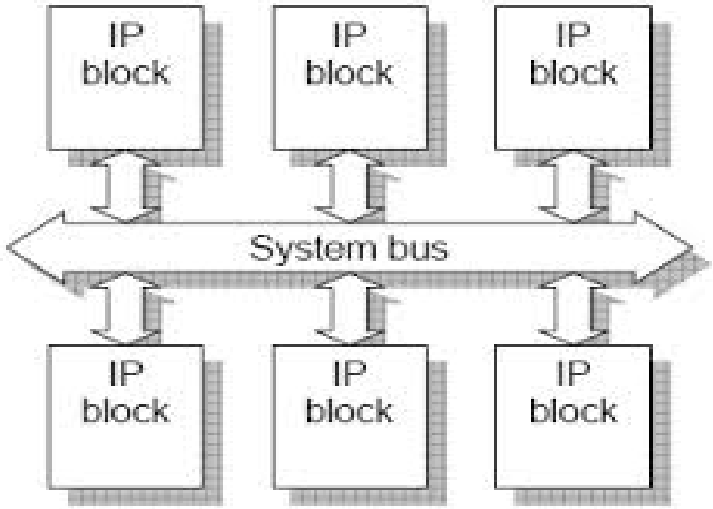
Multi-core Chips: A Necessity

- Need for explosive computational power
  - Consumer/Entertainment Application
  - Scientific Application
- Increasing clock frequency is not possible as it increases power dissipation

Solution: **Core level Parallelism,** distribute tasks to multiple cores

Challenges: Interconnection of Cores

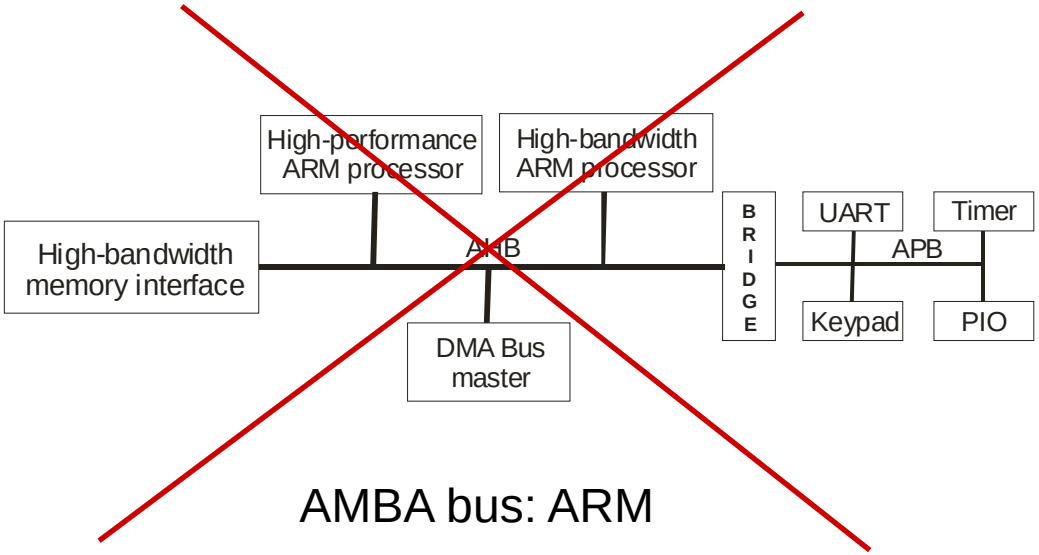
- **Traditional Interconnect** architectures are **not scalable**
  - **Delay limit number of cores**



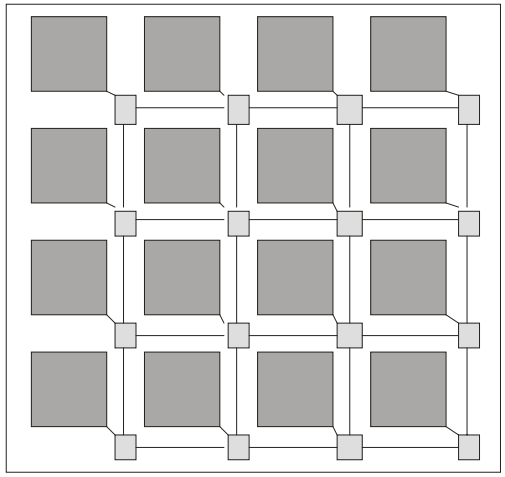
Solution: Scalable interconnect infrastructure for communication

Network-on-Chip (NoC)

- Packet based on-chip network
  - *Route packets, not wires* –Bill Dally, 2000.
- Dedicated infrastructure for data transport
  - Decoupling of functionality from communication
  - A plug-and-play network independent of the cores



AMBA bus: ARM



NoC infrastructure

Multiple publications in IEEE ISSCC, 2010 from Intel, IBM, AMD, and Sun Microsystems show that multi-core NoC is a reality

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Switching

Circuit Switching

- Dedicated path, or circuit, is established over which data packets will travel
- Naturally lends itself to time-sensitive guaranteed service due to resource allocation
- Reservation of bandwidth decreases overall throughput and increases average delays

Packet Switching

- Intermediate routers are now responsible for the routing of individual packets through the network, rather than following a single path
- Provides for so-called best-effort services
- Sharing of resources allows for higher throughput

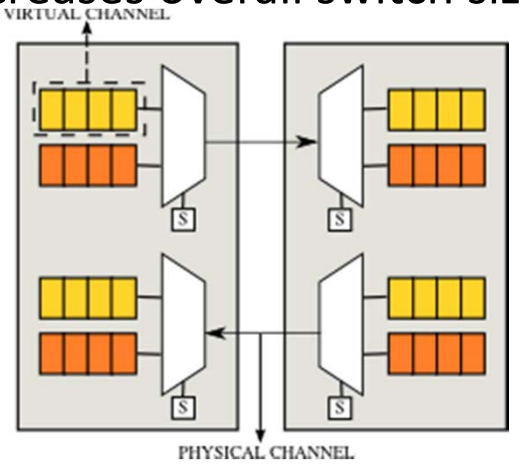
Switching Methodology

Wormhole Switching

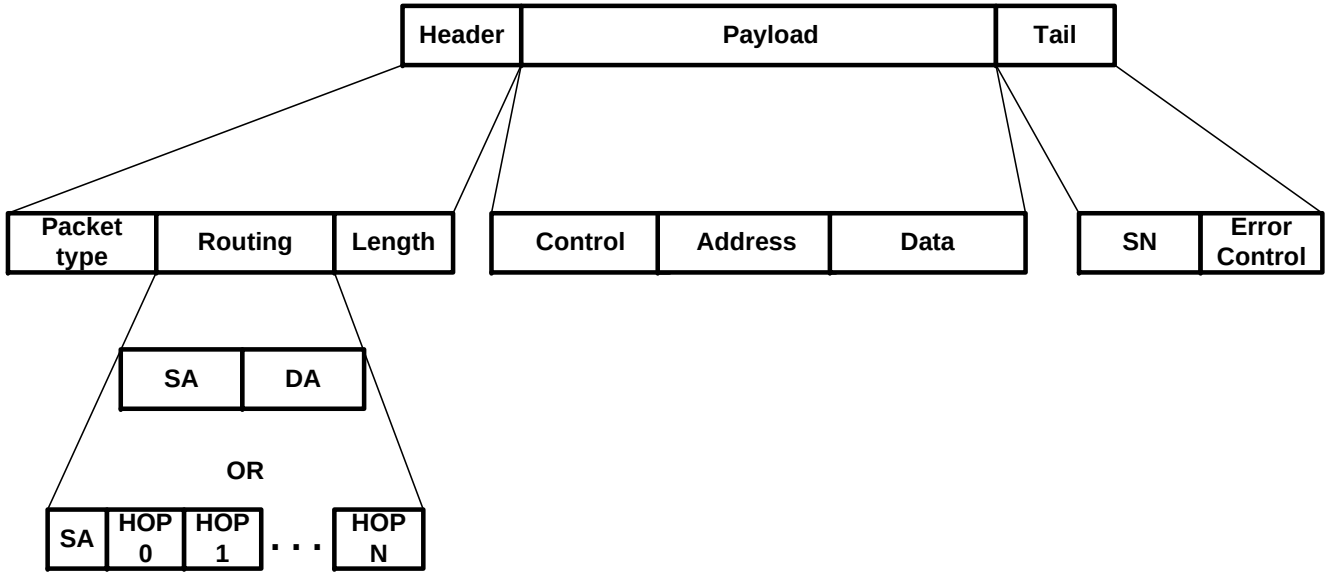
- Message is divided up into smaller, fixed length flow units called flits
- Only first flit contains routing information, subsequent flits follow
- Messages must cross the channel entirety before the channel can be used by another message →decreases channel utilization

Virtual Channels

- Allows for several instances of wormhole switching
- Additional buffers are added, which increases overall switch size, but significantly increases throughput



Typical NoC Packet Format



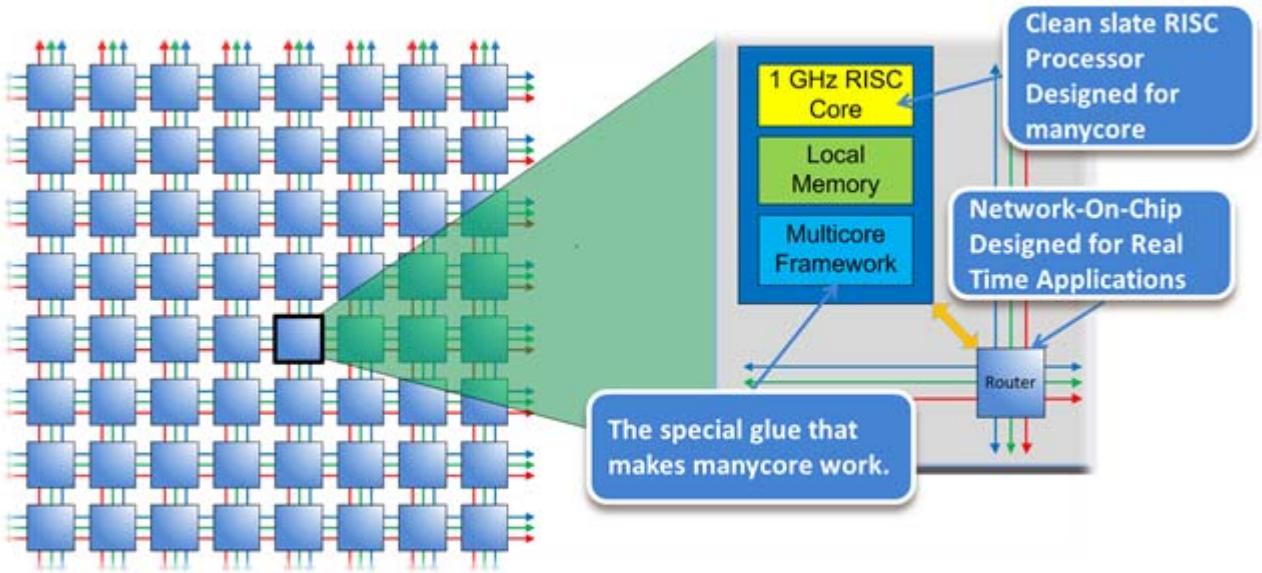
- Header
  - routing and network control information.
  - In the case of distributed routing the information required is the destination and source addresses
  - in the case of source routing the complete routing information is written
  - In the case of variable packet size a length field is required
- Payload
- Tail
  - sequence number
  - error control fields such as hamming code or CRC fields

Topology

- Regular topology: Each node has the same number of neighbors.
- Example: 2D mesh, 2D torus
- Irregular topology: For each node, all neighbors of that node have distinct degrees.
- Example: Hierarchical Mesh, Small-world

2D Mesh

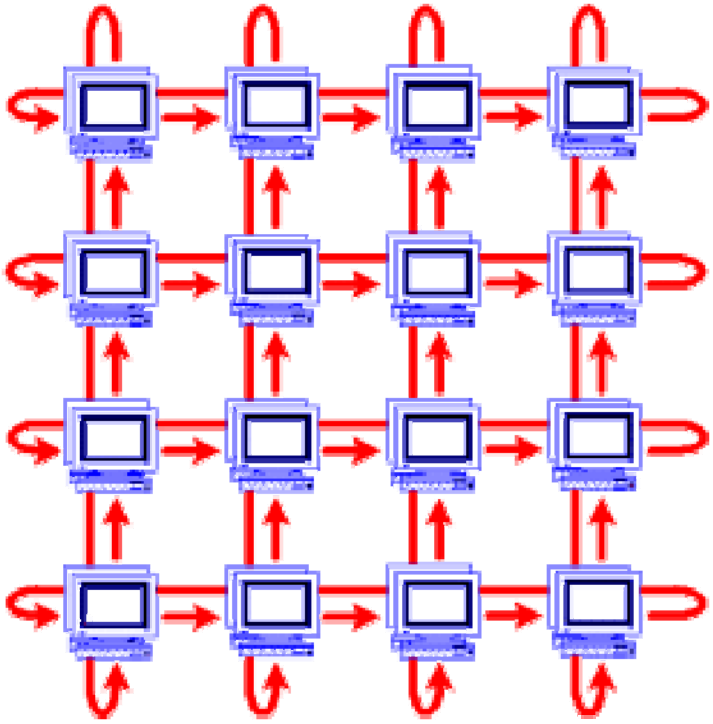
- simplest and most popular topology for NoCs.
- Every switch, except those at the edges, is connected to four neighboring switches and one node.



•High Average path distance; not scalable

2D Torus

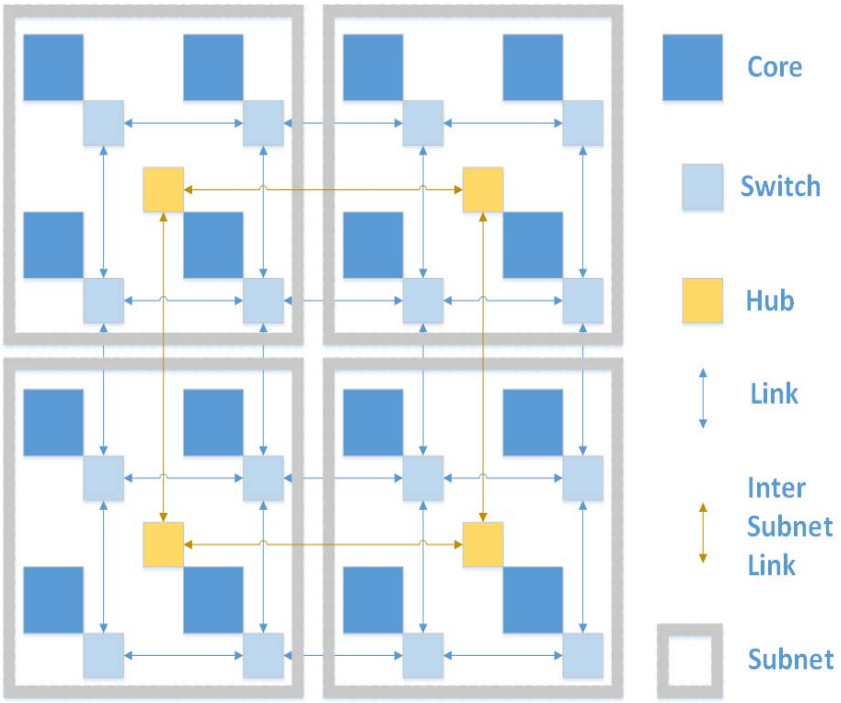
- layout of a regular mesh except that nodes at the edges are connected to switches at the opposite edge via wrap-around routing channels.
- Every switch has five ports



•Long links → high delay and high power dissipation; not scalable

Hierarchical Mesh

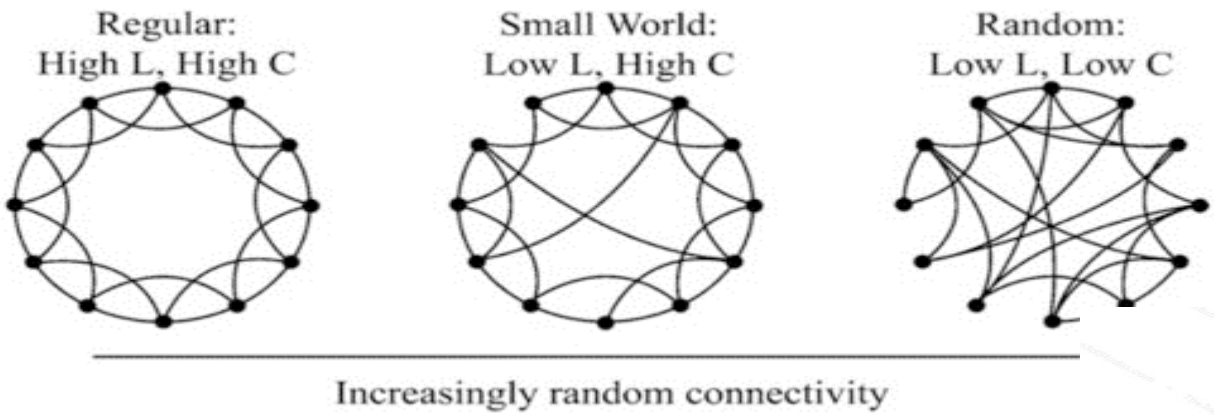
- Two level Hierarchy
- Bottom layer
  - Mesh Connectivity
- Upper layer
  - Switches grouped into subnets
  - One hub per subnet
  - All switches from one subnet connected to the hub from that subnet
  - Hubs interconnected with each other in mesh fashion



•Power hungry Hubs; still has long links

Small World

- Inspired from nature - microbial colonies, neural networks and social networks
- Characterized by many short links and few long links

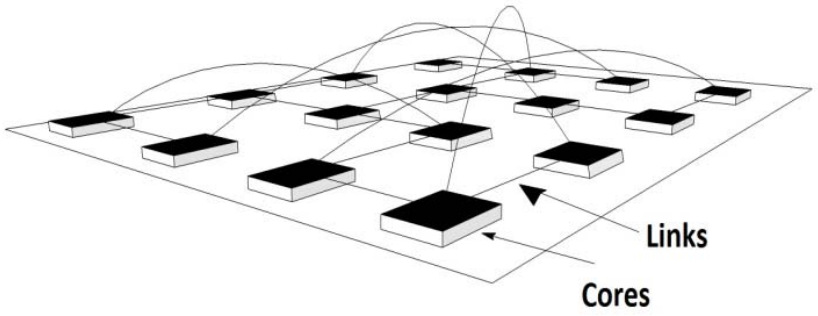


L = Avg. Path distance
C = Avg. Clustering Coefficient
= ratio between existing edges to possible edges between neighbor

SW Topology Construction

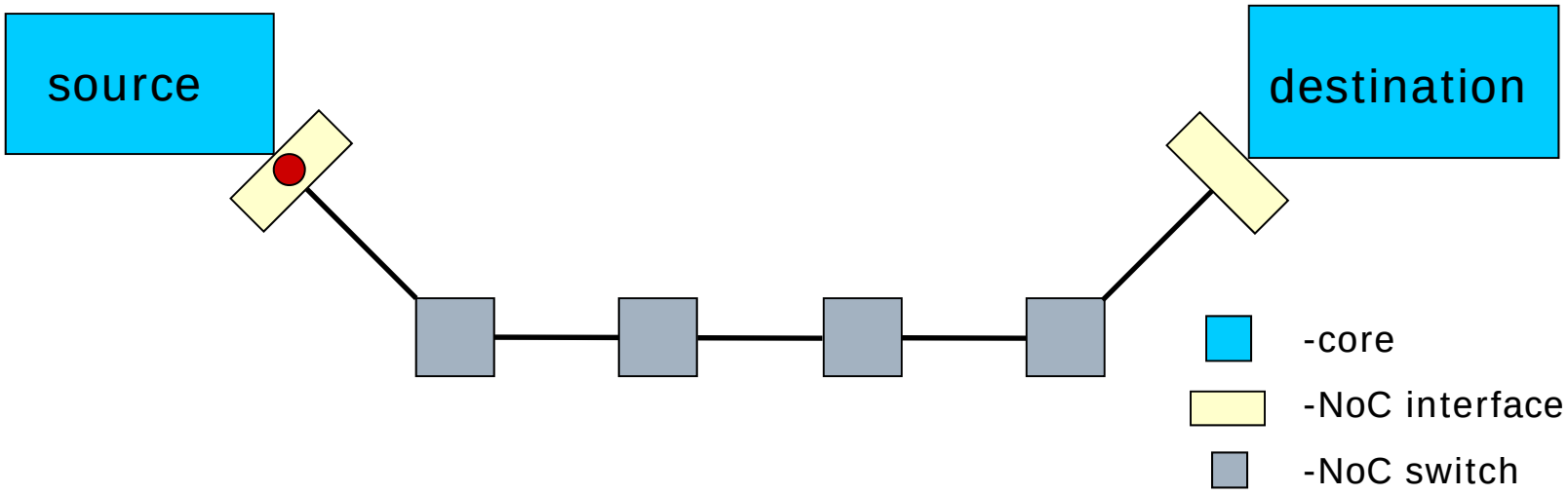
- Small-World topology
  - Inherently fault-tolerant
- Link Insertion
  - Following adjacent probability distribution
- Few high speed shortcuts.
- Local, shorter links.

$$P(i,j) = \frac{l_{ij}^{-\alpha} f_{ij}^{\beta}}{\sum_{\forall i}\sum_{\forall j} l_{ij}^{-\alpha} f_{ij}^{\beta}}$$



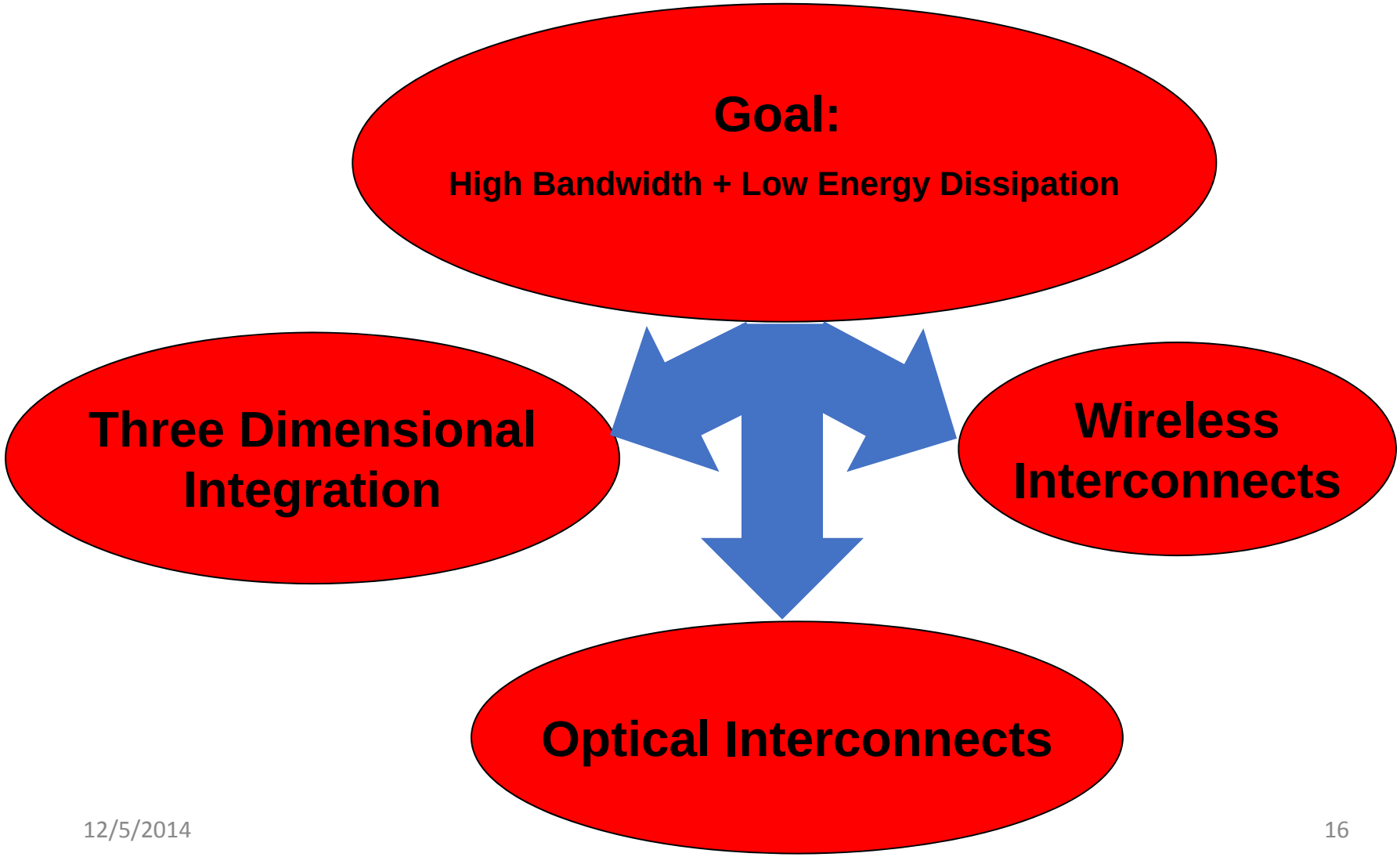
Interconnect

- Limitation of Wireline Interconnect
  - Multi-hop wireline communication
    - High Latency and energy dissipation



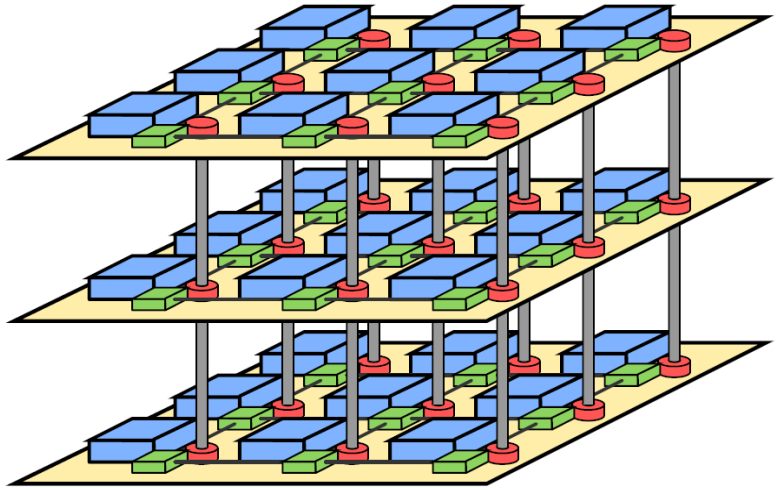
80% of chip power will be from on-chip interconnects in the next 5 years – ITRS, 2007

Emerging Interconnect Technologies



3D Integration

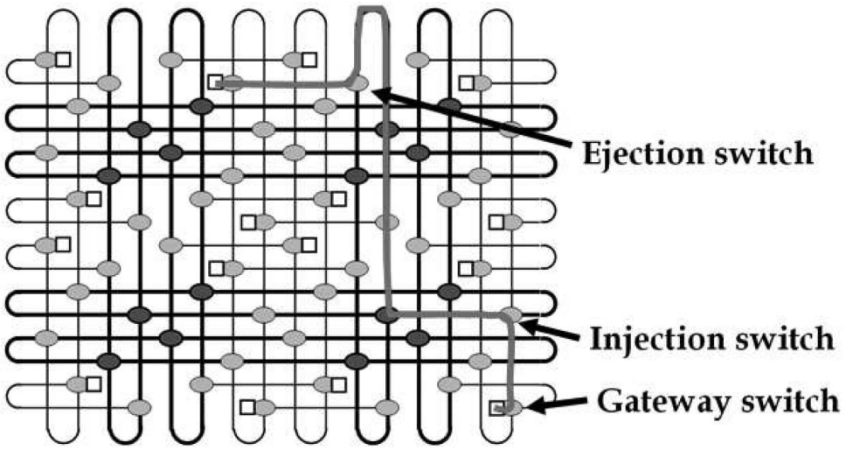
- Stacking multiple active layers
- Manufacturability
  - Mismatch between various layers
  - Yield is an issue
- Temperature concerns
  - Despite power advantages, reduced footprint increases power density

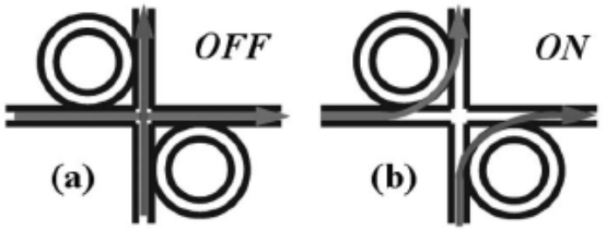


- Pavlidis et al., “3-D topologies for Networks-on-Chip”, IEEE Transactions on Very Large Scale Integration (TVLSI), 2007.

Optical Interconnect

- High bandwidth photonic links for high payload transfers
- Challenges: On-going research
  - On-chip integration of photonic components

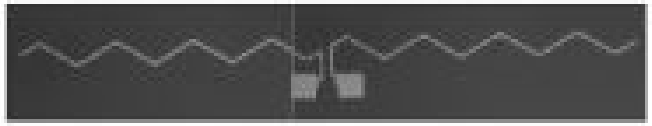




- A. Shacham et al., "Photonic Network-on-Chip for Future Generations of Chip Multi-Processors", IEEE Transactions on Computers, 2008.

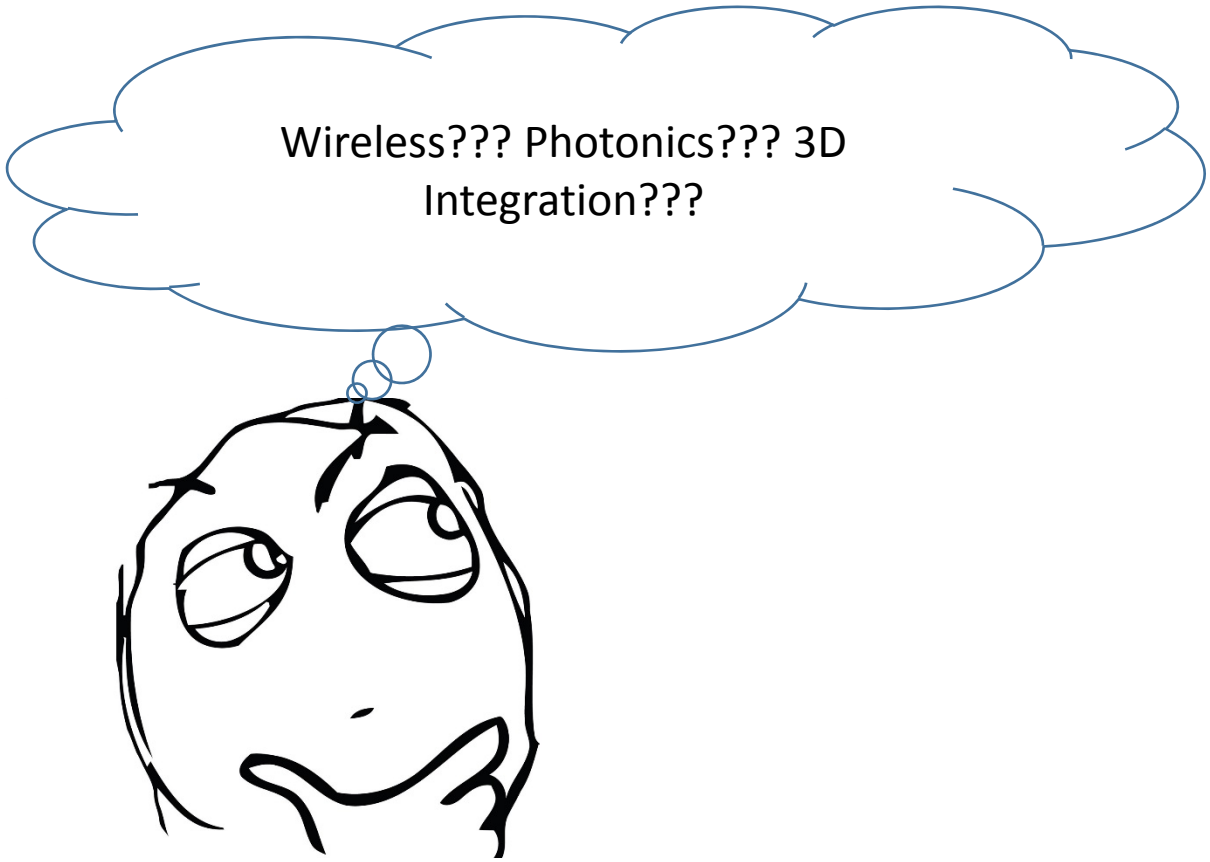
Wireless Interconnect

- Wireless NoC based on
  - Low power and high bandwidth wireless interconnects
  - Wireless port/wireless interface (WI) consists of transceiver and antenna
- Antenna Technology:
  - Metal zigzag antennas (mm-wave) are CMOS compatible[3]
- Transceiver



- J. Lin et al., “Communication Using Antennas Fabricated in Silicon Integrated Circuits,” IEEE Journal of Solid-State Circuits, vol. 42, no. 8, August 2007, pp. 1678-1687.

Where should We bet our money???



Comparisons

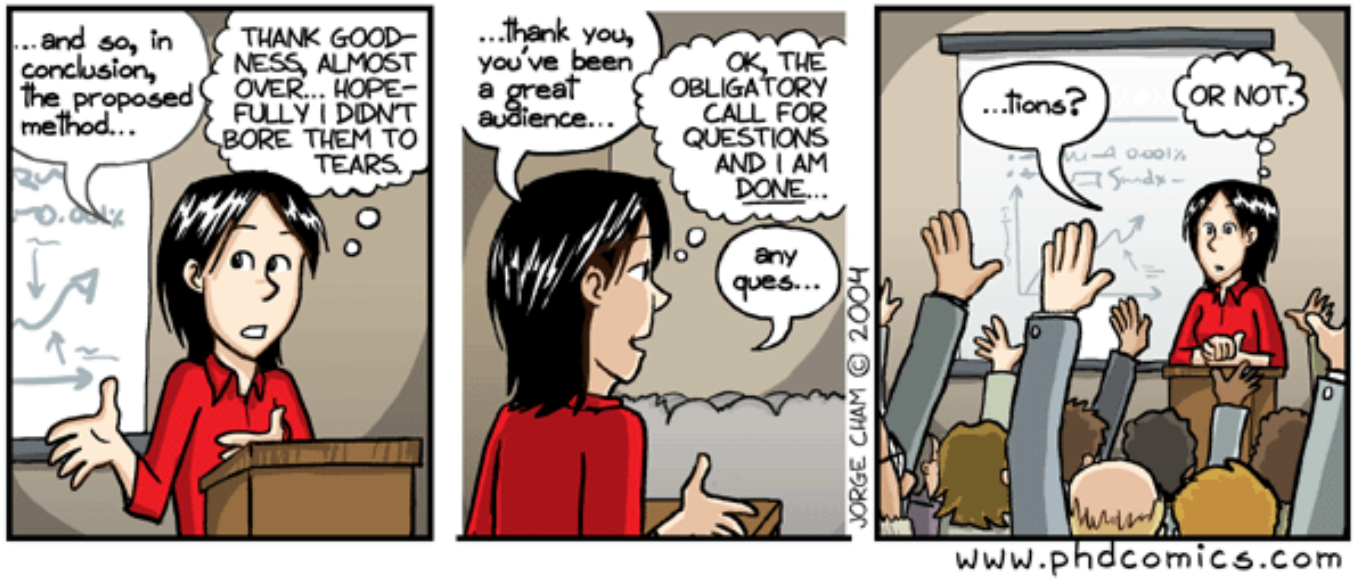
		3D NoC	Photonic NoC	Wireless NoC
Design Requirements		Multiple layers with active devices	Silicon photonic components	On-chip antenna and transceiver
Performance Gains	Bandwidth	Higher connectivity & less hop count	High speed optical devices and links	Single hop shortcuts
	Lower Power	Shorter average path length	Negligible power dissipation in optical data transport	Energy Efficient wireless transmission
Challenges		1. Heat dissipation due to higher power density 2. Fabrication Problem	1. Integration of on-chip photonic components 2. Crosstalk between adjacent wavelengths	1. Limited bandwidth 2. Large area overhead

No Clear Winner!!

Conclusion

- Networks-on-Chip is a natural choice for multicore processors.
- Copper wires are power hungry → need for alternative interconnects
- NoC research is still in primary stage.
  - Many open research problems
  - Need standardized development approach, better application and traffic models, new optimization techniques

Questions???


...and so, in conclusion, the proposed method...
THANK GOODNESS, ALMOST OVER... HOPEFULLY I DIDN'T BORE THEM TO TEARS.
...thank you, you've been a great audience...
OK, THE OBLIGATORY CALL FOR QUESTIONS AND I AM DONE...
any ques...
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...tions?
OR NOT.
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