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Article *in* TELKOMNIKA (Telecommunication Computing Electronics and Control) · June 2017

DOI: 10.12928/TELKOMNIKA.v15i2.6134

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TELKOMNIKA, Vol.15, No.2, June 2017, pp. 869~876
ISSN: 1693-6930, accredited **A** by DIKTI, Decree No: 58/DIKTI/Kep/2013
DOI: 10.12928/TELKOMNIKA.v15i2.6134

Topology Design of Extended Torus and Ring for Low Latency Network-on-Chip Architecture

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Abstract

In essence, Network-on-Chip (NoC) also known as on-chip interconnection network has been proposed as a design solution to System-on-Chip (SoC). The routing algorithm, topology and switching technique are significant because of the most influential effect on the overall performance of Network-on-Chip (NoC). Designing of large scale topology alongside the support of deadlock free, low latency, high throughput and low power consumption is notably challenging in particular with expanding network size. This paper proposed an 8x8 XX-Torus and 64 nodes XX-Ring topology schemes for Network-on-Chip to minimize the latency by decrease the node diameter from the source node to destination node. Correspondingly, we compare in differences on the performance of mesh, full-mesh, torus and ring topologies with XX-Torus and XX-Ring topologies in term of latency. Results show that XX-Ring outperforms the conventional topologies in term of latency. XX-Ring decreases the average latency by 106.28%, 14.80%, 6.7 1%, 1.73%, 442.24% over the mesh, fully-mesh, torus, XX-torus, and Ring topologies.

Keywords*: network-on-chip, system-on-chip, torus topology, ring topology, network latency*

1. Introduction

In Network-on-Chip (NoC), the term network topology [1] is used to refer to how the node is interconnected each other. Accordingly, the key to designing a network is to select an appropriate topology in which will determine the scalability, performance, fault tolerance complexity and power consumption of a NoC. The cost and performance could be the contributing factors in dictate a network topology. However, the performance of topology is limited by the complexity of the chip, symmetry, number of nodes, diameter, the number of edges, and the length of the interconnection. Additionally, the performance can be measured based on the path diversity, throughput and latency. Symmetry plays an important role in topology for load balancing and routing. Symmetry can be classified into two types includes vertex-symmetry and edge-symmetric. Vertex-symmetry sharing the same path, therefore can use the same direction to route to the same target node. In edge-symmetric the packet is using different path to send packet, therefore load balancing can achieve by this symmetric.

In each topology consist of channel, C=(x,y). Where the channel connects from source node, x, to the target node, y, with different width, wxy, frequency, fxy, and time required to send packet. The router connection can be classified into direct or indirect network. In a direct network, every node in the network is both terminal and switch. In this network, every node is connected to fixed number of node. In addition, every router in direct network connects at least one PE. The example of direct network is mesh, torus and ring topology. In an indirect network, a node only can be either a switch or a terminal. The number of router in indirect network is more compared to the number of IP cores and the router is only connected to others router. In this network, some of the router does not attach with PE. The example of indirect network is tree based topology. The simple topologies for general purpose application are mesh topology. However, due to increase of network size, the performance of mesh topology has degraded. Torus topology has reduced the diameter of mesh topology, but it increases the complexity and bisection width.

Received February5, 2017; Revised April 21, 2017; Accepted May 6, 2017

In Figure 1 illustrates the different topologies which are commonly used in Network-on-Chip (NoC).

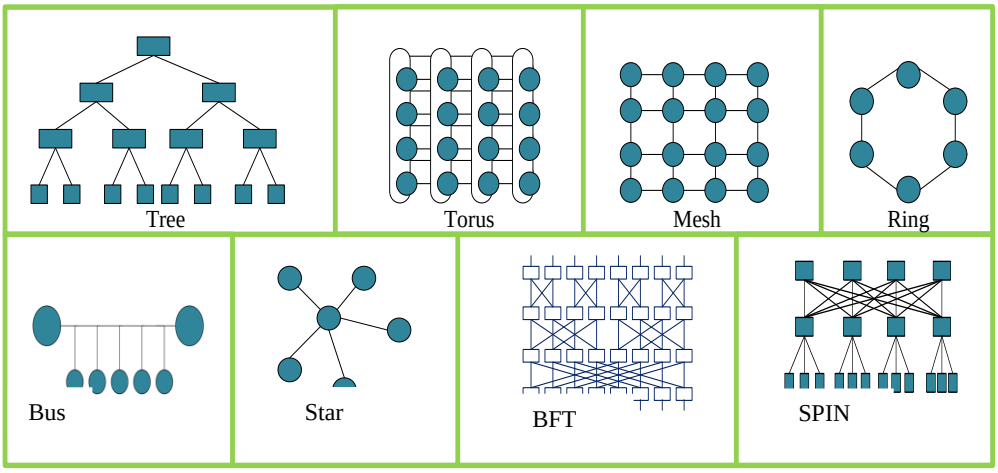

Figure 1. The example of topologies in Network-on-Chip (NoC)

In this paper, two new routing algorithms has proposed called XX-Torus and XX-Ring topology to decrease the average latency of a network. The proposed topologies are based on 8X8 torus and 64 nodes ring topologies. In this paper, we analyze its architectures potential in term of average latency and number of hop count. The number of hop count can reduce by choosing the shortest path to send packet from source node to destination node. Based on the experiment, XX-Ring topology has lower average latency and it is suitable for small and large network. The rest of this paper is organized as follow. Section 2 describes the related work. Section 3, architecture of mesh, fully mesh, torus, ring, XX-Torus, and XX-Ring are discussed and present the number of hop count of all the topologies. Section 4 discussion of the result and analysis, section 5 concludes the paper.

2. Related Work

Currently, the number of research institute focused on Network-on-Chip are increasing. Most of the researchers focused their research on NoC topologies [2, 3], routing protocols [4], architecture [5], power consumption [6, 7], throughput [8, 9] and latency [10].

Regarding [11] has proposed an RRCIES topology based on mesh topology. RRCIES has reduced the average power consumption in Network-on-Chip (NoC). The proposed topology reduced the power consumption by reduced the number of router in the topology. The number of routers is reduced by let more core connect through one router. Usman Ali Gulzari, Sheraz Anjum and Shahrukh Agha [12] proposed a cross by pass-mesh (CBP-Mesh) architecture for on-chip communication. CBP-Mesh topology is the modification of mesh topology by adding two cross by pass link to mesh topology. The average latency and number of hop count are reduced. Besides that, CBP-mesh has better area utilization and power consumption compare to mesh, torus, 2DDgl-Mesh, SD-Mesh, X-Mesh and C2-Mesh. Md. Hasan Furhad and Jong-Myon Kim [13] proposed an extended diagonal mesh topology (XDMesh) for network-on-chip architecture to reduce average latency and power consumption and increase throughput by including diagonal link in the network. Pengfei Yang and Quan Wang [14] proposed a topology name heterogeneous honeycomb-like network-on-chip topology. The objective of this paper is to decrease the latency, power consumption, and area. This paper shows that mesh and torus topology wasting resource and bandwidth when the processing element demands less communication. So heterogeneous honeycomb-like topology can solve the problem by using easy to expand and regular topology. Therefore, the transmission road could work well with varied requirement of different processing element. Arash Farhadi Beldachi, Simon Hollis and Jose L. Nunez-Yanez [15] proposed eXtended torus

(XTRANC) routing topology for NoC. This topology is modification of mesh topology by adding additional link to reduce congestion. This paper achieves the objective of higher throughput and lower latency compare to the mesh, inner torus and full-mesh.

3. Topologies

The performance of XX-Torus and XX-Ring are evaluating, include average latency and the maximum number of hop count require to send a packet from source node to destination node. The mesh, fully mesh, torus, xx-torus, ring, and xx-ring are discussed in section 3.1 and 3.2.

3.1. Mesh, Full-Mesh, Torus and XX-Torus Topologies

Currently, 2D mesh and torus topology are widely used by researchers due to accepted wire cost and high bandwidth. The structure of mesh and torus topology is shown is Figure 2 and 3. The structure of torus topology is fundamentally similar to mesh topology except for the edge of the router in torus topology is connected to another edge of the router. Both of these topologies can be represented in m x n node where m and n are the number of node in x-axis and y-axis respectively. The position of each node is identified by x and y dimension. Normally < 0, 0 > position is assign to the node on the left top corner. The x-dimension and y-dimension is increasing when move towards right and bottom respectively. Tori have better path diversity and load balancing. By using the formula of diameter, torus topology, (2[n/2]) has shorter diameter compare to mesh topology, (2n-2). Bisection width of torus, 2n is larger than mesh, n. The disadvantage of torus topology is with slightly higher latency because of higher hop count. A large number of hop counts is required to reduce the number of path diversity. The weakness of mesh and torus topology is found when the size of the network becomes larger and larger. The lower latency and power consumption normally can achieve by apply on small size network that makes the network bisection limited. The architecture of XX-Torus is the combination of fully mesh and torus topologies.

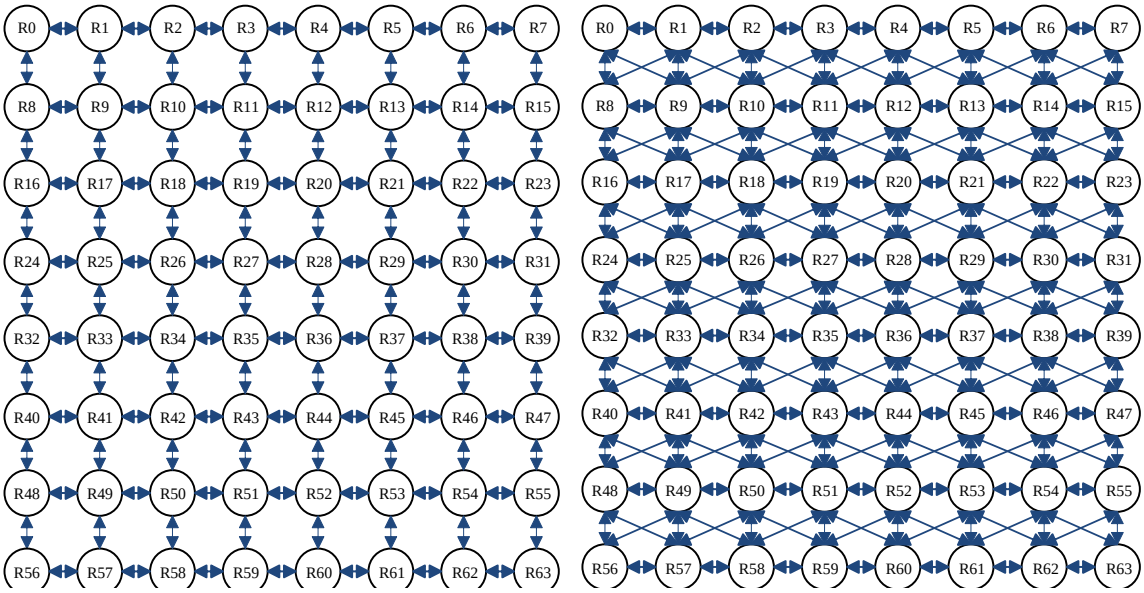

Figure 2. Mesh and Full-Mesh Topologies

Table 1 shows the comparison of hop count between the mesh and fully-mesh topology. Fully mesh shows the less hop count compare to mesh topologies. Besides hop count, fully mesh has lower average latency.

Table 1. Average Hop Count for Mesh and Fully-Mesh Topologies

Source Node	Destination Node	Path		Number of Hop	
		Mesh	Full-Mesh	Mesh	Fully-Mesh
0	63	0→8→16→24→32→40→48→56→57→58→59→60→61→62→63	0→9→18→27→36→45→54→63	14	7
5	35	5→3→21→29→37→36→35	5→13→21→28→35	6	4
10	52	10→18→26→34→42→50→51→52	10→19→28→36→44→52	7	5
15	57	15→23→31→39→47→55→63→62→61→60→59→58→57	15→22→29→36→43→50→57	12	6
20	38	20→28→36→37→38	20→29→38	4	2
25	60	25→26→27→28→36→44→52→60	25→34→43→52→60	7	4

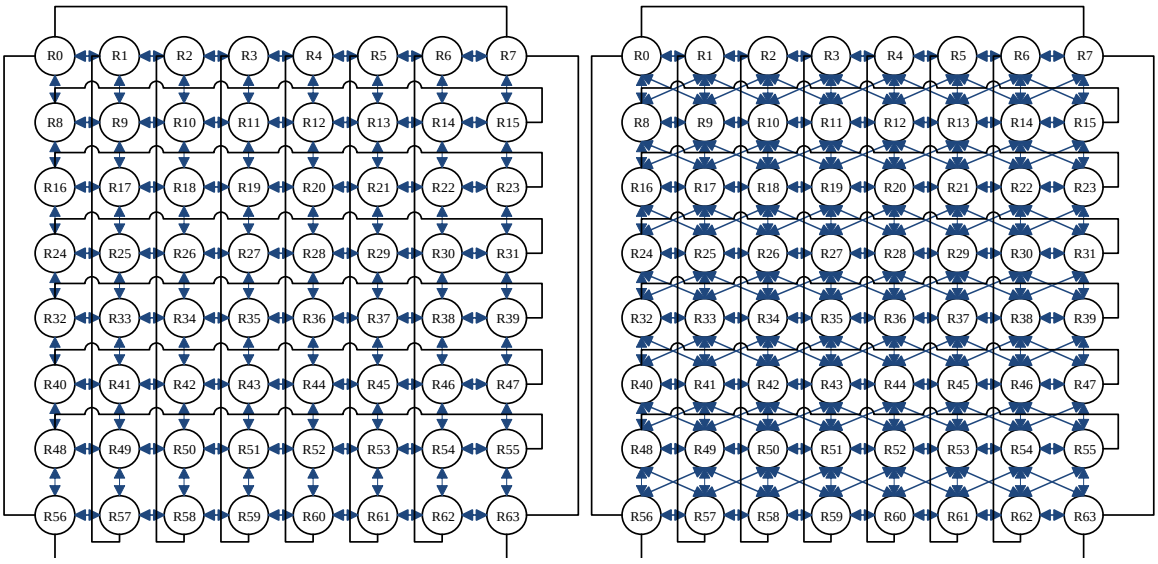

Figure 3. Torus and XX-Torus Topologies

Table 2 shows the comparison of hop count between torus and XX-Torus topology. XX-Torus has less hop count compare to torus topologies. Besides hop count, XX-Torus has lower average latency.

Table 2. Average Hop Count for Torus and XX-Torus Topologies

Source Node	Destination Node	Path		Number of Hop	
		Torus	XX-Torus	Torus	XX-Torus
0	63	0→56→63	0→56→63	2	2
5	35	5→3→21→29→37→36→35	5→13→21→28→35	6	4
10	52	10→2→3→4→60→52	10→3→4→60→52	5	4
15	57	15→7→63→56→57	15→7→63→56→57	4	4
20	38	20→28→36→37→38	20→29→38	4	2
25	60	25→26→27→28→36→44→52→60	25→34→43→52→60	7	4

3.2. Ring and XX-Ring Topologies

Figure 4 shows a ring topology with 64 nodes. In this topology, the first node R0 are connected with the last node R63. The decision to send the packet from source node to the destination node depends on the shotest path routing algorithm.

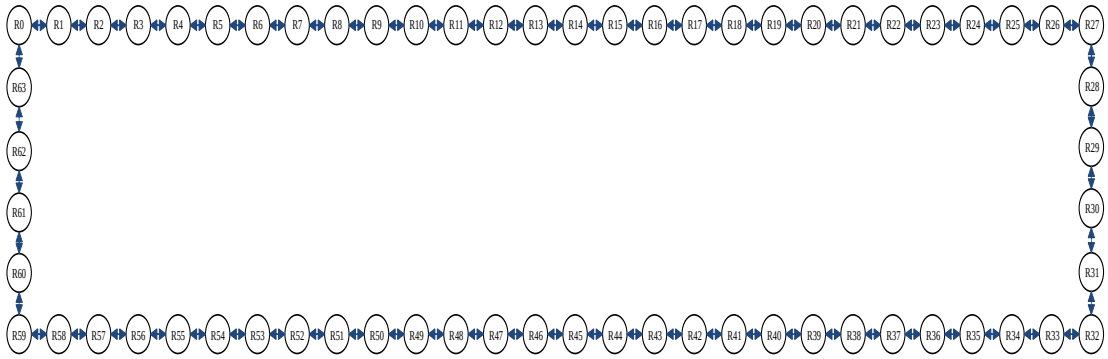

Figure 4. Ring Topology with 64 Nodes

Ring topology has a simple structure and efficient routing protocols. From Figure 4 shows that each PE in ring topology has exactly two neighbors. Low cost is needed to implement ring topology and high throughput is produced. The drawback of ring topology are high latency and fault tolerance may occur. When there is one link failure, the packet is still sending by using another path, but the latency will be high. However, when there is two link failure, the packet may fail to send to the target node. Therefore, 64 nodes XX-Ring topology are proposed to solve the problem of high latency in the ring topology. The 64 node ring topology are divided into 4 connected rings to reduce the total number of hop count to send the packet from source node to destination node as shown in Figure 5 and 6.

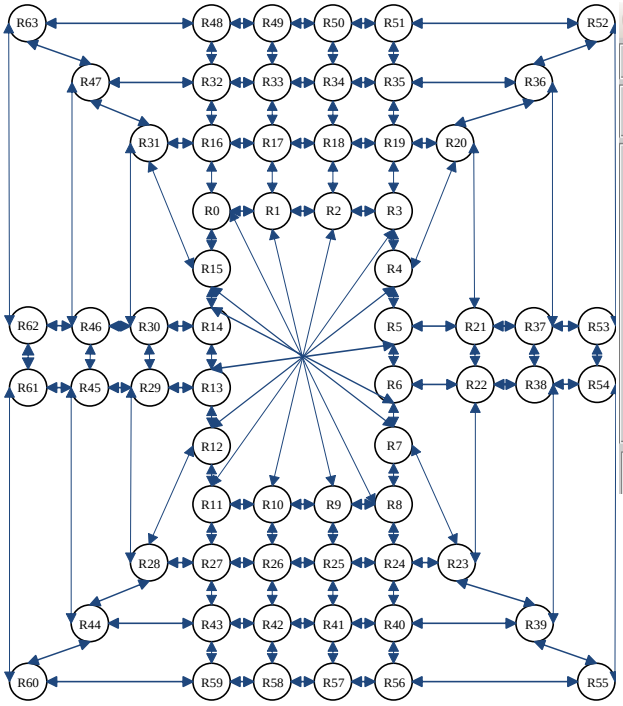

Figure 5. XX-Ring Topology with 64 Nodes

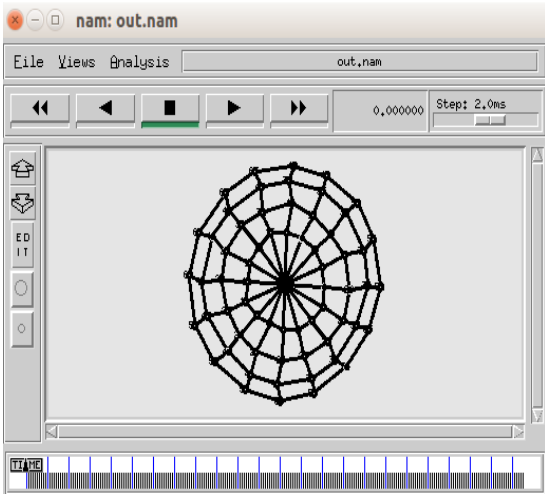

Figure 6. XX-Ring Topology with 64 Nodes Display in NS-2 Simulator

Table 3 shows the comparison of hop count between the ring and XX-Ring topologies. Ring topology shows almost double the hop count of XX-Ring topology. Besides hop count, XXRing topology has lower average latency.

Table 3. Average Hop Count for Ring and XX-Ring Topologies

Source Node	Destination Node	Path		Number of Hop	
		Ring	XX-Ring	Ring	XX-Ring
0	20	1→2→3→4→5→6→7→8→9→10→11→12→13→14→15→16→17→19→20	0→1→2→3→4→20	20	5
5	35	5→6→7→8→9→10→11→12→13→14→15→16→17→18→19→20→21→22→23→24→25→26→27→28→29→30	5→21→37→36→35	30	4
10	52	10→9→8→7→6→5→4→3→2→1→0→63→62→61→60→59→58→57→56→55→54→53→52	10→2→18→34→50→51→52	22	6
15	57	15→14→13→12→11→10→9→8→7→6→5→4→3→2→1→0→63→62→61→60→59→58→57	15→7→23→39→55→56→57	22	6
20	38	20→21→22→23→24→25→26→27→28→29→30→31→32→33→34→35→36→37→38	20→21→22→38	18	3
25	60	25→24→23→22→21→20→19→18→17→16→15→14→13→12→11→10→9→8→7→6→5→4→3→2→1→63→62→61→60	25→26→27→28→44→60	29	5

4. Results and Analysis

The proposed XX-Ring and XX-Torus topologies are compared with mesh, fully mesh, torus and ring topology to analyze the average latency of 64 nodes network. Our experiment used an NS-2 simulator to generate results. Latency is the time taken to send a packet from source node to destination node.

$$\text{Average Latency} = \frac{\sum_{i=1}^{N} PacketLatency}{N} \quad [1]$$

Where N is the total number of packet arrive at destination node and packet latency refer to the latency of packet at the ith packet.

$$\text{Average Number of Hop} = \frac{\sum_{i=1}^{N} PacketHop}{N} \quad [2]$$

Where N is the total number of packet arrive at destination node and packet hop refer to the number of hop count required to send the packet from source node to destination node. Table 4, Figure 7 and 8 shows the result generate from the NS-2 simulator, the comparison is done by comparing the average latency of proposed topologies with existing topologies.

Table 4. Average Latency (ms) of Different Topologies

Topology	Average Latency (ms) of 4 X 4 Network	Average Latency (ms) of 8 X 8 Network
Mesh	472.277	570.764
Full-Mesh	263.196	317.646
Torus	442.181	295.267
XX-Torus	433.661	281.484
Ring	517.722	1500.33
XX-Ring	262.834	276.533

From Figures 7 and 8, we can conclude that XX-Ring has better performance either in small or large network in term of average latency compare to the mesh, fully mesh, torus and xx-torus topologies. From the result, we observe that the number of hop count to sending a packet is proportional to the average latency. After adding an extra link to mesh, torus and ring topologies, the improvement of mesh and torus topology are not obvious as the ring topology.

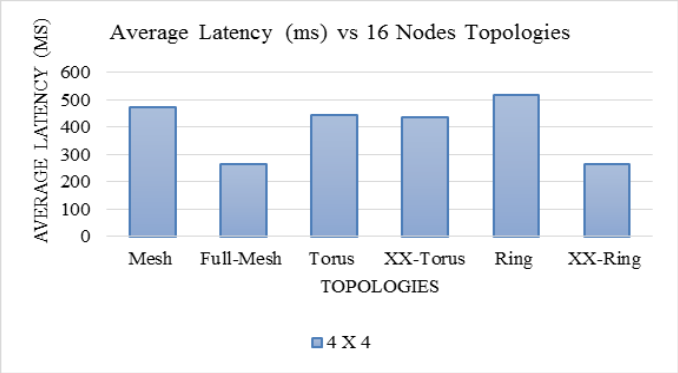

Figure 7. Average Latency (ms) of Different 16 Nodes Topologies

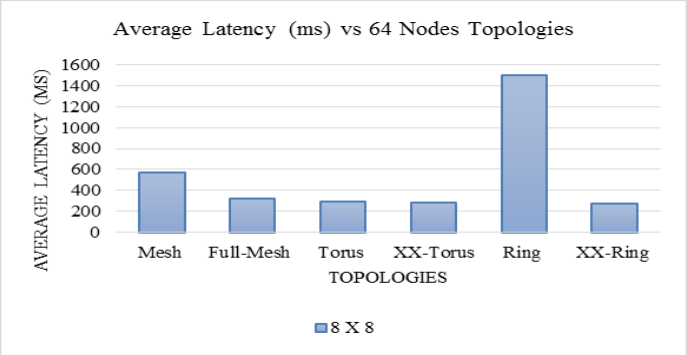

Figure 8. Average Latency (ms) of Different 64 Nodes Topologies

4. Conclusion

In this paper, we have created a 64 nodes XX-Ring and 8x8 XX-Torus topologies to enhance the performance and reduced the average latency of the Network-on-Chip (NoC). We analyzed the performance of XX-Ring and XX-Torus in term of latency and number of hop count. In additional, we compare the proposed topologies with existing topologies such as mesh, fully-mesh, torus and ring topologies. The experiment analysis shows that the XX-Ring decrease the average latency by 106.28%, 14.80%, 6.7 1%, 1.73%, 442.24% over the mesh, fully mesh, torus, xx-torus and ring topologies.

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