AN4879
Application note

USB hardware and PCB guidelines using STM32 MCUs

Introduction

STM32 microcontrollers include a group of products embedding a USB (Universal Serial Bus) peripheral. Full speed and high speed operations are provided through embedded and/or external PHYs (physical layers) of the open system interconnection model.

This application note gives an overview of the USB peripherals implemented on STM32 MCUs, and provides hardware guidelines for PCB design, to ensure electrical compliance with the USB standards.

For more details, refer to the USB section in the reference manual related to the MCU used for your application.

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1 List of abbreviations and acronyms

Table 1. List of abbreviations and acronyms

Acronyms	Meaning
ADP	Attach Detection Protocol
BCD	Battery Charging Detection
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FS	Full-speed
HBM	Human Body Model
HS	High Speed
IEC	International Electrotechnical Commission
LPM	USB 2.0 Link Power Management
LS	Low-speed
MCU	Microcontroller Unit, or microcontroller
OTG	On-the-go
PCB	Printed Circuit Board
PHY	Physical layer
SOF	Start of frame
ULPI	UTMI + low-pin interface
USB	USB Universal serial bus
UTMI	USB 2.0 transceiver macrocell interface

2 USB on STM32 products

The STM32 microcontrollers are based on Arm®(a) cores.

Each device with USB support embeds at least one of the following interfaces:

A: USB 2.0 FS device interface

B: USB 2.0 OTG FS, that is, USB 2.0 FS device/host/OTG controller with on-chip FS PHY

C: USB 2.0 OTG HS, that is, USB 2.0 FS/HS device/host/OTG controller, integrating the transceivers for full-speed operation, and featuring an ULPI for high-speed operation: an external PHY device connected to the ULPI is required.

D: USB 2.0 OTG HS controller with embedded on-chip HS PHYs

To find out which USB peripheral is implemented on your STM32 device refer to *Supported USB* columns in *Table 2*.

Table 2. USB on STM32 MCUs(1)

Series / Line(s)		Supported USB				Size of dedicated packet buffer SRAM	Dedicated V_{DDUSB}	Embedded pull-up resistor on USB_DP line
		A	B	C	D			
STM32F0	F04x, F072, F078	X	-	-	-	1 KByte	No	Yes
	F070x6/B	X	-	-	-			
STM32F1	F102/3	X	-	-	-	512 Bytes	No	(2)
	F105/7	-	X	-	-	1.25 KBytes		Yes
STM32F2		-	X	-	-	1.25 KBytes	No	Yes
		-	-	X	-	4 KBytes		
STM32F3	F302xB/C, F303xB/C, F373	X	-	-	-	512 Bytes	No	(2)
	F302x6/8, F302xD/E, F303xD/E	X	-	-	-	1 KByte		
STM32F4	F405/7, F415/7, F427/9, F437/9, F401, F411(3)	-	X	-	-	1.25 KBytes	No	Yes
		-	-	X	-	4 KBytes		
	F446, F469, F479, F412/3, F423(3)	-	X	-	-	1.25 KBytes	Yes	
		-	-	X	-	4 KBytes		
STM32F7	F74x, F756, F76x, F77x, F7x2	-	X	-	-	1.25 KBytes	Yes	Yes
		-	-	X	-	4 KBytes		
	F7x3	-	X	-	-	1.25 KBytes		
		-	-	-	X	4 KBytes		
STM32L0	L0x2/3	X	-	-	-	1 KByte	Yes	Yes

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 2. USB on STM32 MCUs(1) (continued)

Series / Line(s)		Supported USB				Size of dedicated packet buffer SRAM	Dedicated V_{DDUSB}	Embedded pull-up resistor on USB_DP line
		A	B	C	D			
STM32L1		X	-	-	-	512 Bytes	No	Yes
STM32L4	L4x2/3	X	-	-	-	1 KByte	Yes	Yes
	L4x5/6, L4Rx, L4Sx	-	X	-	-	1.25 KBytes		
STM32H7	H743/H753	-	X(4)	X	-	4 KBytes	Yes(5)	Yes

1. X: supported.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin must be pulled up to a voltage in the 3.0 to 3.6 V range with a 1.5 kΩ resistor.
3. STM32F401 and F411/412/413/423 devices only support FS mode.
4. USB 2.0 OTG HS device/host/OTG peripheral, supporting only full-speed operations.
5. Available through VDD50USB and VDD33USB pins.

2.1 USB implementation on STM32 products

Table 3. USB implementation - Mainstream products(1)

Feature	STM32 F070x6/B	STM32F072/8 STM32F04x	STM32F102/3	STM32F105/7	STM32F302xB/C STM32F303xB/C STM32F373	STM32F302x6/8 STM32F302xD/E STM32F303xD/E
	USB 2.0 FS device interface			USB OTG FS	USB 2.0 FS device interface	
Crystal-less USB	-	X	-			
Number of endpoints	8			4(2)	8	
Host mode channels	-			8	-	
Size of dedicated packet buffer SRAM	1 KByte(3)		512 Bytes(4)	1.25 KBytes(5)	512 Bytes(5)	1 KByte(3)
Pull-up resistor on USB_DP line	Embedded		1.5 kΩ resistor should be added			
LPM	X		-			X
BCD	X		-			
ADP	-					

1. X: supported.
2. Bidirectional, including EP0.
3. When the CAN peripheral is used, only the first 768 Bytes are available to USB, the last 256 Bytes are used by CAN.
4. The USB and CAN share a dedicated 512 Bytes SRAM, and so they can be used in the same application but not at the same time.
5. The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).

Table 4. USB implementation - High performance products(1)

Feature	STM32F2 Series STM32F401 STM32F405/7 STM32F415/7 STM32F427/9 STM32F437/9 STM32F411		STM32F446 STM32F469 STM32F479 STM32F412/3 STM32F423 STM32F74x STM32F756 STM32F76x STM32F77x STM32F7x2		STM32F7x3		STM32H743/753	
	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS
Crystal-less USB	-		-		-		X	
Bidirectional endpoints (including EP0)	4	6	6	9	6	9	9	
Host mode channels	8	12	12	16	12	16	16	
Size of dedicated packet buffer SRAM(2)	1.25 KBytes	4 KBytes	1.25 KBytes	4 KBytes	1.25 KBytes	4 KBytes	4 KBytes	
ULPI available to primary I/Os via muxing	-	X(3)	-	X(4)	-	-	-	X
Integrated PHY	FS(5)					HS(6)	FS(5)	
LPM	-		X		X		X	
BCD	-		X(7)	-	X	-	X	
ADP	-							

1. X: supported.
2. The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).
3. STM32F401 and STM32F411 devices only support FS mode.
4. STM32F412/3 and STM32F423 devices only support FS mode.
5. Internal FS OTG PHY support.
6. Internal HS OTG PHY support.
7. Only STM32F412/3 and STM32F423 devices support BCD.

Table 5. USB implementation - Ultra-low power products(1)

Feature	STM32 L0x2/3	STM32L1 Series	STM32 L4x2/3	STM32L4x5/6 STM32L4Rx STM32L4Sx
	USB 2.0 FS device interface			USB OTG FS
Crystal-less USB	X	-	X	X(2)
Number of endpoints	8			6 (bidirectional)
Host mode channels	-			12
Size of dedicated packet buffer SRAM(3)	1 KByte			1.25 KBytes (with advanced FIFO control)
Pull-up resistor on USB_DP line	X			X
LPM	X			X
BCD	X			X
ADP	-			X

1. X: supported.
2. Except for STM32L47x/L48x devices.
3. The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).

2.2 Supported USB speeds

In host mode, the USB OTG_FS supports full- and low-speed transfers, while in device mode it only supports full-speed transfers.

Table 6. Supported OTG_FS speeds(1)

Mode	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host	X	X
Device	X	-

1. X: supported.

In host mode, the USB OTG_HS supports high-, full- and low-speed transfers, while in device mode, it only supports high- and full-speed transfers.

Table 7. Supported OTG_HS speeds(1)

Mode	HS (480 Mbit/s)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host	X	X	X
Device	X	X	-

1. X: supported.

2.3 Protection against ESD and EMI

Protection against ESD and EMI is needed. The system should comply with both the JESD22-A114D (also known as HBM) and with the IEC 61000-4-2 standards.

The HBM requires that the USB pins of the component device be tolerant up to 2 kV discharge, this is the case for STM32 MCUs. Refer to *Figure 1* and *Table 8* for JESD22-A114D standard test waveform and class levels. For more details on this topic refer to the document *System Level ESD -expanded* available at www.jedec.org.

Figure 1. JESD22-A114D standard test waveform

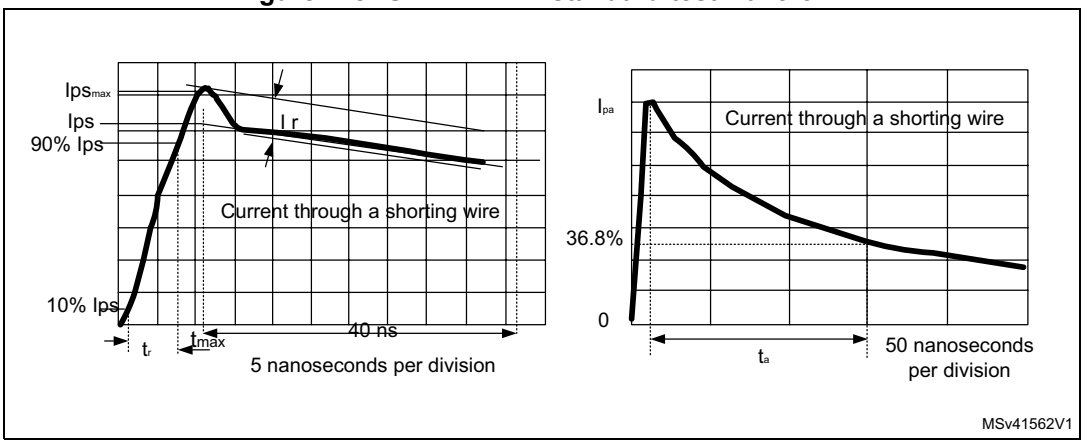


Table 8. JESD22-A114D standard class levels

Class	Voltage range	Current range
Class 0	V < 250 V	I < 0.17 A
Class 1A	250 V < V < 500 V	0.17 A < I < 0.33 A
Class 1B	500 V < V < 1000 V	0.33 A < I < 0.67 A
Class 1C	1 kV < V < 2 kV	0.67 A < I < 1.33 A
Class 2	2 kV < V < 4 kV	1.33 A < I < 2.67 A
Class 3A	1 kV < V < 8 kV	2.67 A < I < 5.33 A
Class 3B	V > 8 kV	I > 5.33 A

The system should also comply with the IEC 61000-4-2 standard on USB lines when they are connected to a receptacle. This standard is fairly different from the HBM standard. Refer to *Figure 2* and *Table 9* for IEC 61000-4-2 standard test waveform and class levels.

Figure 2. IEC 61000-4-2 standard waveform

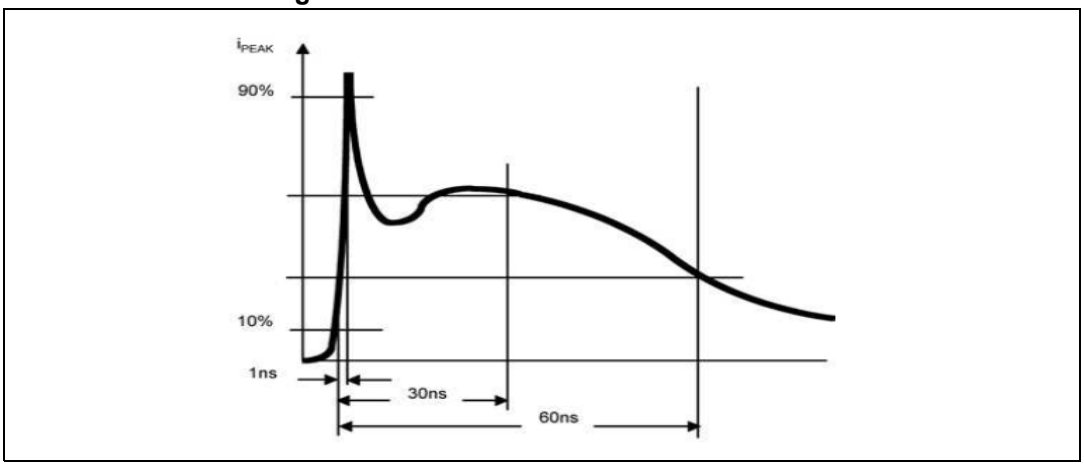


Table 9. IEC 61000-4-2 standard class levels

Level	Contact	Air	Peak current (A)
	Indicated voltage (kV)		
1	2	3	7.5
2	4	4	15
3	6	8	22.5
4	8	15	30

To see the difference between the current pulses applied in the two tests, compare *Figure 1* with *Figure 2*.

To improve the protection against high ESD surges (and then to meet the conditions requested by the standards), dedicated components (see *Table 10*) have to be placed as close as possible to the receptacle.

Table 10. ESD protection

Interface	Protection	
	Low price	Low area on PCB
USB FS	USBLC6-2SC6 (+ ESDA7P60-1U1M for VBUS)	USBLC6-2P6 (+ ESDA7P60-1U1M for VBUS)
USB FS OTG	USBLC6-4SC6	DSILC6-4P6
USB HS	ECMF02-2AMX6 (+ ESDA7P60-1U1M for 5 V VBUS)	
USB HS OTG	ECMF02-2AMX6 (+ ESDA7P60-1U1M for 5 V VBUS + ESDALC6V1-1U2 for ID)	

2.4 Clock

The FS USB device/OTG requires a precise 48 MHz clock. This frequency can be generated from the internal main PLL, or by the internal 48 MHz oscillator.

In the first case the clock source must use an HSE crystal oscillator, in the second case, the synchronization for the oscillator can be taken from:

- the USB data stream itself (SOF signalization), no external resonator/ crystal is needed (this feature is only available for devices embedding a crystal-less USB 2.0 FS device interface), or
- the internal 48 MHz oscillator trimmed on LSE.

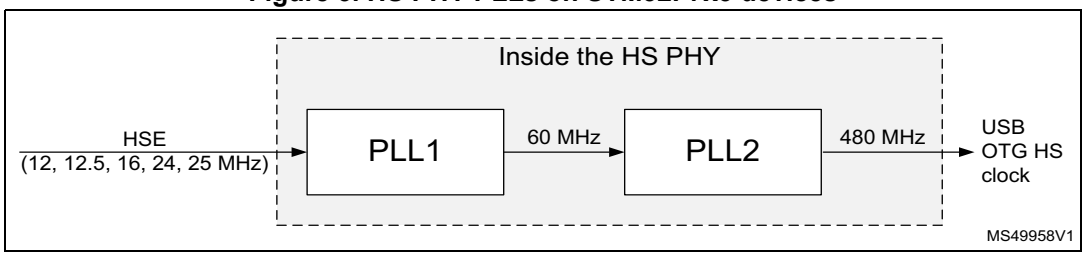
Ich will nur FS, also ok (?)

If HS operation is required, the OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output (provided from the HS PHY).

For STM32F7x3xx devices (see *Figure 3*), the USB HS PHY includes two embedded PLLs:

1. PLL1: has as clock source the HSE clock. The supported values are: 12, 12.5, 16, 24 and 25 MHz. The PLL1 outputs the 60 MHz used as input for the PLL2.
2. PLL2: outputs the high speed (480 MHz) clock.

Figure 3. HS PHY PLLs on STM32F7x3 devices



Caution: The AHB frequency has to be higher than 14.2 MHz to guarantee a correct operation for the USB OTG FS peripheral, and higher than 30 MHz for the USB OTG HS peripheral.

2.5 Power

For USB transceivers, the operating voltage ranges between 3.0 and 3.6 V. This voltage is obtained from either:

- V_{DD}: standard external power supply for the STM32MCU I/Os, or
- V_{DDUSB}: a dedicated independent power supply for USB. This power supply can be connected either to V_{DD} or to an external independent power supply for USB transceivers.

Consequently, the microcontroller can be powered with the minimum specified supply voltage, while an independent power supply 3.3 V can be connected to V_{DDUSB}.

When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA}, but it must be the last supply to be provided and the first to be removed.

Note that:

- the USB full speed transceiver functionality is ensured down to 2.7 V but not the USB full speed electrical characteristics, which are degraded when V_{DD} ranges between 2.7 and 3.0 V
- V_{DDUSB} is not available on all STM32 devices, refer to column *Dedicated VDDUSB* in *Table 2* to check whether this feature is available on the MCU you are using
- the VDDUSB pin must be connected to two external decoupling capacitors (100 nF ceramic + 1 µF tantalum or ceramic)
- some devices, when in high pin count packages, feature a dedicated VDDUSB pin, while, when assembled in low pin count packages, have only the VDD pin to ensure the USB functionality.

Also note that:

- on STM32F7x3xx devices the USB HS PHY subsystem uses an additional power supply pin: VDD12OTGHS pin is the output of the HS PHY regulator (1.2 V). An external capacitor (2.2 µF) must be connected to the VDD12OTGHS pin.
- on STM32H7x3 devices $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via an USB internal regulator, making it possible to support a V_{DD} supply different from 3.3 V. The USB regulator can be bypassed to supply $V_{DD33USB}$ directly when V_{DD} = 3.3 V.

2.6 VBUS sensing detection

Based on the USB specification, USB device shall use VBUS sensing detection. Thus, when the host presence is detected by the device, the device connects its pull up resistor to either D+ or D- data signal. This allows the host to detect the device existence on the bus.

There are two cases:

1. the USB device is bus-powered, VBUS sensing is not mandatory (USB is always connected when the device is powered)
2. the device is self-powered, VBUS sensing is mandatory.

Pin PA9, a 5 V-tolerant pin, is natively dedicated to VBUS sensing. The absolute maximum ratings table of the datasheet indicates that the 5 V-tolerant pin voltage cannot exceed V_{DD} + 4 V. User needs to avoid the situation when the MCU is not powered and 5 V VBUS is connected to PA9, because it violates the condition on absolute maximum ratings and can result in permanent damages to the device. For this purpose, it's mandatory to reduce the voltage on PA9 below 4 V. Additionally, the internal VBUS detection block within the OTG peripheral has a current consumption, as mentioned in the STM32 datasheets: "*When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.*"

For reliable and safe connection, use a voltage divider with a configuration limiting the voltage below 4 V. Additionally, to be detected, voltage needs to be higher than 0.7*V_{DD}.

3 Hardware guidelines for USB implementation

This section describes the hardware requirements for correct operation of the USB peripheral.

3.1 USB FS upstream port

In peripheral mode, VBUS power is always provided through the cable. The USB FS impedance driver is always managed internally to avoid the need to add external serial resistors on the dataline path.

According to the USB specification, there are two main use cases:

1. Self-powered applications: platforms providing their own power supply and acting as an upstream port on the cable insertion. Not allowed, under any condition, to draw any current from the USB interface.
2. Bus-powered applications: a platform supplied only through VBUS and acting as an upstream port.

3.1.1 USB FS upstream port in self-powered applications

To optimize the power consumption on self-powered platforms, only a USB PHY and a controller should be started on the VBUS detection.

It is recommended to implement a resistor bridge (refer to *Section 2.6: VBUS sensing detection* for more details), and to use an ESD protection device, to be placed as close as possible to the USB connector.

To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a voltage in the 3.0 to 3.6 V range.

In several STM32 MCUs, this pull-up resistor is already implemented (refer to column *Embedded pull-up resistor on USB_DP line* in *Table 2*), it must be added by the user in STM32 MCUs where it is not integrated.

Figure 4. USB FS upstream port with embedded pull-up resistor in self-powered applications

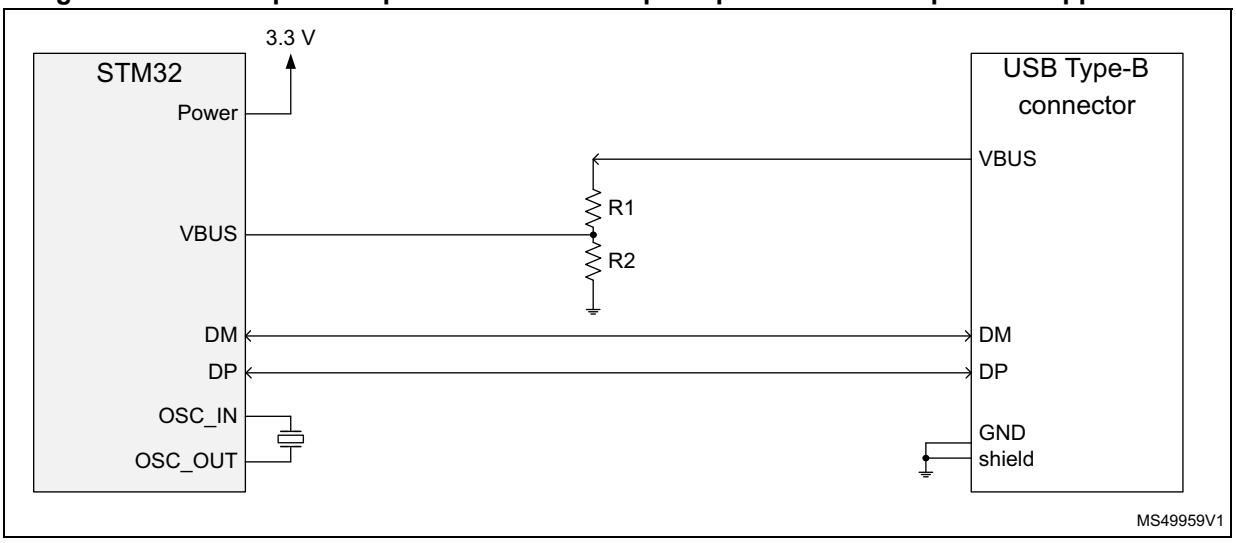
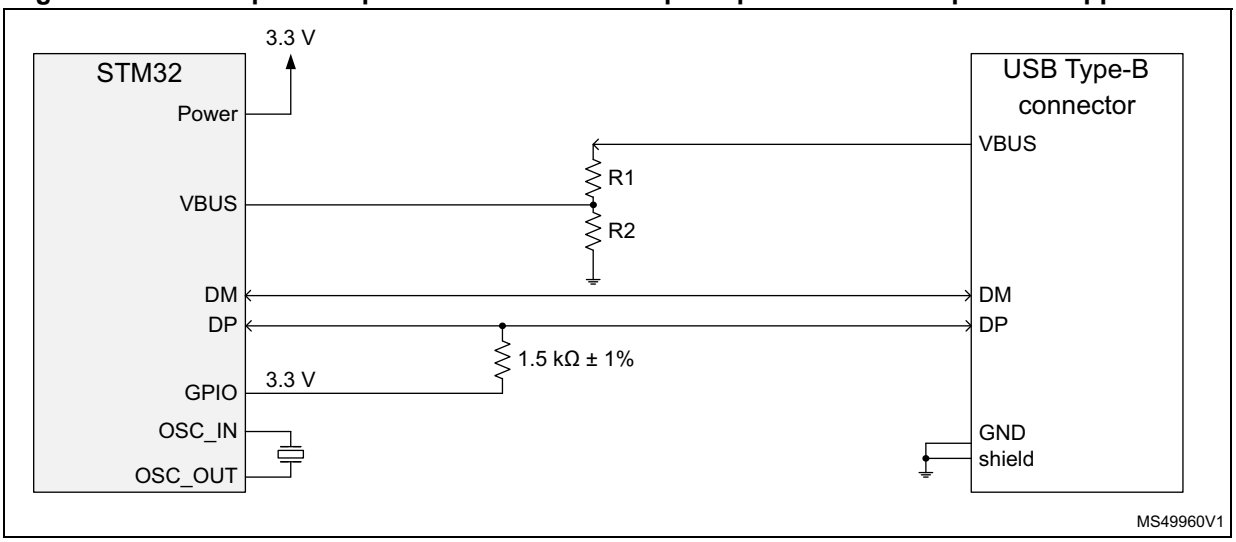


Figure 5. USB FS upstream port without embedded pull-up resistor in self-powered applications



A DP pull-up should be connected only when VBUS is plugged, a GPIO from the MCU is used to drive it after the VBUS detection.

3.1.2 USB FS upstream port in bus-powered applications

A bus-powered application is an application where the supply comes exclusively from VBUS.

The PHY and the controller must be always active to keep the host alive and to keep VBUS available.

It is recommended to use an external low-dropout regulator (LDO) to lower the input supply of the MCU (LDO39050PU33R or an equivalent component can be used), and to place the ESD protection chip (if used) as close as possible to the USB connector.

Figure 6. USB FS upstream port with embedded pull-up resistor in bus-powered applications

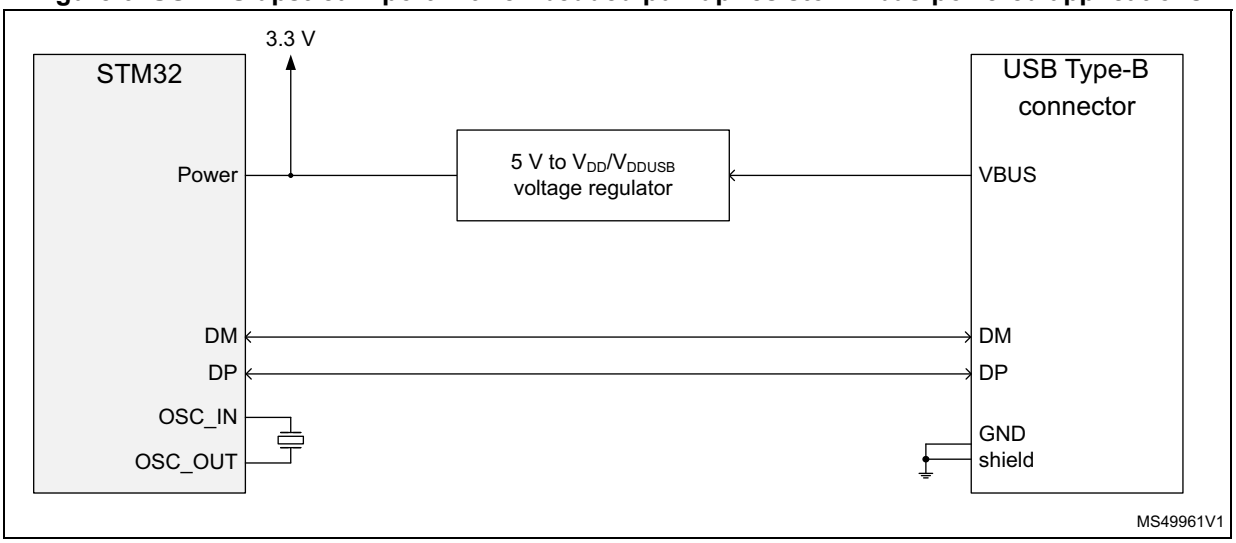
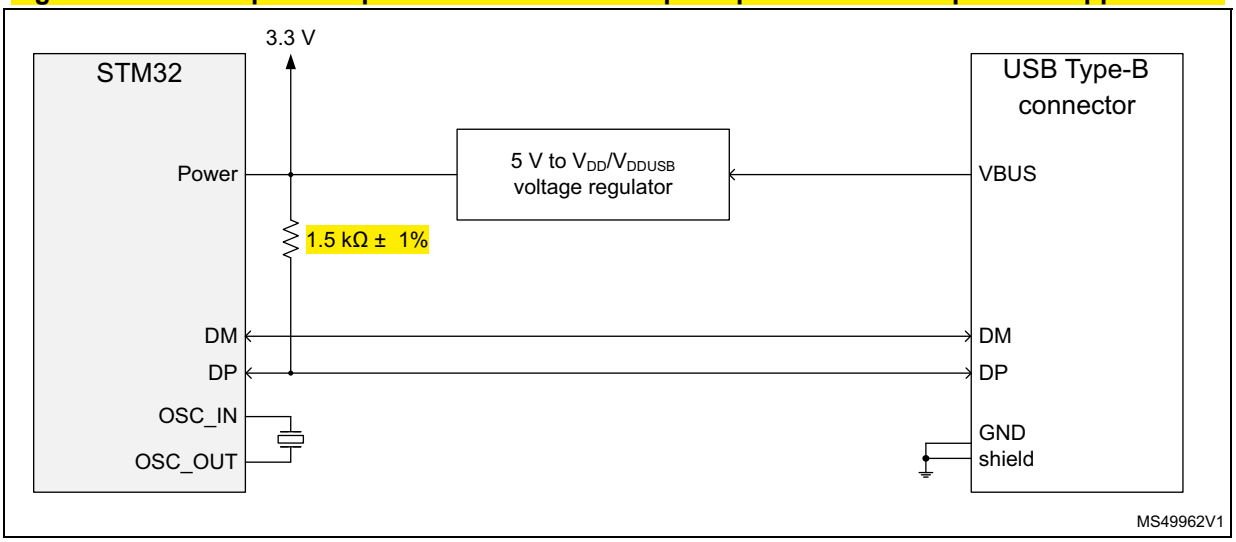


Figure 7. USB FS upstream port without embedded pull-up resistor in bus-powered applications



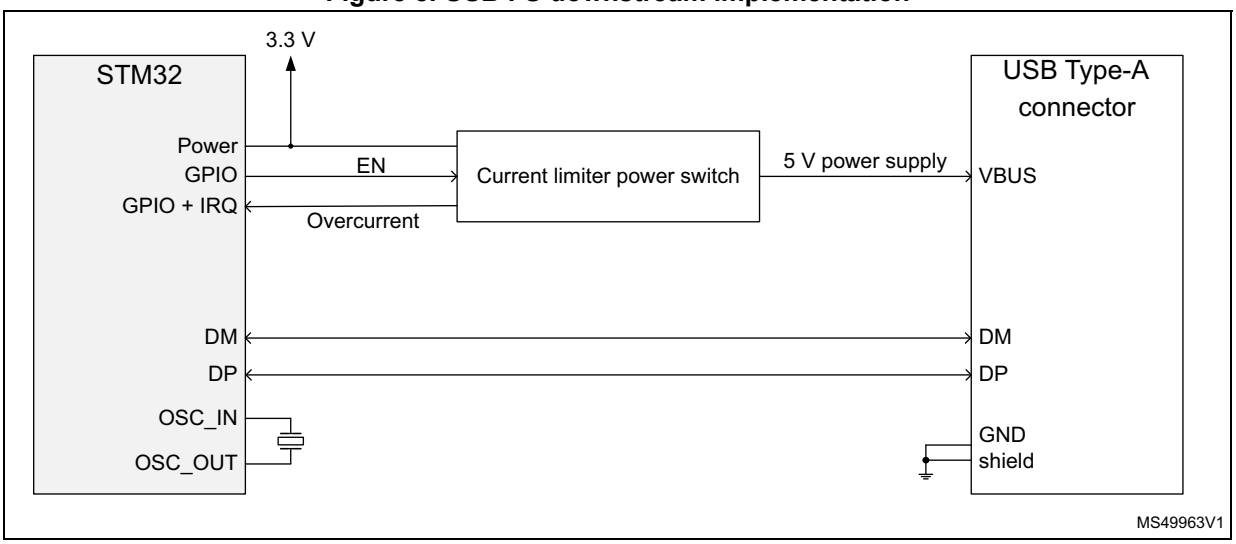
3.2 USB FS downstream port

This section describes the implementation for the USB FS downstream port, available on all the STM32 microcontrollers supporting host connection.

The USB specification requires that, if an overload on VBUS occurs, it should be indicated to the user. A switch with overcurrent protection (STMPS2151STR or an equivalent one) provides the information on the VBUS overload to the STM32 (see *Figure 8*).

The ESD protection chip, if used, has to be placed as close as possible to the USB connector.

Figure 8. USB FS downstream implementation



3.3 OTG applications through embedded PHY

The USB on-the-go products address scenarios that allow portable devices and non-PC hosts to have the following enhancements:

- targeted host capability to communicate with a list of selected USB peripherals
- support for direct connections between OTG devices
- power saving features to preserve battery life
- a new pin on connector, named ID, identifies the USB power role.

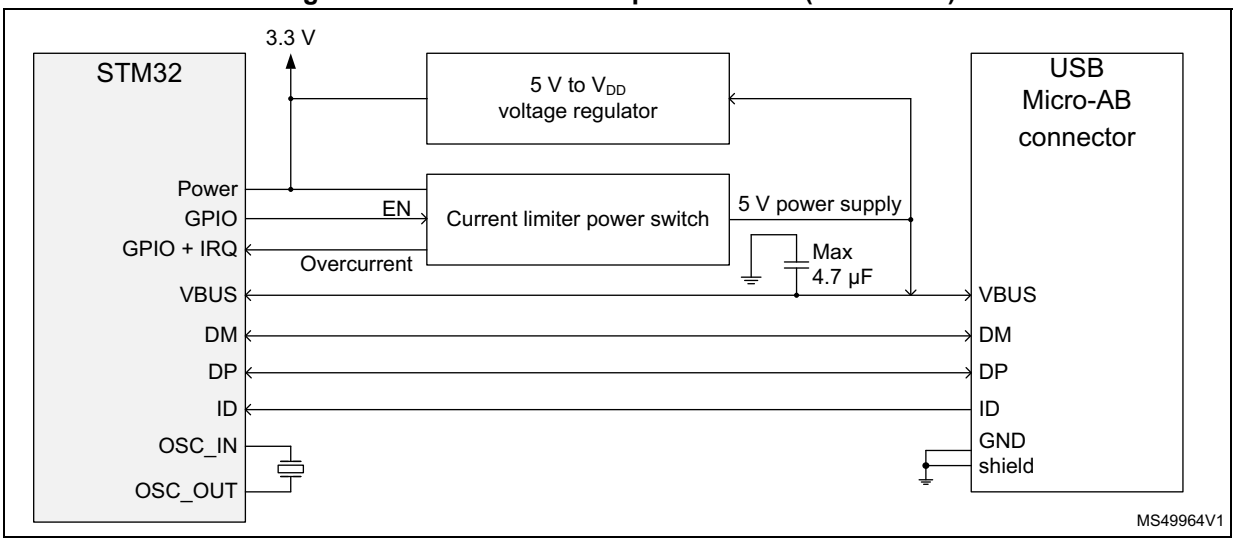
Consequently, the OTG platforms must include:

- an STM32 MCU supporting the OTG feature
- a Micro-AB connector: the USB role is identified through the ID pin
- a VBUS generation when the OTG device acts as a downstream facing port
- a VBUS current overflow, both monitoring and acting as a downstream facing port.

With reference to the scheme shown in *Figure 9*:

- the OTG specification requires the usage of a capacitor (maximum value 4.7 µF) on VBUS
- the ESD protection chip, if used, must be placed as close as possible to the USB connector
- a power switch (such as STMPS2151STR) is required
- when an over-current is detected, the information is sent to the STM32 software, which alerts the user about the issue (it is recommended to route VBUS far from DP/DM)
- the STM32 must always be supplied when the platform is connected as device to an host (in case of dead battery support, voltage on PA9 must be reduced as explained in *Section 2.6: VBUS sensing detection*).

Figure 9. OTG schematic implementation (dual-mode)



Additional considerations:

- external voltage regulator is only needed when building a VBUS powered device.
- the current limiter is required only if the application has to support a VBUS powered device, a basic power switch can be used if 5 V supply is available on the application board
- the ID pin is required in dual role only
- the same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

3.4 OTG_HS PHY connected through ULPI

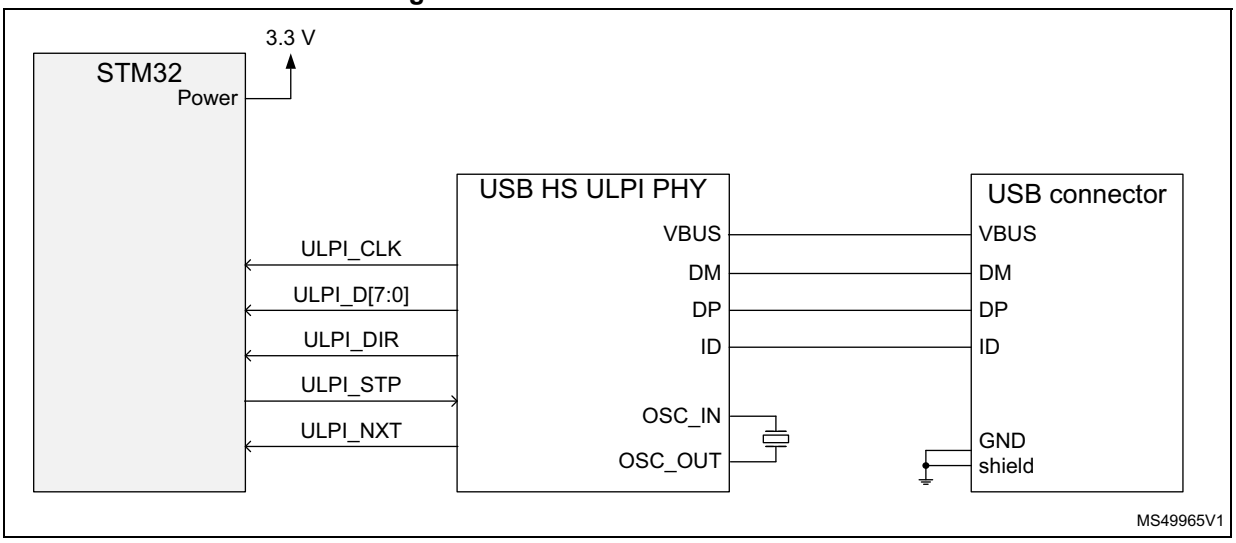
The USB standards propose routing guidelines for high speed USB platforms in the High Speed USB Platform Design Guidelines document available on USB-IF website.

Note that for a full speed driver that is part of an high speed driver, the impedance is 45 Ω ± 10%.

Recommendations:

- because the ULPI PHY is master of an ULPI CLK, a crystal oscillator is required to guarantee clock precision for the ULPI sampling and for the USB HS data sampling
- the OTG specification requires a capacitor (maximum value 4.7 µF) on VBUS
- the ESD protection chip, if used, has to be placed as close as possible to the USB connector.

Figure 10. USB HS via ULPI interface



3.4.1 External USB HS PHYs compatible via ULPI interface

Table 11 lists some external USB HS PHYs compatible through the ULPI interface.

Table 11. Compatible USB HS PHY

USB HS PHY	Tested on	
	Board	MCU
ISP1705AET	STM3240G-Eval	STM32F407
	STM3241G-Eval	STM32F417
	STM3221G-Eval	STM32F207
	STM3220G-Eval	STM32F217
USB3300-EZK	STM32779I-Eval	STM32F777
	STM32769I-Eval	STM32F769
	STM32756G-Eval	STM32F756
	STM32746G-Eval	STM32F746
	STM32479I-Eval	STM32F479
	STM32F446E-Eval	STM32F446
	STM32F439I-Eval	STM32F439
	STM32F429I-Eval	STM32F429
USB3320C-EZK	STM32H753I-Eval	STM32H753
	STM32H743I-Eval	STM32H743
	STM32F769I-Disco	STM32F769
	STM32F746G-Disco	STM32F746

3.5 USB applications through the embedded OTG HS PHY

To operate USB HS on STM32F7x3 devices there is no need to connect an external HS PHY via ULPI, as they already include an internal HS USB PHY.

There are some other recommendations in addition to those detailed for the embedded USB FS PHY:

- an external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin
- the HS PHY has an OTG_HS_REXT pin needed for calibration, this pin must be connected to GND via an external precision resistor (3 KΩ ± 1%).

3.6 STM32 on USB-IF integrators list

The list of the STM32 devices with certified USB peripherals is available on www.usb.org.

Table 12. Certified USB peripherals

STM32 device	Certified category	Speed(s)	TID
STM32F072	Peripheral	LS/FS	40001561
STM32F103	Peripheral	LS/FS	40000455
STM32F105	Peripheral	LS/FS	40001571
STM32F205/7	Peripheral	LS/FS	40001366
STM32F205/7	Peripheral	HS	40001365
STM32F207	Embedded host	FS	120000252
STM32F207	Embedded host	HS	120000251
STM32F303	Peripheral	LS/FS	40001494
STM32F373	Peripheral	LS/FS	40001496
STM32F405/7	Peripheral	HS	40001393
STM32F405/7	Peripheral	LS/FS	40001394
STM32F407	Embedded host	HS	120000253
STM32F407	Embedded host	FS	120000256
STM32F723	Peripheral	HS	40001777
STM32F723	Embedded host	FS	120000703
STM32F723	Embedded host	HS	120000702
STM32F723	Peripheral	LS/FS	40001776
STM32L053	Peripheral	LS/FS	40001612
STM32L152	Peripheral	LS/FS	10730015
STM32L476, STM32L476ZGT6U	Peripheral	LS/FS	40001658
STM32L476, STM32L476ZGT6U	Embedded host	FS	120000348

4 FAQs

Q: What is the minimum operating voltage for USB?

A: The USB, including its internal transceiver, is functional only for $V_{DD}/V_{DDUSB} \geq 2.7$ Volts. However, to be compliant with USB specification, a minimum of 3.0 V is needed.

Below 2.7 Volts the functionality of the internal transceiver is not ensured over the whole temperature range.

Q: The datasheet says that the USB transceiver functionality is ensured down to 2.7 V, but the full speed electrical characteristics are degraded in 2.7 to 3.0 V voltage range. What is the meaning of this sentence?

A: When the USB operating voltage is below 3.0 V, ST guarantees that the PLL generates correctly the 48 MHz and that the analog transceivers are functional: the USB is correctly operating.

However, the electrical signals will not be compliant with the USB2.0 Full speed specification, and, consequently, some tests needed to get the USB certification (such as the eye diagram test) will not pass. In other words, the USB is operational, but the customer cannot get the USB certification.

Refer to www.usb.org for more details about the electrical requirements needed to be compliant with the USB specification.

Q: The pull up resistor on D+ line should be always added for the STM32 acting as a full speed device?

A: A full speed device uses a pull up resistor attached to D+ to specify itself as a full speed device (and to indicate its speed). The pull up resistor at the device end will also be used by the host or hub to detect the presence of a device connected to its port. Without a pull up resistor, USB assumes there is nothing connected to the bus.

On some STM32 microcontrollers the pull up resistor is already embedded. Otherwise, the customer needs to add it. Refer to *Embedded pull-up resistor on USB_DP line* in *Table 2* to know if this resistor is integrated on the STM32 MCU you are using.

Q: Can the external clock source (HSE bypass mode) be used for the USB clock source?

A: Yes, this is possible. HSE ON with an external crystal or HSE in bypass mode are required, but HSI cannot be used.

Q: Can we use two USB ports simultaneously (when they are available)?

A: Yes, this is feasible.

Q: It is possible to connect more than one device to the same USB port configured as host?

A: No, hub operation is not supported.

Q: Can the STM32 USB FS peripheral be used to make a USB LS device?

A: No, only Full speed transfers are supported in device mode. Refer to *Section 2.2: Supported USB speeds* for more details.

Q: According to the USB specification (FS driver characteristics), when the full-speed driver is / is not part of a high-speed capable transceiver, the impedance of each of the drivers must be in the range 40.5 to 49.5 Ω / 28 to 44 Ω, respectively. Are the STM32 devices embedding those matching resistors?

A: Yes. On the internal USB PHYs, the matching output impedance is already embedded in the pad transceiver and is in line with the USB specification. No external resistors are needed.

Q: Is it possible to use the USB peripheral when the operating voltage V_{DD} on the MCU is below 2.7 V?

A: This is possible only if a VDDUSB pin is available to power the USB block.

In this case, the microcontroller can be powered with the minimum specified supply voltage, while an independent 3.3 V power supply can be connected to V_{DDUSB}.

5 References

- System Level ESD-expanded, JEDEC, September 2013.
- Improve System ESD Protection While Lowering On-Chip ESD Protection, www.mobiledevdesign.com, February 2009.
- USB 2.0 specification, revision 2.0, April 2000, available at www.usb.org.
- On The Go and Embedded Host Supplement to the USB revision 2.0 specification, revision 2.0, July 2012 available at www.usb.org.
- High Speed USB Platform Design Guidelines, available at www.usb.org.

6 Conclusion

The requirements described in *Section 3: Hardware guidelines for USB implementation* are mandatory for correct operation of the USB peripheral on STM32 MCUs, and to ensure its electrical compliance with the USB standard.

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
10-Aug-2016	1	Initial release.
24-Nov-2016	2	Confidentiality level of the document updated to ST Restricted.
27-Apr-2018	3	Document classification changed from ST Restricted to Public. Scope extended to all STM32 microcontrollers. Updated *Introduction* and *Section 3: Hardware guidelines for USB implementation* and its subsections. Added *Section 1: List of abbreviations and acronyms*, *Section 2: USB on STM32 products* and its subsections, *Section 4: FAQs* and *Section 6: Conclusion*. Updated all figures in *Section 3: Hardware guidelines for USB implementation*. Removed former *Table 1: Applicable products*, *Section 1: Layout guidelines for USB FS devices*, *Section 1.1: PCB track impedance and routing on FS data lines*, *Section 4: Hardware guideline for OTG product implementation* and *Section 5: OTG USB high speed PHY connected to STM32 through the ULPI link.*