- **Set #5** (Due Wed Nov 16)

1) Compatible SPI devices can be daisy-chained one to another.
a) What advantage does SPI chaining provide? Be specific.

Daisy Chaining can save on chip select pins. This process makes it possible for every target in the chain to execute a different command.

b) What disadvantage is there in daisy chaining? Make sure your answer describes how the disadvantage arises.
c) Why can't the 25LC256 be daisy chained? Give the main reason.

For daisy-chaining to work successfully, all the targets must be able to output at their SDO outputs what is shifted into their SDI inputs, and not respond to any command until the CS line goes high. The 25LC256 cannot be daisy chained because it is not capable of outputting what is input to the SDI to the SDO.

2) PPS
a) What port bits (by port bit name, not actual pin number) can U2RX be assigned to?

RPD9,RPG6,RPB8,RPB15,RPD4,RPB0,RPE3,RPB7,RPF12,RPD12,RPF8, RPC3,RPE9

b) What port bits can U2TX be connected to?

RPD1, RPG9, RPB14, RPD0, RPB6, RPD5, RPB2, RPF3, RPF13(1), RPC2(1), RPE8(1), RPF2(1)

c) What port bits can SDO1 be connected to?

RPD2, RPG8, RPF4, RPD10, RPF1, RPB9, RPB10, RPC14, RPB5, RPC1(1), RPD14(1), RPG1(1), RPA14(1), RPD6(2)

d) What port bits can SCK1 be connected to?

RPD1, RD1
e) Give the C instruction(s) needed to setup U2RTS on port bit B3 (don't include unlocking or locking instructions).

RPB3R = 0010;

f) Give the C instruction(s) needed to setup U2CTS on port bit D6 (don't include unlocking or locking instructions).

U2CTSR = 1110;

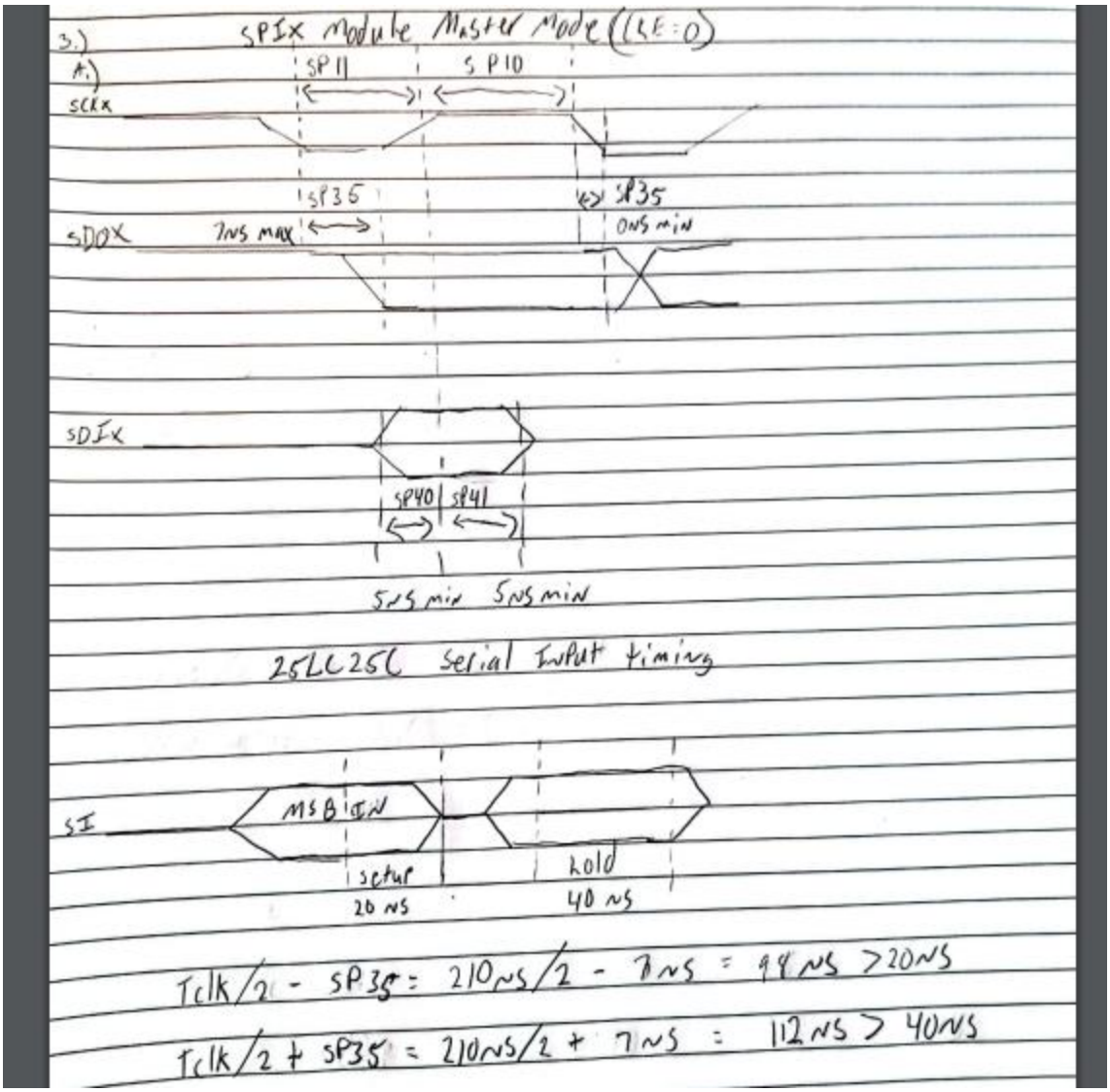
g) Give the C code needed to lock the PPS registers.

CFGCON = (1 | _CFGCON_IOLOCK_MASK);

In **questions 3 and 4**, be sure to give a **timing diagram** with relevant timing parameters clearly labeled and give a **symbolic equation** and a **numeric result**. Symbolic equations should **include min and max** designations where appropriate. Also, don't concern yourself with SP31 and SP30 -- these are the clock rise and fall parameters. For the purposes of this assignment, just assume that the actual clock rise and fall is instantaneous. In your equations use Tclk/2 (or Tsck/2) in place of SP11 and SP10.

3) SPI Timing

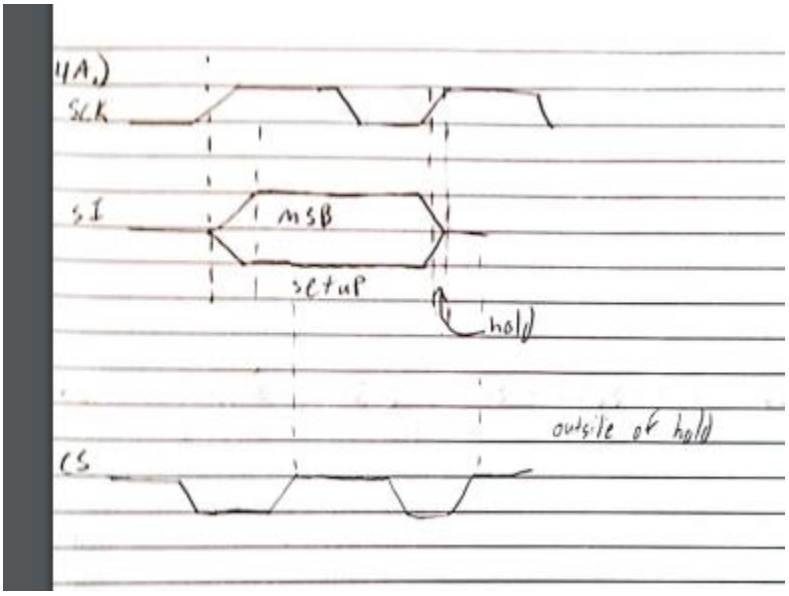
a) In class we determined that the output delay of the 25LC256 and the setup and hold requirements on the PIC32MZ's SDI pin require that the SCK operate with a period of at least 210 ns. Assuming that SCK is operating with a period of 210ns, determine (based on PIC32MZ timing parameter SP35) the actual minimum setup time and hold time that is provided by the PIC32MZ to the SDI input of the 25LC256. Show that these times meet the 25LC256 setup and hold requirements (parameters 5 and 6) for a 3.3V Vcc. Assume CKE =0 and CKP = 1.



b) Parameter 15 of the 25LC256 (T_{DIS}) gives the maximum time from negating the 25LC256's CS line to when the SDO line goes high impedance. We could use this to know how much time needs to be provided between negating the 25LC256 CS and enabling the CS of another SPI device that uses the same SDO line in order to avoid conflict. To do this, we also need to know how soon the other device will start driving the SDO line after we assert its CS line. Note however, that the 25LC256 doesn't provide a timing parameter that tells how long from the time its CS is asserted to when it will start driving its SDO line (see figures 1-2 and 1-3 in the 25LC256 data sheet). Why don't the manufacturers of the 25LC256 need to provide this information? Hint: ask yourself what the only time the 25LC256 drives its SDO line is.

Since the SDO line will only start driving after the LSB of the SDI line has been processed depending on how many bits are being processed the timing will change.

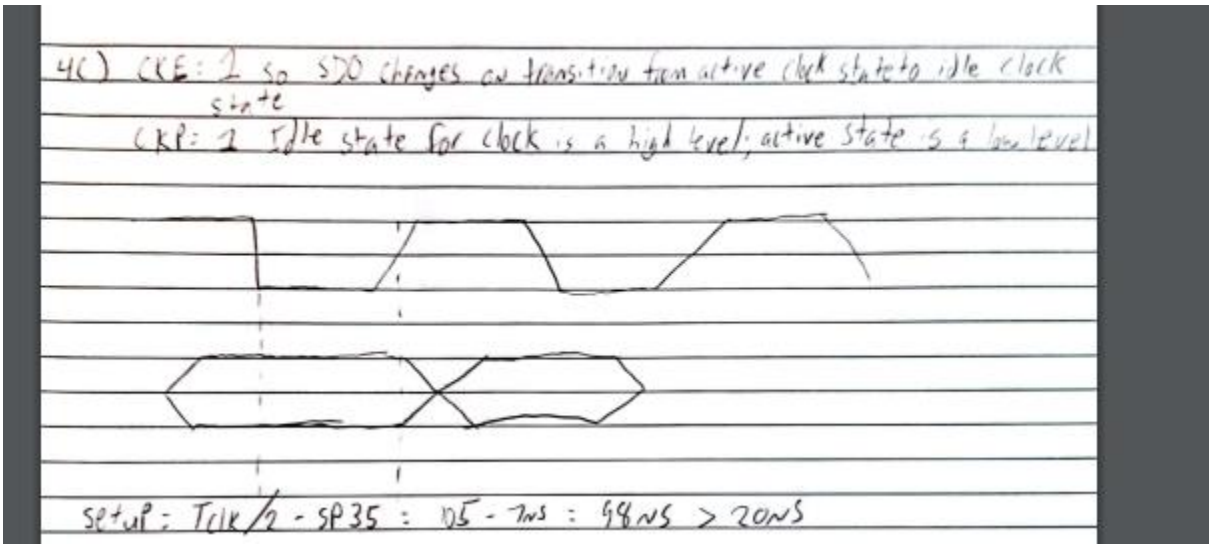
4) In part a above (and in lab) we used CKE = 0 and CKP = 1. Let us consider some of the other possibilities. Remember that the 25LC256 samples data at its inputs on the positive edge of the clock. Assume a 210ns clock period.
a) If CKE = 0 and CKP = 0, determine the minimum setup and hold times that will be provided to the 25LC256 on its data input. Give the actual provided minimum setup and hold times and show that the setup requirement (parameter 5) will be met, but that the hold requirement (parameter 6) is not.



b) Even if the hold requirement in part a was met, this mode would not be appropriate. Why? (Hint consider what the first bit clocked into the 25LC256 will be.)

Since CKP is 0 the active state of CS is high which is the state we start in so we will be starting the process before we are ready.

c) If CKE = 1 and CKP = 1, we won't have the problem outlined in part b, hold times are the same as in part a, and setup times for all but the first bit are the same as in part a. Determine what the setup time is for the first bit. Does it meet the 25LC256 setup requirement?



Yes, it does.

d) If CKE = 1 and CKP = 0 the hold times and the setup times for all but the first bit will be the same as they were in D.2 part a). Determine the setup time for the first bit. Does it meet the 25LC256 setup requirement?