Lab 5 Pseudocode

State 0 // start Check Status

Assert CS

Send Read Status command to 25LC256

Wait for TBE

Send oDummy

Set state to 1

State 1 // mid Check Status

Read iDummy

Set state to 2

State 2 // end Check Status, start Read or Write Enable or repeat Check Status

Read Status

Negate CS

Assert CS if (Status.WIP == 1) { //Write is still in progress, we need to start Check Status sequence again

Send Read Status command to 25LC256

Wait for TBE

Send oDummy

Set state to 1

}

else if (Write operation) { //start Write Enable

Send Write Enable command to 25LC256

Set state to 3

}

else { // start Read n sequence

Send Read command to 25LC256

Wait for TBE

Send MSA to 25LC256

Set state to 4

}

State 3 // end Write Enable, start Write

Read iDummy

Lab 5 Pseudocode

Negate CS

Assert CS

Send Write command to 25LC256

Wait for TBE

Send MSA to 25LC256

Set state to 6

State 4 // Write LSA for read

Read iDummy

Send LSA to 25LC256

Set state to 5

State 5 //Write continued write dummy

Read iDummy

Write oDummy

Set state to 8

State 6 //Write LSA for Write

Read iDummy

Write oDummy

Set state to 7

State 7 //Write data

Read Dummy

Write data

Set state to 10

State 8 //Write continued

Read Dummy

If more than 1 byte write Dummy

Set state to 9

State 9 //

Read data

If more than 1 byte left check if there are more than 2 bytes left

Set state to 9

Lab 5 Pseudocode

Increment index

Increment pointer

If more than 2 bytes left write dummy

Else set EEPromBusy to 0

Set index to 0

Negate CS

Set state to 0

State 10

Read Dummy

If more than 1 bye left to write

Increment index

Increment pointer

Write data

Set state to 10

Else set state to 11

Read dummy

Set EEPrombusy to 0

Set index to 0

Negate CS

Set state to 0