Module: Final1

A picture containing text, clock, screenshot

Description automatically generated

The Final1 module is the top-level module and handles connecting all the modules together to form the final design.

Module: clk\_divider

Diagram, schematic

Description automatically generated

The clk\_divider module takes the onboard 50MHz signal and divides it down the desired 1Hz. It does this by only alternating its output once a count of 25000000 is reached.

Module: taillight\_FSM

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

The taillight\_FSM module handles the changing of states based off the inputs and the execution of each desired outcome. An Idle state is used for when all the inputs are low or more than one incompatible input is high at the same time. Right is the state which handles the right blinker functionality by iterating through lighting up each led one at a time to create the desired effect. Left is the same as right but using the leds on the left side. BK handles the break lights which just turns all leds on and stays that way as long as the BK input is high. HAZ state is the priority state and overrides any other inputs. This state blinks all the leds on and off simultaneously. If the brake input and the left input are both high, we go to LBK state. This state does the standard left blinker but also does the functionality of the BK state on the right leds. If the brake input and the right inputs are both high, we go to the RBK state. This state is the same as the LBK state just reversed having the Right state functionality but with the left leds going high.