Module: Final2

Diagram

Description automatically generated

This is the top level module that makes all the connections for the other modules creating the final product.

Module: clk\_divider

Diagram

Description automatically generated

The clk\_divider module takes the onboard 50MHz signal and divides it down the desired 1Hz. It does this by only alternating its output once a count of 25000000 is reached.

Module: clk\_FSM

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

This module handles both the states and the count for the clock. If set and hour or minute are pressed it changes states to the appropriate state either Hour or Minute to adjust those values. If those cases are not met it will stay in the Count state which increments seconds each second. This state also handles rolling over from 59 seconds to 1 minute and 59 minutes to 1 hour via if statements.

Module: binary\_to\_bcd

Diagram, schematic

Description automatically generated

The binary\_to\_bcd module handles converting a binary value to a BCD value for use with the seven segment displays.

Module: seven\_seg

Diagram

Description automatically generated

The seven segment module uses a case statement to light up the appropriate segments of the display depending on the BCD value it received.