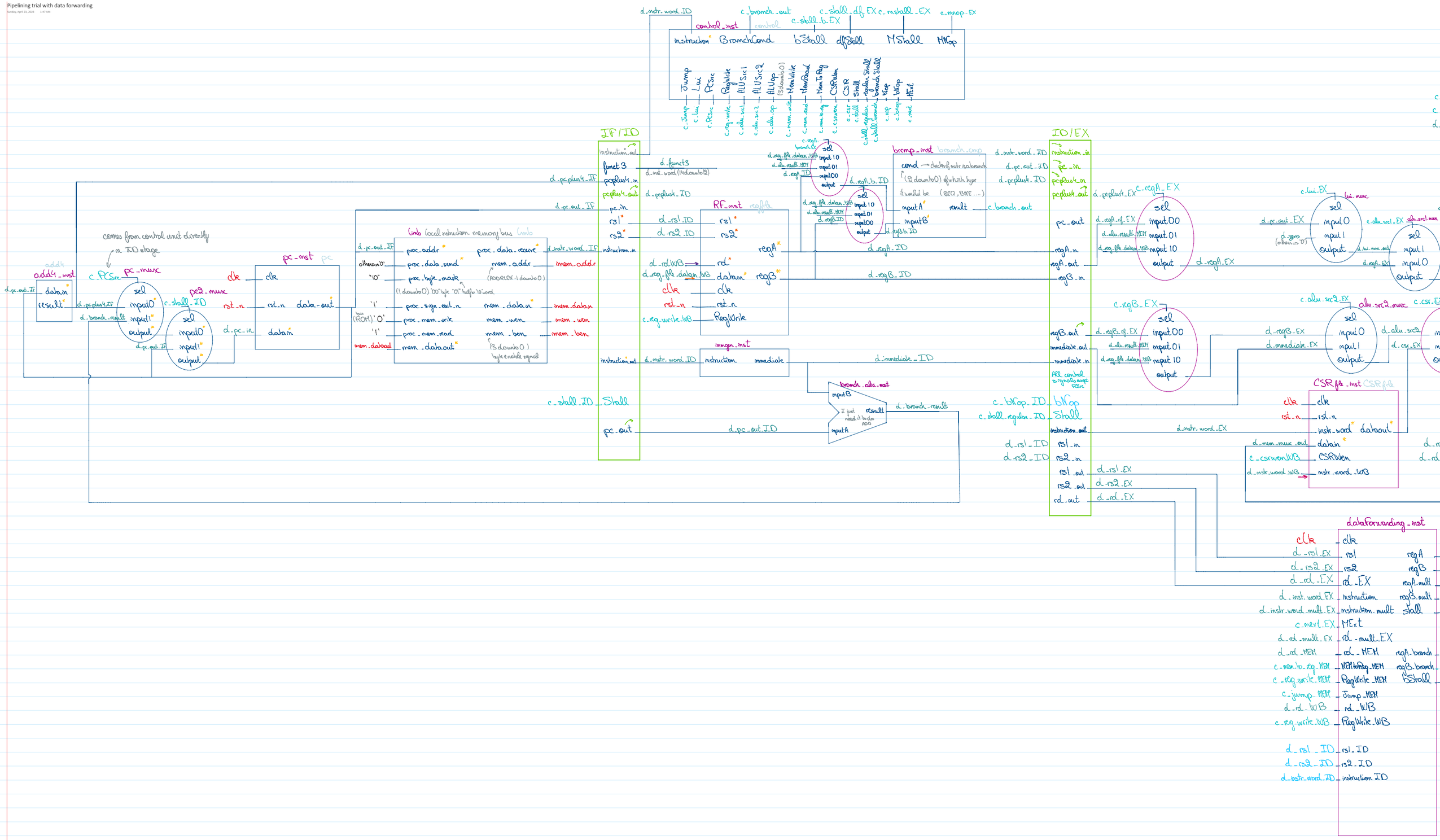
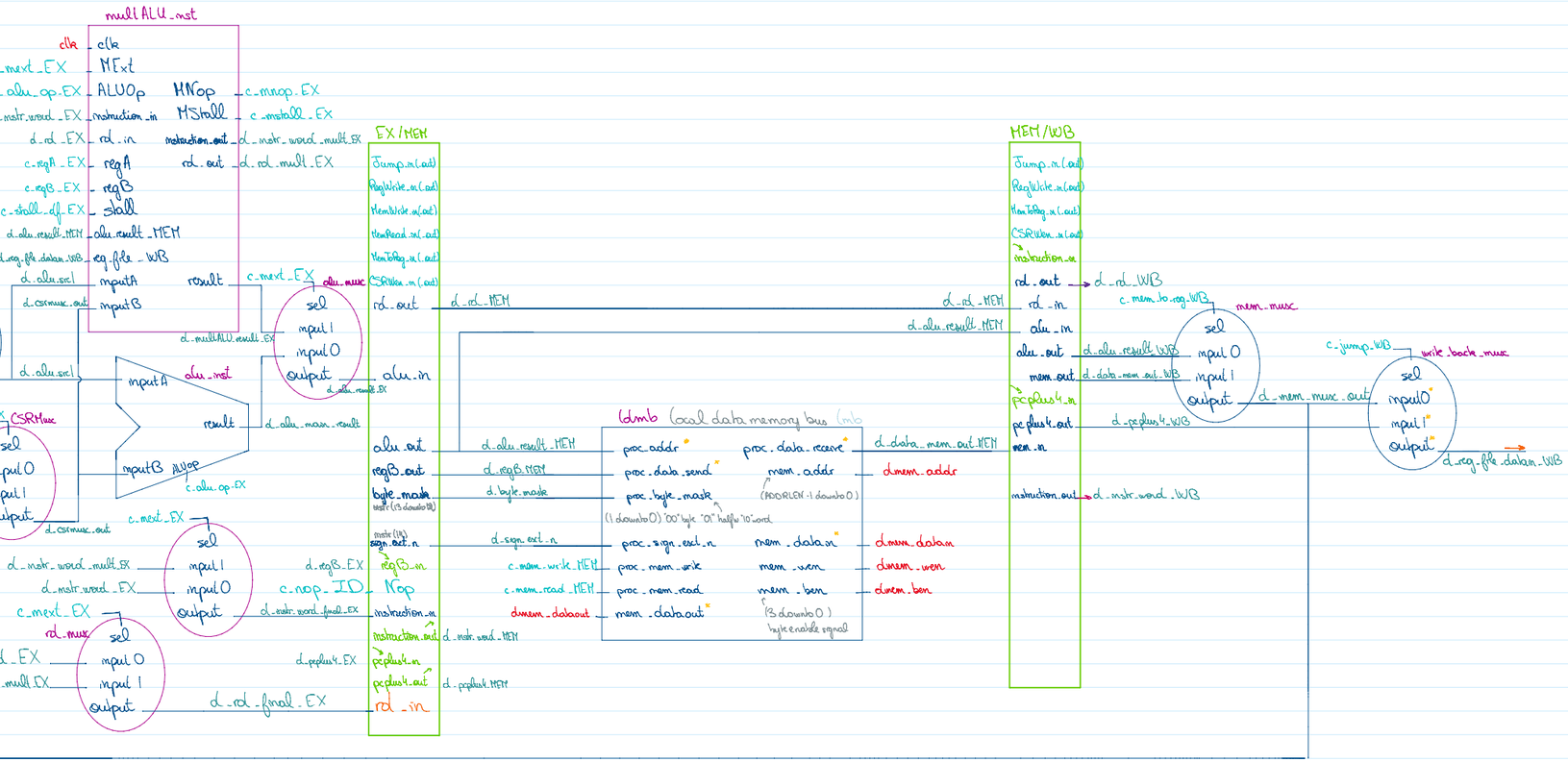
Pipelining trial with data forwarding

Sunday, April 23, 2023 1:47 AM




mult ALU_mst
clk
MExt
ALUOp
instruction_in
rd_in
regA
regB
Stall
alu_result_MEM
reg_file_WB
inputA
inputB
MNop
MStall
instruction_out
rd_out
result
c_mnext_EX
c_mnop_EX
c_mstall_EX
d_mstr_word_mult_EX
d_rd_mult_EX
c_mnext_EX
d_mult_ALU_result_EX
alu_mux
sel
input 1
input 0
output
d_alu_result_EX
alu_mst
d_alu_main_result
c_alu_op_EX
c_mnext_EX
d_mstr_word_mult_EX
d_mstr_word_EX
c_mnext_EX
rd_mux
d_EX
d_mult_EX
d_rd_final_EX
EX/MEM
Jump_in(out)
RegWrite_in(out)
MemWrite_in(out)
MemRead_in(out)
MemToReg_in(out)
CSRWen_in(out)
rd_out
alu_in
alu_out
regB_out
byte_mask
sign_ext_n
regB_in
Nop
instruction_in
instruction_out
pcplus4_in
pcplus4_out
rd_in
d_rd_MEM
d_alu_result_MEM
d_regB_MEM
d_byte_mask
d_sign_ext_n
c_mem_write_MEM
c_mem_read_MEM
dmem_dataout
d_regB_EX
c_nop_ID
d_mstr_word_final_EX
d_mstr_word_MEM
d_pcplus4_EX
d_pcplus4_MEM
ldmb (local data memory bus (mb
proc_addr
proc_data_send
proc_byte_mask
(1 downto 0) "00" byte "01" halfw "10" word
proc_sign_ext_n
proc_mem_write
proc_mem_read
mem_data_out
proc_data_receive
mem_addr
(ADDRLEN-1 downto 0)
mem_data_in
mem_wen
mem_ben
(3 downto 0)
byte enable signal
d_data_mem_out_MEM
dmem_addr
dmem_datain
dmem_wen
dmem_ben
MEM/WB
Jump_in(out)
RegWrite_in(out)
MemToReg_in(out)
CSRWen_in(out)
instruction_in
rd_out
rd_in
alu_in
alu_out
mem_out
pcplus4_in
pcplus4_out
mem_in
instruction_out
d_rd_WB
c_mem_to_reg_WB
mem_mux
d_alu_result_WB
d_data_mem_out_WB
d_pcplus4_WB
d_mstr_word_WB
c_jump_WB
write_back_mux
d_mem_mux_out
d_reg_file_datain_WB
c_regA_EX
c_regB_EX
c_regA_mult_EX
c_regB_mult_EX
c_stall_dff_EX
c_regA_branch_EX
c_regB_branch_EX
c_stall_b_EX