Christopher James – MXXXXXX02

CMPS 5133 – Advanced Architecture

**Project Assignment: K-way Set Associative Cache Memory**

K = 3 + (02 % 4)

K = 3 + 2 = 5

The project consisted of designing and implementing a simulator for a 5-Way Set Associative Cache Memory with a parameterized cache line size and a constant cache size of 10240 bytes.

A simulator was designed and implemented with the following results:

|  |  |  |
| --- | --- | --- |
| **Line Size** | **Hits** | **Misses** |
| 4 | 406031 | 40670 |
| 8 | 413114 | 33587 |
| 16 | 423254 | 23447 |
| 32 | 429978 | 16723 |
| 64 | 433957 | 12744 |
| 128 | 435623 | 11078 |
| 256 | 435864 | 10837 |
| 512 | 434116 | 12585 |
| 1024 | 423348 | 23353 |

As we can see from the results, the hit rate increases up until a line size of 256 bytes, after which, the number of hits begins to decline.

The graph on the next page illustrates this on a line graph.