ELC 2137 Lab 9: Four Digit Display

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Summary

This lab exlpored using a Basys3 board to produce a 4-digit display with the ability to switch between hexadecimal and decimal (BCD) output using the previous 2-digit, 7-segment display and BCD converter. Using Verilog, some skills gained in this lab include: Useing parameters to create flexible, reusable modules, import modules, modify modules, use them to design a modular system using constraint files,and creating a design on a board. Overall, this lab demonstrated how to utilize software and programmable logic to produce a hardware output.

Results

Time (ns):	0-5	5-10	10-15	15-20	20-25	25-30	30-35	35-40	40-45	45-50	50-55
D (hex)	0	0	A	A	3	3	0	0	0→6	6	6
clk	0	1	0	1	0	1	0	1	0	1	0
en	0	0	1	1	1→0	0→1	1→0	0	0→1	1	1
rst	0	0→1	0	0	0	0	0	0	0	0	0
Q (hex)	X	X→0	0	a	a	a	a	a	a	6	6

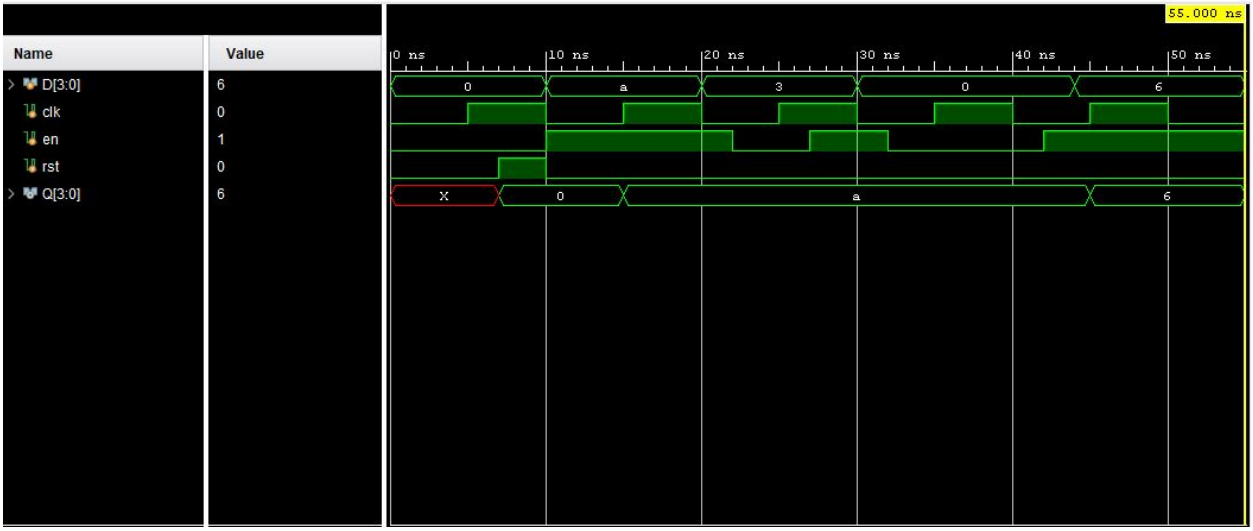

Figure 1: register expected results table and simulation

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Table 1: *alu* expected results table skeleton

Time (ns):	0-10	10-20	20-30	30-40	40-50	50-60
in0 in1 op						
out						

Code

Listing 1: Register Source File

```
// Chris Jones , ELC 2137, 2020 -3-24

module register #(parameter N=1)
(
input clk, rst, en,
input [N-1:0] D,
output reg [N-1:0] Q
);

always @( posedge clk , posedge rst )
begin
if (rst ==1)
Q <= en ;
else if (en==1)
Q <= D ;
end
// Notes:
// - Reset is asynchronous , so this
// block needs to execute when rst
// goes high.
// - We want enable to be synchronous
// (i.e. only happens on rising
// edge of clk), so it is left out
// of "sensitivity" list.
endmodule
```

Listing 2: Mux 2 Test Bench Code

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module mux2_Test( );

reg [15:0] In0, In1;

reg sel;

wire [15:0] Out;

mux2 #(.N(16))  m1(
```

```
.in0(In0), .in1(In1),

.out(Out), .sel(sel)

);


initial begin

In0 = 16'b0000000000000000; In1 = 16'b0000000000000001; sel = 1'd0; #10;

In0 = 16'b0000000000000010; In1 = 16'b0000000000000011; sel = 1'd0; #10;

In0 = 16'b0000000000000100; In1 = 16'b0000000000000101; sel = 1'd1; #10;

In0 = 16'b0000000000000110; In1 = 16'b0000000000000111; sel = 1'd1; #10;


$finish;

end

endmodule
```

Listing 3: Mux 4 Source File

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module mux4 #(parameter N =4)(
input [N-1:0] in0, in1, in2, in3,
input [1:0] sel,
output reg [3:0] out
);

always @*
case(sel)
0: out = in0;
1: out = in1;
2: out = in2;
default: out = in3;
endcase
```

Listing 4: Mux 4 Test Bench Code

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module mux4_Test();
reg [3:0] in0, in1, in2, in3;
reg [1:0] sel;
```

```
wire [3:0] out;

mux4 m4(
.in0(in0), .in1(in1), .in2(in2), .in3(in3), .sel(sel), .out(out)
);

initial begin
in0 = 4'b0000; in1 = 4'b0001; in2 = 4'b0010; in3 = 4'b0011; sel = 2'b00;
   #10;
in0 = 4'b0100; in1 = 4'b0101; in2 = 4'b0110; in3 = 4'b0111; sel = 2'b01;
   #10;
in0 = 4'b1000; in1 = 4'b1001; in2 = 4'b1010; in3 = 4'b1011; sel = 2'b10;
   #10;
in0 = 4'b1100; in1 = 4'b1101; in2 = 4'b1110; in3 = 4'b1111; sel = 2'b11;
   #10;

$finish;
end
endmodule
```

Listing 5: Annode Decoder Source File

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module annode_decoder(
input [1:0] in,
output reg [3:0] out
);

always @*
case(in)
0: out = 4'b1110;
1: out = 4'b1101;
2: out = 4'b1011;
default: out = 4'b0111;
endcase
endmodule
```

Listing 6: Annode Decoder Test Bench Code

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module annode_decoder_test();
reg [1:0] in;
wire [3:0] out;

annode_decoder ant(

.in(in), .out(out)
);

initial begin
```

```
in = 2'b00; #10;
in = 2'b01;  #10;
in = 2'b10;  #10;
in = 2'b11;  #10;

$finish;
end
endmodule
```

Listing 7: Sseg4 Source File

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module sseg4(
input [15:0] data,
input hex_dec,
input sign,
input [1:0] digit_sel,
output [6:0] seg,
output dp,
output [3:0] an
);
wire [15:0] W1 ;
wire [15:0] W2 ;
wire [3:0] W3;
wire [6:0] W4;
wire [3:0] W5;
wire W6;
BCD11_2 B1( .in11(data[10:0]), .out11(W1));
mux2 #(.N(16)) B2( .in0(W1), .in1(data), .sel(hex_dec), .out(W2));
mux4 B3( .in0(W2[3:0]), .in1(W2[7:4]), .in2(W2[11:8]), .in3(W2[15:12]), .
   sel(digit_sel), .out(W3));
sseg_decoder B5( .num(W3), .sseg(W4));
mux2 #(.N(7)) B6( .in0(W4), .in1(7'b0111111), .out(seg) , .sel(W6));
and G2( W6, sign, ~W5[3]);
annode_decoder B7( .in(digit_sel), .out(W5));
assign dp = 1;
assign an = W5;
endmodule
```

Listing 8: Sseg4 Manual Source File

```
// Jake Simmons and Chris Jones , ELC 2137, 2020 -3-24

module sseg4_manual(
input [15:0] sw,
output [6:0] seg,
output dp,
output [3:0] an
);
sseg4 Sseg4(
.digit_sel(sw[13:12]), .sign(sw[14]), .hex_dec(sw[15]),
.data({4'b0000, sw[11:0]}), .seg(seg), .dp(dp), .an(an)
);
```

```
endmodule
```