CMPE 12L

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Lab 1:

Logic Design for part B:

I looked for all the cases where the output was 1(there are 3 of them), then I looked into the input values, such as A, B, C. Whenever I saw 0 for A(for example), I wrote down !A and so on. For 1, I just wrote A. I got three products(because there are 3 outcomes, which result in output of 1) and then I summed all these products and got sum of products.

Original design was 38 transistor(32 of them were 3 ANDS and 1 OR, all the rest were inverters). The NAND gate design came out to be 30 transistors(24 of them were 4 NANDs, and the rest were inverters). As one can see, using NAND gate instead of AND, makes design approximately 25% smaller, because all the ANDs are in fact NANDs with inverters in the output. Inverter takes 2 transistors, so that's why NAND is more efficient.

The final version, which was the same logic, but minimized using the boolean algebra laws and identities resulted in total of 24 transistors.