

Lab 1 : FPGA Basic Design

CME433-01

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Sept 24th, 2021

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# Question 1

When using a case statement, you are inferring ROM functions which means that the synthesis tools are sets of registers that can be replaced with the ALTSYNCRAM or LPM\_ROM IP Core. These tools for the case statement generate optimized decode logic to quickly select which case statement is valid. Whereas the if/else statement can incorporate priority-encoded logic, but the synthesis requires more space as it’s a series of MUXs. Having a MUX for each condition makes the synthesis of the if/else statements more complex in hardware implementation.

# Question 2

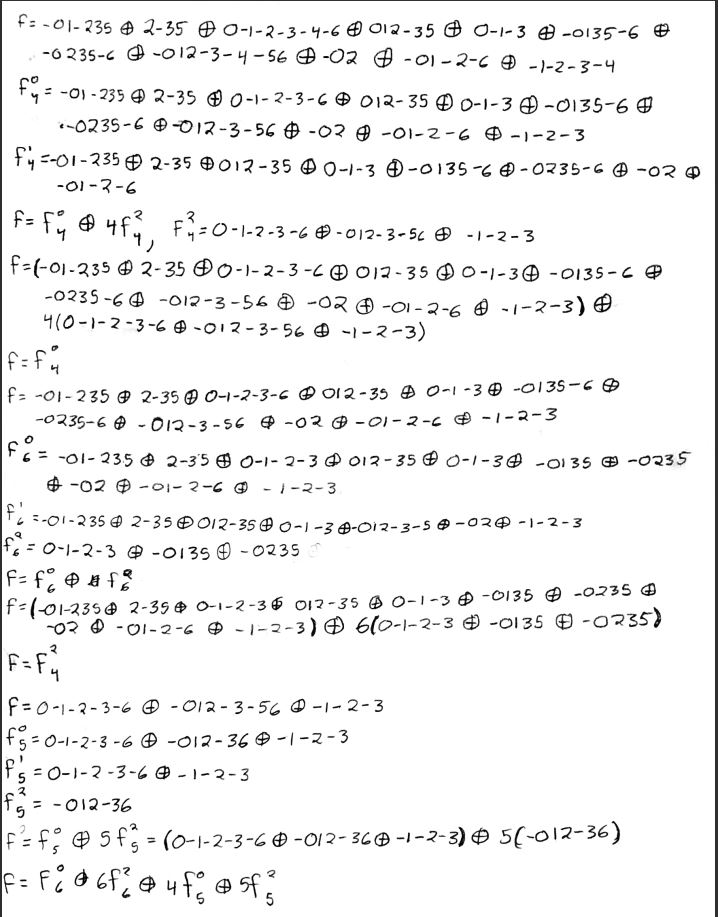
The first step into optimizing your performance and size/area is to determine the purpose of the design.

For example, if your design is a logical applications and combinational functions or adders, counters, accumulators, and comparators, you can configure the LE to a specific operating mode for better performance. LE in normal mode is for general logic and combinational functions. Whereas LE in arithmetic mode is ideal for implementing adders, counters, accumulators, and comparators.

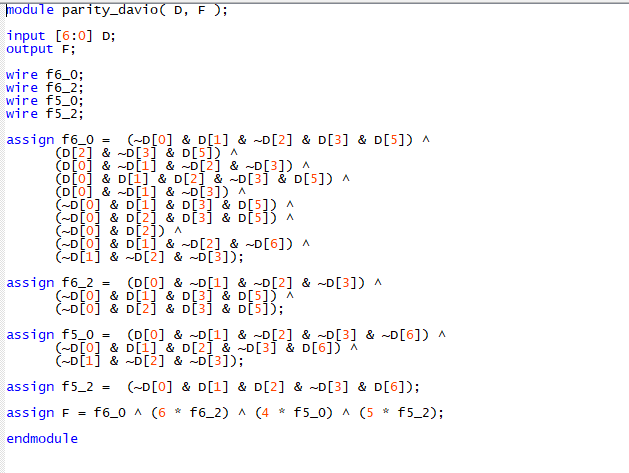
In optimize the size/area of a design, manually configure the carry chain logic to run vertically to allow faster connections through direct link interconnects. Although running vertical may be design specific, the best practice would be to examine how the LE is laid out and in which mode it is in and from there you can determine if the long carry chain would be a better fit vertical or horizontal depending on where the LAB and the M4K memory blocks reside.

# Question 3

Using the following walkthrough for the exercise provided in the class it was fairly easy to copy the logic for each condition



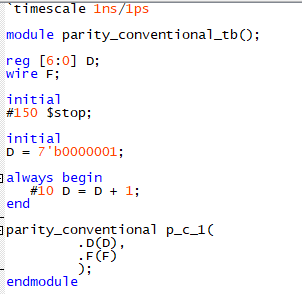
From this paper the following module was made from the template



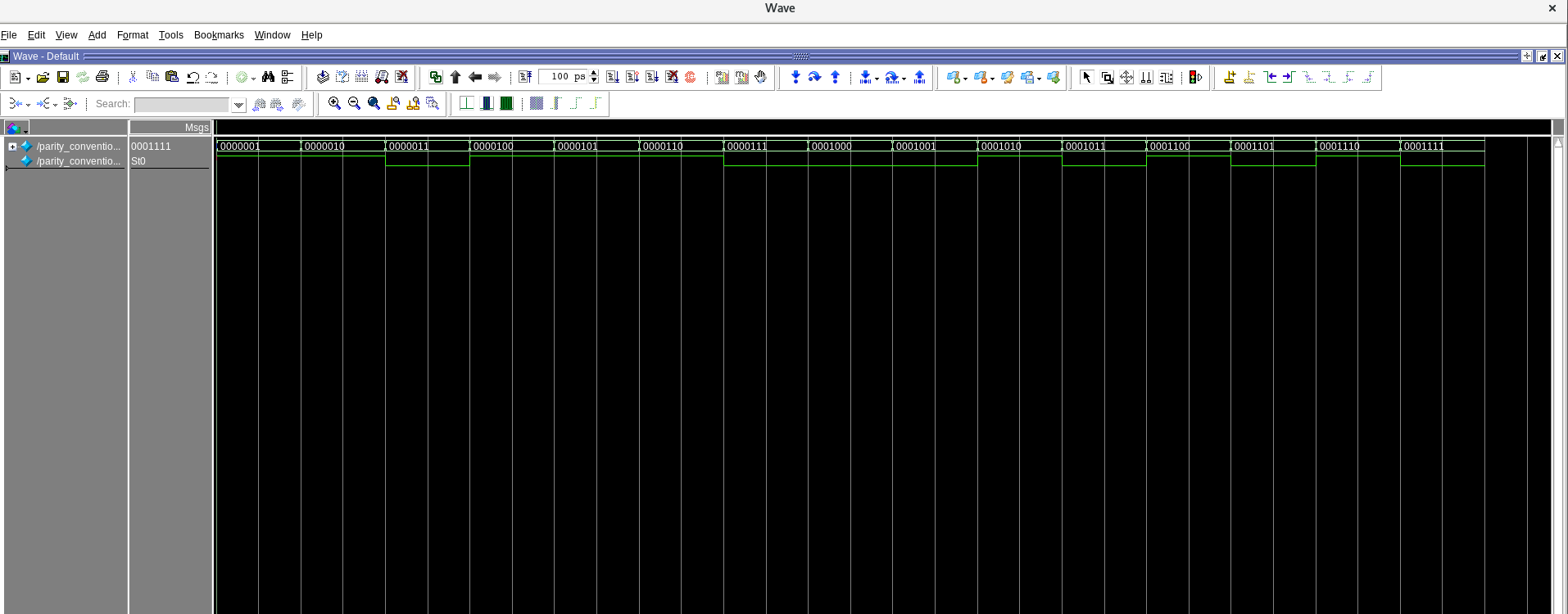
# Question 4

The method that I decided on to test if davio matches the conventional was to make a testbench that just increments the D value and compare the results of both

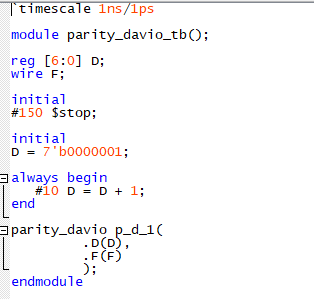
The testbench that I used for the conventional method was as follows



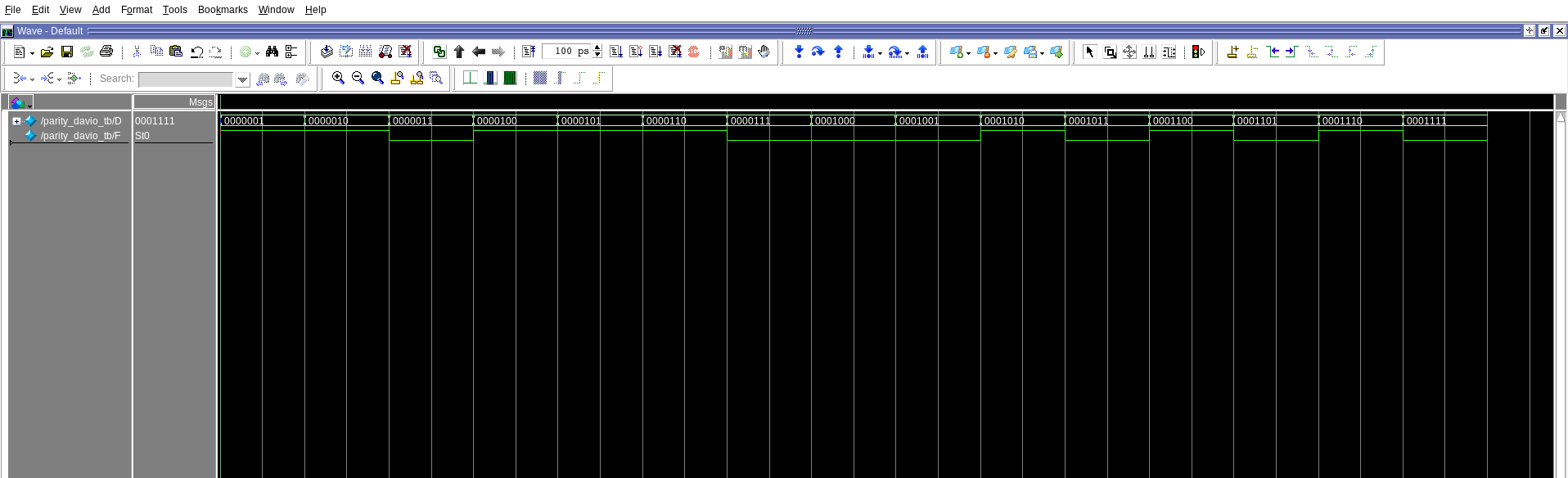
Which provided a wave form of



Now, the testbench that I used for the Davio was similar to that of the conventional



And the wave for that come from it was as follows



As you can see, both wave forms are one to one which means that they both provide the same logic

# Question 5

Area Optimization – Reduce the device area required to implement the design at the cost of performance

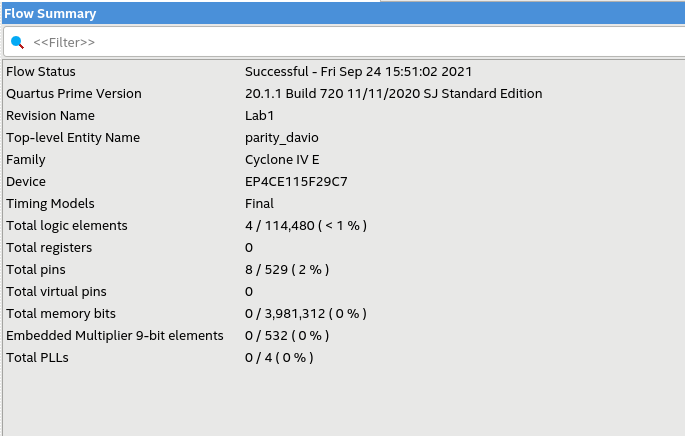
Power Optimization – Optimize synthesis for low power but will reduce speed performance

Performance Optimization – Optimizes speed performance at the cost of synthesis of run time and increased device resources

## Basic Optimization

The following will be the basic optimization for the conventional and davio’s method, respectively.

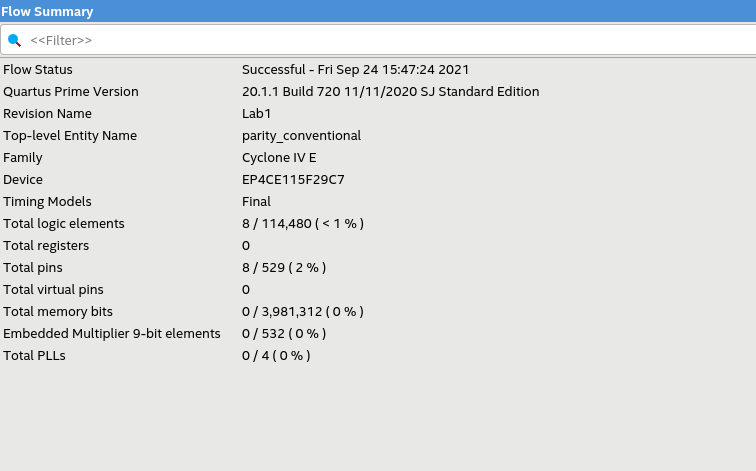


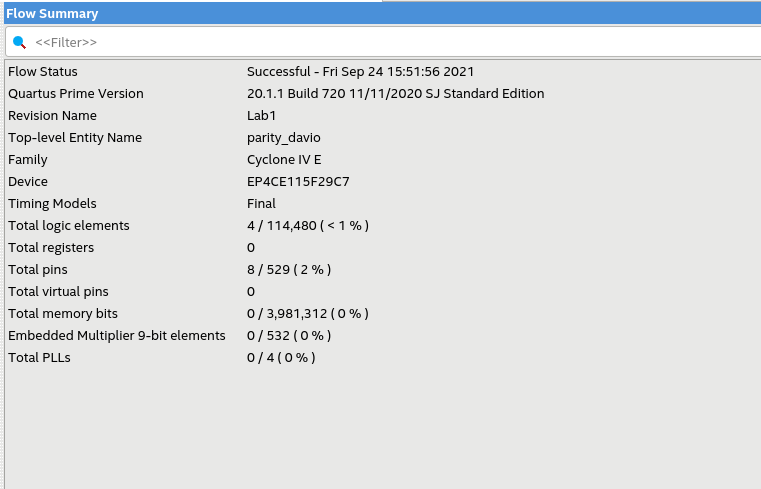


As you can see, the only difference is the number of total logic elements that were used. The CPU time for the conventional method was 27 seconds and the elapsed time 14 seconds. Whereas the CPU time for Davio’s method was 27 seconds and the elapse time was 15 seconds.

## Area Optimization

Now for the area optimization option provided by Quartus. The first picture will be conventional, and the following will be Davio’s.

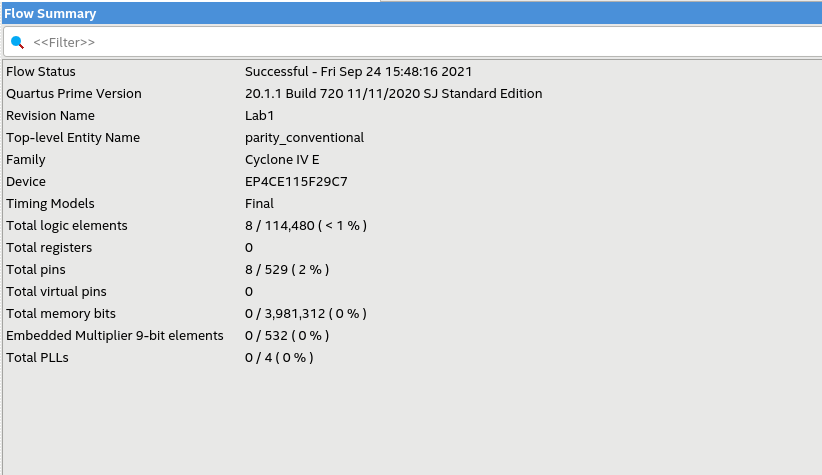


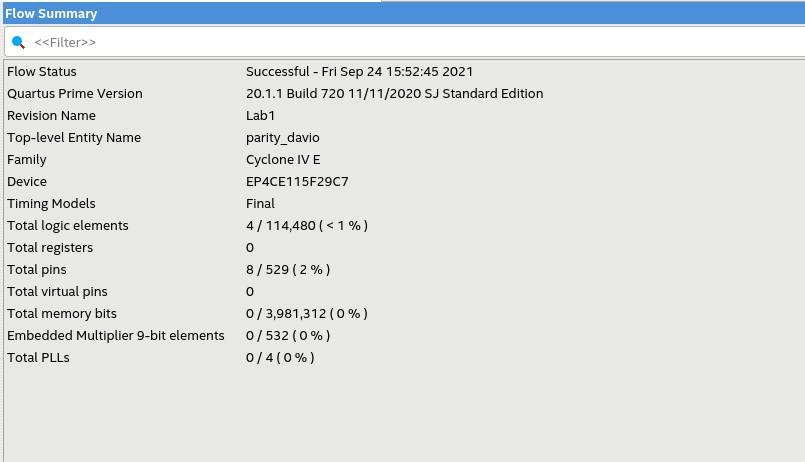


Again, the only difference in the flow summary is the number of total logic elements used. The CPU time for conventional was 27 seconds and the elapsed time was 15 seconds. Whereas the CPU time for Davio was 27 seconds and the elapsed time of 13 seconds

## Power Optimization

The next set of photos will be with the Power optimization in Quartus. The first picture will be the conventional and the second will be for Davio’s.

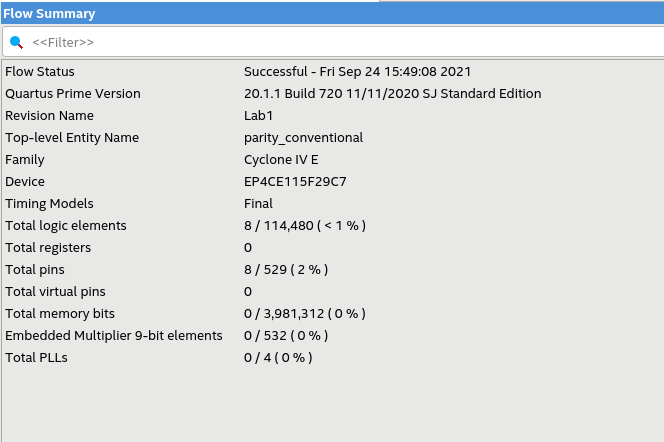


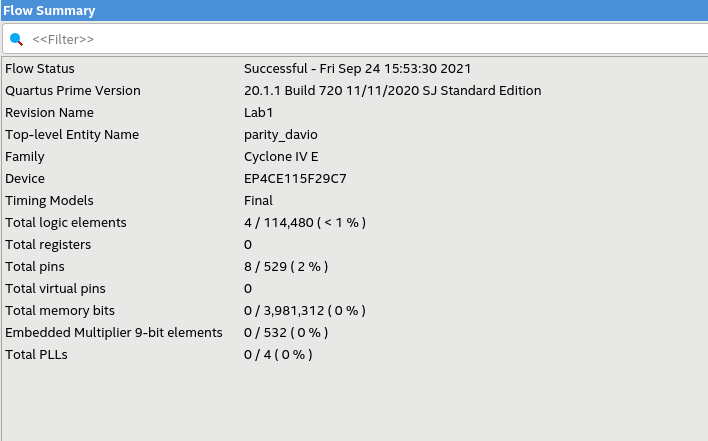


The only difference between the two is again the number of total logic elements used. The CPU time for the conventional method was 33 seconds with an elapsed time of 18 seconds. The CPU time for Davio’s method was 34 seconds with an elapsed time of 19 seconds.

## Performance Optimization

The last optimization that was used was the performance optimization provided by Quartus. Once again, it will go the conventional then Davio’s





Lastly, the only difference is the total logic elements. The CPU time for the conventional method was 32 seconds and the elapsed time was 19 seconds. The CPU time for Davio’s method was 33 seconds and the elapsed time was 18 seconds.

# Conclusion

As a conclusion, I am aware what each optimization does, and it seems that Quartus has already optimized the design to its fullest content to the point that changing the optimization configurations do little to nothing to the entire design. The only major difference that I could find between each optimization mode was the CPU and elapsed time, which was mentioned before. As designs become more complicated and complex, the usefulness of the different optimization modes starts to show.