

Hw5

- 7 A circuit has four inputs RSTU and 4 outputs VWYZ. RSTU represents a binary-coded decimal digit. VW represents the quotient and YZ the remainder when RSTU is divided by 3. (VW and YZ represent 2-bit binary numbers)
 Assume invalid inputs do not occur

A) ROM

B) A minimum two-level Nand-gate

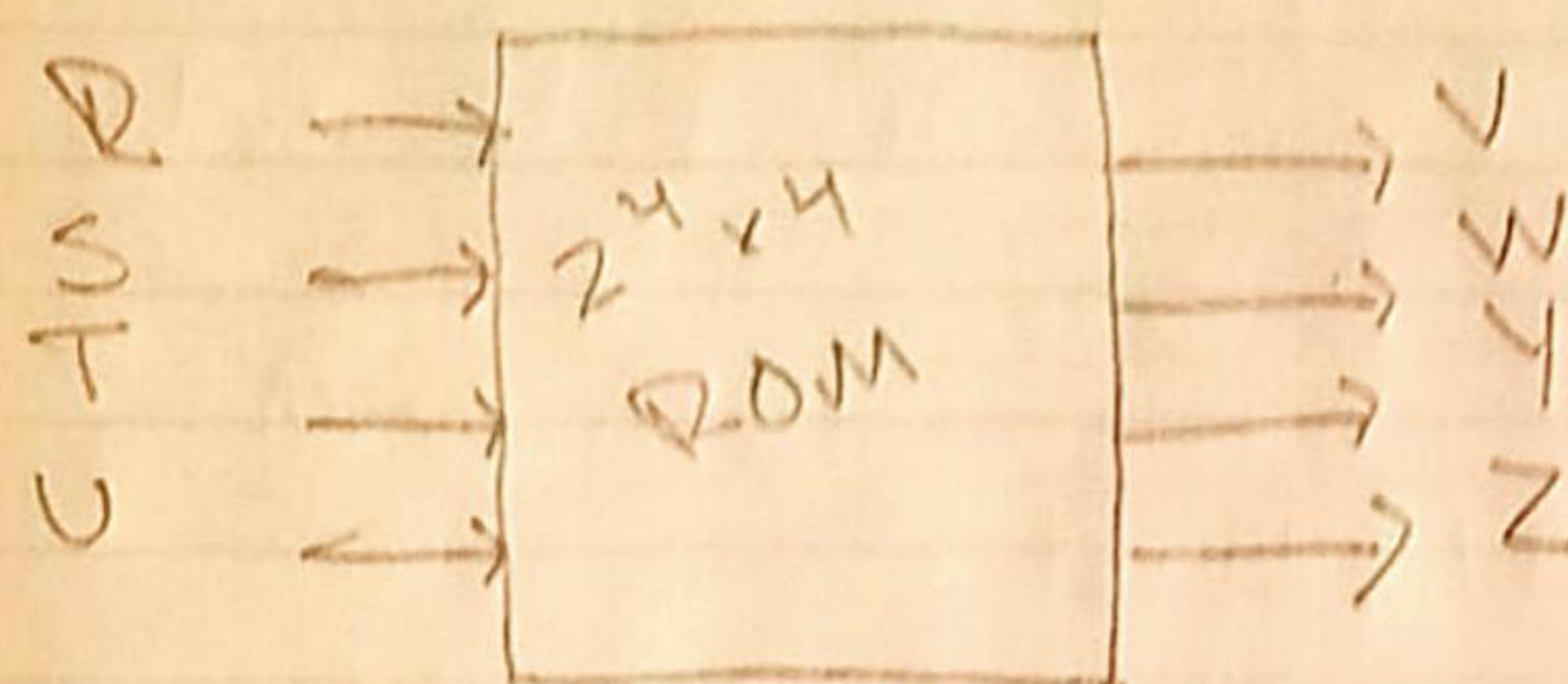
C) PLA

Input					Outputs			
R	S	T	U		V	W	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	1	0	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	1	0
6	0	1	1	0	1	0	0	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	1	0
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

← our outputs
 are invalid after
 9/3 because
 we have nothing
 to represent the
 quotient with.

Part A) ROM

We need 4 inputs and 4 outputs
 $2^4 \times 4$



K-maps for outputs.

RS TU	00	01	11	10
00	*	1	X	1
01	1	*	X	1
11	1	1	X	X
10	1	X	X	*

RS TU	00	01	11	10
00	*	1	1	1
01	1	*	1	1
11	1	1	1	1
10	1	1	1	*

$$V = R + ST$$

$$U = ST' + S'TU + RU$$

RS TU	00	01	11	10
00	*	1	X	V
01	1	*	X	*
11	1	1	X	Y
10	1	X	X	*

RS TU	00	01	11	10
00	*	1	1	*
01	1	*	X	*
11	1	1	X	*
10	1	X	X	*

$$Y = ST'U + RU' + S'TU'$$

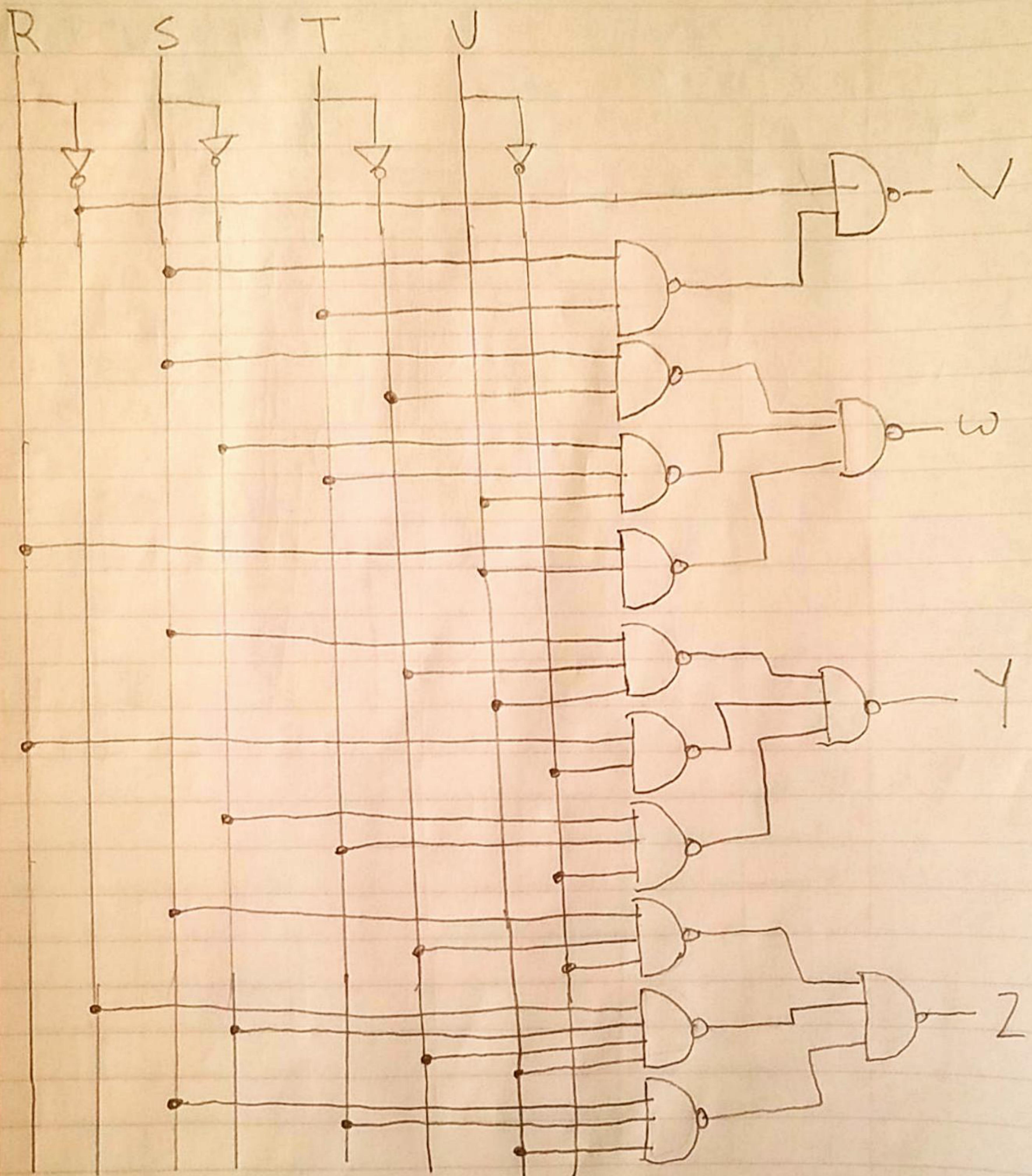
$$Z = ST'U + R'S'T'U + STU$$

$$V = R + ST$$

$$W = ST' + S'TU + RV$$

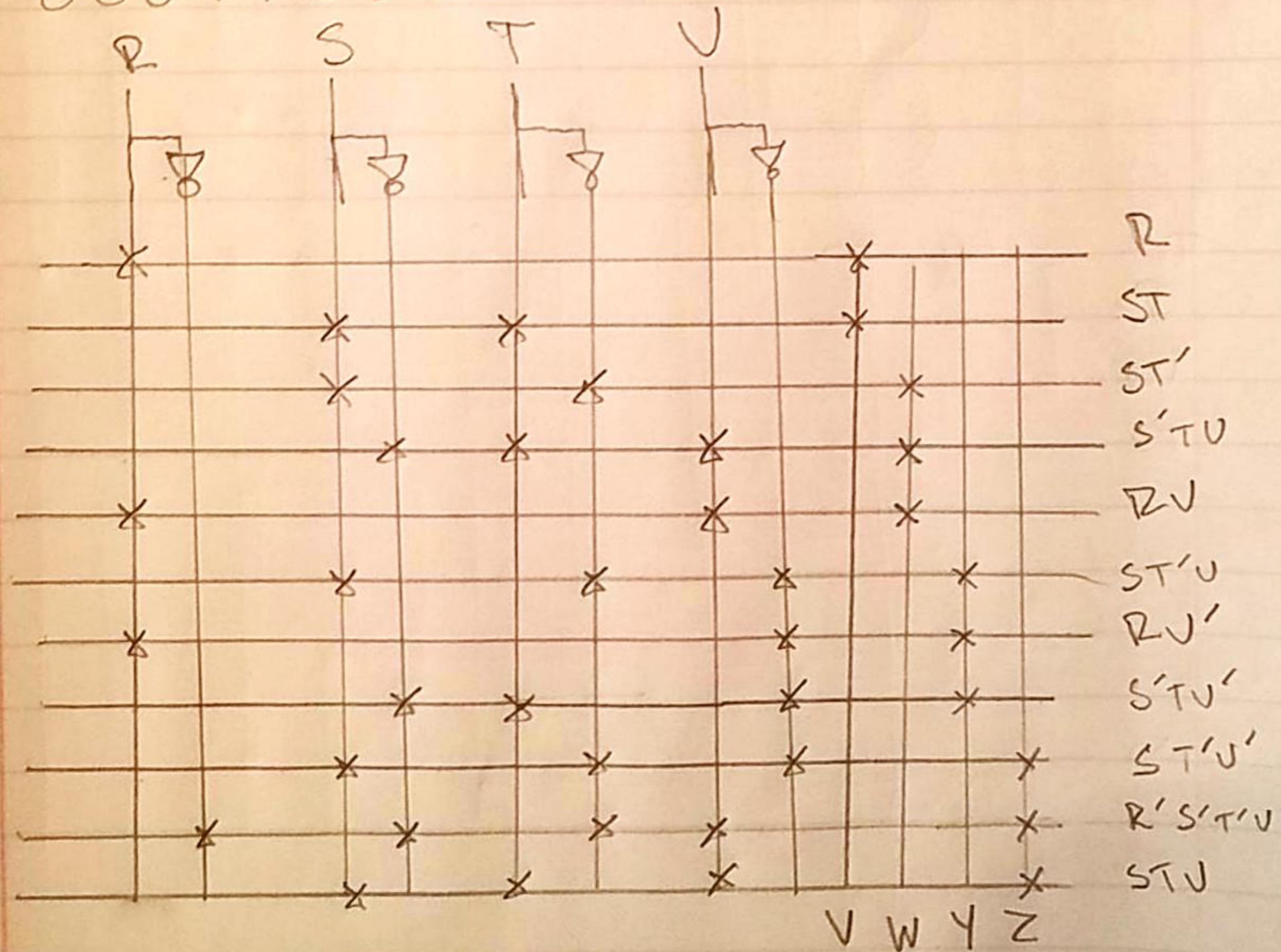
$$Y = ST'U + RU' + S'TU'$$

$$Z = ST'U' + R'ST'U + STU$$



PLA Table

RSTU	VWYZ
-11-	1000
1---	1000
-10-	0100
1--1	0100
-011	0100
1--0	0010
-101	0010
-010	0010
0111	0001
-100	0001
0001	0001



$$V = R + ST$$

$$W = ST' + S'TU + RU$$

$$Y = ST'U + RU' + S'TU'$$

$$Z = ST'V' + R'S'T'U + STU$$