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9/30/18

LAB REPORT 2

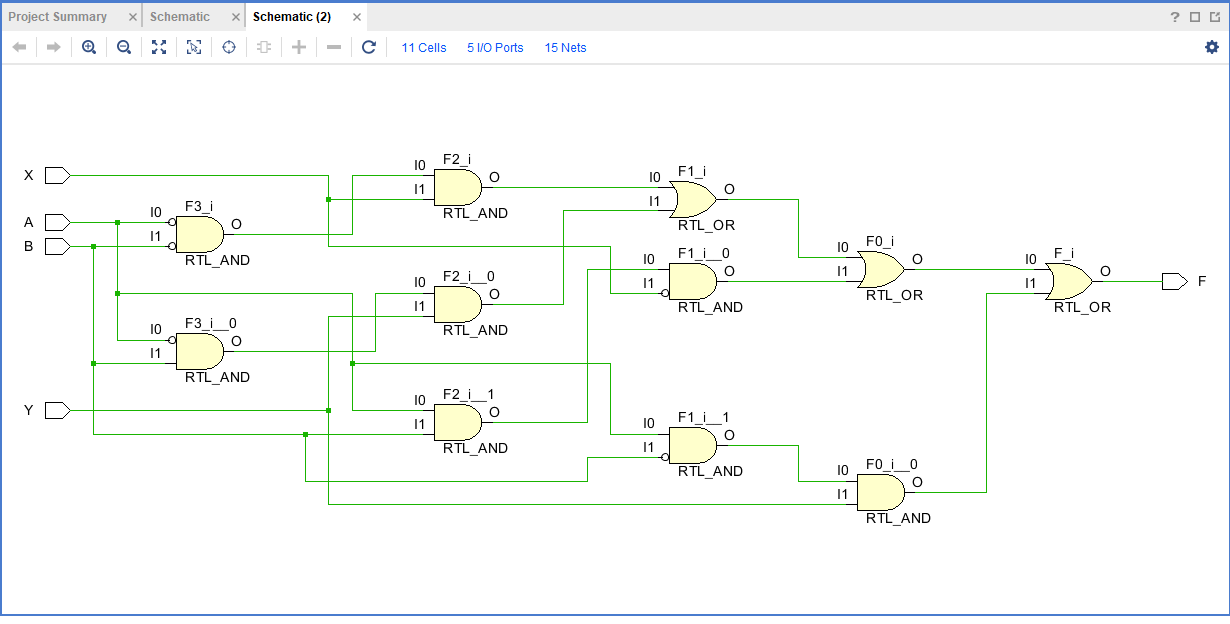
Multi-function Gate

Verilog Code

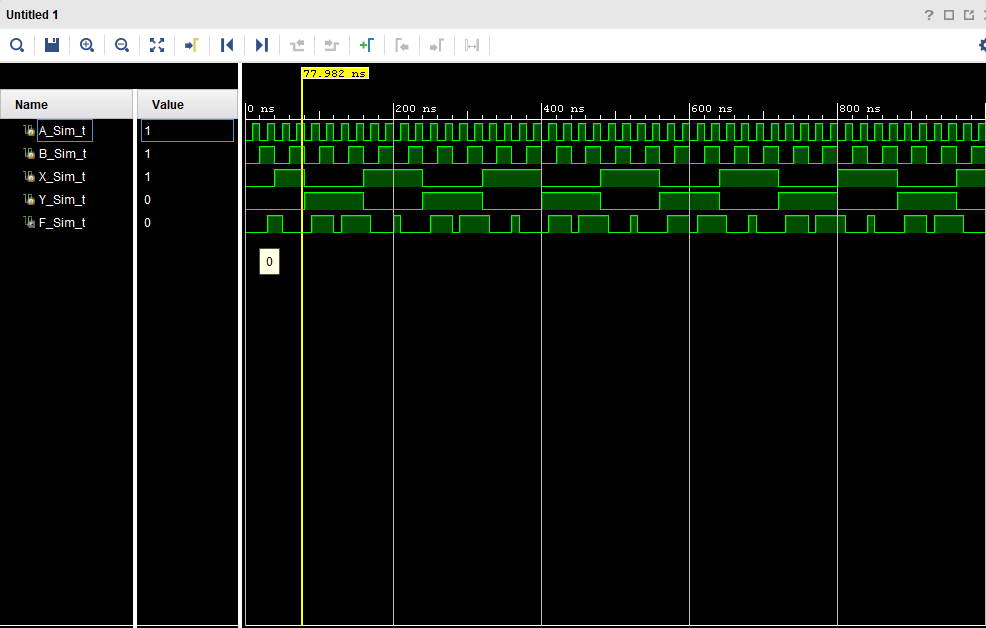
multi\_Function.v testbench.v

|  |  |
| --- | --- |
| This part of the code assigns our inputs, and our output function.  f = A'B'X + A'BY+ABX'+AB’Y | Testbench will assign the values according to the LED board. Sending each input back to our multi\_function.v then sets our output. |
| `timescale 1ns / 1ps  //f = A'B'X + A'BY+ABX'+AB’Y  // we will have 4 inputs to our 1 output.  module multi\_function(A,B,X,Y,F);  input A;  input B;  input X;  input Y;  output F;  assign F = (~A & ~B & X)|(~A & B & Y)|(A & B & ~X)|(A & ~B & Y);  endmodule | `timescale 1ns / 1ps  module testbench(  );  reg A\_Sim\_t;  reg B\_Sim\_t;  reg X\_Sim\_t;  reg Y\_Sim\_t;  wire F\_Sim\_t;    multi\_function UUT (  .F(F\_Sim\_t),  .A(A\_Sim\_t),  .B(B\_Sim\_t),  .X(X\_Sim\_t),  .Y(Y\_Sim\_t)    );    initial begin  A\_Sim\_t = 1'b0;  B\_Sim\_t = 1'b0;  X\_Sim\_t = 1'b0;  Y\_Sim\_t = 1'b0;    end  always #10 A\_Sim\_t = ~A\_Sim\_t;  always #20 B\_Sim\_t = ~B\_Sim\_t;  always #40 X\_Sim\_t = ~Y\_Sim\_t;  always #80 Y\_Sim\_t = ~Y\_Sim\_t;  endmodule |

Schematic



Simulation WaveForm



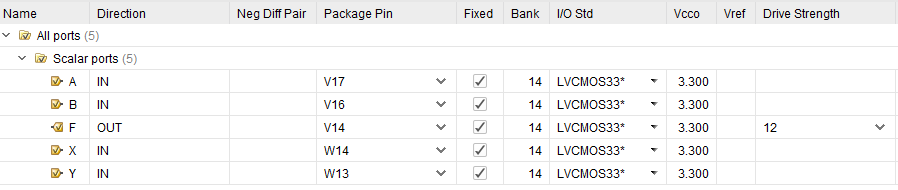
Truth Table

X and Y are responsible for deciding which gate type we will use. We will do the gate operation on A and B to receive our output on the LEDs.

F = A'B'X + A'BY+ABX'+AB’Y

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| X | Y | Gate | A | B | F |
| 0 | 0 | AND | 0 | 0 | 0 |
| 0 | 0 | AND | 0 | 1 | 0 |
| 0 | 0 | AND | 1 | 0 | 0 |
| 0 | 0 | AND | 1 | 1 | 1 |
| 0 | 1 | OR | 0 | 0 | 0 |
| 0 | 1 | OR | 0 | 1 | 1 |
| 0 | 1 | OR | 1 | 0 | 1 |
| 0 | 1 | OR | 1 | 1 | 1 |
| 1 | 0 | NOR | 0 | 0 | 1 |
| 1 | 0 | NOR | 0 | 1 | 0 |
| 1 | 0 | NOR | 1 | 0 | 0 |
| 1 | 0 | NOR | 1 | 1 | 0 |
| 1 | 1 | NAND | 0 | 0 | 1 |
| 1 | 1 | NAND | 0 | 1 | 1 |
| 1 | 1 | NAND | 1 | 0 | 1 |
| 1 | 1 | NAND | 1 | 1 | 0 |

PIN Assignment



Questions

1. Can this Multi-Function Gate be operated as an Inverter? If yes, explain how.
   1. No, it is not possible to use this multi-function gate as an inverter, unless we were to invert each bit each time.
2. Will the change in the number of inputs or outputs affect the number of operation select lines? Explain.
   1. The number of inputs would completely change the experiment. Every input we add increases the number of operations by a power of 2!
   2. As for outputs, it does not affect the number of operations, as each output is associated with an operation. If we increase the number of operations then our outputs much be increased.
3. Will the change in the number of functions alter the number of operation select lines? Explain.
   1. The number of functions within the gate will increase the number of operations per line by a power of 2.
4. Have you met all the requirements of this lab (Design Specification Pla n)?

Yes! I think so.

1. How should your design be tested (Test Plan)?

The code should be separated into two .v files (testbranch being the simulation file).

Input A should be on SW0 (V17), B on SW1 (V16), X on SW6(W14), and Y on SW7(W13) should be assigned pin Values that are associated with SWITCHES on our board. We also need to assign F to LED7 (V14) on the board. (I/O inputs).

After we generate our bitstream (.bit) we will be able to upload our written software to the board.

We can verify our outputs by following alone with the truth table.

When f is 1 the light will turn on otherwise it will stay off.