**1.Describe the features of the Cortex-A9 processor**

* Dual-core processor cluster (Dos core cortex A9)
* 2.5 DMIP/MHz per processor (Benchmarking de las CPU)
* Harvard architecture
* Self-contained 32KB L1 caches for instructions and data
* External memory based 512KB L2 cache
* Automatic cache coherency between processor cores (Mediante el uso de SCU)
* 800-MHz operation (fastest speed grade)

**2.Identify the cache resources in the APU**

* L1 cache
  + Primary cache built into the snoop control unit (SCU)
  + 32KB each for instruction and data
  + One per CPU
* L2 cache
  + Secondary, larger cache
  + 512KB
  + One per SCU

**3.List the timers that are included in the APU**

* Global timer
* System watchdog timer (SWDT)
* Private timer and watchdog timer (AWDT)
  + One per Cortex-A9 processor
* Two triple timer/counters (TTC)