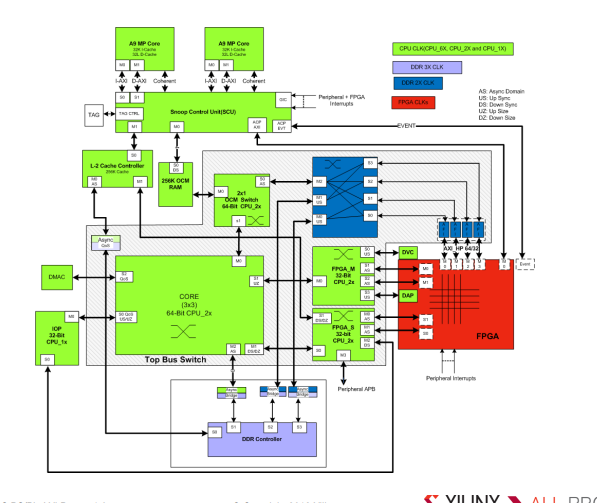
**1.List the PS AXI interfaces to the PL**

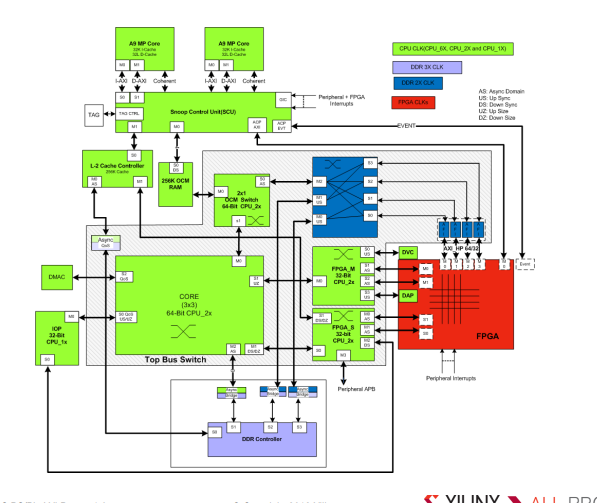


* Two general-purpose master ports
* Two general-purpose slave ports
* Four high-performance slave ports
* One accelerator coherence port (ACP) slave port

**2.Describe the use of the PS master interface to the PL**

Mostly used for CPU and IOP data movement to programmable logic.

**3.List the PS components that are accessible from the PL via the AXI slave interface**



Mostly used for PL masters to access IOP, OCM RAM, and DDRx