1. **List some of the miscellaneous PL-PS ports**

Nine AXI ports

— Seven slaves

— Two masters

Extended multiplexed I/O (EMIO) allows unmapped PS peripherals

to access I/O within the PL

Four PS clock outputs to the PL with enable control

Four PS reset outputs to the PL

Processor configuration access port (PCAP) to support full and

partial PL configuration and secured PS image decryption

XADC interface

JTAG chain

1. **List some of the features of a peripheral clock generator**

Key features of clock generation

— A primary reference clock input from a dedicated pin (typically connected to

an external crystal oscillator) Typical/recommended clock frequency is 30-60MHz

— Three PLLs

CPU PLL: Primarily for generating the CPU clock

DDR PLL: Primarily for generating the DDR DRAM clock

IO PLL: Primarily for generating peripherals clocks

— PLLs share the input reference clock and a programmable 4-bit input divider

— PLLs share a bandgap reference voltage circuit

— Bypass option for each PLL to the input clock pin

— Each PLL has an individually programmable 7-bit feedback divider

— Each clock generation circuit has a PLL source selection multiplexer followed by a programmable divider