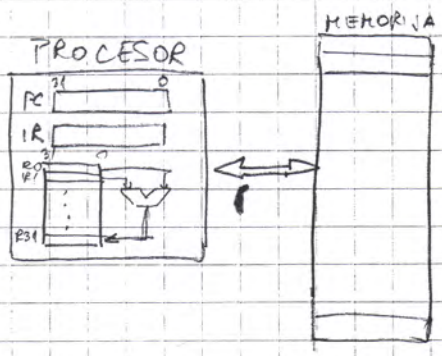
Arhitektura računala s aspekta digitalnih sklopova -

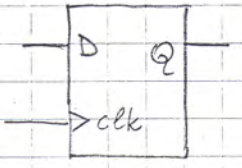


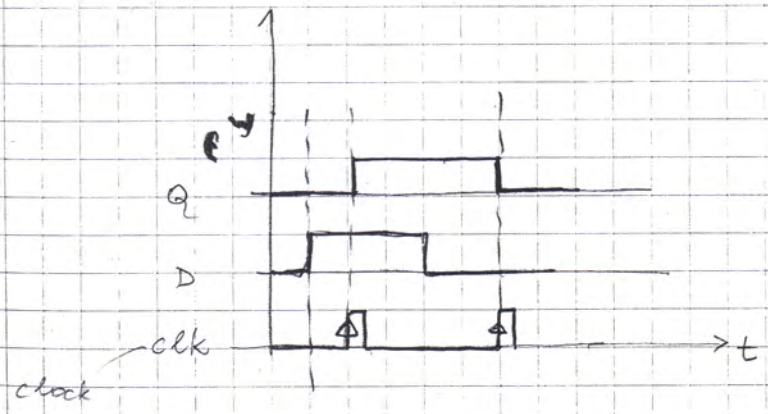
(ISA - instruction set architecture -> to smo radili)

1° Kako realizirati registar?

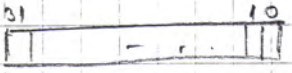
2° Kako povezati registre za prebacivanje podataka

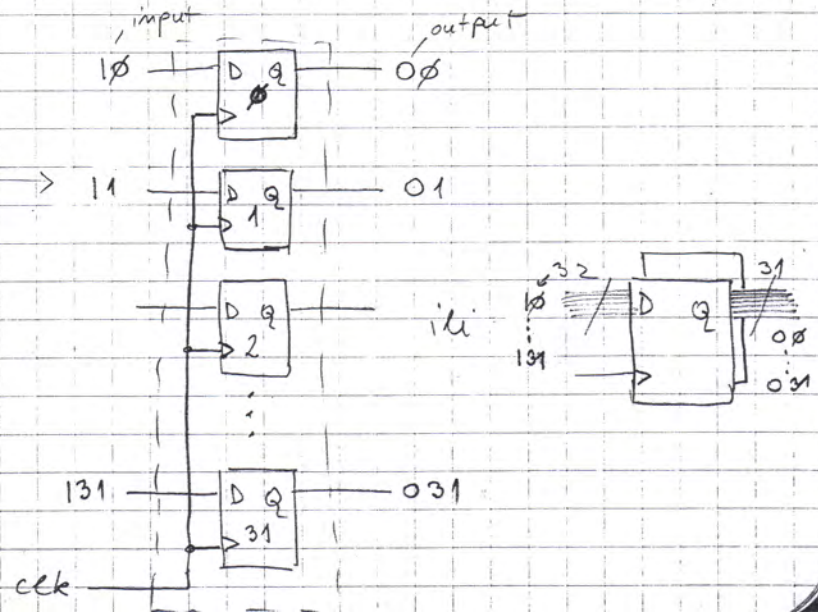
Registar - najbolje odabrati - D bistabil



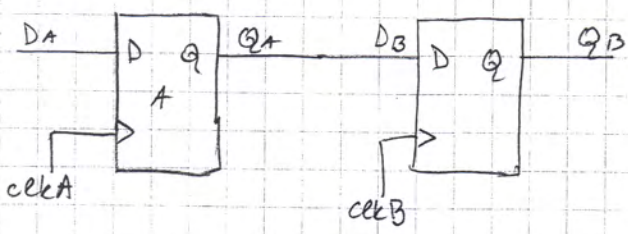


1°

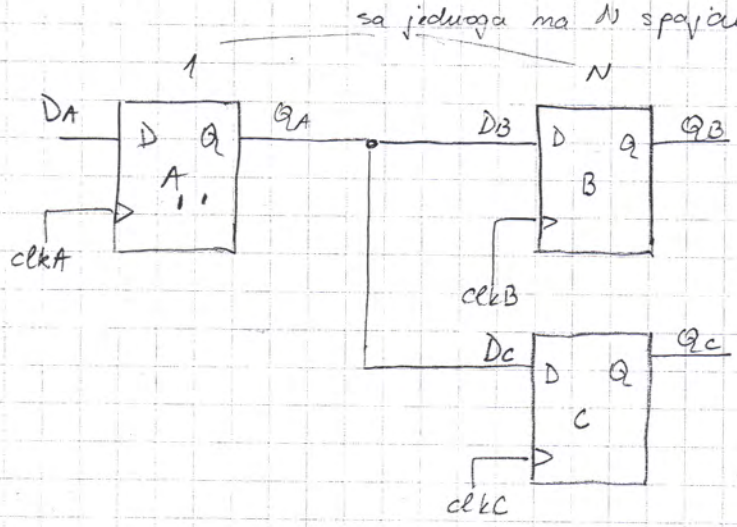




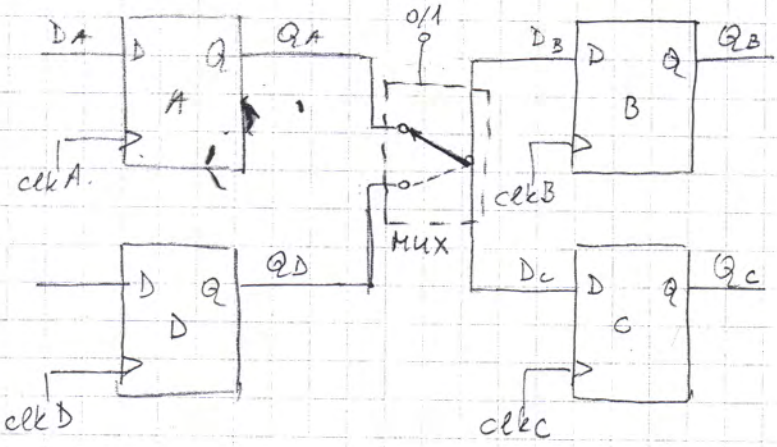
2° Povezivanje registara / bistabila

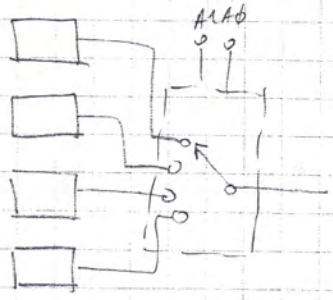


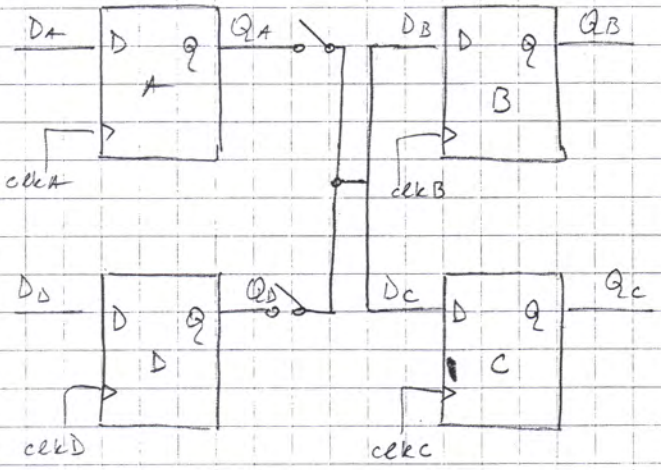
sa clkB upisuje se stanje iz A u B



Npr. aktiviramo clkC ako očekujemo iz A u C, ili clk za iz A u B, ili oboje da ode iz A u B, C

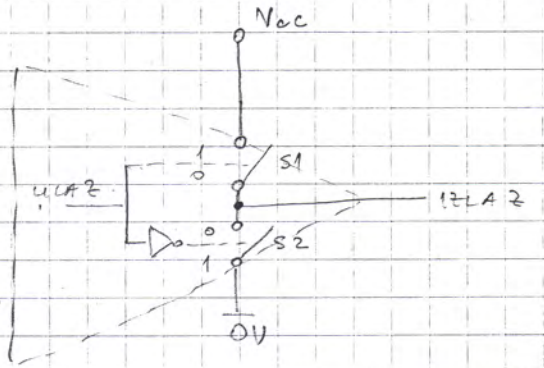




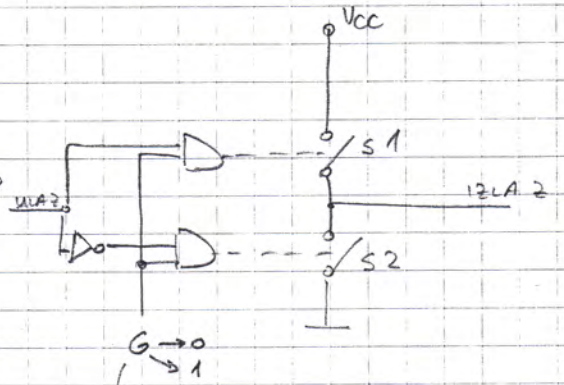


Dopuštamo samo da je otvoren jedan, na QA ili QD

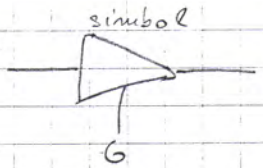
Logika s tri stanja

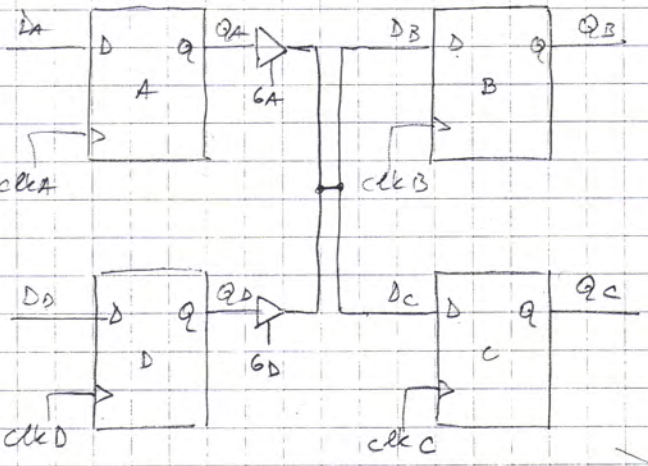


modificira se



Gate - sa tim kontroliramo

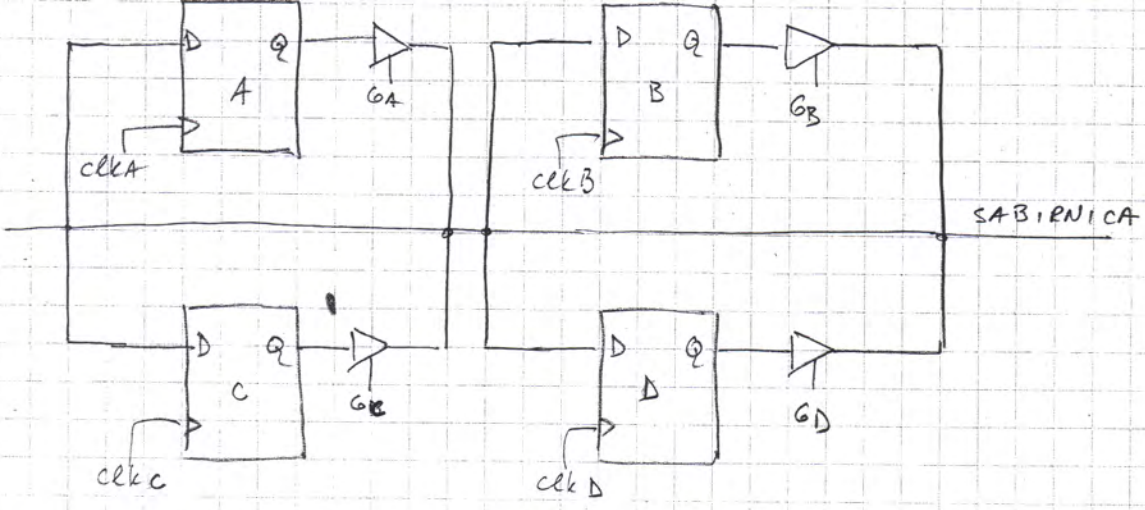




Sa G-ovima upravljamo } Samo jedan G je u jedinici

G = 0 → odspojeno

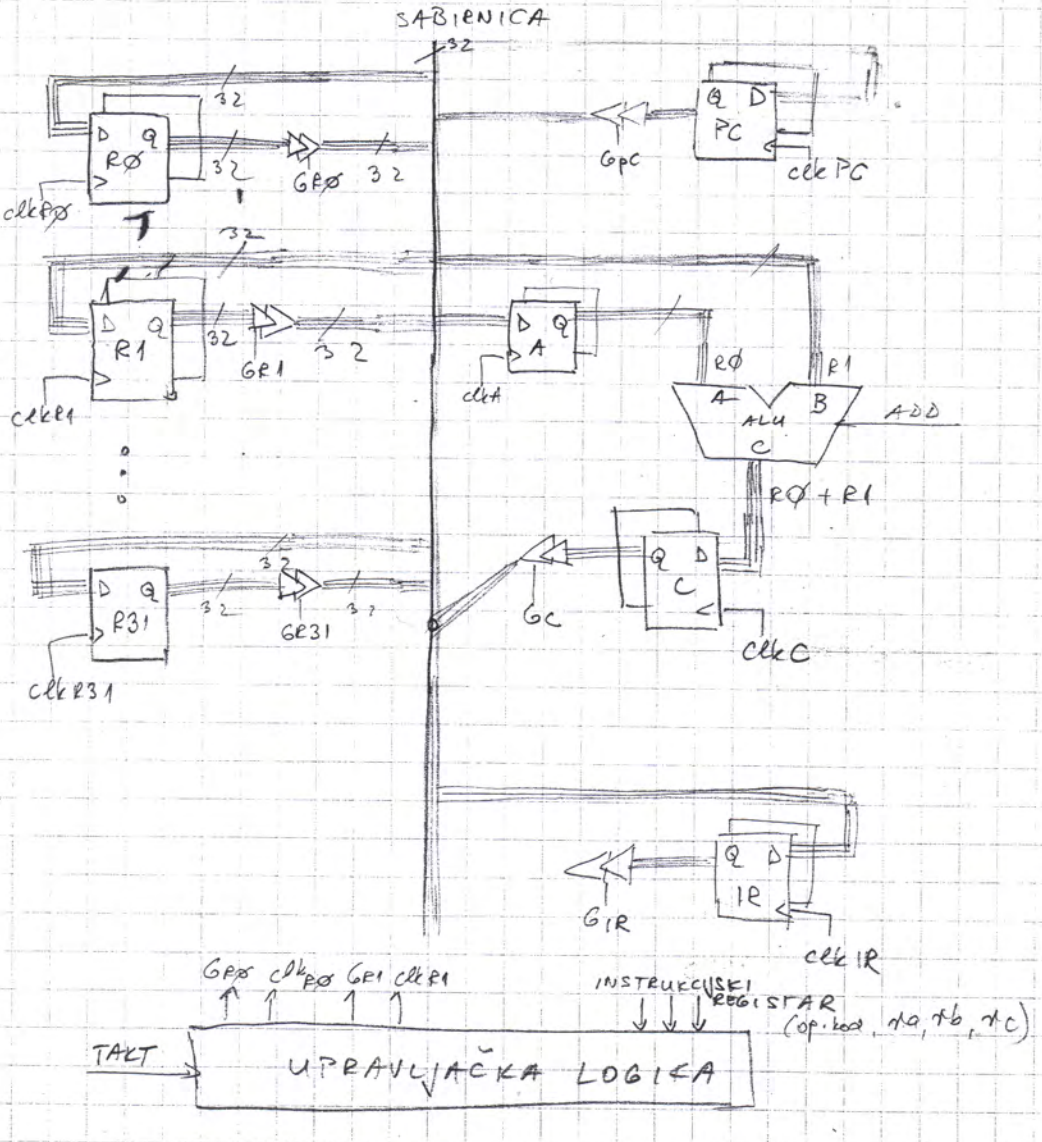
G = 1 → spojeno

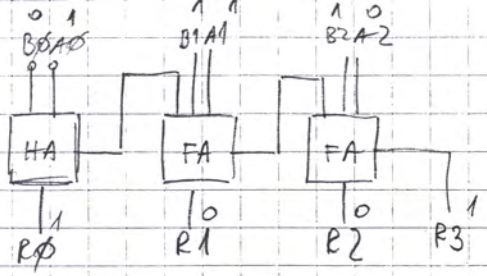


Primjer: iz C upisati u A i D

$$G_C = 1 \quad + \quad clk_A, clk_D$$

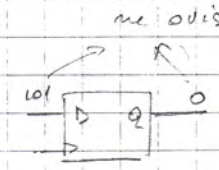
$$G_A, G_B \text{ i } G_D = \emptyset$$



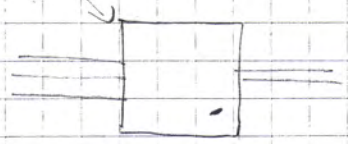


A 011

B 110



KOMBINACIJSKA SEKVENCIJALNA LOGIKA



mpt. 

ovisi samo o ulazu iz laz

ALU je čisto kombinacijska logika

ADD R31, R0, R1;

Koraci:

1. Upisati sadržaj registra R0 u A

$G_{R0} = 1$, clkA

2. - Stavljam sadržaj R1 na sabirnicu:

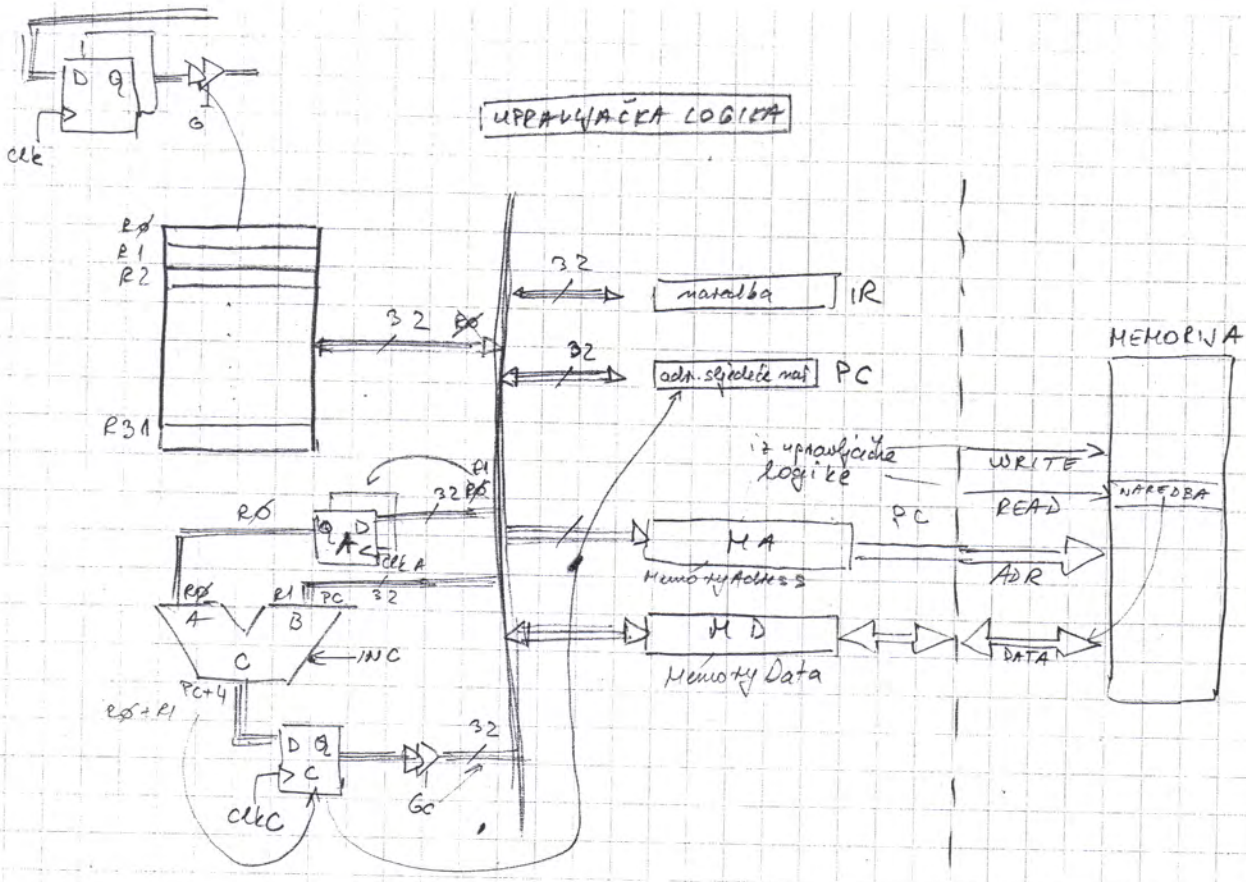
$G_{R1} = 1$,

- zbroji ADD

- upisati rezultat u C; clkC

3. - upisati rezultat u R31

$GC = 1$; clkR31



Procesor radi: dohvati i izvedi naredbu

DOHVATI:

Sa adrese na koju pokazuje PC dohvatiti naredbu i upisati u IR, inkrementirati PC

1. Sadržaj PC na sabirnicu i upisati u MA
   G_{PC} clk_{MA}
   isboristiti priliku kada je sadržaj PC-a na sabirnici (na ulazu B ALU), i inkrementirati ga i spremiti u C
2. Na adresnoj sabirnici je adresa lokacije na kojoj je naredba, postavi se signal READ i učita naredba u MD
   Sabirnica je slobodna, pa se preko nje inkrementirani sadržaj PC prebaci iz C u PC
   G_C, clk_C
3. Naredbu iz MD prebaciti u IR
   G_{MD}, clk_{IR}

IZVOĐENJE NAREDBE: npr. ADD R2, R0, R1

4. Dohvat 1. operanda i upis u privremeni spremnik A

G_{R0}, clkA

5. Dohvat 2. operanda i postavljanje na sabirnicu B – G_{R1}

Naredi se ALU zbrajanje ADD

Rezultat se upiše u privremeni spremnik C – clkC

6. Pohrana rezultata u odredišni spremnik

- sadržaj C na sabirnicu G_C
- upis u R2 → clk_{R2}

ADDI R31, R1, 10

Samo se razlikuje prvi korak izvođenja naredbe

1. operand je u IR.

LD R31, R1, 10.

Razlikuje se 6. korak

6. Upisati iz C u MA, naredbi READ

7. Iz memorije podatak u MD

8. Podatak iz MD u R31

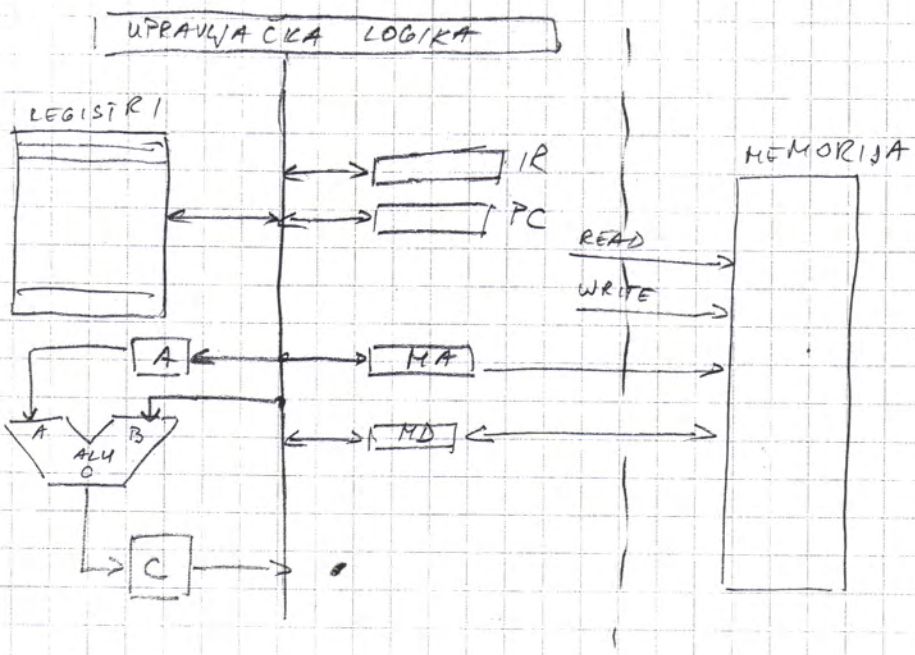
ST R31, R1, 10

6. Upisati iz C u MA (nema READ.)

7. Iz R31 u MD

8. WRITE

13.5 računalo



DOHVATI
1.
2.
3.

IZVOĐENJE
aritm. log. naredba

AL

4. Dohvat op. 1
5. Dohvat op2 + AL
6. spremi rezultat

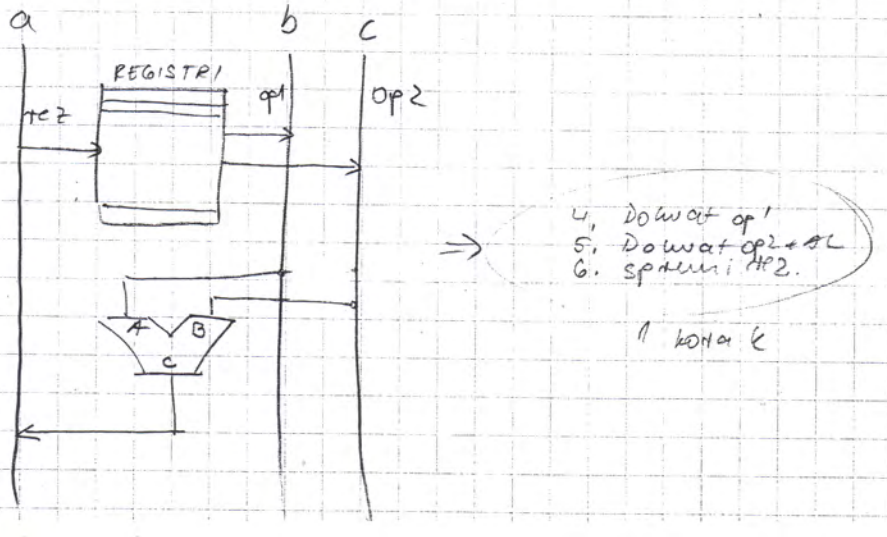
ADD, ADDI

4.
5.
6.
7.
8.

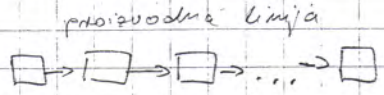
LOAD/STORE

CILJ - brži procesor
a) bržim sklopovima
b) manje koraka → 1 naredba po koraku

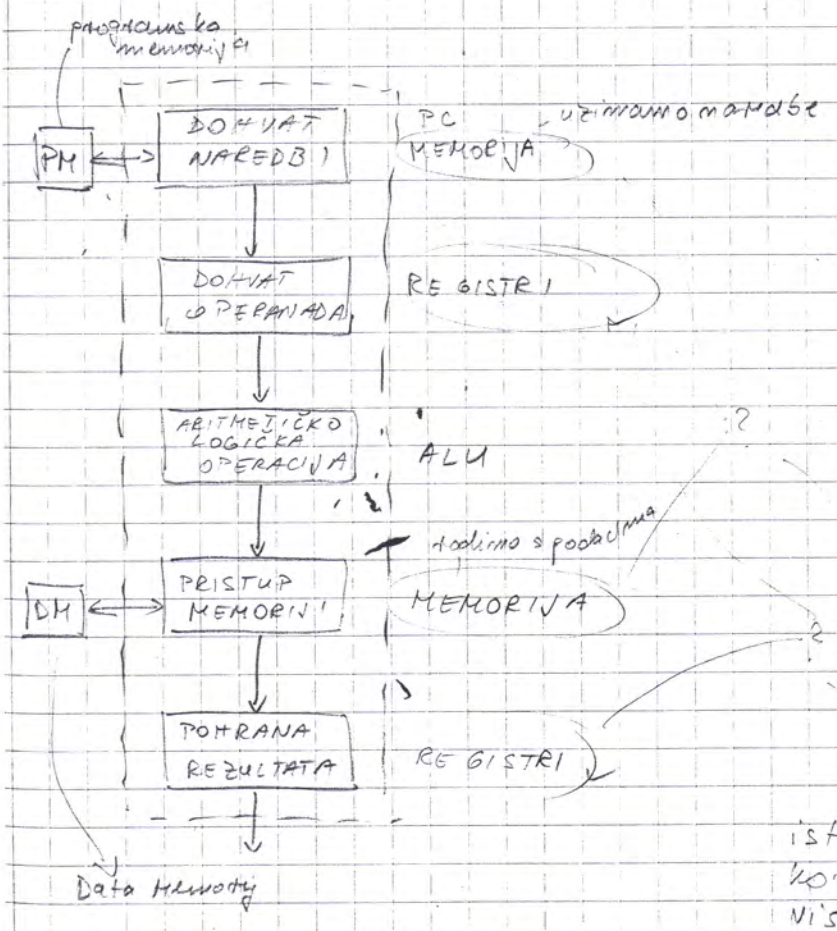
Problem je što je samo jedna sabirnica (samo po jedan korak radimo), pa onda radimo sa 3 sabirnice, za op1, op2, rezultat

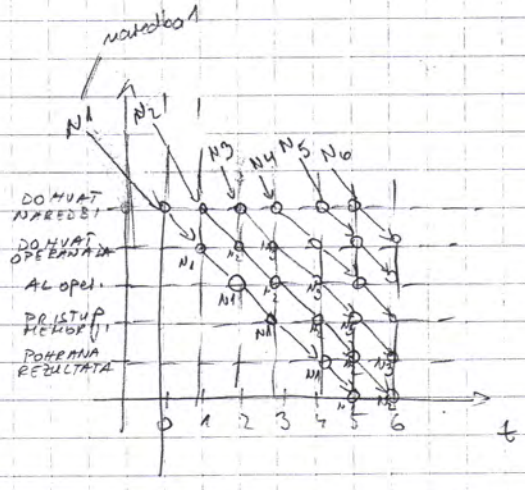


- obradu podijeliti u strogo definirane korake
  - ⇒ dohvat naredbe
    Sa adrese na koju pokazuje PC pročitati naredbu, upisati u IR, inkrementirati PC



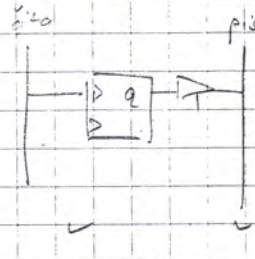
- ⇒ izvođenje naredbe
  - dohvat operanada
  - aritmetičko logička operacija
  - ? - pristup memoriji (dohvat podatka iz memorije) — LOAD/STORE
  - spremi rezultat

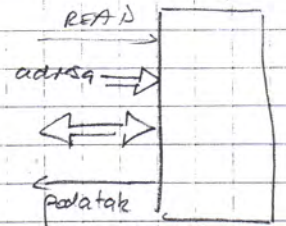




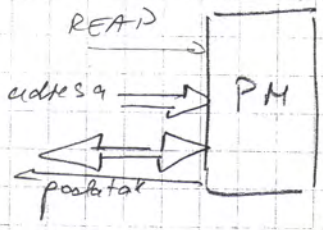
kad se mapiraju svi, u jednom taktu izbacuje jednu naredbu ⇒ to je omogućeno o paralelizmu

istovremeno koriste isto više naredbi?

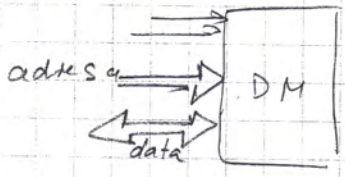




2 → ne može se raditi ciklus 1 i 4 istovremeno

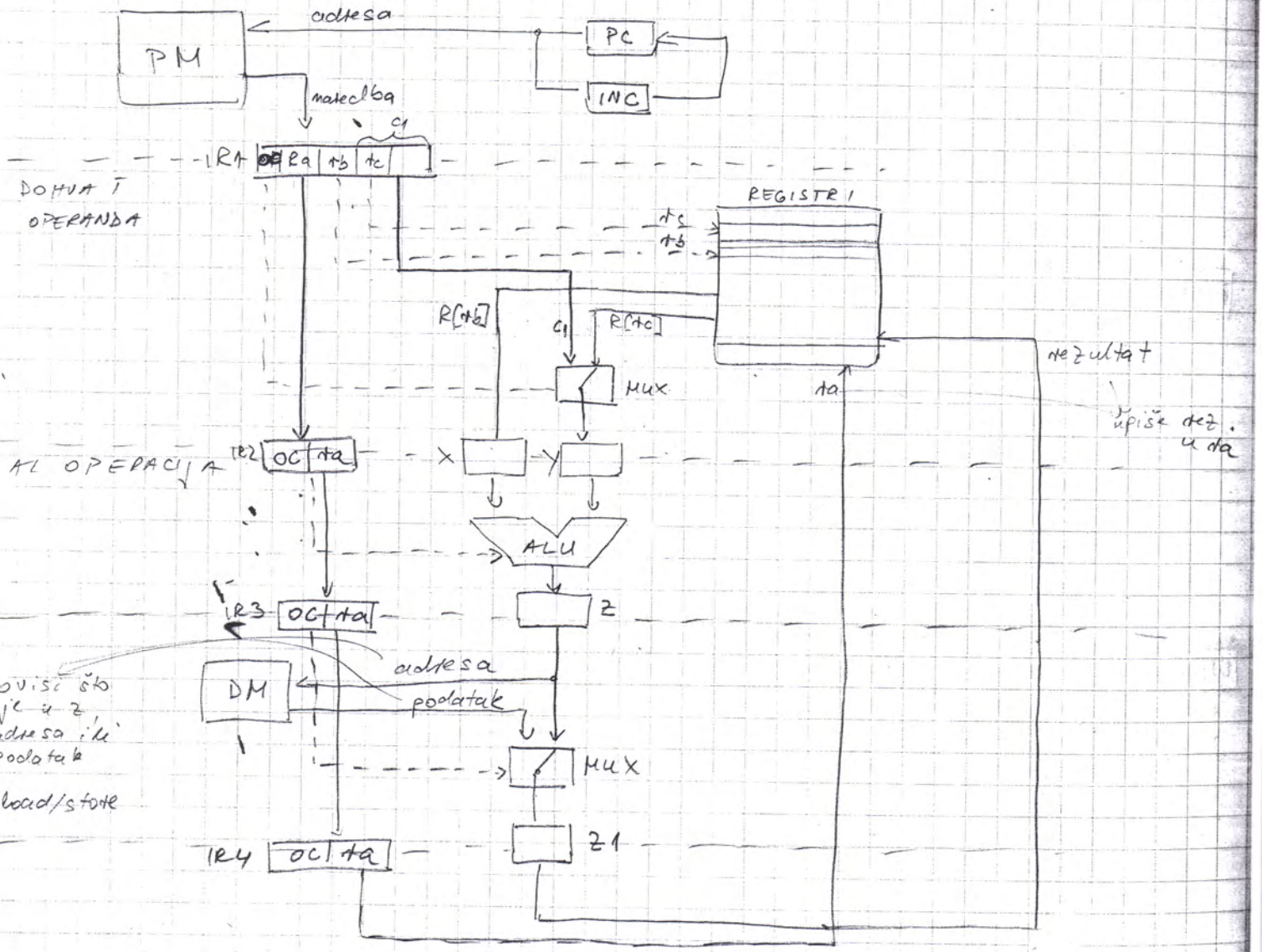


> Harvardska arhitektura



PIPELINING (CJEVOVOD)

DOHVAT NAREDBE



. kolokvij .

ARHITEKTURA RAČUNALA NA RAZINI LOGIČKIH SKLOPOVA

- prijenos podataka između između registara
  - → pomoću MUX
  - → pomoću 3-state logike

- Rješenje jednosabirničkog procesora – malo detaljnije (signali, sabirnice, ...)
- Izvođenje naredbi na jednosabirničkom procesoru (ADD, ADDI, LOAD, STORE)
  - na mnemotehničkoj arhitekturi prikazat
- Trosabirnički procesor (povezivanje registara, brzina).
- Procesor sa cjevovodom